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Paper No. 8
Entered: August 28, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2017-00841
Patent 7,525,189 B2

Before MICHAEL J. FITZPATRICK, JENNIFER MEYER CHAGNON, and SHEILA F. MCSHANE, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Xilinx, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1, 2, 4, and 5 ("the challenged claims") of U.S. Patent No. 7,525,189 B2 (Ex. 1001, "the '189 patent"). Paper 1 ("Pet."). Petitioner relies on the Declaration of Jianmin Qu, Ph.D. (Ex. 1002) to support its positions. Godo Kaisha IP Bridge 1 ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp.").

We have authority to determine whether to institute *inter partes* review. *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, and for the reasons explained below, we determine that the information presented does not show a reasonable likelihood that Petitioner would prevail with respect to any of the challenged claims. *See* 35 U.S.C. § 314(a). Accordingly, we do not institute an *inter partes* review of the '189 patent.

A. Related Proceedings

The parties indicate that the '189 patent is the subject of the following ongoing district court proceeding: *Xilinx, Inc. v. Godo Kaisha IP Bridge 1*, Case No. 5:17-cv-00509 (N.D. Cal.). Pet. 1; Paper 4, 1. Patent Owner also indicates that three petitions for *inter partes* review have been filed for related patents: Cases IPR2017-00842, IPR2017-00843, and IPR2017-00844. Paper 4, 1.

B. The '189 Patent

The '189 patent is titled "Semiconductor Device, Wiring Board, and Manufacturing Method Thereof," and was filed as PCT application No. PCT/JP2005/009061 on May 18, 2005. Ex. 1001, at [22], [54], [86]. The

application entered the U.S. national stage as application No. 11/569,423 meeting the requirements under 35 U.S.C. § 371 on November 20, 2006. *Id.* at [21], [86]. The '189 patent claims priority to Japanese application No. 2004-152618, filed May 21, 2004. *Id.* at [30].

The embodiments described in the '189 patent "provide a highly reliable semiconductor device capable of improving the performance at a low cost." *Id.* at 4:6–8. Figure 1 of the '189 patent is reproduced below.

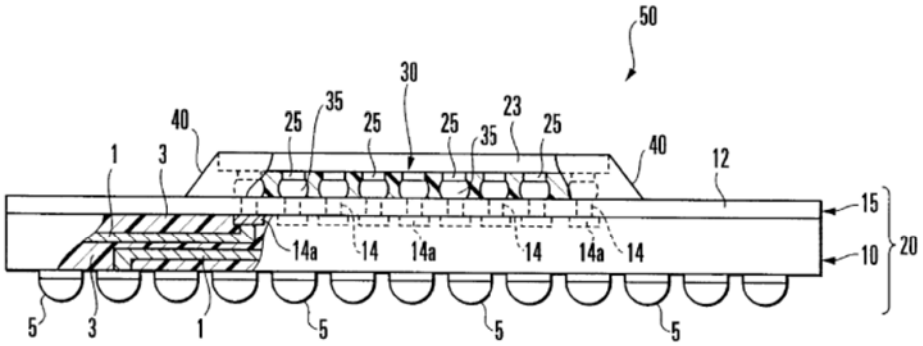


FIG. 1

Figure 1, above, illustrates a "partially cutaway side view schematically showing the first embodiment[] of a semiconductor device and wiring board of the present invention." *Id.* at 4:14–16. As seen in Figure 1, semiconductor device 50 includes semiconductor chip 30 mounted on wiring board 20 by flip chip bonding. *Id.* at 4:58–62. Wiring board 20 includes first wiring portion 10, and second wiring portion 15 electrically connected to and integrated with (i.e., stacked on) first wiring portion 10. *Id.* at 4:63–5:1.

First wiring portion 10 further includes a plurality of wiring layers 1 and interlayer dielectric films 3. *Id.* at 5:1–4. "[E]xternal connecting bumps 5 are formed [on] one surface . . . of the first wiring portion." *Id.* at

5:5–6. Second wiring portion 15 includes base 12 and connecting terminals 14 (each formed of a contact plug formed in a through hole) extending through the base. *Id.* at 5:9–17. In embodiments of the '189 patent, the "planar size of the second wiring portion 15 is equal to that of the first wiring portion 10." *Id.* at 5:22–24.

As further described, "the material of the base 12 of the second wiring portion 15 is selected so that the thermal expansion coefficient of the second wiring portion 15 is smaller than that of the first wiring portion 10, and equal to that of each semiconductor chip 30." *Id.* at 5:49–52. Having the thermal expansion coefficient of the second wiring portion 15 be equal to that of each semiconductor chip 30 makes it possible to suppress the internal stress caused by differences in the thermal expansion coefficients. *Id.* at 6:1–6.

C. Illustrative Claim

Of the challenged claims, claims 1 and 4 are independent. Claims 2 and 5 depend from claims 1 and 4, respectively. Independent claim 1 of the '189 patent is reproduced below, and is illustrative of the challenged claims.

> 1. A semiconductor device characterized by comprising:
>
> a wiring board comprising a plurality of connecting terminals arranged on one surface in a direction of thickness and a plurality of external connecting bumps arranged on the other surface in the direction of thickness; and
>
> at least one semiconductor chip connected to said connecting terminals,
>
> wherein said wiring board comprises:
>
> a first wiring portion comprising a plurality of wiring layers and said external connecting bumps; and

> a second wiring portion electrically connected to said first wiring portion and integrated with said first wiring portion in the direction of thickness,
>
> said connecting terminals are made of contact plugs formed in through holes extending through the second wiring portion in the direction of thickness,
>
> sizes of opposing surfaces of said first wiring portion and said second wiring portion are equal,
>
> a thermal expansion coefficient of said second wiring portion is smaller than a thermal expansion coefficient of said first wiring portion and equal to a thermal expansion coefficient of said semiconductor chip,
>
> said semiconductor chip is a silicon chip,
>
> said second wiring portion comprises a base made of silicon, and
>
> said contact plugs are formed in said base.

Ex. 1001, 14:49–15:8.

D. The Applied References

Petitioner relies on the following references in the asserted grounds.

Pet. 19–20.

Reference	**Date**	**Exhibit**
U.S. Patent Appl. Pub. No. 2002/0180015 A1 (“Yamaguchi”)	Dec. 5, 2002	Ex. 1004
U.S. Patent No. 5,258,648 (“Lin”)	Nov. 2, 1993	Ex. 1005
U.S. Patent No. 6,617,681 B1 (“Bohr”)	Sept. 9, 2003	Ex. 1006

E. The Asserted Grounds

Petitioner sets forth its challenges to claims 1, 2, 4, and 5 as follows. Pet. 19–75.

References	Basis	Claims Challenged
Yamaguchi and Lin	§ 103	1, 4
Yamaguchi, Lin, and Bohr	§ 103	2, 5
Yamaguchi and Lin (alternative theory)	§ 103	1, 4[1]
Yamaguchi, Lin, and Bohr (alternative theory)	§ 103	2, 5

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard). Under the broadest reasonable construction standard, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). The claims, however, "'should always be read in light of the specification and teachings in the underlying patent,'" and "[e]ven under the broadest reasonable

[1] At page 20 of the Petition, this ground is listed as challenging claims 2 and 5, however the substantive discussion beginning at page 58 of the Petition clearly refers to claims 1 and 4. We consider the claim listing at page 20 to be a typographical error.

interpretation, the Board's construction 'cannot be divorced from the specification and the record evidence.'" *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (citations omitted). Further, any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a definition, however, limitations are not to be read from the specification into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

The parties propose constructions for several claim terms. *See* Pet. 12–19; Prelim. Resp. 16–17, 23–32. Upon review of the parties' contentions and supporting evidence, for purposes of this Decision, we need address only the construction of "connecting terminals," which we discuss below. *See, e.g.*, *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("[C]laim terms need only be construed 'to the extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

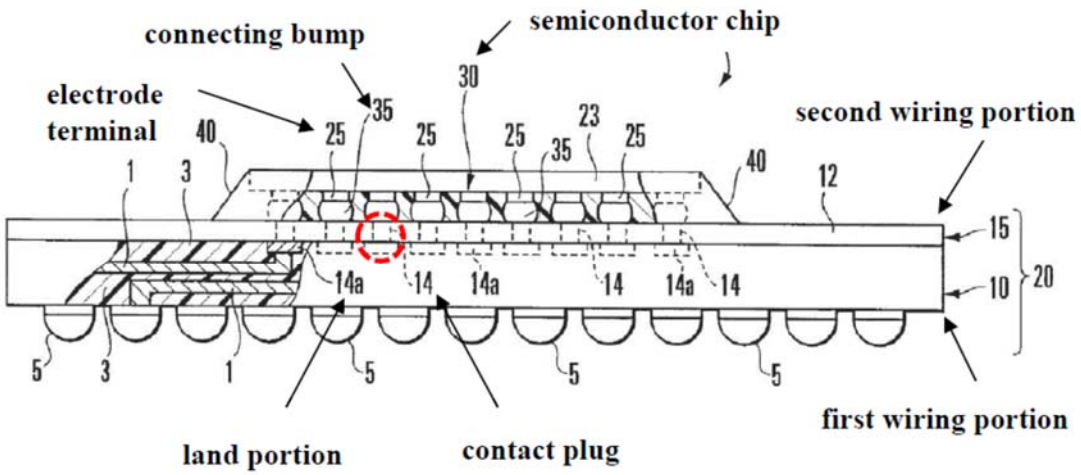
"connecting terminals"

Claim 1 recites, *inter alia*, "a wiring board comprising a plurality of connecting terminals arranged on one surface in a direction of thickness . . . [wherein] said connecting terminals are made of contact plugs formed in through holes extending through the second wiring portion in the direction of thickness." Independent claim 4 includes a similar limitation.

Petitioner does not propose a construction for the term "connecting terminals," but proposes a construction for the claimed "contact plugs" that form the claimed "connecting terminals." Pet. 13. According to Petitioner, "contact plug" means "a conductive material [that] may or may not have

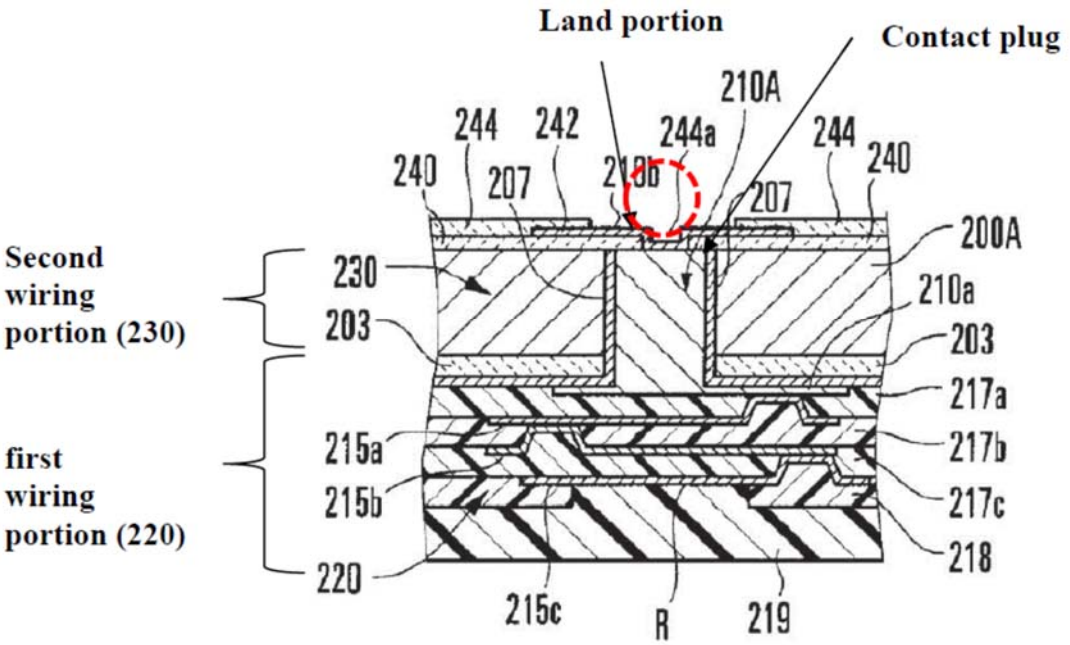
land portion(s) on one or both ends." *Id.* (citing Ex. 1002 ¶ 29; Ex. 1001, 5:17–18, 9:21–24, 9:38–39, 11:43–48, Fig. 1).

Patent Owner argues that the Petition "ignores the proper interpretation of 'connecting terminals.'" Prelim. Resp. 16. Referring to the Specification of the '189 patent, Patent Owner argues that "[t]he contact plug forms a connecting terminal of the wiring board because the wiring board *exposes the contact plug to make it accessible to make a connection to another component*." *Id.* at 24 (emphasis added). Patent Owner provides an annotated version of Figure 1 (*id.* at 25), reproduced below.



The annotated version of Figure 1, above, shows wiring board 20 connected to semiconductor chip 30, with a connecting terminal made of contact plug 14 identified by a red circle. *Id.* at 24. According to Patent Owner, "the connecting terminals connect the wiring board, via the 'connecting [solder] bumps' to a chip 30, and the number of connecting terminals on the wiring board equals the number of electrode terminals 25 on the chip 30." *Id.* (citing Ex. 1001, 5:9–17, 5:34–38).

Patent Owner also provides an annotated version of Figure 6B (*id.* at 26), reproduced below.



Annotated Figure 6B, above, shows "a more detailed cross section of an example of a connecting terminal, which has been annotated to show the location of the 'connecting bump' in red." *Id.* at 25 (citing Ex. 1001, 12:6–26). Figure 6B also illustrates land portion 210b that Petitioner asserts may or may not be included as part of the claimed "contact plug," however, according to Patent Owner, the land portion "is *exposed* in an opening in a protective film *to provide a location to which a connection can be made*, which, in this case is done via the solder ball [shown in red above] attached to the connecting terminal." *Id.* at 26 (citing Ex. 1001, 12:19–21) (emphasis added).

As evidence of the ordinary meaning of the term in the art, Patent Owner provides *The New IEEE Standard Dictionary of Electrical and*

Electronics Terms,[2] which defines a "terminal" in the semiconductor device context as "[a]n *externally available* point of connection to one or more electrodes or elements within the device." *See id.* at 27 (citing Ex. 2001, 1351) (emphasis added). Thus, according to Patent Owner, the Specification of the '189 patent uses the term "terminal," consistently with the ordinary meaning of the term in the art, as an "electrically conductive portion . . . used to connect to another device." *Id.* (citing Ex. 1001, 5:9–17, 5:34–38). Patent Owner argues that "the broadest reasonable interpretation consistent with the specification of 'connecting terminals' *requires exposed points of connection* that allow connection, such as via a solder ball." *Id.* (emphasis added).

Petitioner has not presented any evidence or argument that the construction of "connecting terminal" should be broader than the ordinary meaning of the term in the art, as discussed above. *See* 37 C.F.R. § 42.104(b)(3) ("[T]he petition must set forth . . . [h]ow the challenged claim is to be construed."). We are persuaded by Patent Owner's argument and evidence discussed above and, for purposes of this Decision, construe "connecting terminal" to require an externally available/exposed point of connection.

B. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

[2] THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS (Christopher J. Booth ed., 5th ed. 1993) (Ex. 2001).

subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.[3] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). A prima facie case of obviousness is established when the prior art, itself, would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. *See In re Rinehart*, 531 F.2d 1048, 1051 (CCPA 1976).

We analyze the asserted grounds of unpatentability in accordance with these principles.

C. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art "would have had a Bachelor's degree from an accredited institution in electrical engineering, mechanical engineering, materials science and engineering, physics, or the equivalent; working knowledge of semiconductor processing technologies for integrated circuits; and at least three years of experience in semiconductor processing analysis, design, and development. Graduate

[3] At this stage of the proceeding, the parties have not directed our attention to any objective evidence of non-obviousness.

education could substitute for professional experience." Pet. 21 (citing Ex. 1002 ¶ 11). Patent Owner does not dispute Petitioner's proposed level of ordinary skill in the art for purposes of its Preliminary Response. *See* Prelim. Resp. 15. For purposes of this Decision, we adopt Petitioner's proposal regarding the level of ordinary skill in the art. The level of ordinary skill in the art further is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

D. The Asserted Prior Art

Yamaguchi (Ex. 1004)

Yamaguchi relates to a "multi-chip module including semiconductor devices and a wiring substrate for mounting the semiconductor devices." Ex. 1004, at [57]. Figure 1 of Yamaguchi is reproduced below.

FIG.1

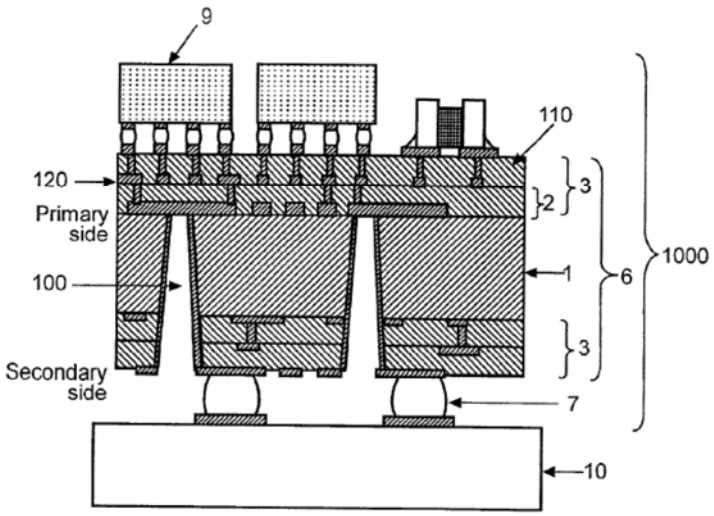


Figure 1, above, is a cross-sectional view of semiconductor module 1000 according to an embodiment of Yamaguchi. *Id.* ¶¶ 25, 59. As seen in Figure 1, semiconductor devices 9 are mounted on multi-layered wiring substrate 6, and semiconductor module 1000 is mounted on mounting substrate 10. *Id.* ¶ 59. Multi-layered wiring substrate 6 includes substrate 1 and multi-wiring layer 3. *Id.* Substrate 1 includes "through holes [100] for establishing electrical connection between the surface and rear face of the substrate." *Id.* ¶ 60. Through holes 100 may be filled with conductive material. *Id.* ¶ 87.

Multi-wiring layer 3 includes "at least one layer of thin film wiring layer 2," however Yamaguchi teaches that "the number of thin film wiring layers 2 . . . can be set freely in accordance with the design of the semiconductor module." *Id.* ¶¶ 60, 95; *see also id.* ¶ 99 ("Whether the multi-layered wiring layer 3 may be formed as a single layer or two or more layers is determined depending on the logic scale of the semiconductor device 9 and the layout therefor, or required high speed signal characteristics"). Each thin film wiring layer 2 includes wirings 120 and interlayer insulation layer 110. *Id.* ¶ 60.

Yamaguchi further describes that because "the heat expansion coefficient of [substrate 1] is close to that of silicon of the semiconductor device 9, the stress caused by the difference of the heat expansion coefficient is small and connection can be ensured between the multi-layered wiring substrate 6 and the semiconductor device 9." *Id.* ¶¶ 66, 68; *see also id.* ¶ 69 (describing an embodiment in which the heat expansion coefficient of substrate 1 "is equal with" that of semiconductor chip 9). Yamaguchi also

describes relieving thermal stress between semiconductor module 1000 and mounting substrate 10. *See id.* ¶ 71.

Lin (Ex. 1005)

Lin relates to a flip chip semiconductor device. Ex. 1005, at [57]. The semiconductor device of Lin includes interposer 22 and semiconductor die 12 mounted on the interposer. *Id.* at 4:49–53, Fig. 1. Lin further teaches that a preferred material for interposer 22 "is one that has a coefficient of thermal expansion (CTE) which closely approximates that of a semiconductor die" to "reduce[the] chance that the electrical bonds . . . will be broken as a result of thermally induced stress." *Id.* at 6:28–31, 6:40–44.

Bohr (Ex. 1006)

Bohr relates to an interposer structure for connecting an integrated circuit to a supporting substrate. Ex. 1006, at [57]. Bohr further teaches that "[v]arious circuit elements may be incorporated into the interposer," such as capacitors or transistors. *Id.* at [57], 4:21–28.

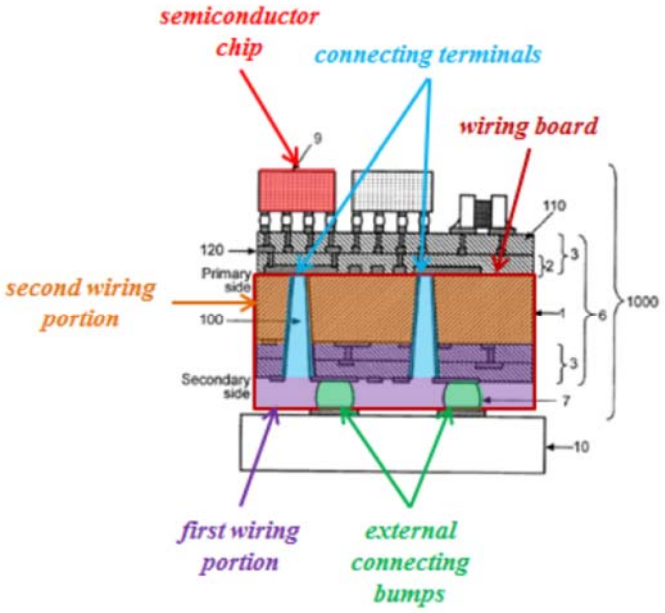
E. Asserted Obviousness Based, at Least in Part, on Yamaguchi and Lin (First Alternative)

Petitioner asserts that claims 1 and 4 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Yamaguchi and Lin. Pet. 22–52. Petitioner asserts that claims 2 and 5 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Yamaguchi, Lin, and Bohr. *Id.* at 52–57. Patent Owner argues that the asserted combinations do not teach or suggest several elements of the claims, as properly construed, and that one of skill in the art would not have combined the asserted references in the manner asserted in the Petition. Prelim. Resp. 15–55.

We have reviewed the parties' contentions and supporting evidence. Given the evidence on this record, and for the reasons explained below, we determine that the information presented does not show a reasonable likelihood that Petitioner would prevail on these asserted grounds.

Independent Claims 1 and 4

Petitioner provides an annotated version of Figure 1 of Yamaguchi, illustrating its mapping of the structural elements of the semiconductor device of Yamaguchi to the claims. Pet. 23. Petitioner's annotated Figure 1 is reproduced below.



Annotated Figure 1, above, shows a cross-sectional view of a semiconductor module of Yamaguchi, annotated by Petitioner. Illustrated in Petitioner's annotated Figure 1 of Yamaguchi and discussed in the Petition in more detail, the following table provides a summary of Petitioner's mapping of Yamaguchi to the structural elements of claim 1.

Claim 1	**Yamaguchi**
wiring board	(certain portions of) wiring substrate 6
plurality of connecting terminals (made of contact plugs formed in through holes)	through holes 100 (filled with conductive material) and wirings 120 on a top surface
plurality of external connecting bumps	solder bumps 7
at least one semiconductor chip	semiconductor devices 9
first wiring portion	(bottom) multi-layer wiring 3 and solder bumps 7
plurality of wiring layers	wirings 120 in (bottom) multi-layer wiring 3
second wiring portion	silicon substrate 1

See Pet. 22–37 (citing Ex. 1004 ¶¶ 17–19, 58–61, 66–69, 71, 75, 86, 87, 89–92, 95, 96, 101–106, 113–114, Figs. 1, 2; Ex. 1002 ¶¶ 29, 32, 57–60, claim chart at pages 42–52). Petitioner refers back to its analysis for claim 1 with respect to the similar limitations of claim 4. *See* Pet. 48–52; Ex. 1002, claim chart at pages 68–79.

In relevant part, Patent Owner argues that Yamaguchi does not teach or suggest the claimed "connecting terminals." Prelim. Resp. 23–32. Patent Owner argues that Petitioner "alleges that [the claimed 'connecting terminals'] are met by conductive material that is internal to the wiring board, not exposed as an available point of connection, and extends along a portion of a conductive path but is not a terminal where the path terminates." *Id.* at 27; *see also* Pet. 23 (Petitioner's annotated version of Figure 1 of Yamaguchi, reproduced above, with blue arrows pointing to the alleged "connecting terminals").

We agree with Patent Owner. Based on our construction of "connecting terminals," discussed above in section II.A, we are not persuaded by Petitioner's contention that Yamaguchi's internal structure comprising through holes 100 (filled with conductive material) and wirings 120 on a top surface of substrate 1 teach or suggest "connecting terminals," as claimed. We also are persuaded by Patent Owner's argument that Petitioner's identification of "terminals" is inconsistent with the usage of that term in Yamaguchi itself. *See* Prelim. Resp. 29. Yamaguchi uses the term "connection terminals" to reference certain external connecting elements of its semiconductor device (*see, e.g.*, Ex. 1004 ¶¶ 61, 80), but never refers to the internal structure relied on by Petitioner as a "terminal."

Petitioner relies on Lin only for its teaching of "matching a CTE of the entire semiconductor die 12 to a CTE of the entire interposer 22 in order to relieve stress," and does not assert Lin for any teaching relevant to the claimed "connecting terminals." *See* Pet. 46; Ex.1002, claim chart at page 66.

Accordingly, for the reasons discussed, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of showing that claims 1 and 4 are rendered obvious by the combination of Yamaguchi and Lin, under its first theory, and do not institute review on this asserted ground.

Dependent Claims 2 and 5

Claims 2 and 5 depend from claims 1 and 4, respectively, and each recites that the semiconductor device "further compris[es] a functional element formed on said second wiring portion which faces said first wiring portion." Petitioner relies on Bohr as disclosing this claim feature. Pet. 52–

57. Petitioner does not assert Bohr for any teaching relevant to the claimed "connecting terminals." *See id.*

Accordingly, for the reasons discussed above with respect to claims 1 and 4, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of showing that claims 2 and 5 are rendered obvious by the combination of Yamaguchi, Lin, and Bohr, under its first theory, and do not institute review on this asserted ground.

F. Asserted Obviousness Based, at Least in Part, on Yamaguchi and Lin (Second Alternative)

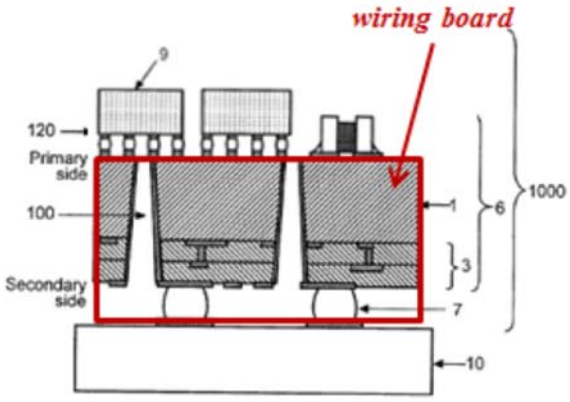
Petitioner asserts that claims 1 and 4 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Yamaguchi and Lin. Pet. 58–72. Petitioner asserts that claims 2 and 5 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Yamaguchi, Lin, and Bohr. *Id.* at 72–75. Patent Owner argues that Petitioner has not provided sufficient motivation for its proposed modification to Yamaguchi, and that one of skill in the art would not have combined the asserted references in the manner asserted in the Petition. Prelim. Resp. 55–62.

We have reviewed the parties' contentions and supporting evidence. Given the evidence on this record, and for the reasons explained below, we determine that the information presented does not show a reasonable likelihood that Petitioner would prevail on these asserted grounds.

Independent Claims 1 and 4

Petitioner's mapping of the semiconductor device Yamaguchi to the structural elements of the claims in its alternative position generally is the same as the mapping for its first position. *See* Pet. 58–72; Ex. 1002, claim

chart at pages 104–159. For its alternative position, however, Petitioner asserts that Yamaguchi would be modified as shown in a modified and annotated version of Figure 1 of Yamaguchi (Pet. 60), reproduced below.



Petitioner's modified and annotated version of Figure 1 of Yamaguchi, above, shows a cross-sectional view of a semiconductor module of Yamaguchi, as modified to remove top multi-wiring layer 3 (composed of thin film wiring layers 2) on the primary side of substrate 1. *Id.* According to Petitioner, a person of ordinary skill in the art "would be motivated to modify Yamaguchi based on Yamaguchi's teaching that 'the number of thin film wiring layers 2 formed on both surfaces of the insulation substrate 1 is **optional and can be set freely in accordance with the design of the semiconductor module**.'" *Id.* (quoting Ex. 1004 ¶ 95 (emphasis Petitioner's); also citing Ex. 1002, claim chart at page 107). Petitioner also points to the teaching in Lin that "semiconductor die 12 may be bonded to conductive traces 26 . . . on a top surface of interposer 22 by solder bumps without any intervening layers between interposer 22 and semiconductor die 12." *Id.* at 59–60 (citing Ex. 1005, 4:52–62, Fig. 4; Ex. 1002, claim chart at page 105).

Patent Owner argues that "there is no supportable rationale" for Petitioner's proposed modification to Yamaguchi. Prelim. Resp. 56; *see id.* at 56–61. First, Patent Owner argues "the Petition misinterprets Yamaguchi" (*id.* at 57). In this regard, Patent Owner argues that, while Yamaguchi teaches that the number of thin film wiring layers 2 in multi-wiring layer 3 may vary depending on how many connections are necessary in the device, there is no suggestion or teaching in Yamaguchi that they can be eliminated entirely as Petitioner asserts. *Id.* at 57–58 (citing Ex. 1004 ¶¶ 9, 72, 73, 97–99). Second, Patent Owner argues that the wiring layers on top of the substrate in Yamaguchi "perform a critical function in Yamaguchi and a [person of ordinary skill in the art] would not have eliminated them." *Id.* at 59. For example, Yamaguchi teaches that the wiring layers provide "signal wirings between the semiconductor devices 9 to each other." Ex. 1004 ¶ 97; Prelim. Resp. 59. According to Patent Owner, Petitioner "does not explain how communications between chips 9 would occur if wiring layers that include the 'signal wirings' for those communications were eliminated." Prelim. Resp. 60. Patent Owner further argues that "the Petition's modification is motivated by nothing but [an] attempt to reconstruct the claims in hindsight." *Id.* at 60–61.

Based on the record before us, we agree with Patent Owner. Yamaguchi expressly states that "multi-wiring layer 3 comprises *at least one* layer of thin film wiring layer 2," and "[w]hether the multi-layered wiring layer 3 may be formed *as a single layer or two or more layers* is determined depending on the logic scale of the semiconductor device 9 and the layout therefor, or required high speed signal characteristics." Ex. 1004 ¶¶ 60, 99 (emphases added). We discern no suggestion in Yamaguchi to remove

entirely the top multi-wiring layer, and are not persuaded by Dr. Qu's conclusory statement that a "[person of ordinary skill in the art] reading Yamaguchi in view of Lin would have understood the thin film wiring layers 2 over substrate 1 are optional and can be removed as a matter of design choice." Ex. 1002, claim chart at page 107; *see also* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."). For the reasons discussed, we are not persuaded that a person of ordinary skill in the art would have been motivated to remove top multi-wiring layer 3 on the primary side of substrate 1 of Yamaguchi. Petitioner's assertions for its alternative theory of obviousness in view of Yamaguchi and Lin are premised on this modification.

Accordingly, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of showing that claims 1 and 4 are rendered obvious by the combination of Yamaguchi and Lin, under its second theory, and do not institute review on this asserted ground.

Dependent Claims 2 and 5

Petitioner again relies on Bohr as disclosing the additional feature of dependent claims 2 and 5. Pet. 73–75. For the reasons discussed above with respect to claims 1 and 4, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of showing that claims 2 and 5 are rendered obvious by the combination of Yamaguchi, Lin, and Bohr, under its second theory, and do not institute review on this asserted ground.

III. CONCLUSION

As discussed above, we do not institute an *inter partes* review of any claim of the ’189 patent.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), no *inter partes* review is instituted as to any claim of U.S. Patent No. 7,525,189 B2.

PETITIONER:

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