

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2017-00842
Patent 7,728,439 B2

Before JENNIFER MEYER CHAGNON, SHEILA F. McSHANE, and
MELISSA A. HAAPALA, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has not shown, by a preponderance of the evidence, that claims 1, 5, 7, and 11 (“the challenged claims”) of U.S. Patent No. 7,728,439 B2 (Ex. 1001, “the ’439 patent”) are unpatentable.

A. Procedural History

Xilinx, Inc. (“Petitioner”) filed a Petition for *inter partes* review of claims 1, 5, 7, and 11 of the ’439 patent. Paper 1 (“Pet.”). Petitioner provided a Declaration of Jianmin Qu, Ph.D. (Ex. 1003) in support of its positions. Godo Kaisha IP Bridge 1 (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 7 (“Prelim. Resp.”). Pursuant to 35 U.S.C. § 314(a), on August 28, 2017, we instituted *inter partes* review on the following grounds:

whether claims 1 and 7 would have been obvious under
35 U.S.C. § 103(a) in view of Hirose¹; and

whether claims 5 and 11 would have been obvious under
35 U.S.C. § 103(a) in view of Hirose and Bohr².

¹ JP Patent Appl. No. 2001-007248, published Jan. 12, 2001 (Ex. 1006). Ex. 1006 includes both the original Japanese application and the certified English translation thereof. We cite to the English portion of the exhibit throughout. Patent Owner filed a Motion to Exclude Exhibit 1006, and portions of Exhibit 1003 based thereon. Paper 18. This Motion has been denied. Paper 36.

² U.S. Patent No. 6,617,681 B1, issued Sept. 9, 2003, filed June 28, 1999 (Ex. 1007).

See Paper 8 (“Inst. Dec.”). Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 12, “PO Resp.”), along with a Declaration of Robert Darveaux, Ph.D. (Ex. 2011³) to support its positions. Petitioner filed a Reply (Paper 14, “Pet. Reply”) to the Patent Owner Response.

³ Petitioner filed a Motion to Exclude Exhibit 2011. Paper 17. This Motion has been denied. Paper 37. Petitioner also argues in its Reply that “[t]he Board should give no weight to [Dr.] Darveaux’s Declaration because of [his] refusal to answer questions regarding the dispositive issue in this proceeding – including the very issue upon which he opined in his declaration – thus disqualify his opinion from having any evidentiary weight.” Pet. Reply 17; *see id.* at 17–24. In particular, Petitioner contends that Dr. Darveaux “flatly refused to construe, define or even address what he meant by the crucial claim term ‘equal.’” *Id.* at 18. Petitioner contends:

[Dr.] Darveaux’s testimony can be distilled down to two oft-repeated and entirely self-contradictory points: (1) [Dr.] Darveaux does not know (or refuses to state) what “equal to” means, but (2) nonetheless [Dr.] Darveaux opines that Hirose does not disclose CTEs that are “equal to” each other. Either [Dr.] Darveaux’s first point is intentionally untrue, or else [Dr.] Darveaux’s second point is completely unsupported. In either event, [Dr.] Darveaux’s cross-examination testimony completely undermines any credibility to his original declaration.

Id. at 23. Notably, however, neither Petitioner nor Dr. Qu proposes a construction for the term “equal to” in this proceeding. *See generally* Pet.; Pet. Reply; *see* Tr. 20:9–21:6, 46:17–21. At oral hearing, Patent Owner argued that express construction of the term “equal to” was unnecessary to compare the prior art to the claims. *See* Tr. 58:3–6; *id.* at 47:1–11. As discussed herein, we agree with Patent Owner that express construction of the term “equal to” beyond its plain meaning is unnecessary in order to assess the sufficiency of Petitioner’s contentions in this proceeding. We, thus, are not persuaded that Dr. Darveaux’s hesitation to provide an express definition of the term “equal to” during his cross-examination is reason to discount entirely his testimony, particularly in view of Petitioner’s lack of proposed construction of the same term.

On April 24, 2018, the Supreme Court held that a final written decision in an *inter partes* review must decide the patentability of all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (“SAS”). Pursuant to SAS, on May 1, 2018, we instituted *inter partes* review on the following additional grounds:

whether claims 1 and 7 are unpatentable under 35 U.S.C. § 102 as anticipated by Milkovich⁴; and

whether claims 5 and 11 would have been obvious under 35 U.S.C. § 103(a) in view of Milkovich and Bohr.

See Paper 31; see also *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360–61 (Fed. Cir. 2018) (reading “the SAS opinion as interpreting the statute to require a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”); *Guidance on the Impact of SAS on AIA Trial Proceedings* (April 26, 2018) (available at <https://www.uspto.gov/patents-application-process/patent-trial-and-appealboard/trials/guidance-impact-sas-aia-trial>) (“[I]f the PTAB institutes a trial, the PTAB will institute on all challenges raised in the petition.”). By agreement of the parties, no additional briefing on the Milkovich grounds was authorized. See Papers 32, 38; Ex. 2020 (transcript of April 30, 2018 conference call), 14:14–15:15, 16:10–13, 16:19–24.

An oral hearing was held on May 3, 2018. A transcript of the hearing is included in the record. Paper 34 (“Tr.”).

⁴ U.S. Patent No. 6,399,892 B1, issued June 4, 2002 (Ex. 1005).

B. Related Proceedings

The parties indicate that the '439 patent is the subject of the following district court proceeding: *Xilinx, Inc. v. Godo Kaisha IP Bridge 1*, Case No. 3:17-cv-00509 (N.D. Cal.). Pet. 1; Paper 4, 1. This proceeding appears to have been dismissed according to a stipulation by the parties. *See Xilinx, Inc. v. Godo Kaisha IP Bridge 1*, No. 3:17-cv-00509-JD, 2017 WL 6993548 (N.D. Cal. June 16, 2017).

C. The '439 Patent

The '439 patent is titled “Semiconductor Device, Wiring Substrate, and Method for Manufacturing Wiring Substrate,” and was filed as PCT application No. PCT/JP03/14917 on November 21, 2003. Ex. 1001, at [22], [54], [86]. The application entered the U.S. national stage as application No. 10/536,025, meeting the requirements under 35 U.S.C. § 371 on May 23, 2005. *Id.* at [21], [86]. The '439 patent claims priority to Japanese application No. 2002-337376, filed November 21, 2002. *Id.* at [30].

The '439 patent relates to improving the reliability of a wiring substrate and semiconductor apparatus “by reducing the internal stress caused by the difference in thermal expansion coefficients between a base substrate and a semiconductor chip.” *Id.* at [57]. Figure 2A of the '439 patent, as annotated by Petitioner showing structural elements of claim 1 (Pet. 7), is reproduced below.

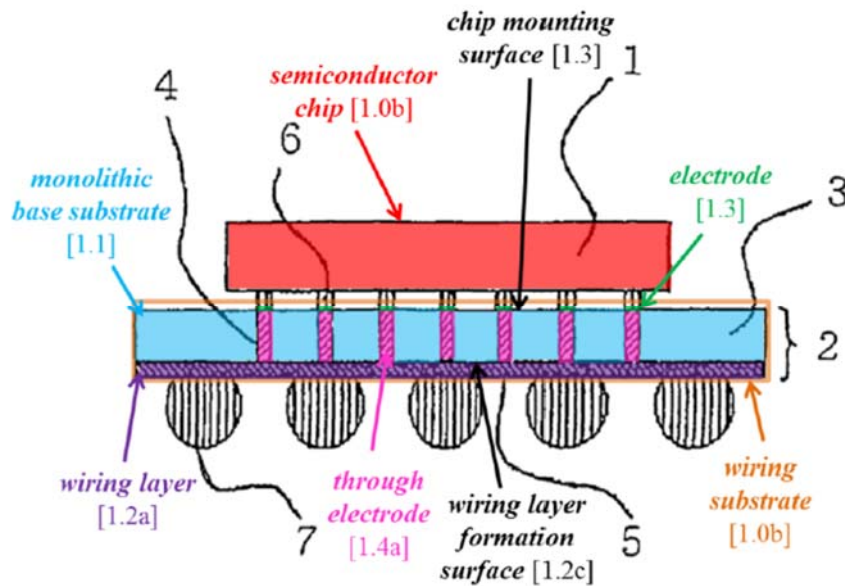


Figure 2A, above, is a cross-sectional view of a semiconductor apparatus according to a first embodiment of the '439 patent, as annotated by Petitioner. Ex. 1001, 6:52–54. As shown in Figure 2A, wiring substrate 2 includes base substrate 3 and wiring layer(s) 5 formed on one side thereof. *Id.* at 7:31–33. Bumps 7 are provided for external bonding. *Id.* at 7:34–35. Through-electrodes 4 “electrically connect[] wiring substrate 5 and an electrode terminal on the other side of base substrate 3” (i.e., “chip mounting surface”). *Id.* at 7:35–39. The “electrode terminal . . . and semiconductor chip 1 are electrically and mechanically bonded with internal bonding bump 6.” *Id.* at 7:39–40. “Functional elements, for example, a capacitor, a resistor, and an inductor are fabricated in wiring layer 5.” *Id.* at 8:38–39.

According to the '439 patent, a “thermal expansion coefficient of base substrate 3 . . . is substantially equal to that of semiconductor chip 1 and less than that of wiring layer 5.” *Id.* at 7:43–45. Because of these relative

thermal expansion coefficients (or “CTEs”⁵), “a stress caused by the difference of thermal expansion coefficient between semiconductor chip 1 and base substrate 3 is substantially small.” *Id.* at 7:45–48. When silicon is used for semiconductor chip 1, the ’439 patent teaches appropriate materials for forming base substrate 3 include silicon, ceramics, or photosensitive glass. *See id.* at 9:53–59.

D. Illustrative Claim

Of the challenged claims, claims 1 and 7 are independent. Claims 5 and 11 depend from claims 1 and 7, respectively. Independent claim 1 of the ’439 patent is reproduced below, and is illustrative of the challenged claims.

1. A semiconductor apparatus in which a semiconductor chip is mounted on a wiring substrate with Flip-Chip,

wherein the wiring substrate comprises:

a monolithic base substrate formed from any one of a silicon, a ceramic, or a photosensitive glass;

a wiring layer having an insulating layer and a wiring formed on a wiring layer formation surface which is one surface of the monolithic base substrate;

an electrode formed on a chip mounting surface which is a backside of the wiring layer formation surface of the monolithic base substrate; and

a through-electrode formed on the monolithic base substrate electrically connecting the wiring layer formed on the

⁵ *See* Ex. 1003 ¶ 41 n.1 (Dr. Qu noting that the “coefficient of thermal expansion” (“CTE”) is referred to in the art using different phrases, including “thermal expansion coefficient”). The CTE “is a physical property of a material and is a measurement of the linear expansion of the material per unit change in temperature.” *Id.* ¶ 41.

wiring layer formation surface and the electrode formed on the chip mounting surface,

wherein a thermal expansion coefficient of the monolithic base substrate is equal to a thermal expansion coefficient of the semiconductor chip, and the thermal expansion coefficient of the monolithic base substrate is less than a thermal expansion coefficient of the wiring layer,

wherein the semiconductor chip is bonded to the chip mounting surface with face-down.

Ex. 1001, 13:57–14:11.

II. ANALYSIS

A. *Principles of Law*

To prevail in its challenges to the patentability of the claims, Petitioner must demonstrate by a preponderance of the evidence that the challenged claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). The burden of persuasion never shifts to Patent Owner. See *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378–79 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burdens of persuasion and production in *inter partes* review).

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference.

See Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *accord In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). Further, to be anticipating, a prior art reference must be enabling and must describe the claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000); *In re Paulsen*, 30 F.3d 1475, 1479 (Fed. Cir. 1994).

A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁶ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art

⁶ The parties have not directed our attention to any objective evidence of non-obviousness.

would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007).

In an *inter partes* review, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record” to support an obviousness determination. *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380–81 (Fed. Cir. 2016). The “factual inquiry . . . must be thorough and searching, and the need for specificity pervades.” *In re NuVasive, Inc.*, 842 F.3d 1376, 1381–82 (Fed. Cir. 2016) (internal quotations and citations omitted). A determination of obviousness cannot be reached where the record lacks “explanation as to *how* or *why* the references would be combined to produce the claimed invention.” *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016); *see NuVasive*, 842 F.3d at 1382–85; *Magnum Oil*, 829 F.3d at 1380–81. Thus, to prevail Petitioner must explain how the prior art would have rendered the challenged claim unpatentable.

At this final stage, we determine whether a preponderance of the evidence of record shows that the challenged claims would have been anticipated by or rendered obvious in view of the asserted prior art. We analyze the asserted grounds of unpatentability in accordance with these principles.

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have a Bachelor’s degree from an accredited institution in [] electrical engineering, mechanical engineering, materials science and engineering, physics, or the equivalent, working knowledge of semiconductor processing technologies for integrated circuits, and at least three years of experience in

semiconductor processing analysis, design, and development. Graduate education could substitute for professional experience, and significant work experience could substitute for formal education.

Pet. 20–21 (citing Ex. 1003 ¶ 11). Patent Owner “does not dispute Petitioner’s asserted level of ordinary skill in the art.” PO Resp. 22; *see also* Ex. 2011 ¶ 29 (Dr. Darveaux agreeing with Petitioner’s and Dr. Qu’s description of a person of ordinary skill in the art). For purposes of this Final Written Decision, and based on the complete record now before us, we adopt Petitioner’s proposal regarding the level of ordinary skill in the art. The level of ordinary skill in the art in this case further is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). “Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history.” *TriVascular*, 812 F.3d at 1062 (citing *Straight Path IP Grp., Inc. v. Sipnet EU S.R.O.*, 806 F.3d 1356, 1362 (Fed. Cir. 2015)). “Even under the broadest reasonable interpretation, the Board’s construction ‘cannot be divorced from the specification and the record evidence.’” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015)

(citations omitted). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *See In re Paulsen*, 30 F.3d at 1480 (Fed. Cir. 1994). In the absence of such a definition, however, limitations are not to be read from the specification into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

Claims 1 and 7 recite, “wherein a thermal expansion coefficient of the monolithic base substrate is equal to a thermal expansion coefficient of the semiconductor chip” (the “equal CTEs limitation”). The parties dispute whether the asserted references disclose or render obvious this claim limitation. The Decision on Institution did not construe the term “equal to” in the equal CTEs limitation of claims 1 and 7. In discussing the asserted grounds, however, the Decision cited to dictionary definitions of “equal” and “match” as relevant to the equal CTEs limitation. Specifically, the Decision cited to a dictionary defining “equal” as “1a(1): ‘of the same measure, quantity, amount, or number as another;’ or 1a(2): ‘identical in mathematical value or logical denotation’” (Inst. Dec. 18 (quoting *Equal Definition*, MERRIAM-WEBSTER.COM (available at <https://www.merriam-webster.com/dictionary/equal>))), and defining “match” as “1a: ‘a person or thing equal or similar to another’” (*id.* at 23 (quoting *Match Definition*, MERRIAM-WEBSTER.COM (available at <https://www.merriam-webster.com/dictionary/match>))).

In the post-institution briefing, neither party proffered an express construction for the term “equal to,” nor provided declaratory expert testimony for the construction of that term. *See generally* PO Resp.; Pet. Reply; Ex. 1003; Ex. 2011; *see also* Tr. 20:9–21:6 (Petitioner’s counsel indicating, “[t]here is no definition, I guess, necessarily on the record for

‘equal.’ What we know, or what we put forth in our petition, is that equal is narrower than matched. . . . And so once Hirose’s matched is -- you know, once Hirose teaches matched, from there you can, you can optimize to *whatever the appropriate definition of equal is.*” (emphases added)), 46:17–21 (Patent Owner’s counsel, in response to the question “What does ‘equal’ . . . mean?”, indicating, “[s]o that’s an issue that hasn’t been raised in the proceeding and nobody has answered it and you asked the same question to petitioner. They didn’t answer it.”).

For purposes of this Final Written Decision, we apply the plain meaning of the term equal, and use the dictionary definitions discussed above as evidence of the plain meaning. As discussed below in more detail in our analysis of the asserted grounds, we agree with Patent Owner that further express construction of the term “equal to” is unnecessary to assess the sufficiency of Petitioner’s contentions. *See* Tr. 47:1–11.

The parties’ dispute does not require express construction of any other claim term.⁷ *See, e.g., See Nidec Motor Corp. v. Zhongshan Broad Ocean*

⁷ The Decision on Institution addressed the construction of a “wiring layer having an insulating layer and a wiring formed on a wiring layer formation surface of the monolithic base substrate.” *See* Inst. Dec. 7–8. In particular, the panel was “not persuaded by Patent Owner’s argument that any particular processing techniques are required in order to meet this claim limitation.” *Id.* at 8. Patent Owner did not renew its arguments regarding this limitation in its Patent Owner Response. *See generally* PO Resp.; *see also* Paper 9, 5 (cautioning Patent Owner “that any arguments for patentability not raised in the [Patent Owner Response] will be deemed waived”); *NuVasive*, 842 F.3d at 1380–81 (determining Patent Owner waived arguments made only in its Preliminary Response but not raised in the Patent Owner Response after institution). Further consideration of this claim limitation is not necessary to resolve any dispute between the parties for purposes of this Final Written Decision.

Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. The Asserted Prior Art

Milkovich (Ex. 1005)

Milkovich relates to a “multilayer CTE compensated chip interposer for connecting a semiconductor chip to a laminate chip carrier.” Ex. 1005, at [57]. Figure 4 of Milkovich is reproduced below.

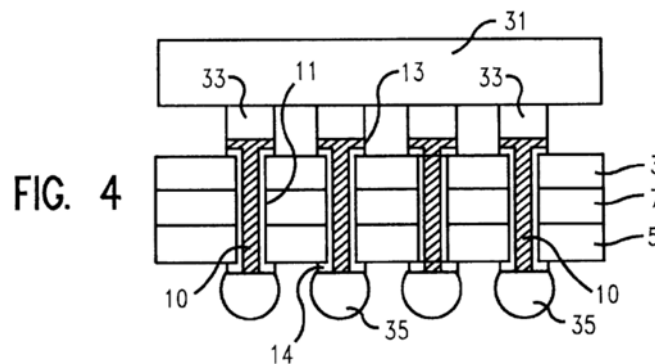


Figure 4, above, is a cross-sectional view of the multilayer CTE compensated chip interposer according to Milkovich, with a chip mounted thereon. *Id.* at 3:30–32. As seen in Figure 4, the CTE compensated interposer 1 (labeled in Figure 1) includes top layer 3, intermediate layer 7, and bottom layer 5. *Id.* at 3:48–50. Chip 31 is mounted on the CTE compensated interposer via solder balls 33. *Id.* at 7:22–24. Vias have walls plated with copper 11, for example, and are filled with solder 10. *Id.* at 3:58–60, 7:27–29. “The vias terminate at opposing interposer surface with pads 13 and 14, which may also be copper, for example.” *Id.* at 3:60–62.

“Solder balls 35 are attached to interposer pads 14 for mounting to a laminate chip carrier.” *Id.* at 7:25–26.

According to Milkovich, “top layer 3, bottom layer 5 and intermediate layer 7 are each made of dielectric materials having a different CTE, with the CTEs of top layer 3 and bottom layer 5 selected to closely match the CTEs of the nearest material.” *Id.* at 3:66–4:3. Milkovich continues:

Thus, top layer 3, upon which a semiconductor chip is to be mounted, is selected from materials hav[ing] a CTE closely matching the CTE of a semiconductor chip. . . . Materials suitable for this purpose are[:] ceramic material which has a CTE of around 5 PPM per degree C. . . . ; glass which has a CTE of about 4 to 8 PPM per degree C. . . . ; and silicon which has a CTE of about 3.4 PPM per degree C. . . . Thus, materials having a range of CTEs between 3 and 8 PPM per degree C. . . . would be sufficient for this purpose.

Id. at 4:3–18. Similarly, “[b]ottom layer 5 of CTE compensated chip interposer 1 is selected from an embedded core laminate material that closely matches the CTE of the chip carrier laminate upon which the chip, with interposer, is to be mounted.” *Id.* at 4:23–26. Typically, “materials having . . . a composite CTE within the range of about 15 to 20 PPM per degree C. are sufficient for this purpose.” *Id.* at 4:41–45. For intermediate layer 7, “it would be sufficient to have a conductive/dielectric laminate material combination exhibiting a composite CTE in the range of about 9 to 14 PPM per degree C.” *Id.* at 5:43–45.

Hirose (Ex. 1006)

Hirose relates to a package substrate for mounting an IC chip or other electronic parts, in which the package substrate includes “an interlayer resin

insulation layer and a wiring layer built up on a ceramic board.” Ex. 1006

¶ 1. Figure 5 of Hirose is reproduced below.

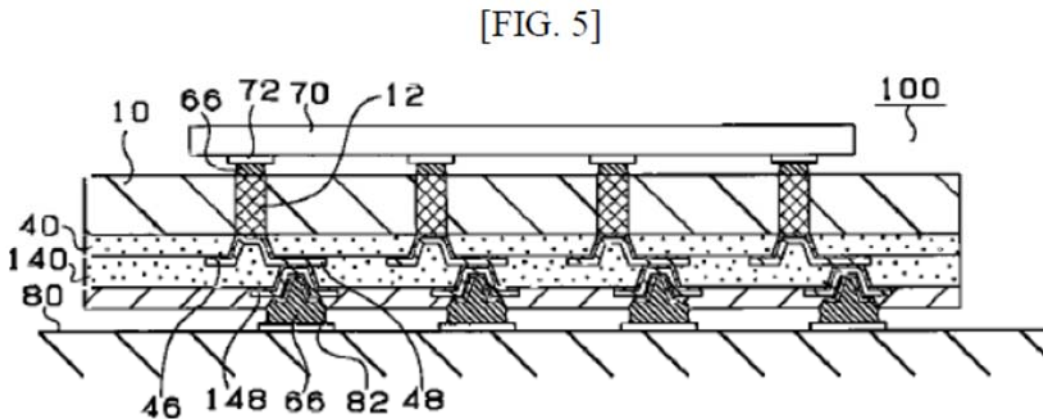


Figure 5, above, shows an embodiment of package substrate 100, according to Hirose. Package substrate 100 includes ceramic board 10 and interlayer resin insulation layers 40, 140. *Id.* ¶ 10. Via holes 46 and conductor circuits 48 are formed in interlayer resin insulation layer 40, and via holes 146⁸ that are connected to conductor circuits 48 are formed in interlayer resin insulation layer 140. *Id.* Through-holes 12, which may be “formed by firing silver metallizing ink” (*id.* ¶ 30), are formed in ceramic board 10. *Id.* ¶ 10. IC chip 70 is connected to the external board (i.e., daughter board 80) via the following path: pads 72 – bumps 66 – through-holes 12 – via holes 46 – conductor circuits 48 – via holes 146 – bumps 66 – pads 82. *Id.* ¶ 11.

According to Hirose, the package substrate of the embodiments described therein can “absorb the difference in thermal expansion between the [IC chip and an external board],” in order to avoid cracking caused by

⁸ Via holes 146 appear to be mislabeled as 148 in Figure 5.

the difference in thermal expansion seen in prior art package substrates. *Id.*

¶¶ 2–3. In particular, in the embodiments of Hirose,

an IC chip that has a low coefficient of thermal expansion is attached on the side of a ceramic board that has a low coefficient of thermal expansion, and an external board that is composed of a resin and has a high coefficient of thermal expansion is attached on the side of interlayer resin insulation layers that have a high coefficient of thermal expansion, thereby preventing the cracking and so forth attributable to a difference in thermal expansion.

Id. ¶ 8; *see id.* ¶ 12. Hirose recognized that “cracking is less likely to occur at the interlayer resin insulation layers [(i.e., in the vias, conductor circuits, or insulation layers)] because the coefficients of thermal expansion are matched.” *Id.* ¶ 33; *see also id.* ¶ 7 (recognizing that, in the prior art, the “cracks . . . are attributable to the fact that an IC chip that is composed of silicon and has a low coefficient of thermal expansion is attached over an interlayer resin insulation layer that has a high coefficient of thermal expansion, and an external board that is composed of a resin and has a high coefficient of thermal expansion is attached on the side of a ceramic board that has a low coefficient of thermal expansion.”).

Bohr (Ex. 1007)

Bohr relates to an interposer structure for connecting an integrated circuit to a supporting substrate. Ex. 1007, at [57]. Bohr further teaches, “[v]arious circuit elements may be incorporated into the interposer,” such as capacitors or transistors. *Id.* at [57], 4:21–28.

E. Asserted Grounds Based on Milkovich

Petitioner asserts that claims 1 and 7 are unpatentable under 35 U.S.C. § 102 as anticipated by Milkovich, and that claims 5 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Milkovich and Bohr.

Pet. 21–53. Patent Owner disagrees. See Prelim. Resp.⁹ 18–35. Having considered the complete record now before us, we determine that Petitioner has not demonstrated, by a preponderance of the evidence, that claims 1 and 7 are unpatentable as anticipated by Milkovich or that claims 5 and 11 are unpatentable as obvious in view of Milkovich and Bohr.

1. Anticipation by Milkovich – Independent Claims 1 and 7

Petitioner provides an annotated version of Figure 4 of Milkovich, illustrating its mapping of the structural elements of the interposer structure of Milkovich to the claims. Pet. 23. Petitioner’s annotated Figure 4 is reproduced below.

⁹ As noted above, we did not institute *inter partes* review on these grounds in the Decision on Institution, but these grounds subsequently were instituted in response to the Supreme Court’s Decision in SAS. See Papers 8, 31. No additional briefing on the Milkovich grounds was authorized (see Papers 32, 38); we, thus, rely on the parties’ arguments in the Petition and Preliminary Response in discussing these grounds.

See Pet. 21–36 (citing Ex. 1005, 1:7–10, 1:12–24, 2:21–28, 2:45–46, 3:46–47, 3:58–62, 4:3–5, 4:10–14, 4:24–5:8, 5:25–30, 5:48–60, 6:36–40, 7:21–29, Figs. 2–4; Ex. 1003 ¶¶ 62, 63, claim chart at pages 35–45). Petitioner refers back to its analysis for claim 1 with respect to the similar limitations of claim 7. See Pet. 39–47; Ex. 1003, claim chart at pages 49–59.

Claims 1 and 7 further include the equal CTEs limitation, which requires that the CTE of the monolithic base substrate (i.e., top layer 3 of Milkovich) is “equal to” the CTE of the semiconductor chip (i.e., chip 31 of Milkovich). Regarding this claim feature, Petitioner points to the disclosure in Milkovich that “top layer 3 . . . is selected from materials have a CTE *closely matching* the CTE of a semiconductor chip.” Ex. 1005, 4:3–6 (emphasis added); Pet. 36. Petitioner further relies on the specific examples of materials for top layer 3, provided in Milkovich, which are summarized as “materials having a range of CTEs between 3 and 8 PPM per degree C.” Ex. 1005, 4:15–16; Pet. 36. As Petitioner notes, Milkovich also teaches that the CTE for a typical semiconductor chip may be about 3 PPM per degree C. Pet. 36 (citing Ex. 1005, 1:38–41). Thus, according to Petitioner, “Milkovich discloses that a semiconductor chip (*e.g.*, chip 31) has a CTE of about 3 PPM per degree C, which is equal to a CTE of top layer 3 (3 PPM per degree C).” *Id.* (citing Ex. 1003, claim chart at page 46).

Patent Owner argues that Milkovich does not disclose the equal CTEs limitation. See Prelim. Resp. 18–19, 26–30. Patent Owner asserts that Milkovich’s disclosure of “closely matched” CTEs is not sufficient for Petitioner’s asserted anticipation ground to disclose CTEs that are “equal,” as claimed. *Id.* at 18. According to Patent Owner, none of the examples Milkovich provides as materials suitable for top layer 3 has a CTE equal to

that of chip 30 (which is about 3 PPM per degree C.). *Id.* at 26–27.

As noted by Patent Owner, the actual examples provided in Milkovich are as follows: “ceramic material which has a CTE of around 5 PPM per degree C.,” “glass which has a CTE of about 4 to 8 PPM per degree C.,” or “silicon which has a CTE of about 3.4 PPM per degree C.” Ex. 1005, 4:10–15; Prelim. Resp. 27.

Patent Owner also argues that, although Milkovich “states more generally that suitable materials for [top] layer 3 . . . can have a CTE in a range between 3 and 8 PPM/°C.,” “the disclosure of a range does *not* disclose every value in a range,” and Petitioner has not demonstrated that Milkovich teaches the equal CTEs limitation “with sufficient specificity” to satisfy its burden to demonstrate anticipation of the claims. Prelim. Resp. 27–29 (citing Ex. 1005, 4:15–18; *Atofina v. Great Lakes Chem. Corp.*, 441 F.3d 991, 999–1000 (Fed. Cir. 2006)). Patent Owner further argues:

Milkovich does not teach with “sufficient specificity” a desirability of using a material in forming [top] layer 3 . . . that would result in the layer 3 having a CTE equal to that of chip 31. Milkovich teaches only that the CTEs be “closely matched,” explicitly characterizes CTEs that are ***not equal*** as being closely matched, and . . . teaches a need to consider criteria beyond CTE (including the elastic modulus) in selecting the material for the alleged wiring substrate.

Id. at 29; *see also id.* at 29–30 (discussing in more detail the material selection process of Milkovich, which takes into account at least the elastic modulus of the materials, in addition to the CTE of the materials). We agree with Patent Owner that Petitioner has not shown sufficiently that Milkovich discloses the equal CTEs limitation. Considering the disclosure of Milkovich as a whole, we are not persuaded that Milkovich discloses top

layer 3 having a CTE “equal to” that of chip 31 with sufficient specificity. In particular, none of the examples in Milkovich discloses a chip interposer in which top layer 3 has a CTE that is equal to the CTE of chip 31.

Further, we agree with Patent Owner that disclosure of “materials having a range of CTEs between 3 and 8 PPM per degree C.” (Ex. 1005, 4:15–16) for top layer 3 is disclosure “only that of a range, not a specific [value] in that range, and the disclosure of a range is no more a disclosure of the end points of the range than it is of each of the intermediate points.” *Atofina*, 441 F.3d at 1000. Even were we to consider the specific values in the range of CTE values disclosed in Milkovich, Petitioner relies on Milkovich’s teachings that materials having a CTE of 3 PPM per degree C. would be sufficient for top layer 3, and that the CTE for a typical semiconductor chip may be about 3 PPM per degree C. *See* Pet. 36. Petitioner has not provided any argument or evidence that disclosure of values of “about” the same number equates to the required “equal to” claim limitation. Thus, we are not persuaded that Petitioner has met its burden to demonstrate that 3 PPM per degree C. and *about* 3 PPM per degree C. are “equal to” each other within the meaning of claims 1 and 7 of the ’439 patent. *See* 37 C.F.R. § 42.104(b)(3) (“[T]he petition must set forth . . . [h]ow the challenged claim is to be construed.”); *Harmonic Inc.*, 815 F.3d at 1363 (“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.”) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”))). Dr. Qu’s testimony closely tracks the Petition, and merely provides a statement that “Milkovich

discloses that a semiconductor chip (*e.g.*, the chip 31) has a CTE of about 3 PPM per degree C. and that, depending upon the material composition, the top layer 3 can have a CTE of 3 PPM per degree C. Thus, the top layer 3 has a CTE equal to the CTE of the semiconductor chip 31,” without further explanation. Ex. 1003, claim chart at page 46; *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Accordingly, for the reasons discussed, we are not persuaded that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1 and 7 are anticipated by Milkovich.

2. Obviousness in View of Milkovich and Bohr – Claims 5 and 11

Claims 5 and 11 depend from claims 1 and 7, respectively, and each recites, “wherein a functional element is formed on at least any one of the wiring layer formation surface or the wiring layer.” Petitioner relies on Bohr as disclosing this claim feature. Pet. 48–53. Petitioner does not assert Bohr for any teaching relevant to the equal CTEs limitation. *See generally id.*; *see also id.* at 49 (“As discussed above, Milkovich discloses every element of [independent] claim 1.”), 52 (similar statement for independent claim 7). Accordingly, for the reasons discussed above with respect to claims 1 and 7, we are not persuaded that Petitioner has demonstrated, by a preponderance of the evidence, that claims 5 and 11 are rendered obvious by the combination of Milkovich and Bohr.

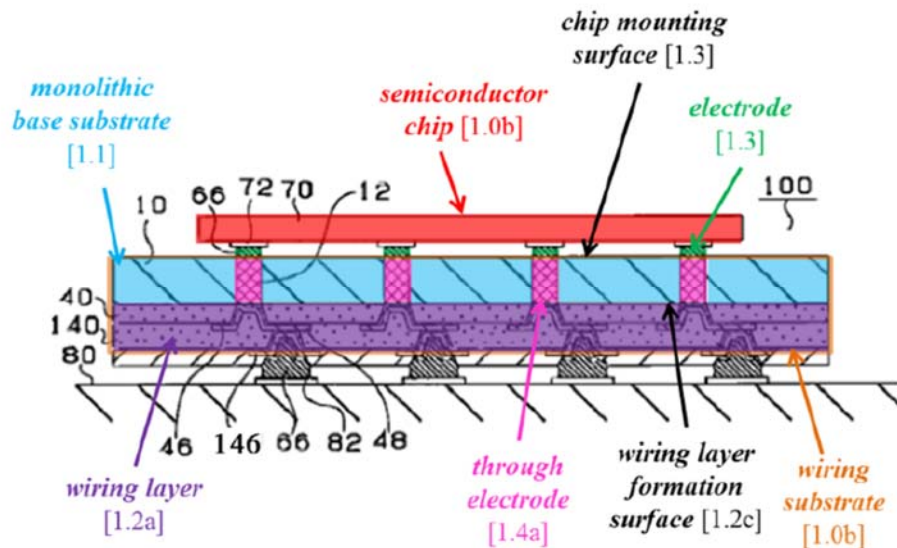
F. Asserted Grounds Based on Hirose

Petitioner asserts that claims 1 and 7 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Hirose, and that claims 5 and 11 are

unpatentable under 35 U.S.C. § 103(a) as obvious in view of Hirose and Bohr. Pet. 53–82. Patent Owner disagrees. See PO Resp. 22–46. Having considered the complete record now before us, we determine that Petitioner has not demonstrated, by a preponderance of the evidence, that claims 1 and 7 are unpatentable as obvious in view of Hirose or that claims 5 and 11 are unpatentable as obvious in view of Hirose and Bohr.

1. Obviousness in view of Hirose – Independent Claims 1 and 7

Petitioner provides an annotated version of Figure 5 of Hirose, illustrating its mapping of the structural elements of the semiconductor device of Hirose to the claims. Pet. 54. Petitioner’s annotated Figure 5 is reproduced below.



Annotated Figure 5, above, shows package substrate 100 of Hirose, as annotated by Petitioner. Illustrated in Petitioner’s annotated Figure 5 of Hirose and discussed in the Petition in more detail, the following table provides a summary of Petitioner’s mapping of Hirose to the structural elements of claim 1.

Claim 1		Hirose
semiconductor chip		IC chip 70
wiring substrate		package substrate 100
monolithic base substrate		ceramic board 10
wiring layer	insulating layer	interlayer resin insulation layers 40, 140
	wiring	via holes 46, 146 and conductor circuits 48
electrode		solder bump 66 / top end of through-hole 12
through-electrode		through-hole 12

See Pet. 53–66, 69–71 (citing Ex. 1006 ¶¶ 1–3, 7, 10–12, 18–24, 28, 30, 33; Ex. 1003 ¶¶ 67–69, claim chart at pages 67–78, 80–82). Petitioner refers back to its analysis for claim 1 with respect to the similar limitations of claim 7. See *id.* at 71–77; Ex. 1003, claim chart at pages 82–92.

Claims 1 and 7 further include the equal CTEs limitation, which requires that the CTE of the monolithic base substrate (i.e., ceramic board 10 of Hirose) is “equal to” the CTE of the semiconductor chip (i.e., IC chip 70 of Hirose). Regarding this limitation, Petitioner asserts, “Hirose recognizes that differences in CTEs between chip 70 and ceramic board 10 can cause cracking,” and “solves this problem by matching the CTE of chip 70 and the CTE of ceramic board 10.” Pet. 67 (citing Ex. 1006 ¶¶ 12, 30; Ex. 1003, claim chart at pages 78–79); see *id.* at 77 (referring back to claim 1 discussion for claim 7; citing Ex. 1003, claim chart at pages 92–93). Petitioner argues that, in Hirose, “the CTEs of chip 70 and ceramic board 10 are matched, for example, to prevent cracking.” *Id.* at 67 (citing Ex. 1006 ¶¶ 12, 33; Ex. 1003, claim chart at pages 78–79). Petitioner also argues, “Hirose recognizes the relationship of the CTEs of chip 70 and ceramic board 10 as a result-effective variable, i.e., a variable which achieves a

recognized result. Thus, it would be obvious for a [person of ordinary skill in the art] to reach the claimed relationship of the CTEs (*e.g.*, equal CTEs) through routine experimentation and optimization.” *Id.* (citations omitted). Based on the evidence available at institution, we considered Hirose’s teaching of “matched” CTEs (Ex. 1006 ¶ 33), along with Dr. Qu’s testimony that a person of ordinary skill in the art could reach equal CTEs “through routine experimentation and optimization” (Ex. 1003, claim chart at page 79), sufficient to demonstrate a reasonable likelihood that Hirose teaches or suggests the equal CTE’s limitation of claims 1 and 7. *See* Inst. Dec. 21–23.

In its Patent Owner Response, Patent Owner presents several arguments against Petitioner’s obviousness challenge of the independent claims in view of Hirose. *See* PO Resp. 22–43. Petitioner presents several arguments in response thereto in its Reply. *See* Pet. Reply. 3–15. We discuss certain aspects of the parties’ arguments below. Because, as discussed below, we are persuaded by Patent Owner’s contentions on these points, we do not rely on or discuss the other arguments presented in the Patent Owner Response or Petitioner’s Reply thereto.

As noted above, Petitioner relies on Hirose’s teaching that “the CTEs of chip 70 and ceramic board 10 are *matched*,” to show that Hirose teaches or suggests making the CTEs of chip 70 and ceramic board 10 *equal* “through routine experimentation and optimization.” Pet. 67 (citing Ex. 1006 ¶¶ 12, 33; Ex. 1003, claim chart at pages 78–79) (emphasis added). Patent Owner argues that the “Institution Decision unreasonably interpreted ‘matched’ to mean ‘equal,’ even while acknowledging that ‘matched’ could

also mean ‘similar.’”¹⁰ PO Resp. 32 (citing Inst. Dec. 23). According to Patent Owner, a person of ordinary skill in the art “would have understood ‘match’ in the context of Hirose to mean make ‘**similar**,’ not to make ‘**equal**.’” *Id.* at 32–33 (emphasis Patent Owner’s). Patent Owner also argues that “[o]nce the layers of Hirose’s package substrate are rearranged as in Figure 5, Hirose no longer recognizes any problem with CTE differences in the device and there is no suggestion that further optimization is needed.” *Id.* at 14 (citing Ex. 2011 ¶¶ 59, 71–74, 79). According to Patent Owner, Hirose provides no suggestion to further modify the Figure 5 embodiment to have equal CTEs because “[t]here is no disclosure in Hirose that [this embodiment] suffers from the ‘cracks’ that made prior art devices unreliable.” *Id.* at 42.

Petitioner argues, in its Reply, that “‘matched’ is at least broad enough to encompass ‘equal’ CTEs, and thus, it would have been obvious for a [person of ordinary skill in the art to make the CTE of ceramic board 10 ‘equal to’ the CTE of chip 70 through routine experimentation and optimization of a result-effective variable.” Pet. Reply 3–4. Petitioner also argues that a person of ordinary skill in the art “would [have] be[en] motivated . . . to minimize the difference of the CTEs of ceramic board 10 and chip 70 until they are equal.” *Id.* at 8.

Hirose teaches that cracking in the vias, the conductor circuits, and the interlayer resin insulation layers is caused by the difference in thermal

¹⁰ The Decision on Institution did not construe the term “matched” (which does not appear in the challenged claims), but rather referred to a definition of “match” as including “equal . . . to” in making a determination that Petitioner had met the reasonable likelihood standard for institution of *inter partes* review. See Inst. Dec. 21–23.

expansion between the IC chip and the daughter board.¹¹ See Ex. 1006 ¶ 3. Hirose further teaches that this cracking is “attributable to the fact that an IC chip that is composed of silicon and has a low coefficient of thermal expansion is attached over an interlayer resin insulation layer that has a high coefficient of thermal expansion,” and “an external board that is composed of a resin and has a high coefficient of thermal expansion is attached on the side of a ceramic board that has a low coefficient of thermal expansion.” *Id.* ¶ 7. In other words, according to Hirose, attaching materials with high CTEs to materials with low CTEs can cause problems in the package substrate. Hirose solves this problem by flipping the orientation of a “known multilayer wiring board”—that includes an interlayer resin insulation layer and a wiring layer on a ceramic board (Ex. 1006 ¶ 2)—such that, in the package substrate of the disclosed embodiments, “an IC chip that has a low coefficient of thermal expansion is attached on the side of a ceramic board that has a low coefficient of thermal expansion,” and “an external board that is composed of a resin and has a high coefficient of thermal expansion is attached on the side of interlayer resin insulation layers that have a high coefficient of thermal expansion.” *Id.* ¶ 8; see *id.* ¶ 12; compare *id.* at Fig. 5 (package substrate of Hirose’s first embodiment), with *id.* at Fig. 8 (conventional package substrate). Hirose recognizes that “because the coefficients of thermal expansion are matched,” “cracking is less likely to occur at the interlayer resin insulation layers” (i.e., the problematic

¹¹ We note that this teaching differs from Petitioner’s characterization that “Hirose recognizes that differences in CTEs between chip 70 and ceramic board 10 can cause cracking.” Pet. 67. The portions of Hirose to which Petitioner cites do not support Petitioner’s contention, as discussed below.

“cracking” identified in paragraph 3), and reliability is improved. Ex. 1006 ¶ 33. In other words, according to Hirose, attaching the materials with low CTEs to each other and attaching the materials with high CTEs to each other solves the problems in the conventional package substrate described in Hirose.

Based on the teachings of Hirose as a whole, we agree with Patent Owner that a person of ordinary skill in the art would understand that “matched,” as used in Hirose, means “to make similar” rather than “to make equal.” See PO Resp. 30–34. In particular, we agree with Patent Owner’s assertion that a person of ordinary skill in the art “would have understood Hirose to be using the term ‘match’ according to its plain meaning to describe that the silicon IC chip and ceramic board should both have similarly low, but not equal, CTEs.” *Id.* at 34. In other words, Hirose is not concerned with the exact numerical values for the CTEs of the materials, but instead is concerned with the relative CTEs (e.g., low versus high) of adjacent layers in the package substrate. Testimony from Dr. Darveaux further supports this reading of Hirose. For example, Dr. Darveaux testifies:

Even if this passage [of Hirose (¶ 33)] is interpreted to describe that other layers are “matched,” it is only describing “matching” in the sense that materials with low CTE are adjacent to materials of low CTE, and materials with high CTE are adjacent to materials of high CTE. . . . [E]ach of the low CTE materials (silicon IC chip and ceramic board) have different CTEs, and each of the high CTE materials (interlayer resin insulation layers and daughter board) have different CTEs. Given that all of the layers have different CTE’s, a [person of ordinary skill in the art]

would not understand Hirose to be teaching these materials be “matched” in the sense that they have been made equal.

Ex. 2011 ¶ 66; *see also id.* ¶ 82 (similar testimony). Dr. Darveaux further testifies:

Because it is physically impossible to “match” the CTE of every interface in a semiconductor apparatus when there is a difference in CTE between the IC chip and the motherboard, a [person of ordinary skill in the art] would not have understood Hirose to be making an unrealizable proposal to make all materials have the same CTE.

Id. ¶ 58.

This determination that Hirose describes that IC chip 70 and ceramic board 10 should both have similarly low, but not necessarily equal, CTEs, does not end the inquiry, however, as Petitioner argues that a person of ordinary skill in the art would have been motivated “to make the CTE of ceramic board 10 ‘equal to’ the CTE of chip 70 through routine experimentation and optimization of a result-effective variable.”

Pet. Reply 3–4; *see id.* at 8 (arguing that a person of ordinary skill in the art “would [have] be[en] motivated . . . to minimize the difference of the CTEs of ceramic board 10 and chip 70 until they are equal”); Pet. 67. Petitioner, however, does not explain sufficiently or produce adequate evidence in support of this assertion as to *why* a person of ordinary skill in the art would have been motivated to do so.¹² The entirety of Petitioner’s argument in the

¹² The parties spend a significant portion of their respective briefing discussing arguments regarding whether Hirose teaches away from Petitioner’s proposed modification. We need not reach these arguments, however, because we are not persuaded that Petitioner has made a sufficient showing that one of skill in the art would have been motivated to pursue the

Petition regarding the motivation to make the CTEs equal is reproduced below:

Hirose recognizes that differences in CTEs between chip 70 and ceramic board 10 can cause cracking. Hirose's design of package substrate 100 solves this problem by matching the CTE of chip 70 and the CTE of ceramic board 10. Hirose specifically discloses the CTEs of chip 70 and ceramic board 10 are matched, for example, to prevent cracking.

Therefore, Hirose recognizes the relationship of the CTEs of chip 70 and ceramic board 10 as a result-effective variable, *i.e.*, a variable which achieves a recognized result. Thus, it would be obvious for a [person of ordinary skill in the art] to reach the claimed relationship of the CTEs (*e.g.*, equal CTEs) through routine experimentation and optimization.

Pet. 67 (citations omitted). We address various aspects of this argument in turn.

We agree with Patent Owner, that contrary to Petitioner's assertion that "Hirose recognizes that differences in CTEs between chip 70 and ceramic board 10 can cause cracking" (Pet. 67¹³), "Hirose never states that the interface between the silicon IC chip and ceramic board contribute to cracks in the interlayer resin insulation layers." PO Resp. 32; *see* Ex. 1006 ¶¶ 3, 7, 8, 12, 33; *see also* Ex. 2010, 76:1–3 (Dr. Qu testifying that "the degree of thermal mismatch between [chip] 70 and [ceramic board] 10 *may or may not* affect the degree of failure in [interlayer resin insulation layers] 40 and 140 depending upon the specific design, specific materials, . . . and a number of other factors.") (emphasis added); Ex. 2011 ¶ 65 (The "matching

proposed modification, regardless of whether Hirose can be said to teach away from that modification.

¹³ Petitioner reiterates this argument in the Reply. Pet. Reply 15.

[in Hirose] is describing a way to address cracking at the interlayer resin insulation layers, which are separated from the IC chip by the ceramic board and is, thus unrelated to equalizing the CTE of the IC chip to that of the ceramic board”), ¶ 67. Instead, as discussed above, Hirose describes that such cracking is due to attaching materials with high CTEs to materials with low CTEs in the package substrate. *See* Ex. 1006 ¶¶ 3, 7. The “matching” of the CTEs of IC chip 70 and ceramic board 10 described with respect to Hirose’s first embodiment as solving the problem of cracking, refers to the concept of attaching the materials with low CTEs to each other and attaching the materials with high CTEs to each other, rather than to any adjusting of the CTEs of the materials themselves. *See* Ex. 1006 ¶¶ 8, 12, 33; Ex. 2011 ¶ 66.

We also agree with Patent Owner that Petitioner has not supported sufficiently with evidence its assertion that Hirose suggests modifying or optimizing the relative CTEs of chip 70 and ceramic board 10. *See, e.g.*, PO Resp. 14, 42. The only evidence cited by Petitioner, beyond Hirose itself (which is not persuasive as discussed above), in support of its assertions that the “relationship of the CTEs of chip 70 and ceramic board 10 [is] a result-effective variable” and that “it would [have] be[en] obvious for a [person of ordinary skill in the art] to reach the claimed relationship of the CTEs (*e.g.*, equal CTEs) through routine experimentation and optimization” (Pet. 67) is the following testimony of Dr. Qu:

Hirose discloses “the IC chip 70, which is composed of silicon and has a low coefficient of thermal expansion, is attached on the side of the ceramic board 10, which has a low coefficient of thermal expansion Therefore, cracking and so forth attributable to a difference in thermal expansion are prevented.” Ex. 1006, [0012]. Hirose further explains that “[w]ith the

package substrate structure of the present invention, cracking is less likely to occur . . . because the coefficients of thermal expansion are matched.” Ex. 1006, [0033].

I have been informed that the discovery of an optimum value of a result-effective variable, *i.e.*, a variable which achieves a recognized result, is a rationale for finding obviousness.

Hirose recognizes the problem that differences in CTEs between the IC chip 70 and the ceramic board 10 can cause cracking. *See*, Ex. 1006, [0012] and [0030]. Hirose’s design of the package substrate 100 solves this problem by matching the CTE of the IC chip 70 and the ceramic board 10. *See id.* Therefore, Hirose recognizes that the relationship of the CTEs of the IC chip 70 and the ceramic board 10 as a result-effective variable, *i.e.*, a variable which achieves a recognized result.

Thus, it would be obvious for a [person of ordinary skill in the art] to reach the claimed relationship of the CTEs (*e.g.*, equal CTEs) through routine experimentation and optimization.

Accordingly, Hirose teaches ***a thermal expansion coefficient of the monolithic base substrate (ceramic board 10) is equal to a thermal expansion coefficient of the semiconductor chip (IC chip 70).***

Ex. 1003, claim chart at pages 78–79 (§ [1.5]). Dr. Qu’s testimony, however, merely recites the arguments of the Petition and does not cite to any underlying evidence in support thereof. We afford little weight to Dr. Qu’s conclusory and unsupported testimony, and are not persuaded that Petitioner has presented evidence sufficient to show that the “relationship of the CTEs of chip 70 and ceramic board 10” would have been recognized as a result-effective variable. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *Magnum Oil*, 829 F.3d 1380–81 (holding that Petitioner cannot satisfy its burden of proving obviousness by

employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record” to support an obviousness determination); *In re Antonie*, 559 F.2d 618, 620 (CCPA 1977) (holding that a parameter to be optimized must be recognized as a result-effective variable in order for the rule set forth in *In re Aller*, 220 F.2d 454 (CCPA 1955), that “discovery of an optimum value of a variable in a known process is normally obvious” to apply). Thus, we are not persuaded that Petitioner has presented sufficient evidence to support a conclusion that a person of ordinary skill in the art would have been motivated to minimize the difference of the CTEs of ceramic board 10 and chip 70 until they are equal.

Even assuming one of skill in the art would have been motivated to minimize the difference of the CTEs of ceramic board 10 and IC chip 70 until they are equal, we also are not persuaded that such a modification would have been a matter of “routine experimentation and optimization,” as asserted by Petitioner. Pet. 67. Patent Owner argues that Petitioner only “vaguely allege[s]” the proposed modification would have been achieved “through routine experimentation and optimization.” PO Resp. 35 (citing Pet. 67). According to Patent Owner, “Petitioner has introduced no evidence other than a conclusory statement from Dr. Qu (Ex. 1003 [¶] 79) that such a modification would have been routine.” *Id.* at 38. In its Reply, Petitioner argues that a person of ordinary skill in the art “would have knowledge of numerous ceramics with CTEs within the range of the CTE of a semiconductor chip,” and, “[a]ccordingly, it would be routine for a [person of ordinary skill in the art] to choose one of the ceramics with a CTE ‘equal to’ the CTE of a semiconductor chip.” Pet. Reply 12.

Petitioner relies on testimony of Dr. Qu as support for its assertion that the proposed modification would have been “routine experimentation and optimization.” Pet. 67 (citing Ex. 1003, claim chart at pages 78–79). Dr. Qu’s testimony, however, does not expand upon or explain how such a modification would have been routine.

Patent Owner argues, for example, that a person of ordinary skill in the art “would have understood that reliability of semiconductor apparatus depends on many things—not just the difference in CTE at a single interface.” PO Resp. 36; *see also id.* (“[C]hanging the CTE of a material to equalize the CTE at one interface would likely change the difference in CTE at other interfaces.”). In support of this assertion, Dr. Darveaux testifies:

Overall reliability of the semiconductor apparatus depends on whether differences in CTE at interfaces would impact failures of the semiconductor apparatus. This, in turn depends on the properties of the materials used at that interface, including the strength of those materials, and potentially other properties of materials used in other layers in the apparatus, such as thermal conductivity.

Ex. 2011 ¶ 37. Patent Owner further asserts that the “CTE of a material is not a property that can be independently tweaked,” but instead “the material used to make the component must itself be changed.” PO Resp. 36–37; *see also* Ex. 2010, 89:5–15 (“[Y]ou can’t change the CTE of a material if the material is a monolithic single atomic material because that’s a mature property. You can change the CTE of a composite material by changing the composition of it, but then you are looking at a different materials; in other words, the CTE of a material is in the intrinsic property of that material. If you change the composition, you are really looking at a slightly different material.”). “When the material is changed, . . . an entire series of associated

material properties will change in addition to the CTE.” PO Resp. 37 (citing Ex. 2010, 35:18–24 (Q: “Changing the composition and the processing, not only affects CTE, but other properties of the material as well; is that correct?” A. “Generally speaking, when you change the composition of a material and when you process it, you will change a lot of things, that is correct.”)).

Further, on cross-examination, Dr. Qu testified, “CTE is one of probably tens of, maybe even hundreds, of factors to be considered” in designing a semiconductor package. Ex. 2010, 13:12–14¹⁴; PO Resp. 37; *see also* Ex. 2010, 113:20–114:7 (Q: “What other properties of the ceramic

¹⁴ Petitioner argues that Dr. Qu’s testimony in this regard is taken out of context. Pet. Reply 13–14. Petitioner contends that this statement is “in response to open-ended questions regarding designing a semiconductor package, not specific questions about modifying the structure in Figure 5 of Hirose.” *Id.* at 13. However, even assuming “changing the material of ceramic board 10 of Hirose would be well within the skill of a [person of ordinary skill in the art]” as Petitioner asserts (Pet. Reply 14 (citing Ex. 2010, 38:10–18)), a person of ordinary skill in the art necessarily would take into account such general design considerations when considering a change of material, to ensure the newly selected material is appropriate. *Cf.* Ex. 2011 ¶ 74 (A person of ordinary skill in the art “wishing to optimize the semiconductor apparatus of Hirose would have considered the combined impact of failures at all the interfaces and would not have as a matter of routine optimized, in isolation, the different of CTE’s at the interface between the IC chip and the ceramic board. Rather, a [person of ordinary skill in the art] would have understood that differences in CTE at the other interfaces would have to be simultaneously considered.”), ¶ 36 (“[N]ot all differences in CTE result in failures of the semiconductor apparatus. In some instances, one or more of the materials with different CTE at an interface may have sufficient resiliency that, though the materials expand or contract by different amounts, the materials tolerate this difference without failure.”).

boards are relevant in the design of the package in figure five of Hirose?”

A: “That’s a complicated question. It really depends on a lot of things. It depends on the other materials that you use in the package. It depends on how the package will be used. It depends on the size of the package. Lots of things that you have to consider. So that when you look at – when you do the material selection, you do have consider all of these things.”). Without further explanation from Petitioner or supported testimony on the issue from Dr. Qu, we are not persuaded that Petitioner has presented evidence sufficient to demonstrate that minimizing the difference of the CTEs of ceramic board 10 and IC chip 70 until they are equal would have been routine, when many other technical aspects of the modified package substrate (in addition to the CTE values of the IC chip 70 and ceramic board 10) would need to be considered by one of ordinary skill in the art.

We, thus, are not persuaded that Petitioner has shown that minimizing the difference of the CTEs of ceramic board 10 and IC chip 70 until they are equal is a matter of routine optimization, nor that it would have been obvious. As discussed, Dr. Qu’s testimony on this point is conclusory and not supported by additional evidence or explanation. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *Magnum Oil*, 829 F.3d 1380–81 (holding that Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record” to support an obviousness determination).

Based on the complete record now before us, and for the reasons discussed, we are not persuaded that Petitioner has demonstrated, by a

preponderance of the evidence, that claims 1 and 7 would have been obvious in view of Hirose.

2. Obviousness in View of Hirose and Bohr –Claims 5 and 11

Claims 5 and 11 depend from claims 1 and 7, respectively, and each recites, “wherein a functional element is formed on at least any one of the wiring layer formation surface or the wiring layer.” Petitioner relies on Bohr as disclosing this claim feature. Pet. 78–82. Petitioner does not assert Bohr for any teaching relevant to the equal CTEs limitation. *See generally id.*; *see also id.* at 78 (“As discussed above, Hirose teaches every element of [independent] claim 1.”), 81 (similar statement for independent claim 7). Accordingly, for the reasons discussed above with respect to claims 1 and 7, we are not persuaded that Petitioner has demonstrated, by a preponderance of the evidence, that claims 5 and 11 are rendered obvious by the combination of Hirose and Bohr.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has not demonstrated, by a preponderance of the evidence, that claims 1 and 7 are unpatentable under 35 U.S.C. § 102 as anticipated by Milkovich; or that claims 5 and 11 would have been obvious under 35 U.S.C. § 103(a) in view of Milkovich and Bohr. We also determine that Petitioner has not demonstrated, by a preponderance of the evidence, that claims 1 and 7 would have been obvious under 35 U.S.C. § 103(a) in view of Hirose; or that claims 5 and 11 would have been obvious under 35 U.S.C. § 103(a) in view of Hirose and Bohr.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1, 5, 7, and 11 of U.S. Patent No. 7,728,439 B2 have not been shown to be unpatentable by a preponderance of the evidence.

Because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-00842
Patent 7,728,439 B2

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