

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GLOBALFOUNDRIES U.S. INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2017-00903
Patent RE41,980 E

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and
JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

FITZPATRICK, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner, GlobalFoundries U.S. Inc., filed a Petition to institute an *inter partes* review of claims 18, 19, 30–36, and 47–51 of U.S. Patent No. RE41,980 E (Ex. 1001, “the ’980 patent”) pursuant to 35 U.S.C. § 311(a). Paper 2 (“Pet.”). Patent Owner, Godo Kaisha IP Bridge 1, filed a Preliminary Response under 35 U.S.C. § 313. Paper 8 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and Preliminary Response, and for the reasons explained below, we determine that the information presented does not show a reasonable likelihood that Petitioner would prevail with respect to any claim challenged in the Petition. *See* 35 U.S.C. § 314(a); 37 C.F.R. § 42.108. The Petition is denied.

A. Related Matters

The ’980 patent issued from Serial No. 11/984,551, which was a continuation reissue application of Serial No. 10/438,348 (now U.S. Patent No. RE39,932), which was a reissue application of Serial No. 09/387,834 (now U.S. Patent No. 6,232,656), which was a divisional application of Serial No. 08/925,442 (now U.S. Patent No. 5,989,992), which was filed September 8, 1997. Ex. 1001, 1:10–20.

A different petitioner has filed three petitions for an *inter partes* review of the ’980 patent, all of which have been denied. *See* IPR2016-01331, Paper 9; IPR2016-01367, Paper 8; IPR2017-00931, Paper 9.

Patent Owner asserted the '980 patent in *Godo Kaisha IP Bridge 1 v. Broadcom Ltd.*, No. 2-16-cv-00134 (E.D. Tex.). Pet. 86; Paper 4, 2.

B. The '980 Patent

The '980 patent “relates to a semiconductor device having a metal wire layer and a passivation film in the upper most layer” and, more particularly, to “improvement in the structures of a bonding pad and a surface protecting film.” Ex. 1001, 1:23–27. The stated “object” of the '980 patent is “providing a semiconductor device having high integration, high reliability, and high performance . . . by decreasing a parasitic capacitance between metal wires with a small pitch in a metal wire layer, by preventing a coverage defect in depositing a silicon nitride film used as a passivation film, and by suppressing moisture absorption through an opening for forming a bonding pad.” *Id.* at 2:40–48.

Figure 1 of the '980 patent is reproduced below.

Fig. 1

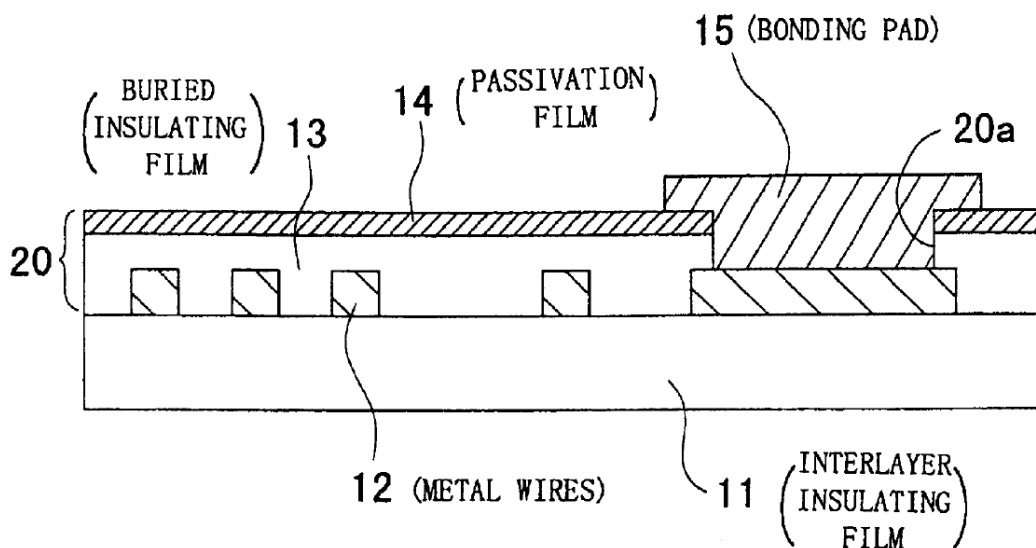


Figure 1 shows a sectional view of a semiconductor device embodiment of the invention of the '980 patent. *Id.* at 6:21–23. The embodiment includes interlayer insulating film 11 on which is formed a metal wire layer including a plurality of metal wires 12. *Id.* at 7:29–32. Surface protecting film 20 covers the interlayer insulating film and the metal wires. *Id.* at 7:33–35. The surface protecting film “is a composite film including a buried insulating film 13 of an insulating film with a small dielectric constant (such as a TEOS film) and a passivation film 14 of an insulating film with a large dielectric constant and high moisture absorption resistance (such as a silicon nitride film).” *Id.* at 7:35–40. Bonding pad 15 is buried in opening 20a of the surface protecting film, completely covers the side faces of the buried insulating film, and is drawn above the passivation film. *Id.* at 7:43–49.

C. The Challenged Claims

Of the challenged claims, claims 18 and 35 are independent. Claim 18 is illustrative and reproduced below.

18. A semiconductor device comprising:
- a semiconductor substrate bearing semiconductor elements;
 - an interlayer insulating film formed on said semiconductor substrate;
 - a metal wire layer including plural metal wires formed on said interlayer insulating film;
 - a surface protecting film including a first dielectric film with a small dielectric constant for filling at least a part of areas among said metal wires in said metal wire layer and a second dielectric film with a higher moisture absorption preventing function than said first dielectric film for covering said metal wire layer and said first dielectric film, said second dielectric film having a function of suppressing moisture absorption of said first dielectric film;
 - an opening for a bonding pad formed in said surface protecting film; and
 - a bonding pad formed in said opening for obtaining external electrical connection,
- wherein said bonding pad in said opening and said second dielectric film of said surface protecting film completely cover said first dielectric film so as not to expose said first dielectric film.

D. Asserted Grounds of Unpatentability

Petitioner asserts numerous grounds of unpatentability that it groups as follows:

References	Basis ¹	Claims
Cheung ² alone or in view of one or more of Chiang ³ , Shinoda ⁴ , and El-Kareh ⁵ (collectively, the “Cheung-based grounds”)	§ 103(a)	18, 19, 30–36, 47–51
Chiang alone or in view of Cheung and/or El-Kareh (collectively, the “Chiang-based grounds”)	§ 103(a)	18, 19, 30–36, 47–51

Pet. 22.

II. ANALYSIS

A. Claim Construction

Patent Owner filed a Motion for a district court-type claim construction, asserting that the ’980 patent will expire on September 8, 2017,

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, which was enacted September 16, 2011, made amendments to 35 U.S.C. §§ 102 and 103. AIA § 3(b) and (c). Those amendments became effective eighteen months later on March 16, 2013. *Id.* at § 3(n). Because the application from which the ’980 patent issued was filed before March 16, 2013, our citations to 35 U.S.C. §§ 102 and 103 are to their pre-AIA versions.

² U.S. Patent No. 5,785,236 to Cheung et al. (Ex. 1004).

³ U.S. Patent No. 5,739,579 to Chiang et al. (Ex. 1005).

⁴ U.S. Patent No. 3,617,824 to Shinoda et al. (Ex. 1006).

⁵ BADIH EL-KAREH, FUNDAMENTALS OF SEMICONDUCTOR PROCESSING TECHNOLOGIES (1995) (Ex. 1007).

which is less than eighteen months after entry of the Notice of Filing Date Accorded to the Petition. Paper 7; *see also* 37 C.F.R. § 42.100(b) (“A party may request a district court-type claim construction approach to be applied if a party certifies that the involved patent will expire within 18 months from the entry of the Notice of Filing Date Accorded to Petition.”). Petitioner agrees with Patent Owner as to the expiration date of the ’980 patent.

Pet. 23. We grant Patent Owner’s Motion.

In district court, claim terms are given their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Independent claims 18 and 35 both recite an “interlayer insulating film.” In Cases IPR2016-01331 and IPR2016-01367, we⁶ construed “interlayer insulating film” to mean “an insulating film located between but not within other layers.” *See, e.g.*, Ex. 1010 (IPR2016-01331, Paper 9), 8. Petitioner applies that construction here, with which Patent Owner agrees. Pet. 33; Prelim. Resp. 10.

⁶ The instant panel is the same as that in Cases IPR2016-01331 and IPR2016-01367.

No other express constructions are necessary for purposes of this Decision.

B. The Law of Obviousness

A claim is unpatentable “if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103(a). “Obviousness is a question of law based on underlying facts.” *MobileMedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1167 (Fed. Cir. 2015), *cert. denied*, 136 S. Ct. 270 (2015). The underlying facts include (i) the scope and content of the prior art, (ii) the differences between the prior art and the claimed invention, (iii) the level of ordinary skill in the field of the invention, and (iv) any relevant objective considerations of nonobviousness that are presented. *Id.* (citing *Graham v. John Deere*, 383 U.S. 1, 17–18 (1966)). An additional underlying fact is whether there was a reason to combine prior art teachings when so asserted. *Id.*

C. The Cheung-Based Grounds

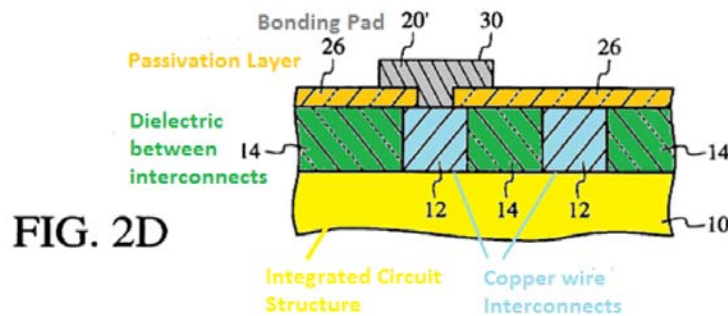
1. *Cheung*

Cheung was filed November 29, 1995, and issued July 28, 1998. Ex. 1004, at [22], [45]. The earliest possible effective filing date of the challenged claims of the ’980 patent is September 10, 1996. Ex. 1001, at [30]. In its Preliminary Response, Patent Owner does not argue that the challenged claims have an invention date earlier than the date on which

Cheung was filed. *See generally* Prelim. Resp. Thus, on the record presented, Cheung is prior art under 35 U.S.C. § 102(e), as argued by Petitioner. *See* Pet. 11 n.2.

Cheung is titled “Advanced Copper Interconnect System That Is Compatible With Existing IC Wire Bonding Technology.” Ex. 1004, at [54]. Cheung “relates generally to metal interconnects and wire bonding employed in semiconductor technology, and, more particularly, to wire bonding to form electrical connection with copper interconnects which are used for connecting IC (integrated circuit) devices formed in semiconductor wafers.” *Id.* at 1:8–13.

Petitioner’s annotated Figure 2D of Cheung is reproduced below.



Cheung, Fig. 2D (annotated)

See Pet. 21. Petitioner’s annotated Figure 2D, above, shows “integrated circuit structure 10” in yellow (Ex. 1004, 4:30–31); “copper interconnects 12” in blue (*id.* at 4:32); “interlayer dielectric 14” in green (*id.* at 4:34–35); “insulating layer or passivation layer 26” in orange (*id.* at 4:36–37); and “aluminum pad 20’” in grey with “surface 30” (*id.* at 4:8–11).

2. *Obviousness over Cheung*

All of the challenged claims require an “interlayer insulating film” (i.e., “an insulating film located between but not within other layers”). Petitioner does not identify any express disclosure in Cheung that purportedly meets this limitation. Instead, to meet this limitation, Petitioner asserts the following:

A [person of ordinary skill in the art (“POSITA”)] would understand from the disclosure [in Cheung] of a “multilayer interconnect structure” that each layer of interconnects must be separated by an insulating film to ensure interconnects between different layers do not short with one another and to reduce parasitic capacitance between interconnect layers. Ex. 1003, ¶ 48. Although Fig. 2D depicts wires 14 directly on “integrated circuit structure 10,” a POSITA would understand that “integrated circuit structure 10” includes an insulating film (not shown) between the layer of wires 12 and the components of integrated circuit structure 10—i.e., transistor components and lower level interconnects that are in contact with the semiconductor substrate. Ex. 1003, ¶ 62.

Pet. 34. We are not persuaded by this argument. First, Cheung neither mentions nor illustrates such an insulating film. Second, even assuming Petitioner is correct that some form of insulation is necessary between copper interconnects 12 and integrated circuit structure 10 in Cheung Figure 2D, it does not follow (as Petitioner implies) that such insulation necessarily would be in the form of an interlayer insulating film. As Patent Owner points out, it could alternatively be in the form of a buried insulating film.

See Prelim. Resp. 35–36.

Petitioner additionally argues “[t]o the extent Patent Owner asserts that Cheung does not disclose an interlayer insulating film ‘located between but not within other layers,’ *Cheung discloses* this limitation in combination with the knowledge of a POSITA.” Pet. 34 (emphasis added). But, to support its argument, Petitioner cites only to the ’980 patent. *Id.* at 34–35 (citing Ex. 1001, 1:35–37, 1:39–41, 1:45–48). Petitioner’s citations to the ’980 patent are probative that an “interlayer insulating film” was a known feature of prior art semiconductor devices, but they are not probative of Petitioner’s assertion that *Cheung discloses* this feature. See Pet. 34. Thus, this argument also is not persuasive.

For the forgoing reasons, there is not a reasonable likelihood that Petitioner would prevail in proving that any challenged claim is obvious over Cheung.

3. *Obviousness over Cheung in view of one or more of Chiang, Shinoda, and El-Kareh*

As just discussed above, all of the challenged claims require an “interlayer insulating film,” and Petitioner has not shown that Cheung meets this limitation. Petitioner, however, also challenges the claims as obvious over Cheung in view of Chiang, Shinoda, and/or El-Kareh. See, e.g., Pet. 31. With respect to the “interlayer insulating film” limitation, Petitioner relies on either Chiang or Shinoda. *Id.* at 35. Petitioner does not rely on El-Kareh for this limitation. *Id.* at 33–39.

Petitioner argues that it would have been “obvious to combine Cheung with Chiang or Shinoda to disclose ‘an insulating film located between but

not within other layers formed on said semiconductor substrate.’” *Id.* at 35. Petitioner explains how Chiang and Shinoda purportedly disclose an interlayer insulating film. *Id.* at 36 (discussing Chiang), 37 (discussing Shinoda). Then, Petitioner asserts the following: (1) “[a]s discussed in Section V.B, *supra*, a POSITA would be motivated to combine Chiang with Cheung”; and (2) “[a]s discussed in Section V.B., *supra*, a POSITA would be motivated to combine Cheung with Shinoda.” *Id.* at 37–38.

Section V.B. of the Petition begins with arguments that a person of ordinary skill in the art would have combined the asserted references generally, without explaining what teachings within those references would be combined. Pet. 28 (“A POSITA would be motivated to combine Cheung with Chiang and/or Shinoda because each reference focuses on a portion of integrated circuit manufacturing related to fabrication of interconnects, bonding pads, and a moisture-blocking passivating layer, which protects the integrated circuit from the surrounding environment.”), *id.* (“Chiang, Cheung, and Shinoda all relate to BEOL^[7] and a person of ordinary skill would be motivated to combine them.”), *id.* at 29 (“A POSITA would be motivated to combine Cheung and Chiang as designing and manufacturing a semiconductor device requires knowledge of both bonding pads for external connection and the various lower layers that comprise a semiconductor device.”). These initial and general arguments are insufficient, as they fail to

⁷ “The portion of integrated circuit fabrication regarding interconnects, bonding pads, and passivation layers (as opposed to the fabrication of transistors) is called Back-End-of-Line (‘BEOL’).” Pet. 28.

identify specific teachings from the asserted references that allegedly would have been combined and what the result of that combination would be.

Section V.B. of the Petition continues, however, to present more specific arguments. With respect to combining Cheung with Chiang, Section V.B. states the following:

Starting from the teaching of Cheung, a POSITA would immediately recognize that wires 12 extending longitudinally across the integrated circuit structure 10 of Cheung without an insulating film would create shorts between transistor gates, resulting in a non-functional semiconductor device. The POSITA would understand the integrated circuit structure 10 necessarily includes an insulating film that prevents such undesired electrical connections. The POSITA would also understand according to, for example, Chiang, that a dielectric layer can prevent undesired shorts. Chiang, Fig. 9 (illustrating a dielectric layer (comprised of BPSG layer 22 and silicon nitride layer 23) between substrate 20 and interconnects 60 and 61). A POSITA would understand that a common way to prevent shorts in the semiconductor device of Cheung would be to separate transistor components within circuit structure 10 from wires 12 using a dielectric layer. Because a POSITA immediately understands the need for an interlayer dielectric to prevent shorts, a POSITA *would* combine the teaching of Chiang with Cheung to prevent wires 12 of Cheung from shorting with the circuits implemented on circuit structure 10 of Cheung.

Id. at 29–30. This argument is not persuasive because it is premised on Cheung being defective—that there is a “need [in Cheung] for an interlayer

dielectric to prevent shorts.” *Id.* at 30. That premise is not supported adequately in the record.

With respect to combining Cheung with Shinoda, Section V.B. of the Petition states the following:

A POSITA would similarly be motivated to combine Cheung with Shinoda, which like Chiang describes the lower layers that comprise a semiconductor device, including metal interconnects, dielectric layers (including an interlayer dielectric to prevent undesired electrical shorts), and a silicon substrate. Shinoda, 4:63–70; Fig. 7.

Pet. 31. This argument is not persuasive because no actual reason to combine is provided. At best, Petitioner implies that a person of ordinary skill in the art would have combined Cheung with Shinoda for the same reason Petitioner offered with respect to combining Cheung with Chiang. That reason, however, is no more persuasive here as it was above. Petitioner has not shown, with evidentiary support, that the Cheung device would short out absent the addition of an interlayer insulating film.

For the forgoing reasons, there is not a reasonable likelihood that Petitioner would prevail in proving that any challenged claim is obvious over Cheung in view of one or more of Chiang, Shinoda, and El-Kareh.

D. The Chiang-Based Grounds

1. *Chiang*

Chiang was filed September 10, 1996, and issued April 14, 1998. Ex. 1005, at [22], [45]. The earliest possible effective filing date of the challenged claims of the ’980 patent is September 10, 1996—the same day

that Chiang was filed. Ex. 1001, at [30]. Chiang, however, was filed as “a continuation of application Ser. No. 08/430,759, filed Apr. 27, 1995, now abandoned, which is a division of application Ser. No. 08/314,248, filed Sep. 28, 1994, now abandoned, which is a continuation in part of application Ser. No. 07/905,473, filed Jun. 29, 1992, now U.S. Pat. No. 5,612,254.” Ex. 1005, 1:7–12. Petitioner argues that Chiang’s effective filing date is September 28⁸, 1994, and Chiang is thus prior art under 35 U.S.C. § 102(e). Pet. 11–12 n.3. In its Preliminary Response, Patent Owner does not dispute that Chiang is prior art to the challenged claims. *See generally* Prelim. Resp.

Chiang is titled “Method For Forming Interconnections For Semiconductor Fabrication And Semiconductor Device Having Such Interconnections.” Ex. 1005, at [54]. It discloses “form[ing] an interconnect channel and an interconnect within a semiconductor device.” *Id.* at 2:66–3:1.

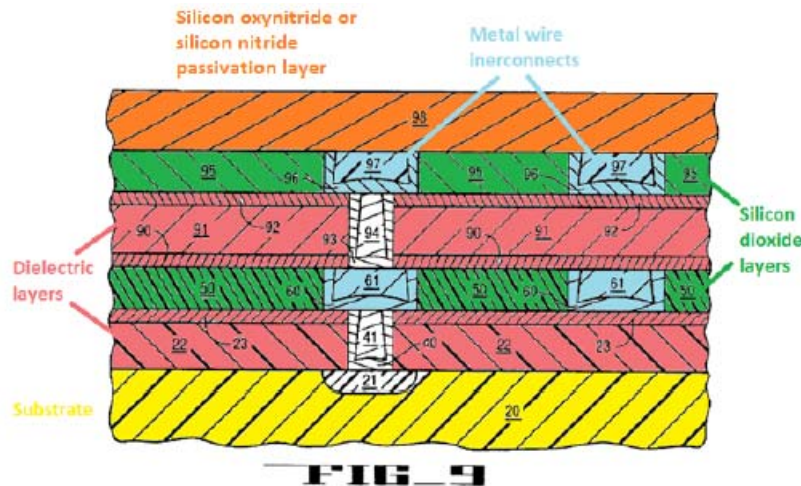
In general a first dielectric layer is deposited over a substrate and patterned to form a contact or via opening that is filled to form a contact or via plug. A second dielectric layer is deposited over the patterned first dielectric layer and the contact or via plug and is selectively etched to form an interconnect channel in the second dielectric layer. The first or second dielectric layers may comprise more than one individual dielectric layer. Preferably, the first dielectric layer acts as an etch stop when the second dielectric layer is selectively

⁸ Petitioner lists “Sept. 24, 1994” as the date but it is clear from its argument that “24” is a typographical error and was intended as “28.” *See* Pet. 11–12 n.3.

etched to form the interconnect channel. An interconnect layer is deposited over the second dielectric layer and within the interconnect channel.

Id. at 3:1–12.

Petitioner’s annotated Figure 9 of Chiang is reproduced below.



Chiang, Fig. 9 (annotated)

See Pet. 26. Petitioner’s annotated Figure 9, above, shows “substrate having a monocrystalline silicon layer 20” in yellow (Exhibit 1005, 7:64–65), “borophosphosilicate glass (BPSG) layer 22” in red (*id.* at 7:66), “silicon nitride layer 23” in red (*id.* at 8:10–11), “titanium nitride layer 40” in white (*id.* at 8:26–27), “tungsten layer 41” in white (*id.* at 8:30), “silicon dioxide layer 50” in green (*id.* at 8:61–62), “titanium nitride barrier layer 60” in blue (*id.* at 8:60), “copper metal layer 61” in blue (*id.* at 8:66), “second silicon nitride layer 90” in red (*id.* at 10:52), “second silicon dioxide layer 91” in red (*id.* at 10:52–53), “third silicon nitride layer 92” in red (*id.* at 10:53), “second titanium nitride layer 93” in white (*id.* at 10:56), “second tungsten layer 94” in white (*id.* at 10:57), “third silicon dioxide layer 95” in green (*id.*

at 10:63–64), “second titanium nitride barrier layer 96” in blue (*id.* at 10:67–11:1), “second copper metal layer 97” in blue (*id.* at 11:1), and “silicon oxynitride passivation layer 98” in orange (*id.* at 11:8). Additionally, a contact plug is formed by layers 40 and 41 (*id.* at 10:40–41), and a via plug is formed by layers 93 and 94 (*id.* at 10:56–58).

2. *Obviousness over Chiang*

All of the challenged claims require “an opening for a bonding pad formed in said surface protecting film; and a bonding pad formed in said opening for obtaining external electrical connection.” Claims 18, 19, and 30–34 further specify “wherein said bonding pad in said opening and said second dielectric film of said surface protecting film completely cover said first dielectric film so as not to expose said first dielectric film.” Similarly, claims 35, 36, and 47–51 further specify “wherein said bonding pad covers said opening and said second dielectric film of said surface protecting film completely covers said first dielectric film so as not to expose said first dielectric film.” We refer to these last two limitations as the “wherein/bonding pad” limitations.

Petitioner asserts that the challenged claims would have been obvious over Chiang alone. Pet. 59 (“The Challenged Claims are obvious in view of Chiang alone or in combination with Cheung and/or El-Kareh.”). Petitioner, however, never actually argues that Chiang alone meets the wherein/bonding pad limitations. *See id.* at 78. Instead, for both wherein/bonding pad limitations, Petitioner argues that they are met only by combining the prior art. *Id.* (“It would have been obvious to a POSITA to combine Chiang with

Cheung to disclose this limitation.”).

Thus, there is not a reasonable likelihood that Petitioner would prevail in proving that any challenged claim is obvious over Chiang.

*3. Obviousness over Chiang in view of Cheung
and/or El-Kareh*

As just discussed above, Petitioner has not shown that Chiang meets either of the wherein/bonding pad limitations. Petitioner, however, also challenges the claims as obvious over Chiang in view of Cheung and/or El-Kareh. *See, e.g.*, Pet. 59.

With respect to the wherein/bonding pad limitations, Petitioner relies exclusively on Cheung and not on El-Kareh. *See id.* at 78. Petitioner’s argument is as follows:

It would have been obvious to a POSITA to combine Chiang with Cheung to disclose this limitation. *See* Section V.B., *supra* (regarding motivation to combine). Cheung discloses this element. *See* Section, V.C.8 [and 9], *supra*.

Pet. 78.

As discussed above, Section V.B. of the Petition begins with arguments that a person of ordinary skill in the art would have combined the asserted references generally, without explaining what specific teachings within those references would be combined. *See supra* Section II.C.3; Pet. 28–29. These initial and general arguments are insufficient, as they fail to identify specific teachings from the asserted references that allegedly would have been combined and what the result of that combination would be.

Section V.B. of the Petition continues, however, to present more specific arguments. With respect to combining Chiang with Cheung, Section V.B. states the following:

Starting from the teaching of Chiang, a POSITA would understand that the semiconductor device of Chiang inherently includes a bonding pad to enable the semiconductor device to interface with an external circuit. But, even if such a feature were not considered inherent, a POSITA would immediately recognize a need for a bonding pad and be motivated to enable the semiconductor device of Chiang to receive or send electronic signals to or from an external circuit or system. Hence, a person of ordinary skill *would* look to combining the teaching of Chiang with Cheung to enable the semiconductor device of Chiang to interface with other electronic circuits or systems.

Pet. 30. This argument is not persuasive because it is premised on Chiang being defective—that there is a “need [in Chiang] for a bonding pad.” *Id.* That premise is not supported adequately in the record.

Additionally, even assuming that a person of ordinary skill in the art would have had a reason to add a bonding pad to Chiang, Petitioner has not shown that he would have added it in a manner such that the wherein/bonding pad limitations would be met. *See id.* at 28–31 (not addressing the wherein/bonding pad limitations). For example, claims 18, 19, and 30–34 require “wherein said bonding pad in said opening and said second dielectric film of said surface protecting film completely cover said first dielectric film so as not to expose said first dielectric film.” Petitioner never explains how the asserted combination of Chiang in view of Cheung would meet this limitation or the corresponding wherein/bonding pad limitation of claims 35,

36, and 47–51. Petitioner merely asserts that a bonding pad would be added to the semiconductor device of Chiang.

For the forgoing reasons, there is not a reasonable likelihood that Petitioner would prevail in proving that any challenged claim is obvious over Chiang in view of Cheung and/or El-Kareh.

III. CONCLUSION

There is not a reasonable likelihood that Petitioner would prevail with respect to any challenged claim. *See* 35 U.S.C. § 314(a); 37 C.F.R. § 42.108.

IV. ORDER

Accordingly, it is
ORDERED that the Petition is denied.

IPR2017-00903
Patent RE41,980 E

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