

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GLOBALFOUNDRIES U.S. INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2017-00935
Patent 8,354,726 B2

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and
JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Petitioner GlobalFoundries U.S. Inc. filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62 of U.S. Patent No. 8,354,726 B2 (Ex. 1001, “the ’726 patent”) pursuant to 35 U.S.C. § 311(a). Patent Owner Godo Kaisha IP Bridge 1 filed a Preliminary Response (Paper 8, “Prelim. Resp.”) pursuant to 35 U.S.C. § 313. Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons that follow, we have decided not to institute an *inter partes* review.

I. BACKGROUND

A. The ’726 Patent¹

The ’726 patent describes “a semiconductor device having a structure in which an insulating film with internal stress covering a gate electrode of a field effect transistor produces stress in a channel region.” Ex. 1001, col. 1, ll. 8–12. A “conventional semiconductor device” in the prior art included a liner film over a gate electrode with a side-wall insulating film, where the liner film applies two types of stress on the channel region. *Id.* at col. 1, l. 21–col. 2, l. 42, Figs. 18A–B. First, the liner film applies “tensile stress S1 in the channel length direction of the channel region,” which “enhances the carrier mobility to increase the current therein,” allowing the

¹ Taiwan Semiconductor Manufacturing Company, Ltd. previously filed two petitions challenging claims 1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62 of the ’726 patent in Cases IPR2016-01439 and IPR2016-01442, which were denied.

semiconductor device to operate at a higher speed. *Id.* at col. 1, l. 60–col. 2, l. 3. Second, the liner film “covers an end of a protruding portion of the gate electrode” located on the isolation region, which compresses the protruding portion “in the direction of the channel width that is perpendicular to the channel length region.” *Id.* at col. 2, ll. 4–17. This results in “compressive stress S2 in the channel width direction,” which decreases carrier mobility and “counteract[s]” the increased carrier mobility provided by tensile stress S1. *Id.* at col. 2, ll. 14–32. Also, as smaller channel widths are used, the effect of the compressive stress “becomes more significant.” *Id.* at col. 2, ll. 33–42. Figure 17 of the ’726 patent is reproduced below.

FIG. 17 PRIOR ART

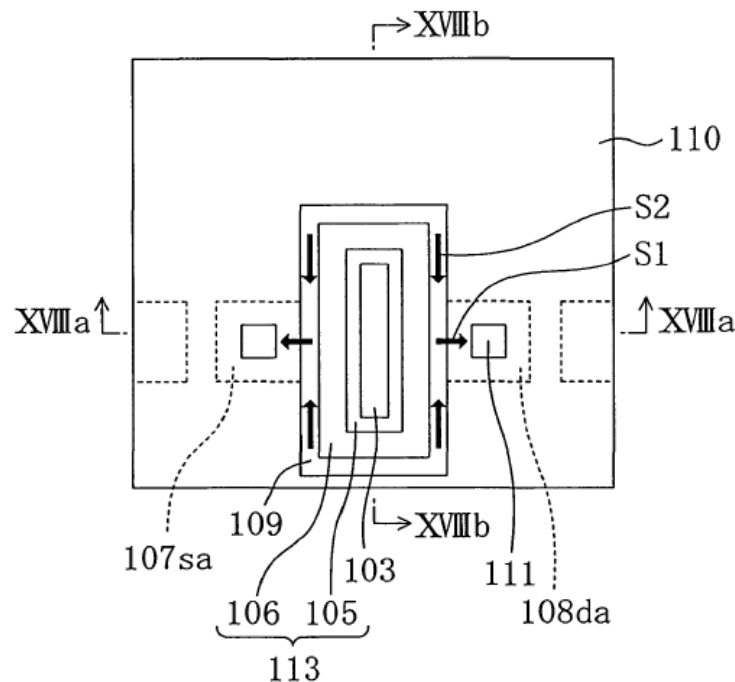


Figure 17 is a plan view of the prior art device including gate electrode 103, side-wall insulating film 113, source region 107s, drain region 108d, and

contact plugs 111, and shows the directions of tensile stress S1 and compressive stress S2.

The device described in the '726 patent purportedly solves the above issues by placing the gate electrode next to an "auxiliary pattern" (e.g., another gate electrode) and forming a stress-containing insulating film over both components and their side-wall insulating films, which reduces the compressive stress in the channel width direction. *Id.* at col. 9, ll. 40–56, col. 11, ll. 3–6. Figures 2A and 2B of the '726 patent are reproduced below.

FIG. 2A

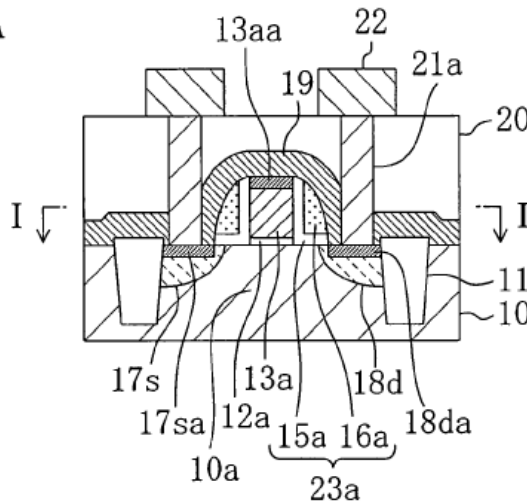
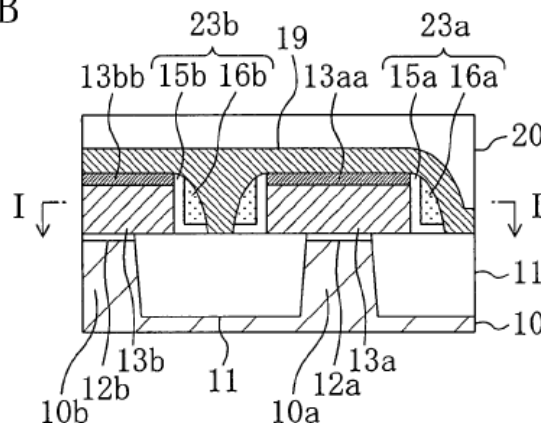


FIG. 2B



Figures 2A and 2B are sectional views of the disclosed device including liner film 19 formed over gate electrodes 13a and 13b and side-wall insulating films 23a and 23b.

The '726 patent further discloses an optimal distance between the two gate electrodes for relieving compressive stress in the channel width direction, namely “smaller than the sum total of: the sum of the thicknesses of the first and second side-wall insulating films; and the double of the thickness of the stress-containing insulating film.” *Id.* at col. 3, ll. 1–14, col. 10, ll. 16–62. Figure 3A of the '726 patent is reproduced below.

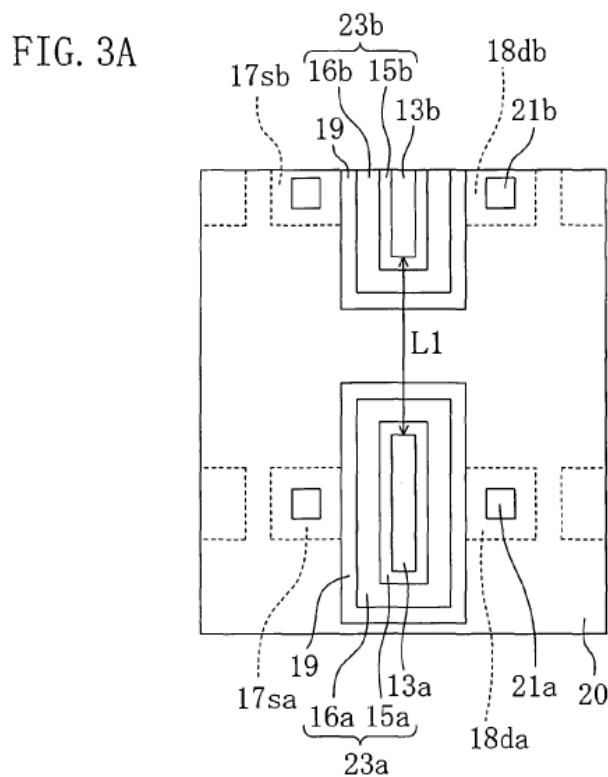


Figure 3A is a plan view of the disclosed device showing the distance L1 between gate electrodes 13a and 13b. Using the disclosed distance “enhances the carrier mobility in a channel of a field effect transistor including the first gate electrode, and provides the structure applicable to miniaturization of the semiconductor device.” *Id.* at col. 3, ll. 11–14.

B. Illustrative Claim

Claim 1 of the '726 patent recites:

1. A semiconductor device comprising:
 - a first active region surrounded with an isolation region of a semiconductor substrate;
 - a first gate electrode formed over the first active region and having a protrusion protruding on the isolation region;
 - a first side-wall insulating film formed on the side surface of the first gate electrode;
 - an auxiliary pattern formed over the semiconductor substrate to be spaced apart in the gate width direction from the protrusion of the first gate electrode;
 - a second side-wall insulating film formed on the side surface of the auxiliary pattern; and
 - a stress-containing insulating film containing internal stress and formed to cover the first gate electrode, the first side-wall insulating film, the auxiliary pattern, and the second side-wall insulating film,
- wherein the distance between the first gate electrode and the auxiliary pattern is smaller than the sum total of: the sum of the thicknesses of the first and second side-wall insulating films; and the double of the thickness of the stress-containing insulating film,
- the first side-wall insulating film includes a first sidewall formed on the side surface of the first gate electrode, and having an L-shaped cross section, and a second sidewall formed on the first sidewall,
- the first sidewall is made of an oxide film, and
- the second sidewall is made of a nitride film.

C. The Prior Art

Petitioner relies on the following prior art:

U.S. Patent No. 7,279,746 B2, filed June 30, 2003, issued Oct. 9, 2007 (Ex. 1012, “Doris”);²

Semiconductor Insights Inc., LOGIC DETAILED STRUCTURAL ANALYSIS OF THE INTEL 65NM DUAL CORE PROCESSOR (Feb. 2006) (Ex. 1006, “Intel 65 nm Report”);

Semiconductor Insights Inc., DETAILED STRUCTURAL ANALYSIS I OF THE INTEL PENTIUM 3.0E GHZ PROCESSOR “PRESCOTT” (Mar. 2004) (Ex. 1005, “Intel 90 nm Report”); and

T. Ghani et al., “Scaling Challenges and Device Design Requirements for High Performance Sub-50nm Gate Length Planar CMOS Transistors,” *IEEE 2000 Symposium on VLSI Technology Digest of Technical Papers* (2000) (Ex. 1007, “Intel IEEE Paper”).

D. The Asserted Grounds

Petitioner challenges claims 1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62 of the ’726 patent on the following grounds:

Reference(s)	Basis	Claims Challenged
Intel 90 nm Report	35 U.S.C. § 102(b) ³	1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62

² On March 25, 2017, Petitioner filed a corrected version of Doris including the appropriate labeling required by 37 C.F.R. § 42.63(d). See Papers 6, 7. The originally filed version will be expunged.

³ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Because the ’726 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

Reference(s)	Basis	Claims Challenged
Intel 65 nm Report	35 U.S.C. § 102(a)	1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62
Intel 90 nm Report and Intel IEEE Paper	35 U.S.C. § 103(a)	20 and 54
Intel 90 nm Report and Doris	35 U.S.C. § 103(a)	22 and 56
Intel 65 nm Report and Doris	35 U.S.C. § 103(a)	22 and 56

E. Claim Interpretation

The Board interprets claims using the “broadest reasonable construction in light of the specification of the patent in which [they] appear[.]” 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard as the claim interpretation standard to be applied in *inter partes* reviews). The parties do not provide proposed interpretations for any claim terms, but Petitioner refers to a district court decision interpreting certain terms. See Pet. 11 (citing Ex. 1008). For purposes of this Decision, we conclude that no claim terms require interpretation.

II. DISCUSSION

A. Preliminary Matters

Petitioner filed the Intel 65 nm Report as “Filing Party and Board Only” and the Intel 90 nm Report as “Parties and Board Only” in the PTAB

E2E system. Petitioner also filed a document entitled “Petition to the Chief Administrative Patent Judge Pursuant to 37 C.F.R. § 181(3) and 37 C.F.R. § 41.(3)” (Paper 2). As explained below, we determine that Petitioner has not established a reasonable likelihood of prevailing on any of its asserted grounds, and we are able to explain the basis for our decision by referring only to the portions of the Intel reports reproduced in the Petition, accompanying declaration (Ex. 1003), and Preliminary Response. Accordingly, as no trial will take place and there is no need to keep the Intel reports in the record, we intend to expunge them from the record of this proceeding. *See* 37 C.F.R. § 42.7(a). For the same reasons, we also need not determine whether the Intel reports are prior art printed publications or whether we should exercise our discretion to deny the Petition under 35 U.S.C. §§ 314(a) or 325(d). *See* Pet. 7–10; Prelim. Resp. 7–34.

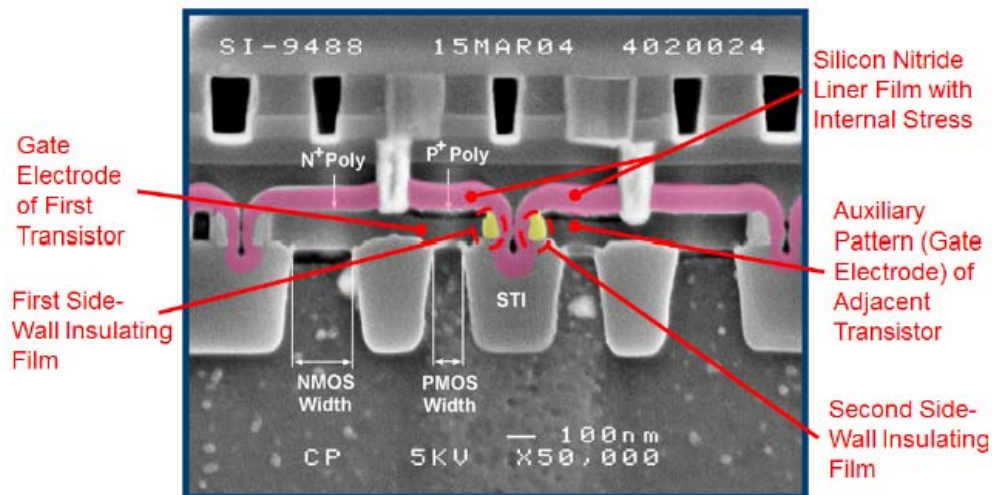
*B. Anticipation Ground Based on the Intel 90 nm Report
(Claims 1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62)*

Petitioner contends that claims 1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62 are anticipated by the Intel 90 nm Report under 35 U.S.C. § 102(b), citing the testimony of Richard B. Fair, Ph.D. as support. Pet. 11–94 (citing Ex. 1003). We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted ground for the reasons explained below.

1. Claim 1

Petitioner argues that claim 1 is anticipated by the Intel 90 nm Report. Pet. 12–45. The Intel 90 nm Report is a structural analysis report for the

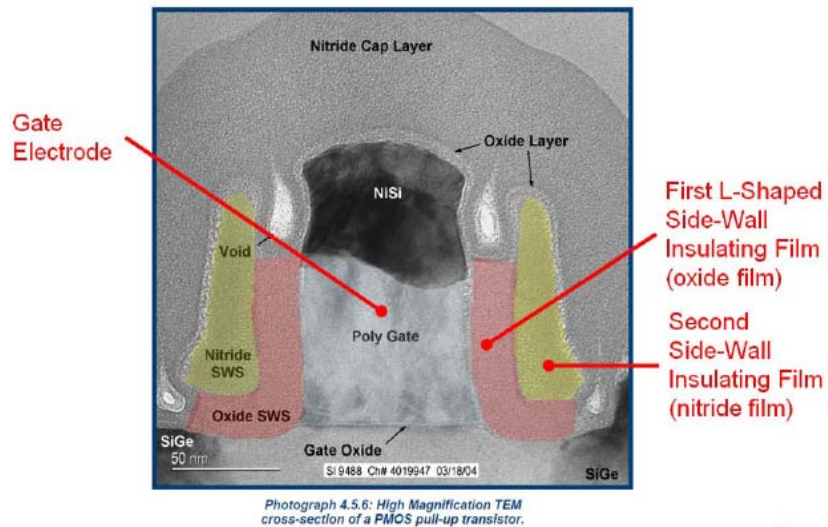
Intel BX80546PG3000E “Prescott” processor, prepared by Semiconductor Insights Inc. *Id.* at 1, 12. Petitioner relies on the standard random access memory (SRAM) transistors described in Section 4.0 of the report for its unpatentability arguments. *Id.* at 11. Petitioner provides various annotated versions of Photograph 4.2.4 of the Intel 90 nm Report, including the following version on page 35 of the Petition.



Photograph 4.2.4: High magnification SEM cross-section along a common poly line (silicon etch).

The annotated photograph above depicts two transistors, the gate electrodes of which Petitioner contends are a “first gate electrode” and “auxiliary pattern.” *Id.* at 18–19, 24–25. Petitioner argues that the left gate electrode (the alleged “first gate electrode”) has a “first side-wall insulating film” on its side surface, and the right gate electrode (the alleged “auxiliary pattern”) has a “second side-wall insulating film” on its side surface, both shown in yellow and circled with a red dotted line. *Id.* at 22, 28–29. Petitioner further contends that the Intel 90 nm Report discloses a silicon nitride liner film (the alleged “stress-containing insulating film”) covering the alleged “first gate electrode” and “auxiliary pattern,” as shown in pink in the annotated photograph above. *Id.* at 33–35. Finally, Petitioner provides the following

annotated version of Photograph 4.5.6 of the Intel 90 nm Report on page 44 of the Petition.

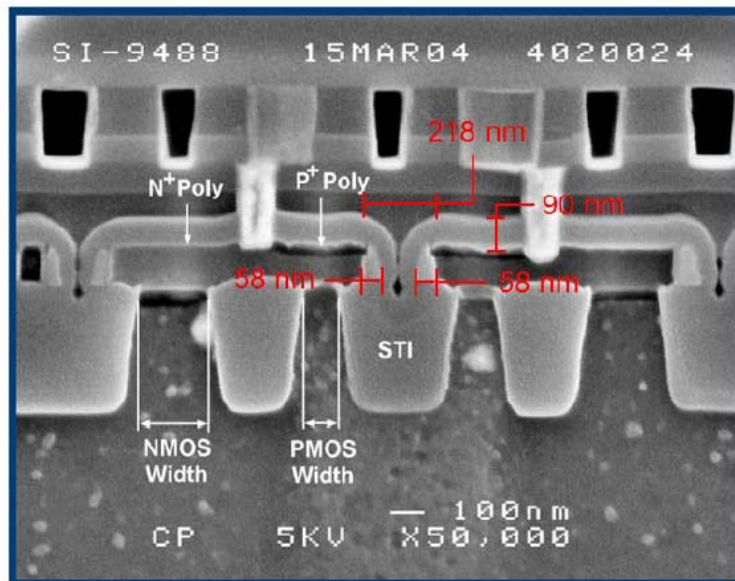


The annotated photograph above depicts the portions of the alleged “first side-wall insulating film” that Petitioner contends are an oxide film “first sidewall” having an “L-shaped cross section” (shown in red) and a nitride film “second sidewall” (shown in yellow). *Id.* at 43–44.

Petitioner argues that the Intel 90 nm Report discloses the limitation of claim 1 that “the distance between the first gate electrode and the auxiliary pattern is smaller than the sum total of: the sum of the thicknesses of the first and second side-wall insulating films; and the double of the thickness of the stress-containing insulating film” (“the distance limitation”). *Id.* at 37–40. According to Petitioner, the thickness of the “first side-wall insulating film,” which includes a “first sidewall” having an “L-shaped cross section” and a “second sidewall” formed on the first sidewall, is to be measured “at the widest portion of the side-wall insulating film near the bottom of the gate electrode.” *Id.* at 37–38. We agree with Petitioner that the thickness should be calculated at the base of the film, as such a

measurement is consistent with the exemplary embodiment described in the Specification of the '726 patent with respect to Figure 2B.⁴ *Id.*; see Ex. 1001, col. 10, ll. 39–53 (describing exemplary thicknesses where the thickness of the second sidewall is 2.5 times the thickness of the first sidewall).

Turning to the substance of the Intel 90 nm Report, Petitioner provides the following annotated version of Photograph 4.2.4 on page 40 of the Petition.



Photograph 4.2.4: High magnification SEM cross-section along a common poly line (silicon etch).

⁴ Although we need not expressly interpret the term because Petitioner's contentions are deficient for the reasons explained herein, Petitioner's view is consistent with the following interpretation of the distance limitation agreed upon by Patent Owner and the defendants in the related litigation involving the '726 patent: "the distance between the two closest points of the first gate electrode and the auxiliary pattern is smaller than the sum total of: the sum of *the thicknesses of the bases of the first and second side-wall insulating films*; and the double of the thickness of the stress-containing insulating film." See Ex. 1008, 7, 50 (emphasis added).

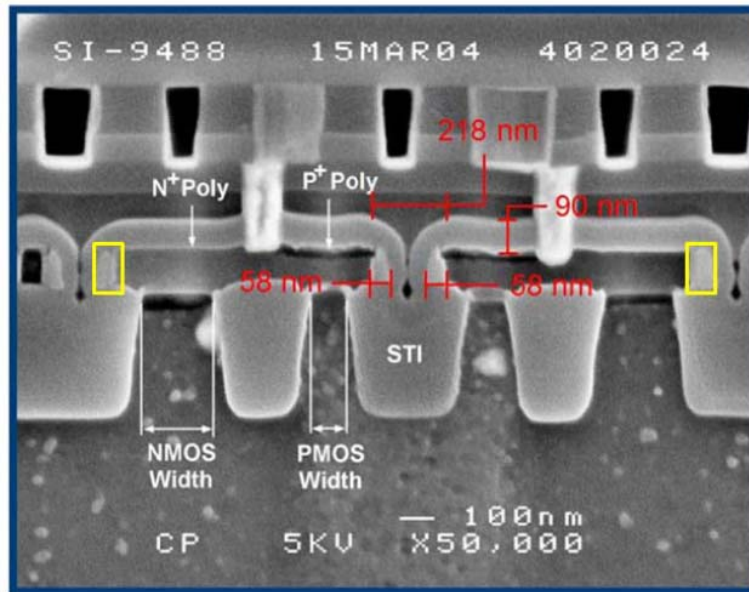
The annotated photograph above depicts, using the 100 nm scale of the photograph, the “distance between the first gate electrode and the auxiliary pattern” as 218 nm, the “thicknesses of the first and second side-wall insulating films” each as 58 nm, and the “thickness of the stress-containing silicon nitride insulating film” as 90 nm. Pet. 39. Thus, according to Petitioner, the distance between the first gate electrode and auxiliary pattern (218 nm) is less than the sum total of the thicknesses of the side-wall insulating films and double the thickness of the stress-containing insulating film (296 nm). *Id.* Petitioner does not explain in the Petition how the values in the annotated photograph were calculated, but cites Dr. Fair’s testimony as “identifying [his] measurement methodology” for the calculations. *Id.* (citing Ex. 1003 ¶¶ 93–99). Dr. Fair states that he measured “the four sidewall spacers present in” Photograph 4.2.4 and calculated their average thickness. Ex. 1003 ¶ 96. Dr. Fair similarly calculated the average of “six measurements” of the silicon nitride liner film thickness “at different locations where the film was horizontal and relatively flat,” and the average spacing between gate electrodes measured “in four places.” *Id.* ¶¶ 97–98.

We are not persuaded by Petitioner’s analysis regarding the distance limitation of claim 1. Petitioner does not point to any express disclosure in the Intel 90 nm Report of the relevant distance and thicknesses, instead relying on averages of various measurements made by Dr. Fair. See Pet. 39–40; Ex. 1003 ¶¶ 93–99. Petitioner and Dr. Fair, however, do not explain any basis for why it is appropriate to rely on averages of measurements of different components at different locations—as opposed to actual measurements of each component asserted to be the “first gate electrode,” “auxiliary pattern,” “first side-wall insulating film,” “second side-wall

insulating film,” and “stress-containing insulating film” recited in the claim—for purposes of calculating the distance limitation. For example, Petitioner does not contend that a person of ordinary skill in the art would have calculated averages and understood the reference to disclose certain values based on such a methodology. “Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference,” *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1255–56 (Fed. Cir. 1989), and that the claim limitations be “arranged or combined in the same way as recited in the claim[],” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Petitioner’s reliance on averages of various measurements, without any supporting explanation, is insufficient to show that the Intel 90 nm Report discloses the distance limitation of claim 1.

Moreover, even if Petitioner had provided a basis for using calculated averages, we are not persuaded by Dr. Fair’s calculation of “the thicknesses of the first and second side-wall insulating films.” As shown in the annotated versions of Photograph 4.2.4 above, Petitioner argues that the left gate electrode has a “first side-wall insulating film” on its right side, and the right gate electrode has a “second side-wall insulating film” on its left side, both shown in yellow and circled with a red dotted line. Pet. 22, 28–29, 33–35. Thus, there is one portion of the photograph that Petitioner relies on as a “first side-wall insulating film” and one portion that Petitioner relies on as a “second side-wall insulating film.” Dr. Fair, however, states that he measured “the *four* sidewall spacers present in the image” at the base of each sidewall spacer and then calculated the average of all four. Ex. 1003 ¶ 96 (emphasis added). Patent Owner provides the following additional

annotated version of Photograph 4.2.4 on page 46 of its Preliminary Response.



Photograph 4.2.4: High magnification SEM cross-section along a common poly line (silicon etch).

The annotated photograph above depicts Petitioner's alleged "first and second side-wall insulating films" (shown in red) and the other two sidewalls measured by Dr. Fair (shown in yellow boxes). Petitioner does not explain why the thicknesses of the other two sidewalls are relevant to calculating "the thicknesses of the first and second side-wall insulating films" recited in claim 1, or why it is proper to include them when calculating an average thickness. We agree with Patent Owner that Petitioner has not shown sufficiently that the Intel 90 nm Report discloses the distance limitation of claim 1. See Prelim. Resp. 44–49.

Accordingly, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claim 1 is anticipated by the Intel 90 nm Report.

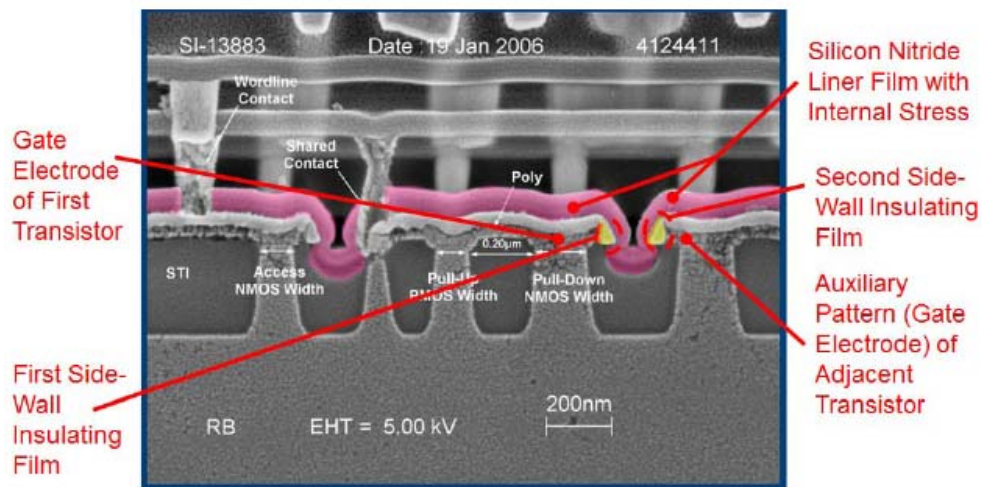
2. Other Claims

Independent claim 43 recites limitations similar to those of claim 1, including a “second gate electrode” (rather than an “auxiliary pattern” as in claim 1), “silicon nitride film” (rather than a “stress-containing insulating film” as in claim 1), and a similar distance limitation. Petitioner relies on its analysis of claim 1 for the distance limitation of claim 43. Pet. 45–46. We are not persuaded for the reasons explained above. *See supra* Section II.B.1. Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claims 1 and 43, or claims 4, 8–11, 13, 17–24, 26–28, 46, 49, 50, and 52–62, which depend therefrom, are anticipated by the Intel 90 nm Report.

C. Anticipation Ground Based on the Intel 65 nm Report (Claims 1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62)

Petitioner contends that claims 1, 4, 8–11, 13, 17–24, 26–28, 43, 46, 49, 50, and 52–62 are anticipated by the Intel 65 nm Report under 35 U.S.C. § 102(a), again relying on the testimony of Dr. Fair. Pet. 11–94 (citing Ex. 1003). We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted ground.

Petitioner's contentions regarding the Intel 65 nm Report are very similar to those regarding the Intel 90 nm Report. *See id.* at 12–45. For example, Petitioner provides the following annotated version of Photograph 4.3.4 of the Intel 65 nm Report on page 37 of the Petition.



Photograph 4.3.4: High magnification SEM cross-section showing the width of MOS transistors (glass etch).

The annotated photograph above depicts the two gate electrodes that Petitioner contends are a “first gate electrode” and “auxiliary pattern,” as well as the alleged “stress-containing insulating film” and “first and second side-wall insulating films.” *See id.* at 20, 22–23, 26–27, 29–30, 35–37. As with the Intel 90 nm Report, Petitioner relies on Dr. Fair’s calculations of various distances and thicknesses for the distance limitation of claim 1. *Id.* at 40–41 (citing Ex. 1003 ¶¶ 100–106). Dr. Fair states that he measured “the four sidewall spacers present in” Photograph 4.3.4 and calculated their average thickness, and calculated the average of “six measurements” of the silicon nitride liner film thickness “at different locations where the film was horizontal and relatively flat” and the average spacing between gate electrodes measured “in two places.” Ex. 1003 ¶¶ 103–105.

We are not persuaded by Petitioner's analysis regarding the distance limitation of claim 1, for reasons similar to those explained above regarding the Intel 90 nm Report. *See supra* Section II.B.1. Petitioner does not explain any basis for why it is appropriate to rely on averages of measurements of different components at different locations for purposes of meeting the distance limitation, and Dr. Fair relies on an average thickness of the alleged "first and second side-wall insulating films" and two other sidewalls (one of which is part of an entirely different gate electrode), without any explanation for why the other sidewalls are relevant. *See* Prelim. Resp. 44–49 (including an annotated version of Photograph 4.3.4 depicting the other two sidewalls in yellow boxes). Accordingly, Petitioner has not shown a reasonable likelihood of prevailing as to claim 1.

As discussed above, independent claim 43 recites limitations similar to those of claim 1, including a corresponding distance limitation. Petitioner relies on its analysis of claim 1 for the distance limitation of claim 43. Pet. 45–46. Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claims 1 and 43, or claims 4, 8–11, 13, 17–24, 26–28, 46, 49, 50, and 52–62, which depend therefrom, are anticipated by the Intel 65 nm Report.

*D. Other Asserted Grounds
(Claims 20, 22, 54, and 56)*

Petitioner contends that claims 20 and 54 are unpatentable over the Intel 90 nm Report and the Intel IEEE Paper, claims 22 and 56 are unpatentable over the Intel 90 nm Report and Doris, and claims 22 and 56 are unpatentable over the Intel 65 nm Report and Doris, under 35 U.S.C.

§ 103(a). Pet. 77–83. Claims 20 and 22 depend from claim 1, and claims 54 and 56 depend from claim 43. Petitioner does not argue that the distance limitation of claims 1 and 43 is taught by the Intel IEEE Paper or Doris, alone or in combination with the Intel reports. *Id.* We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on its asserted grounds for the reasons explained above with respect to parent claims 1 and 43. *See supra* Sections II.B, II.C.

E. Conclusion

We conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the '726 patent challenged in the Petition. Therefore, we do not institute an *inter partes* review on any of the asserted grounds as to any of the challenged claims.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied as to all challenged claims of the '726 patent;

FURTHER ORDERED that the version of Exhibit 1012 filed on February 16, 2017, is expunged from the record of this proceeding; and

FURTHER ORDERED that Exhibits 1005 and 1006 shall be expunged from the record of this proceeding after the deadline for filing a request for rehearing of this Decision has passed.

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Patent 8,354,726 B2

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