

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

Case IPR2017-01346
Patent 8,161,344 B2

Before MINN CHUNG, DANIEL J. GALLIGAN, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, NVIDIA Corporation (“Petitioner”) challenges the patentability of claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51 of U.S. Patent No. 8,161,344 B2 (“the ’344 patent,” Ex. 1001), which is assigned to Polaris Innovations Limited (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1, 4, 8–12, 16, 18, 43, 45, and 48–51 of the ’344 patent are unpatentable in this proceeding but has not proven by a preponderance of the evidence that claims 2, 19, 20, 22, 26–30, and 44 are unpatentable. See 35 U.S.C. § 316(e) (“In an *inter partes* review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.”).

A. Procedural History

On July 25, 2017, Petitioner requested *inter partes* review of claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51 of the ’344 patent. Paper 2 (“Pet.”). Patent Owner elected not to file a Preliminary Response. See Paper 7 (waiving right to file Preliminary Response). We instituted trial on all grounds of unpatentability, which are as follows:

1. Whether claims 1, 2, 4, 8–12, 19, 20, 22, 26–30, 43–45, and 48–51

are unpatentable under 35 U.S.C. § 102(b) over ADSL;¹

2. Whether claims 16 and 18 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of ADSL and Voith;² and
3. Whether claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51 are unpatentable under 35 U.S.C. § 103(a) over Grube.³

Paper 8 (“Dec. on Inst.”), 23.

During the trial, Patent Owner filed a Response (Paper 14, “PO Resp.”), and Petitioner filed a Reply (Paper 18, “Pet. Reply”). An oral hearing was held on August 17, 2018, a transcript of which appears in the record. Paper 25 (“Tr.”). Following the hearing, with our authorization (Paper 26), the parties filed additional briefing addressing the broadest reasonable interpretation of “data arrangement alteration.” Papers 27, 28.

B. Real Parties in Interest

Patent Owner identifies itself, Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 6, 2.

C. Related Matters

Petitioner and Patent Owner cite the following judicial matter involving the ’505 patent: *Polaris Innovations Ltd. v. Dell Inc. & NVIDIA Corp.*, Case No. 4:16-cv-07005 (N.D. Cal.). Pet. 97; Paper 4, 2–3. The ’344 patent is also at issue in IPR2017-01781, in which we are issuing a final written decision concurrently with this Decision.

¹ American National Standard for Telecommunications – Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface, ANSI T1.413-1998 c.1 (© 1999) (Ex. 1004).

² US 5,737,337, issued Apr. 7, 1998 (Ex. 1006).

³ US 5,606,577, issued Feb. 25, 1997 (Ex. 1005).

D. The '344 Patent and Illustrative Claim

The '344 patent generally relates to circuits for error coding.
Ex. 1001, Abstract, 1:11–12. Figure 1A, reproduced below, illustrates an embodiment of such a circuit.

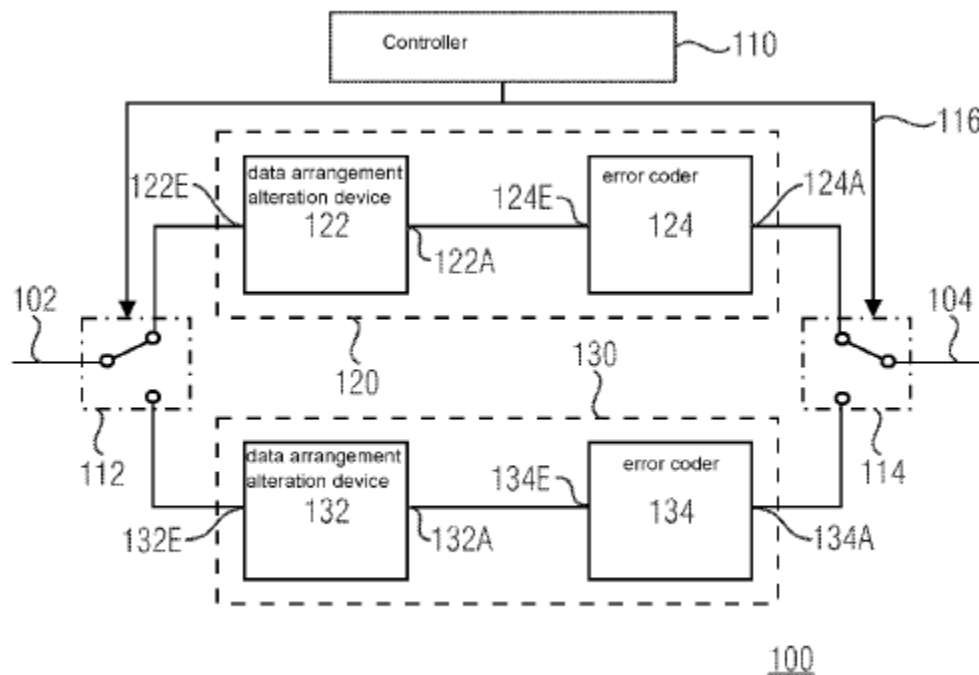


FIG 1A

Figure 1A illustrates an error coding circuit having controller 110, input 102, first error coding path 120, second error coding path 130, and output 104.

Ex. 1001, 3:27–30. As illustrated in Figure 1A, each of error coding paths 120 and 130 has a data arrangement alteration device and an error coder.

Ex. 1001, 3:30–34. The '344 patent explains that control indicator 116 is used to select between the first and second error coding paths. Ex. 1001, 4:41–47.

Of the claims at issue in the present proceeding, claims 1, 16, 19, and 43 are independent claims. Claim 1 is illustrative and is reproduced below.

1. A circuit for creating an error coding data block for a first data block, the circuit comprising:
 - a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding;
 - and
 - a second error coding path adapted to selectively create a second error coding data block in accordance with a second error coding;
 - the first error coding path and the second error coding path being selected as a function of a control indicator, and at least the first error coding path comprising a data arrangement alteration device.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Tredennick, testifies that "[a] person of ordinary skill in the art as of the time of the '344 patent (POSITA) would have had a Bachelor's degree in Electrical Engineering and at least 2 years of experience working in the field of semiconductor logic design." Ex. 1003

¶ 13. Neither Patent Owner, nor its declarant, Dr. Przybylski, offers a different assessment of the level of ordinary skill in the art. See Ex. 2002 ¶ 38 ("I am applying the definition of the level of experience of a person of ordinary skill in the art that has been put forward by Dr. Tredennick in his declaration. I do not necessarily agree with the definition offered there, but I do not presently believe that the exact level of experience of a person of ordinary skill impacts my opinions offered herein.").

Based on the evidence of record, we adopt Dr. Tredennick's statement of the level of ordinary skill in the art with the exception of the language "at least." Thus, we determine that the skill level of a person of ordinary skill in the art would have been that of a person with a bachelor's degree in

electrical engineering and two years of experience working in the field of semiconductor logic design.

B. Claim Interpretation

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2016). In applying a broadest reasonable construction, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). This presumption may be rebutted when a patentee, acting as a lexicographer, sets forth an alternate definition of a term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Furthermore, only terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). We determine it is necessary to construe expressly only the claim terms discussed below to resolve the disputed issues before us in this proceeding.

1. Data Arrangement Alteration

Each of the challenged claims recites a “data arrangement alteration device” or a “data arrangement alteration algorithm.” The broadest reasonable interpretation of “data arrangement alteration” is at issue in this case and in IPR2017-01781, but the disputes in each proceeding are different. Here, there are two main disputes, namely (1) what types of

operations are encompassed within “data arrangement alteration” and (2) whether data arrangement alteration must be performed at a block level. Following oral argument, we authorized the parties to file additional briefing addressing the broadest reasonable interpretation of “data arrangement alteration.” Papers 26, 27, 28.

a. Operations encompassed within “data arrangement alteration”

Petitioner argues that the “[t]he ’344 patent imposes no requirements on how ‘data arrangement alteration’ is achieved.” Paper 27, 2. In support, Petitioner cites the following disclosure in the ’344 patent: “Any implementations which may change an arrangement of data such that these data will be processed in an optimum manner for a subsequent error detection or correction algorithm may be considered as a potential data arrangement alteration device 222.” Ex. 1001, 10:34–38, *cited in* Paper 27, 3. According to Petitioner, “[t]hrough this disclosure, the ’344 patent places no limit on how ‘data []arrangement alteration’ is achieved, and covers any rearrangement whether it is achieved through bit reordering, inversion, or other types of logical bit operations.” Paper 27, 3; *see also* Pet. Reply 6 (arguing that “alter[ing] the arrangement of the data by randomizing the data in a deterministic way that can be descrambled in the receiver” is within the broadest reasonable interpretation of “data arrangement alteration”). Patent Owner argues that Petitioner’s proposed interpretation “is so broad as to encompass a myriad of alterations that are understandable and reversible (e.g., $y = x^3$) but which clearly are not arrangement alterations.” Paper 28, 5. We agree with Patent Owner. Even if the ’344 patent does not limit how data arrangement alteration is achieved, the *arrangement* of the data must be altered to give full effect to the claim

language. The portions of the specification of the '344 patent cited by Petitioner confirm this.

In one instance, the '344 patent states:

In the first error coding path 120, the first data arrangement alteration device 122 is adapted to create a second data block on the basis of the first data block, which comprises the given number of data *in a second arrangement*, and to output it to the first error coder 124.

Ex. 1001, 3:63–67 (emphasis added), *cited in* Paper 27, 2. Another passage states:

The data arrangement alteration device 222 is adapted to receive, at the input 222E or 102, a first data block comprising a given number of data in the first arrangement, and to generate, on the basis of the first data block, a second data block comprising the given number of data *in a second arrangement*

Ex. 1001, 6:14–18 (emphasis added), *cited in* Paper 27, 2. These passages show that data arrangement alteration takes data and puts those data into a different arrangement. Petitioner also cites the '344 patent's disclosure of a deserializer changing the "representation" of data. Paper 27, 2–3 (citing Ex. 1001, 8:58–62, 9:2–7). But, in this operation, "the second data block 440 . . . *comprises the same data*, namely the 72 bits of the first data block 435 in a second arrangement which is different from the first arrangement of the first data block." Ex. 1001, 9:32–35 (emphasis added). Petitioner also cites an example in the '344 patent in which the burst length is halved from eight time pulses to four time pulses. Ex. 1001, 11:52–61, *cited in* Paper 27, 4. The '344 patent describes that, in this scenario, only half of the bits (36 out of 72) "will be occupied with processable data." Ex. 1001, 11:59–60. Petitioner contends that this describes an output of 72

bits that is larger and different than the input of only 36 bits. Paper 27, 4. The '344 patent, however, describes providing “a further subarea of the matrix 420 for this mode, and to control the multiplexer 430, via the mode register 110, *such that this subarea will be read out*, so that, for example, only 36 of the 72 bits will be occupied with processable data.” Ex. 1001, 11:56–60 (emphasis added). Thus, it is the subarea having the 36 bits of processable data that is read out. But even if Petitioner is correct that the output is larger than the input in this example, data *arrangement* alteration still requires an alteration of the arrangement of the input data, even if the output contains additional data.

In all of the examples in the specification of the '344 patent, therefore, the arrangement of the data is altered. We see nothing in the intrinsic record to support a conclusion that merely altering data satisfies the requirement of data arrangement alteration. Petitioner also cites Dr. Przybylski's testimony that the word “alter” means “[t]o change in an understandable way.” Ex. 1020, 119:12–15, *cited in* Pet. Reply 18–19. Petitioner contends, under this definition of “alter,” “a reversible operation” that “changes the data in an ‘understandable way,’” allowing the original data to be regenerated, is within the broadest reasonable interpretation of “data arrangement alteration.” Pet. Reply. 19. But this describes data alteration, not necessarily data *arrangement* alteration.

Petitioner also cites testimony from both parties' declarants that Petitioner argues supports its contention that data arrangement alteration encompasses inverting data, which is an operation relied upon by Petitioner in IPR2017-01781 to teach data arrangement alteration. Paper 27, 2 (citing Ex. 1019 ¶¶ 60–61; Ex. 1029, 50:12–51:5; Ex. 1030, 148:13–150:1). This

extrinsic evidence, however, fails to explain how “data arrangement alteration,” as described in the ’344 patent, would have been understood. In light of the intrinsic record discussed above, we do not find the extrinsic evidence to be particularly useful in determining the broadest reasonable interpretation of “data arrangement alteration.” *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (en banc) (authorizing the consideration of extrinsic evidence in determining the meaning of claims but noting that it is “in general . . . less reliable than the patent and its prosecution history in determining how to read claim terms”).

For its part, Patent Owner argues that “a ‘data arrangement alteration device’ should be interpreted as a device that *can* alter the arrangement of data in a data block.” PO Resp. 8–9 (emphasis added). As explained above, however, the specification of the ’344 patent describes a data arrangement alteration device as a device that alters the arrangement of data, not a device that merely has the capability to do it. Consider a data block of eight bits, having four 0s and four 1s, that goes into a device that inverts each bit. The result of the inversion operation will be eight bits having 1s where the 0s were and 0s where the 1s were. Although the device alters the data by inverting each bit, the *arrangement* of the data is also changed because the input data were evenly divided between 0s and 1s. This arrangement alteration, however, is merely a circumstance of the input data. Patent Owner’s proposed construction would encompass seemingly any data alteration device because there likely will be some input to the device that will result in the data’s arrangement being altered. This is not consistent with the description of the claimed subject matter in the specification of the ’344 patent. *See In re Smith Int’l, Inc.*, 871 F.3d 1375, 1382–83 (Fed. Cir.

2017) (quoting *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997)) (stating that the broadest reasonable interpretation “is an interpretation that corresponds with what and how the inventor describes his invention in the specification, i.e., an interpretation that is ‘consistent with the specification’”).

Thus, “data arrangement alteration” requires the alteration of the arrangement of data, not merely the alteration of data.

b. Data arrangement alteration at a block level

Patent Owner argues that data arrangement alteration must be performed at a block level such that “each data block is encoded by itself completely and independently, without influence from any other data block coming before or after the processed data block.” PO Resp. 10; *see also* Paper 28, 1–4. Petitioner disagrees. Pet. Reply 8–11; Paper 27, 5. The following passage from the ’344 patent is instructive:

A piece of data may be, for example, a bit, and a data word may consist of several bits, for example. It is possible for a data word to be formed of several bits which are received in a serial manner, i.e., successive in time, or to be formed by several bits which are received at the same time (parallel interface). In this context, what is meant by data block is a serial data word, a parallel data word, or a serial sequence of parallel data words, as is depicted, for example, by reference numeral 435 in FIG. 4. Embodiments of the data arrangement alteration device 222 are adapted to change any of these types of data blocks or all of them in accordance with at least one data arrangement alteration algorithm so as to optimize error detection, or at least to improve error detection as compared to an approach without any change in the data arrangement, by means of the subsequent error coding algorithms.

Ex. 1001, 11:66–12:14. A data word may be several bits and a “data block” may be a data word. Thus, the ’344 patent uses the term “data block” to

refer to a grouping of data.

Determining whether an arrangement of data is altered requires looking at a particular grouping of data from input to output. To that extent, we agree with Patent Owner that the '344 patent describes performing data arrangement alteration on data blocks. The term "data block," however, is not limited by the '344 patent to any particular structure or length.

Dr. Przybylski testifies that "[a] block of data as it is used in the '344 specification, and generally in the industry, is a unit of data that is conceptually, physically, or temporally treated as a single unit." Ex. 2002 ¶ 48. Patent Owner argues that "[a] data block is an associated, delimited set of data." PO Resp. 10. These definitions are not helpful in understanding what a data block is beyond how it is described in the '344 patent—as a grouping of data.

As to Patent Owner's argument that in the claims "each data block is encoded by itself completely and independently, without influence from any other data block coming before or after the processed data block" (PO Resp. 10), we find no intrinsic support for imposing this negative limitation, which is not found in the claims, on "data arrangement alteration." Rather, as discussed above, the specification of the '344 patent describes that data arrangement alteration requires altering the arrangement of data. It does not impose a restriction that data arrangement alteration must be performed "without influence from any other data block coming before or after the processed data block."

Nor do the challenged claims require that all data in a particular block, or grouping of data, be rearranged. Claim 8 is instructive on this point. Claim 8 recites:

The circuit as claimed in claim 1, wherein the data arrangement alteration device is adapted to create a second data block, *comprising a given number of data* in a second arrangement, *on the basis of* the first data block *comprising the given number of data* in a first arrangement, in accordance with a data arrangement alteration algorithm.

Ex. 1001, 14:59–64 (emphases added). Claim 8, therefore, uses the open-ended term “comprising,” which means that each data block may have data in addition to the “given number of data,” but the claim requires putting the “given number of data” into a different (second) arrangement. Thus, the challenged claims do not require that all data in a particular grouping of data be rearranged. By contrast, claim 39, which is not challenged, recites a device “adapted to convert a first data block to a parallel intermediate arrangement, *so that all data* of the first data block are arranged in parallel with one another.” Ex. 1001, 17:36–41 (emphasis added).

c. Conclusion as to data arrangement alteration

Based on the foregoing and upon considering the complete record, we determine that “data arrangement alteration device” is a device that alters the *arrangement* of data in a grouping of data. A “data arrangement alteration algorithm,” similarly, is an algorithm that specifies how to alter an arrangement of data in a grouping of data.

2. Means-Plus-Function Limitations

In the Decision on Institution, we addressed, but did not adopt, Petitioner’s proposed constructions for several means-plus-function limitations, and, instead, we set forth our own constructions. Dec. on Inst. 5–9. For purposes of this Decision, it is necessary to discuss only two means-plus-function limitations, for which Petitioner’s proposed constructions are set forth in the table below.

Limitation	Petitioner's Proposed Function and Structure
Claim 19: means for selectively performing a first error coding so as to create a first error coding data block	<u>Function:</u> selectively performing a first error coding so as to create a first error coding data block <u>Structure:</u> one or more devices, including a first error coder. Pet. 13–14 (citing Ex. 1001, 3:27–34, 3:57–4:25, 7:16–24, 13:45–67).
Claim 19: means for performing a data arrangement alteration algorithm	<u>Function:</u> performing a data arrangement alteration algorithm <u>Structure:</u> a data arrangement alteration device. <i>Id.</i> at 14–15 (citing Ex. 1001, 6:14–25, 6:42–65, 7:10–24).

In the Decision on Institution, we construed these terms as set forth in the table below.

Limitation	Function and Structure
Claim 19: means for selectively performing a first error coding so as to create a first error coding data block	<u>Function:</u> selectively performing a first error coding so as to create a first error coding data block <u>Structure:</u> first error coding path 120 and equivalents. <i>See</i> Ex. 1001, 3:27–34, 3:57–4:25, 5:53–64, Figs. 1A, 1E.
Claim 19: means for performing a data arrangement alteration algorithm	<u>Function:</u> performing a data arrangement alteration algorithm <u>Structure:</u> data arrangement alteration devices 122, 132, and 222 and equivalents. <i>See id.</i> at 3:27–34, 5:65–6:25, 6:42–65, 8:55–57, 10:34–45, Figs. 1–4.

Dec. on Inst. 8–9.

Patent Owner argues that our preliminary determination for “means for selectively performing a first error coding so as to create a first error coding data block” does not address the selectivity recited in the claim and argues that the corresponding structure includes the structure that adds selectivity, such as switches 112 and 114. Petitioner argues that switching structure is unnecessary because the paths selectively perform error coding based on whether they have received data. Pet. Reply 21–22. Petitioner also argues that claim 19’s recitation that the first and second means are “selected as a function of a control indicator” “confirms that the selection is between the two, distinct means and, thus, necessarily prior to and outside of either one.” Pet. Reply 22.

This dispute is about whether additional structure, beyond that stated in our previous construction above, is required for performing the recited functions. Neither party asserts that the corresponding structure for “means for selectively performing a first error coding” does not include at least what we identify as corresponding structure above. Because Petitioner has not shown that either ADSL or Grube teaches the same or equivalent structure using our constructions outlined above, we need not address the parties’ dispute as to whether additional structure is required. We, therefore, apply the constructions outlined in our Decision on Institution for “means for selectively performing a first error coding so as to create a first error coding data block” and “means for performing a data arrangement alteration algorithm.” See Dec. on Inst. 8–9.

C. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Anticipation by ADSL *(Claims 1, 2, 4, 8–12, 19, 20, 22, 26–30, 43–45, and 48–51)*

Petitioner contends claims 1, 2, 4, 8–12, 19, 20, 22, 26–30, 43–45, and 48–51 of the ’344 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL. Pet. 1, 4–9, 16–46.

1. ADSL

ADSL is a publication of the American National Standards Institute (ANSI) entitled *Network and Customer Installation Interfaces – Asymmetric*

Digital Subscriber Line (ADSL) Metallic Interface, and it bears a copyright date of 1999. Ex. 1004. Citing the Declaration of Jessica Coral Sheldon-Hess, Petitioner contends ADSL is prior art under 35 U.S.C. § 102(b). Pet. 2 (citing Ex. 1014, 4–5). Ms. Sheldon-Hess testifies that, based on ADSL’s Machine Readable Cataloging (MARC) record obtained from Illinois State Library, ADSL was available to the public as of 1999. Ex. 1014 ¶¶ 8–10. Patent Owner does not dispute the prior art status of ADSL.

Petitioner’s evidence establishes that ADSL was publicly available as a printed publication more than one year before the U.S. filing date for the ’344 patent, which is March 11, 2008. *See* Ex. 1001, [22]. Based on this evidence, we determine that ADSL qualifies as a prior art printed publication under 35 U.S.C. § 102(b).

ADSL is a “standard [that] describes the interface between the telecommunications network and the customer installation in terms of their interaction and electrical characteristics. The requirements of this standard apply to a single asymmetric digital subscriber line (ADSL).” Ex. 1004, 1.⁴ ADSL describes an ADSL Transceiver Unit (ATU) supporting asynchronous transfer mode (ATM) having “[t]wo paths . . . between the Mux/Sync control and Tone ordering; the ‘fast’ path provides low latency; the interleaved path provides very low error rate and greater latency.” Ex. 1004, 10.

⁴ We cite to the page numbers of the reference itself rather than to the Exhibit page numbers assigned by Petitioner.

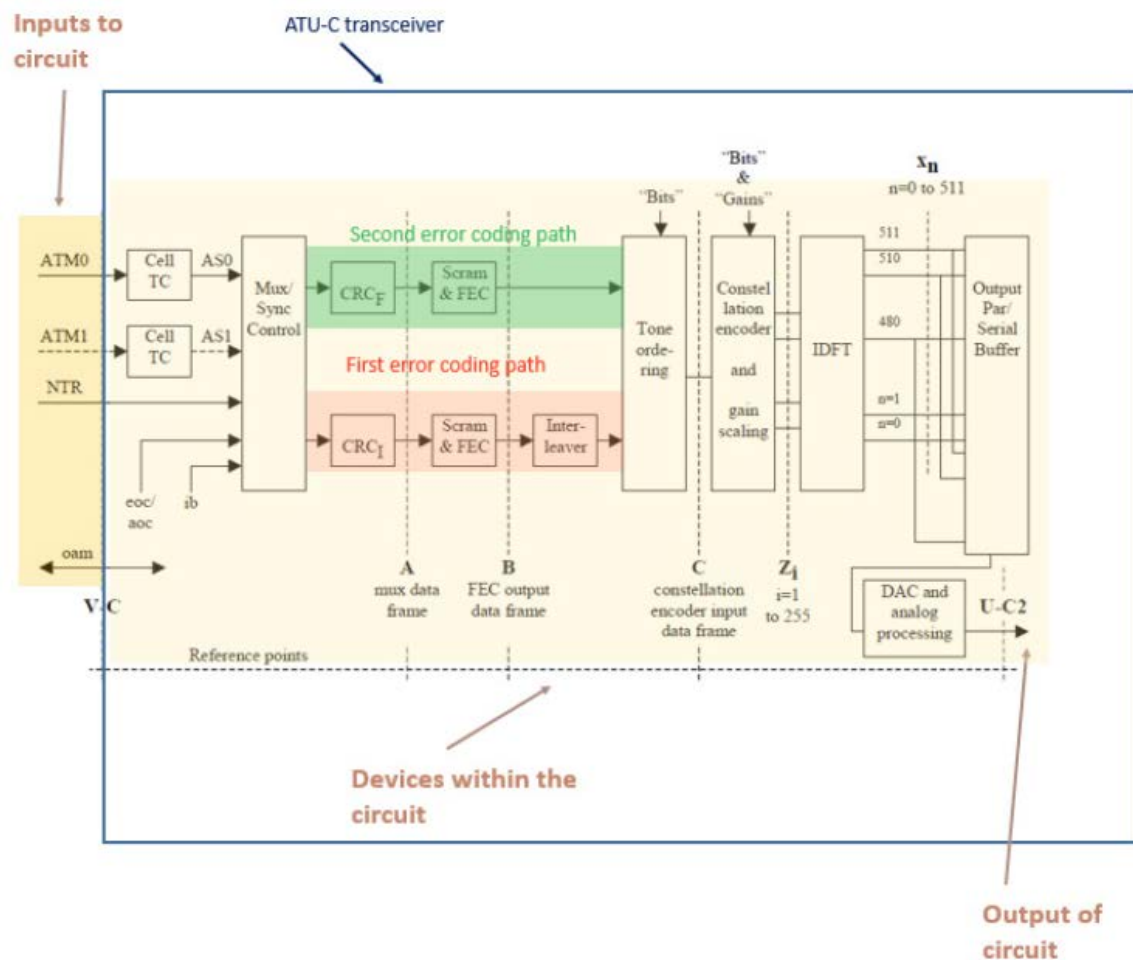
2. Claim 1

a. First and second error coding paths

Independent claim 1 is reproduced above and is directed to “[a] circuit for creating an error coding data block for a first data block.” Petitioner contends ADSL’s ATU-C (ADSL transceiver unit, central office end) discloses the claimed “circuit.” Pet. 16–17 (citing Ex. 1004, vi, 11, 25–40, Figs. 1, 3; Ex. 1003 ¶¶ 60–72).

Claim 1 recites that the circuit comprises “a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding” and “a second error coding path adapted to selectively create a second error coding data block in accordance with a second error coding.” Claim 1 further recites “the first error coding path and the second error coding path being selected as a function of a control indicator.”

With its anticipation analysis, Petitioner provides an annotated version of Figure 3 from ADSL, which is reproduced below.



In this annotated version of Figure 3 from ADSL, Petitioner identifies a “first error coding path” in red and a “second error coding path” in green. Pet. 17. Referring to Figure 3, ADSL discloses that “[t]wo paths are shown between the Mux/Sync control and Tone ordering; the ‘fast’ path provides low latency; the interleaved path provides very low error rate and greater latency.” Ex. 1004, 11.

Petitioner contends that the “interleaved path” of ADSL’s Figure 3 discloses the claimed “first error coding path” and that the “fast path” discloses the claimed “second error coding path.” Pet. 20–23. Petitioner contends each of these paths includes two error coding devices, CRC (cyclic redundancy check) device and FEC (forward error correction) encoder.

Pet. 18–19 (citing Ex. 1004, 25; Ex. 1003 ¶¶ 60–72). According to Petitioner, both paths “create[] CRC and FEC codes, both of which are error coding blocks for message data that serves as a first data block.” *Id.* at 21, 22 (citing Ex. 1004, 25–26, 32–33, 38–39, 87–88; Ex. 1003 ¶¶ 73–89). Petitioner contends these paths are “selected as a function of a control indicator,” as recited in claim 1. *Id.* at 23–25. In particular, Petitioner argues Virtual Path Identifier and Virtual Connection Identifier disclose the claimed control indicator. *Id.* Although Patent Owner does not provide specific arguments regarding these particular limitations of claim 1, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware LLC, v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). For the reasons explained below, we are persuaded by Petitioner’s arguments and evidence.

ADSL discloses performing cyclic redundancy checks (CRC) in both the fast and the interleaved paths, after which a “Mux data frame” is generated, which is “the multiplexed, synchronized data after the crc has been inserted.” Ex. 1004, 25, 32–33. ADSL discloses Reed-Solomon coding as the forward error correction (FEC) coding, as a result of which a “FEC output data frame” is generated. Ex. 1004, 26, 38–39. Dr. Tredennick testifies that “ADSL uses the CRC codes and the FEC Reed-Solomon codes as error coding data blocks for error coding purposes” and that the CRC device and the FEC encoder are adapted to create error coding data blocks. Ex. 1003 ¶¶ 72, 73, 78. Based on this evidence, we find ADSL describes “a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding” and “a second error coding

path adapted to selectively create a second error coding data block in accordance with a second error coding.”

We further find ADSL describes “the first error coding path and the second error coding path being selected as a function of a control indicator.” In particular, ADSL discloses that “[t]he ATM Layer performs cell multiplexing from and demultiplexing to the appropriate physical port (i.e. latency path - fast or interleaved) based on the Virtual Path Identifier (VPI) and Virtual Connection Identifier (VCI), both contained in the ATM cell header.” Ex. 1004, 220 (Annex J), *quoted in* Pet. 24; *see also* Ex. 1004, 11 (“The Cell TC Sublayer has an interface towards the ATM Layer (V-C interface) and an interface towards the ADSL (Mux/Sync Control block interface). Informative details on the relationship between these Cell TC Sublayer interfaces are provided in Annex J.”). Thus, the fast and interleaved paths are chosen based on the Virtual Path Identifier (VPI) and Virtual Connection Identifier (VCI), thereby describing that the paths are selected as a function of a control indicator.

b. Data arrangement alteration

Claim 1 further recites “at least the first error coding path comprising a data arrangement alteration device.” Petitioner argues that two devices in ADSL describe data arrangement alteration devices—the scrambler in each path and the interleaver in the interleaved path. Pet. 25–28. Patent Owner argues that neither of these devices describes a data arrangement alteration device. PO Resp. 20–33. We address the parties’ contentions with respect to each of these devices below.

i. Interleaver

Petitioner contends ADSL's interleaver receives data and outputs that data in a different order, thus describing a data arrangement alteration device. Pet. 26–27 (citing Ex. 1004, 11, 25, 39–40, Fig. 3; Ex. 1003 ¶¶ 82–85). Patent Owner argues that ADSL's interleaver does not change the order of the data in a codeword and, therefore, is not a data arrangement alteration device. PO Resp. 20–25.

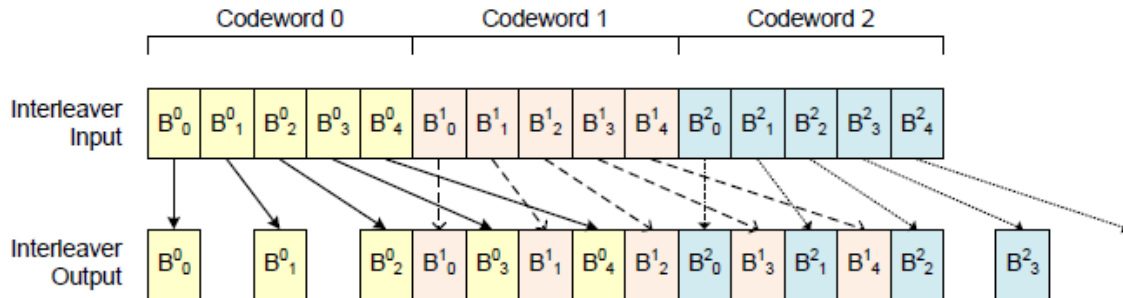
ADSL's Table 11, reproduced below, shows interleaver input and output data sequences.

Table 11 - Convolutional interleaving example for $N = 5$, $D = 2$

Inter-leaver input	B^j_0	B^j_1	B^j_2	B^j_3	B^j_4	B^{j+1}_0	B^{j+1}_1	B^{j+1}_2	B^{j+1}_3	B^{j+1}_4
Inter-Leaver output	B^j_0	B^{j-1}_3	B^j_1	B^{j-1}_4	B^j_2	B^{j+1}_0	B^j_3	B^{j+1}_1	B^j_4	B^{j+1}_2

Table 11 shows a convolutional interleaving example for a codeword size (N) of 5 bytes and an interleave depth (D) of 2. Ex. 1004, 39. The superscript j denotes the codeword, and the subscript i denotes the byte in the codeword. Ex. 1004, 39; *see also* PO Resp. 23. Therefore, B^j_0 – B^j_4 denote bytes 0 through 4 of the j -th codeword. Ex. 1004, 39; *see also* PO Resp. 23. ADSL explains that the interleaver delays B_i by the product of $(D-1)$ and i . Ex. 1004, 39. In the example in Table 11, byte B^j_0 occupies the same time slot in the input and in the output because multiplying $(2-1)$ by 0 results in 0. Byte B^j_1 is delayed one time slot because multiplying $(2-1)$ by 1 results in 1, and a byte from the previous codeword is placed between byte B^j_0 and B^j_1 in the output.

Patent Owner provides the following illustration showing interleaving:



The image above shows an example of interleaving for three codewords. PO Resp. 24 (citing Ex. 2002 ¶ 80). Patent Owner’s example is consistent with Table 11 of ADSL. According to Patent Owner, “[t]his presentation of convolution interleaving shows clearly that the bytes and/or bits of each codeword are not changed in order or rearranged in any way.” PO Resp. 24. We disagree. Although the bytes in each codeword are in the same time sequence—from B^1_0 to B^1_4 in codeword 1, for example—in both the input and the output, the bytes are not in the same *arrangement*. Every byte except B^1_0 in codeword 1 was moved to a different time slot in the output, as shown in Patent Owner’s illustration, and other data were interleaved with the bytes from codeword 1.

With its anticipation analysis, Petitioner provides the following annotated version of ADSL’s Table 11:

Inter-leaver input	B^j_0	B^j_1	B^j_2	B^j_3	B^j_4	B^{j+1}_0	B^{j+1}_1	B^{j+1}_2	B^{j+1}_3	B^{j+1}_4
Inter-leaver output	B^j_0	B^{j+1}_3	B^j_1	B^{j+1}_4	B^j_2	B^{j+1}_0	B^j_3	B^{j+1}_1	B^j_4	B^{j+1}_2

Petitioner's annotated Table 11 shows a color correspondence between input bytes and their location in the output from the interleaver. Pet. 27. As shown, bytes B^j_0 through B^j_4 are in consecutive time slots in the input to the interleaver, but their arrangement in the output is changed with bytes B^j_1 through B^j_4 being moved to different time slots in the output according to the interleaving formula discussed above. Ex. 1004, 39. Although the output includes data from codewords B^{j-1} and B^{j+1} interleaved with data from codeword B^j , the arrangement of bytes B^j_0 through B^j_4 is still altered from input to output, thus satisfying the definition of "data arrangement alteration device" set forth above. See Section II.B.1.c above. Patent Owner's argument that the interleaver in ADSL does not alter the arrangement of data in a data block is also premised on Patent Owner's claim construction argument that "each data block is encoded by itself completely and independently, without influence from any other data block coming before or after the processed data block." See PO Resp. 10, 24–25. As discussed above, however, we disagree with Patent Owner's proposed construction, and we conclude the challenged claims do not require that all data in a particular block, or grouping of data, be rearranged. See Section II.B.1.b above. Thus, we find ADSL's interleaver alters the arrangement of data by moving bytes into different time slots from input to output, as shown in Patent Owner's illustration of interleaving above.

Based on the foregoing, we find ADSL's interleaved path, which has an interleaver, describes "at least the first error coding path comprising a data arrangement alteration device."

ii. Scrambler⁵

Petitioner also argues that the scrambler in both paths discloses a “data arrangement alteration device” because it “re-arranges the order of the bits of data according to the same algorithm.” Pet. 27–28 (citing Ex. 1004, 37–38; Ex. 1003 ¶¶ 86–88). According to Petitioner, “ADSL’s scrambler receives bits from CRC device, re-orders the bits, and outputs re-ordered bits to FEC encoder.” Pet. 28 (citing Ex. 1004, 37–38; Ex. 1003 ¶¶ 86–88). Petitioner cites the scrambler in ADSL’s Figure 15, which is reproduced below.

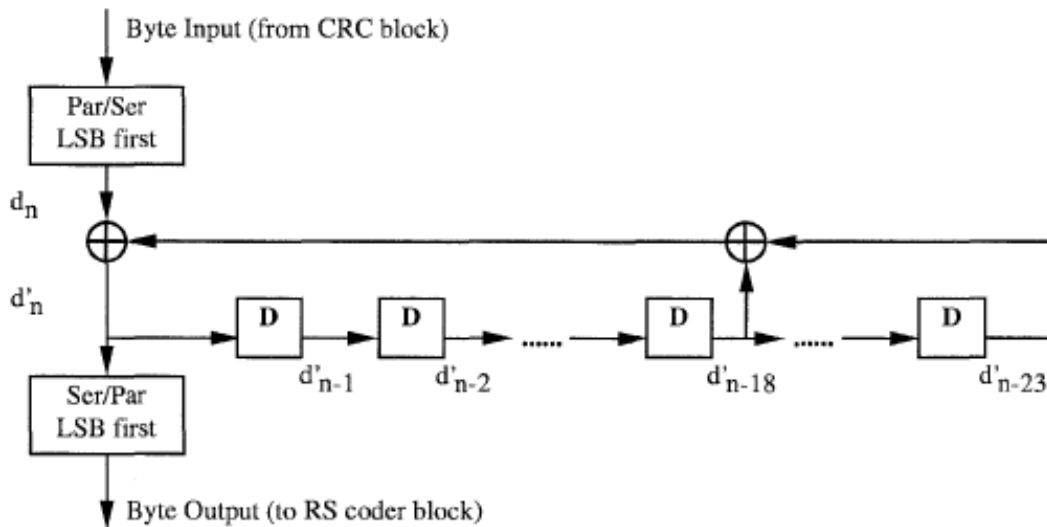


Figure 15 - Scrambler

Ex. 1004, 38. Figure 15 illustrates a scrambler that operates according to the following formula:

⁵ Although we have determined that ADSL’s interleaved path teaches an error coding path with a “data arrangement alteration device” commensurate with the limitation in claim 1, we nonetheless consider Petitioner’s additional arguments regarding ADSL’s scrambler because they are germane to our analysis of certain other challenged claims, as discussed below.

$$d_n' = d_n \oplus d_{n-18}' \oplus d_{n-23}'$$

Ex. 1004. 37. In the equation, “ d_n is the n -th output from the fast or interleaved buffer (i.e., input to the scrambler), [and] d_n' is the n -th output from the corresponding scrambler.” Ex. 1004, 37. The symbol $\oplus$ denotes the exclusive-or operation.

Patent Owner’s declarant, Dr. Przybylski, provides a detailed explanation of the operation of ADSL’s scrambler. Ex. 2002 ¶¶ 68–74, *cited in* PO Resp. 29. Petitioner does not dispute Dr. Przybylski’s technical characterization of the scrambler’s operation in ADSL. Tr. 33:25–34:9. Dr. Przybylski shows that injecting a single “1” as an input to the scrambler with all other inputs in the stream being “0” will create significant variation in the output data over time, such that, by cycle number 2000, there will be ten “1’s” in the previous 23 outputs from the scrambler. Ex. 2002 ¶¶ 68–71. Dr. Przybylski testifies that, “[b]y this behavior of the circuit, even a long string of zeros or ones is ‘randomized’ or turned into an output sequence involving a mix of ones and zeros in a way that can be reversed in the receiver to produce the original input stream.” Ex. 2002 ¶ 72.

Petitioner argues,

ADSL’s scrambling does not change the meaning of the data either—it temporarily and reversibly changes the data’s *arrangement*. The scrambling operation is fundamentally similar to the examples in the ’344 patent, in that scrambling is an operation designed to be fully reversible so that the meaning of the data is never changed—rather, its binary representation (i.e., arrangement) undergoes temporary alteration.

Pet. Reply 18. We are not persuaded by Petitioner’s position. ADSL’s scrambler alters data, as shown by Dr. Przybylski. Petitioner’s argument that ADSL’s scrambling operation is reversible does not, however, explain

how the operation alters the *arrangement* of data. Merely because an operation can be reversed does not mean that operation performs data arrangement alteration, as claimed in the '344 patent. As discussed above, this interpretation of “data arrangement alteration” is not supported by the specification of the '344 patent, and, therefore, is not consistent with our construction of that term. *See* Section II.B.1.a above.

Although ADSL's scrambler alters data in a reversible manner, Petitioner has not shown the scrambler alters the *arrangement* of data, as required by claim 1. Thus, we are not persuaded ADSL's scrambler describes a “data arrangement alteration device.”

c. Determination of unpatentability of claim 1

Although Petitioner has not shown ADSL's scrambler describes a “data arrangement alteration device,” Petitioner has shown ADSL's interleaver describes this subject matter. As discussed above, we find ADSL describes all of the limitations of claim 1. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 1 of the '344 patent is unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

3. Independent Claim 43

Independent claim 43 is directed to “[a] method of creating an error coding data block for a first data block” and recites “receiving the first data block” before reciting method steps that correspond to the limitations of claim 1. Petitioner contends ADSL describes receiving a first data block via ATM0 and ATM1 channels in Figure 3 and performing a method of creating an error coding data block for a first data block. Pet. 42–43 (citing Ex. 1004, 11, 16, 20, 25; Ex. 1003 ¶¶ 144–145). For the remaining limitations of

claim 43, Petitioner refers to its analysis of the limitations of claim 1 reciting similar subject matter. Pet. 43–44.

Patent Owner relies on the same arguments for claim 43 that it raises for claim 1, namely that ADSL does not describe data arrangement alteration. PO Resp. 20–33. Nonetheless, the burden remains on Petitioner to prove unpatentability.

We are persuaded by Petitioner’s contentions that ADSL describes the subject matter of claim 43. We find ADSL describes “receiving the first data block” based on Figure 3’s disclosure of data being input via ATM0 and ATM1. Ex. 1004, 11; *see also* Ex. 2002 ¶ 58 (Dr. Przybylski referring to ADSL’s Figure 3 and testifying that “[d]ata to be sent to the customer arrives in the ATU-C at the inputs at the left. ATM0 and ATM1 are the principal paths for incoming high-speed data.”). Claim 43 recites “at least the step of selectively performing the first error coding comprises the step of performing a data arrangement alteration algorithm.” As discussed above with respect to claim 1, we find ADSL describes how its interleaver alters the arrangement of data, and, therefore, we find ADSL describes “performing a data arrangement alteration algorithm” in the interleaved path. *See* Section II.D.2.b.i above. For the reasons discussed above with respect to similar limitations of claim 1, we find ADSL describes the “selectively performing” steps of claim 43 and also describes that the first and second error coding data blocks are “selectively created as a function of a control indicator.” *See* Section II.D.2.a above.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that

claim 43 of the '344 patent is unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

4. Dependent Claims 2 and 44

Claim 2 recites that “the first error coding path and the second error coding path are adapted to perform the same data arrangement alteration algorithm for the first and second error codings.” Claim 44 depends from claim 43 and similarly recites that “performing the first error coding and performing the second error coding comprise performing the same data arrangement alteration algorithm.”

Petitioner relies on the scrambler in each of ADSL’s two paths to show that the same data arrangement alteration algorithm is performed in both paths. Pet. 29–30, 45. As discussed above with respect to claim 1, however, Petitioner has not shown ADSL’s scrambler alters the *arrangement* of data, as required by claim 1. See Section II.D.2.b.ii above. Although ADSL’s interleaving operation describes data arrangement alteration, the interleaver is only in one of the two paths in ADSL.

Thus, Petitioner has not shown claims 2 and 44 are unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

5. Dependent Claims 4 and 45

Claim 4 depends from claim 1 and recites that “the first error coding path and the second error coding path are adapted to perform the same error coding algorithm for the first and second error codings.” Claim 45 depends from claim 43 and similarly recites that “performing the first error coding and the second error coding comprise performing the same error coding algorithm.”

Petitioner argues ADSL describes using the same CRC and FEC algorithms in both error coding paths. Pet. 30–31 (citing Ex. 1004, 32–33, 38–39, 219; Ex. 1003 ¶¶ 94–99). We are persuaded by Petitioner’s arguments and evidence. ADSL discloses an equation that is used for computing the cyclic redundancy checks in both the fast and the interleaved paths. Ex. 1004, 32. ADSL also discloses a formula for Reed-Solomon coding, which is the FEC algorithm described in ADSL, and ADSL shows FEC in both the fast and the interleaved paths. Ex. 1004, 11, 38–39.

Thus, we find ADSL describes the additional limitations of claims 4 and 45. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claims 4 and 45 of the ’344 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

6. Dependent Claim 8

Claim 8 recites,

The circuit as claimed in claim 1, wherein the data arrangement alteration device is adapted to create a second data block, comprising a given number of data in a second arrangement, on the basis of the first data block comprising the given number of data in a first arrangement, in accordance with a data arrangement alteration algorithm.

Petitioner argues “ADSL’s interleaver creates ‘output’ with a ‘given amount of data’ (5 Bytes) in a ‘second arrangement’ based on ‘input’ with the ‘given amount of data’ (5 Bytes) in a ‘first arrangement.’” Pet. 32 (citing Ex. 1004, 39; Ex. 1003 ¶¶ 100–104). Patent Owner argues that the output of the interleaver (the alleged “second data block”) will have a different number of data from the “first data block” because of the CRC and FEC codes that are added to the data before going to the interleaver. PO

Resp. 41–42. Patent Owner contends, therefore, that “the alleged first and second data blocks do not have the *same* given number of data.” PO Resp. 42 (emphasis added).

We disagree with Patent Owner’s interpretation of the claim language. As explained in our claim construction discussion, claim 8 uses the open-ended term “comprising,” which means that each data block may have data in addition to the “given number of data.” See Section II.B.2.b above. We agree with Petitioner that, “by using the term ‘comprising,’ the claim recites that the second data block includes but is not limited to a ‘given number of data in a second arrangement’ and the first data block includes but is not limited to ‘the given number of data in a first arrangement.’” Pet. Reply 26–27. Thus, the claim language encompasses first and second data blocks of different sizes, as “long as the second data block includes *at least* the given number of data and that given number of data is in a different arrangement from the first data block.” Pet. Reply 27.

As discussed with respect to claim 1, bytes B^j_0 through B^j_4 in ADSL’s Table 11 are in consecutive time slots in the input to the interleaver, but their arrangement in the output is changed with bytes B^j_1 through B^j_4 being moved to different time slots in the output according to ADSL’s interleaving formula. Ex. 1004, 39. Although the output of the interleaver may include additional data, there are still a “given number of data” from the first data block that end up in a different arrangement in a second data block.

Thus, we find ADSL describes the additional limitations of claim 8. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 8 of the

'344 patent is unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

7. Dependent Claims 9 and 48

Claim 9 depends from claim 1 and recites that “an input of the circuit is a parallel input which may receive several data at the same time.”

Claim 48 depends from claim 43 and recites that “receiving the first data block comprises receiving several data at the same time.”

Petitioner contends ADSL describes these limitations by disclosing that its ATU-C receives parallel inputs at the same time. Pet. 33–34 (citing Ex. 1004, 11, 16, 20; Ex. 1003 ¶¶ 111–112), 45 (citing Ex. 1004, 11, 25; Ex. 1003 ¶ 154). We are persuaded by Petitioner’s arguments and evidence. ADSL’s Figure 3 shows inputs ATM0 and ATM1, and ADSL describes a “dual latency mode, in which user data are allocated to both paths.” Ex. 1004, 11. ADSL also discloses that channel ATM0 is always provided and further discloses providing ATM1 “for support of dual latency mode.” Ex. 1004, 20. Based on this evidence and Dr. Tredennick’s testimony about the reception of multiple data inputs in parallel at the same time via ATM0 and ATM1, we find ADSL describes the limitations of claims 9 and 48. Ex. 1003 ¶¶ 111–112.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claims 9 and 48 of the '344 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

8. Dependent Claims 10, 11, 49, and 50

Claim 10 depends from claim 1 and recites that “an error coding device is adapted to perform an error detection or error correction algorithm

as an error coding algorithm.” Claim 49 depends from claim 43 and similarly recites that “the error coding algorithm is an error detection or an error correction algorithm.” Claim 11 depends from claim 1 and recites that “an error coding device is adapted to perform a cyclic redundancy code algorithm as an error coding algorithm.” Claim 50 depends from claim 43 and similarly recites that “the error coding algorithm is a cyclic redundancy code algorithm.”

As to claims 10 and 49, Petitioner contends that ADSL’s CRC and FEC devices describe devices that perform, respectively, error detection and error correction algorithms. Pet. 35 (citing Ex. 1004, 11, 25, 38, Fig. 3; Ex. 1003 ¶¶ 114–118), 45. As to claims 11 and 50, Petitioner relies on ADSL’s description of CRC devices in both fast and interleaved paths. Pet. 36 (citing Ex. 1004, 25, 32–33, 86–87; Ex. 1003 ¶¶ 119–123), 46.

We are persuaded by Petitioner’s arguments and evidence, and we find that ADSL’s disclosure of CRC (cyclic redundancy check) devices describes an error detection algorithm based on Dr. Tredennick’s testimony that CRC devices are used to detect CRC anomalies. Ex. 1003 ¶ 116; *see* Ex. 1004, 87 (describing CRC anomalies). We also find ADSL’s forward error correction (FEC) devices perform error correction. Ex. 1003 ¶ 116.

Thus, we find ADSL describes the additional limitations of claims 10, 11, 49, and 50. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claims 10, 11, 49, and 50 of the ’344 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

9. Dependent Claims 12 and 51

Claim 12 depends from claim 1 and recites that “the control indicator is dependent on an operating mode.” Claim 51 depends from claim 43 and similarly recites that “the value of the control indicator depends on an operating mode.”

Petitioner contends that ADSL describes choosing the fast and interleaved paths based on the mode of operation—that is, low latency mode or high latency/low error mode. Pet. 37 (citing Ex. 1004, 11, 25; Ex. 1003 ¶¶ 124–128). According to Petitioner, the fast path is used for low latency transmission whereas the interleaved path is used for transmissions that require a lower error rate but not low latency. Pet. 37. Thus, Petitioner argues that the Virtual Path Identifier (VPI) and Virtual Connection Identifier (VCI), which describe the control indicator as discussed above for claim 1, depend on the particular operating mode. Pet. 37.

We are persuaded by Petitioner’s arguments and evidence. ADSL discloses that “the ‘fast’ path provides low latency” and that “the interleaved path provides very low error rate and greater latency.” Ex. 1004, 11. ADSL further discloses that “[t]he ATM Layer performs cell multiplexing from and demultiplexing to the appropriate physical port (i.e. latency path - fast or interleaved) based on the Virtual Path Identifier (VPI) and Virtual Connection Identifier (VCI), both contained in the ATM cell header.” Ex. 1004, 220. Thus, the value of the Virtual Path Identifier (VPI) and Virtual Connection Identifier (VCI) depends on the operating mode—low latency mode or high latency/low error mode.

Therefore, we find ADSL describes the additional limitations of claims 12 and 51. Having considered the full record developed during trial,

we determine that Petitioner has proven by a preponderance of the evidence that claims 12 and 51 of the '344 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by ADSL.

10. Claims 19, 20, 22, and 26–30

Independent claim 19 recites several means-plus-function limitations. As to the “means for selectively performing a first error coding so as to create a first error coding data block,” we identified the corresponding structure as “first error coding path 120 and equivalents.” *See* Section II.B.2 above; Dec. on Inst. 8 (setting forth same construction). As to the “means for performing a data arrangement alteration algorithm,” we identified the corresponding structure as “data arrangement alteration devices 122, 132, and 222 and equivalents.” *See* Section II.B.2 above; Dec. on Inst. 9 (setting forth same construction). During the trial, Petitioner did not dispute these constructions. *See* Pet. Reply 21 (arguing that “[t]he Board properly identified the corresponding structure of the claimed ‘means for selectively performing a first error coding’ . . . as ‘first error coding path 120 and equivalents’”).

For the “means for selectively performing a first error coding so as to create a first error coding data block,” Petitioner’s contentions are as follows:

Interleaved path of the ATU-C includes CRC and FEC error coders, each of which creates a first error coding data block. ADSL’s CRC and FEC error coders include the same structure as the “one or more devices, including a first error coder” described in the '344 patent as set forth in Section IV [of the Petition].

Pet. 38 (citing Pet. § V.A.[1.1]; Ex. 1003 ¶ 131).

Claim 19 further recites “at least the first means for performing the first error coding comprising a means for performing a data arrangement alteration algorithm.” Petitioner’s contentions as to this limitation are as follows:

The one or more devices in ADSL’s paths each include “means for performing a data arrangement alteration algorithm” through ADSL’s scrambler and interleaver in interleaved path, and ADSL’s scrambler in fast path. Each of ADSL’s scrambler and interleaver include the same structure as the “data arrangement alteration device” described in the ’344 patent as set forth in Section IV [of the Petition].

Pet. 39 (citing Pet. § V.A.[1.4]; Ex. 1003 ¶ 134).

Patent Owner argues that, in the specification of the ’344 patent, the data arrangement alteration device is located in front of, and outputs data to, the error coder. PO Resp. 18. According to Patent Owner, therefore, the corresponding structure for the “means for selectively performing a first error coding so as to create a first error coding data block” “is one in which, when an error coding path includes a data arrangement alteration device, that data arrangement alteration device outputs a data block to an error coder.”

PO Resp. 19. Patent Owner argues that

the interleaver in ADSL does not output a data block to an error coder. In contrast, the interleaver receives data from a Reed-Solomon encoder. As a result, the interleaver cannot be a “means for performing a data arrangement alteration algorithm” that is included in the “means for selectively performing a first error coding so as to create a first error coding data block.”

PO Resp. 34.

We agree with Patent Owner that, in first error coding path 120, which we identified as the corresponding structure for “means for selectively performing a first error coding so as to create a first error coding data

block,” the data arrangement alteration device is always located in front of the error coder and outputs data to the error coder. Ex. 1001, 3:27–34, 3:57–4:3, 5:53–64, Figs. 1A, 1E. Petitioner relies on ADSL’s scrambler and interleaver as describing the “means for performing a data arrangement alteration algorithm.” Pet. 39. For the reasons discussed for claim 1, Petitioner has not established that ADSL’s scrambler is a data arrangement alteration device as described in the ’344 patent and, therefore, has not shown that ADSL’s scrambler describes the structure of data arrangement alteration devices 122, 132, and 222.

We also agree with Patent Owner that ADSL’s interleaver is located after the error coders in ADSL. Ex. 1004, 11, Fig. 3. ADSL’s interleaver does not output data to the error coder but, rather, receives data after the error coders have operated on the data. Ex. 1004, 11, Fig. 3. Thus, Petitioner has not shown that ADSL’s interleaved path describes the same structure as first error coding path 120 in the ’344 patent.

We also consider whether Petitioner has shown ADSL’s interleaved path to be a structural equivalent to first error coding path 120. “Structural equivalence under § 112, ¶ 6 is met only if . . . the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification.” *Odetics, Inc. v. Storage Tech. Corp.*, 185 F.3d 1259, 1267 (Fed. Cir. 1999) (citations omitted). Petitioner does not provide argument or evidence demonstrating that ADSL’s interleaved path, which performs data arrangement alteration after error coding, performs the claimed function in substantially the same way to achieve substantially the same result as first error coding path 120. Thus, Petitioner has not shown

that ADSL's interleaved path describes structure equivalent to first error coding path 120 in the '344 patent. Petitioner, therefore, has not proven, by a preponderance of the evidence, that ADSL anticipated claim 19.

Claims 20, 22, and 26–30 incorporate the “means for selectively performing a first error coding so as to create a first error coding data block” limitation of independent claim 19, and, therefore, Petitioner has not proven, by a preponderance of the evidence, that ADSL anticipated these claims.

*E. Obviousness over ADSL and Voith
(Claims 16 and 18)*

Petitioner contends claims 16 and 18 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combined teachings of ADSL and Voith. Pet. 1, 9–10, 46–58.

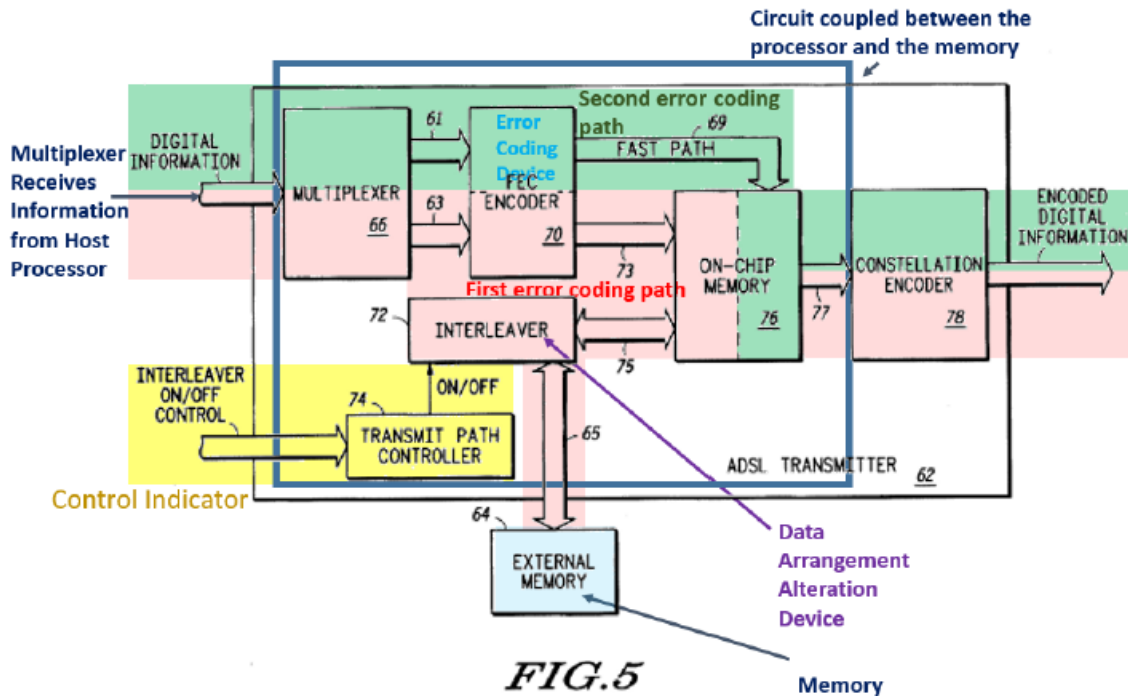
1. Claim 16

Claim 16 is an independent claim directed to a “system” having “a processor,” “a memory,” and “a circuit coupled between the processor and the memory, the circuit for creating an error coding data block for a first data block, the circuit comprising” the first and second error coding paths as recited in claim 1.⁶ Petitioner argues “ADSL's ATU-C performs read operations where it reads out data from a memory in the ATU-R transceiver,” but, according to Petitioner, ADSL “does not explicitly disclose a processor connected to a memory via the ATU-C.” Pet. 46–47 (citing Ex. 1004, vi; Ex. 1003 ¶ 161). Petitioner relies on Voith's “host processor” and “external memory” to teach, respectively, the claimed

⁶ Claim 16 recites “the first error coding path and *the second data path* being selected as a function of a control indicator.” (Emphasis added). Claim 16 does not previously introduce “a second data path,” and, therefore, we understand “the second data path” to refer to “a second error coding path.”

“processor” and “memory.” Pet. 49–51 (citing Ex. 1006, 4:53–59, 4:67–5:1, 5:6–19, 6:12–18, 7:43–67, Fig. 5; Ex. 1003 ¶¶ 170–182).

With its obviousness analysis, Petitioner provides an annotated version of Figure 5 from Voith, which is reproduced below.



Pet. 51. In this annotated version of Figure 5 from Voith, Petitioner identifies the components that it contends disclose a “host processor,” a “memory,” and a “circuit coupled between the processor and the memory.” Pet. 51. Voith discloses that “ADSL transmitter 62 receives digital information, for example from a host processor.” Ex. 1006, 5:6–7. Voith further discloses that “[o]n-chip memory 76 is bi-directionally coupled to interleaver 72 via a bus 75, which in turn is bi-directionally coupled to external memory 64 via a bus 65.” *Id.* at 4:65–5:1.

Petitioner argues that “it would have been obvious to [a person of ordinary skill in the art] to use a processor in ADSL’s system to provide data to an ATU-C transmitter because processors are ubiquitous components in

digital devices, including ones that transmit or receive data” and that a person of ordinary skill in the art “would have understood that ADSL’s ATU-C receives data from a communicating device and would have found it obvious that the communicating device includes a processor, as disclosed by Voith.” Pet. 50 (citing, *inter alia*, Ex. 1003 ¶ 172; Ex. 1004, vi, 4–5, 11, 16–39, 220–221; Ex. 1006, 5:6–19). Petitioner further argues a person of ordinary skill in the art “would have been motivated by Voith to use Voith’s memory in ADSL to avoid delays caused by prior art ADSL interleaving.” Pet. 52 (citing Ex. 1006, 3:11–22, 3:59–4:14; Ex. 1003 ¶ 181). Petitioner also argues that, based on Voith’s disclosed circuit configuration, a person of ordinary skill in the art “would have found it obvious to arrange ADSL’s transceiver between the processor and memory of Voith.” Pet. 53 (citing Ex. 1006, 5:6–19, Fig. 5; Ex. 1003 ¶¶ 183–184).

Patent Owner, citing the testimony of its declarant, Dr. Przybylski, argues that external memory 64 is part of the interleaver because it is used by the interleaver. PO Resp. 46–47 (citing Ex. 2002 ¶¶ 89–91). Thus, according to Patent Owner, external memory 64 “is not a separate memory coupled to a circuit including the ADSL interleaver.” PO Resp. 47.

Dr. Przybylski testifies as follows:

Voith makes clear that the external memory 64 is used to temporarily store data that is in the process of being interleaved. Ex 1006 at 5:62-6:25. The external memory is not the final destination of the encoded data. In that sense the ADSL transmitter 62 is not a circuit for encoding data between a processor and a memory, but rather the external memory 64 is an integral part of the circuit as a whole. Without that memory, the circuit could not operate to interleave the data as required of it.

Ex. 2002 ¶ 89.

Although Voith discloses that external memory 64 is used by the interleaver, we do not agree with Patent Owner's argument and Dr. Przybylski's analysis. Voith discloses that memory for the interleaver "can be provided on-chip, but the silicon area needed is somewhat extensive." Ex. 1006, 6:9–11. Because of that drawback of on-chip memory, Voith discloses that, "in a preferred embodiment, interleaver memory is provided as an external memory 64." Ex. 1006, 6:12–14. Thus, Voith expressly describes memory 64 as external and distinguishes it from memory internal to the chip ("on-chip"). As to Dr. Przybylski's statement that Voith's "external memory is not the final destination of the encoded data" (Ex. 2002 ¶ 89), this is not a requirement of claim 16. Claim 16 requires a circuit coupled between a processor and a memory. It does not require the memory to be the final destination for the encoded data.

We find Voith's host processor teaches "a processor," as recited in claim 16. *See* Ex. 1006, 5:6–7 ("ADSL transmitter 62 receives digital information, for example from a host processor . . ."). We also find Voith's external memory 64 teaches "a memory," as recited in claim 16. For the reasons explained for claim 1, we find ADSL teaches a "circuit for creating an error coding data block for a first data block, the circuit comprising" the first and second error coding paths as recited in claim 1. We find Voith discloses ADSL transmitter 62 coupled between Voith's host processor and external memory 64. *See* Ex. 1006, Fig 5. We also are persuaded that, based on Voith's disclosed circuit configuration, a person of ordinary skill in the art "would have found it obvious to arrange ADSL's transceiver between the processor and memory of Voith." Pet. 53 (citing Ex. 1006, 5:6–19, Fig. 5; Ex. 1003 ¶¶ 183–184). We find Petitioner's reasons for combining

the references, discussed above, to be articulated reasoning with rational underpinning.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 16 of the '344 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of ADSL and Voith.

2. Claim 18

Claim 18 recites,

The system as claimed in claim 16, wherein the circuit is adapted to read out the information of the first data block along with the error coding data block in a reading operation; and to perform, by means of the error coding data block, an error detection or error correction for read-out information of the first data block.

Petitioner asserts Voith discloses a circuit reading out codewords, which include basic data and redundancy bytes, from the external memory in a reading operation. Pet. 55 (citing Ex. 1006, 5:20–49, 8:31–9:39; Ex. 1003 ¶¶ 194–197). Petitioner further contends Voith discloses performing error correction or detection on received data at the customer end. Pet. 57 (citing Ex. 1006, 6:26–36; Ex. 1003 ¶¶ 198–204). Petitioner contends that a person of ordinary skill in the art “would have found it obvious to use Voith’s error coding data block to perform an error detection/correction for read-out information of the first data block, because it was well-known in the prior art to use error coding blocks to detect and/or correct errors in conjunction with a transmission.” Pet. 58 (citing Ex. 1003 ¶¶ 202–203; Ex. 1011 ¶¶ 8–10, 46–48, 98–99; Ex. 1013, 4:20–5:10, 10:1–44; Ex. 1017, xiii–xvi, 12–13, 257–282; Ex. 1018, 189–201). According to Petitioner,

the purpose of the ADSL/Voith CRC/FEC error coding data blocks is to perform error detection/correction, so a [person of ordinary skill in the art] would have found it straightforward and routine to use the ADSL/Voith CRC/FEC error coding data blocks to perform error detection/correction for information read-out of Voith's memory.

Pet. 58.

We are persuaded by Petitioner's arguments and evidence. Voith discloses that, "[i]n forward error correction encoding, redundant bytes of information are added to the basic data bytes to form a codeword." Ex. 1006, 5:32–34. We agree with Petitioner that redundant bytes of information added by FEC encoding teach an "error coding data block." Voith also discloses reading out codewords during the interleaving process. Ex. 1006, 10:28–36.⁷ Thus, we find Voith teaches a circuit that "is adapted to read out the information of the first data block along with the error coding data block in a reading operation." We also agree with Petitioner that the purpose of error coding, such as FEC encoding, is to perform error detection and correction. Ex. 1003 ¶¶ 202–203. Indeed, Voith discloses that the addition of "redundant bytes" using a forward error correction technique "allows a degree of error detection and correction at the receiving end of the communication system." Ex. 1006, 2:2–9. Therefore, we find the combination of ADSL and Voith teaches a circuit adapted "to perform, by means of the error coding data block, an error detection or error correction for read-out information of the first data block."

⁷ By use of the short form citation "*Id.*," Petitioner mistakenly cites a different passage of Voith for the material quoted in the Petition. Pet. 55–56. The quoted material appears in Voith at column 10, lines 28–36.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 18 of the '344 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of ADSL and Voith.

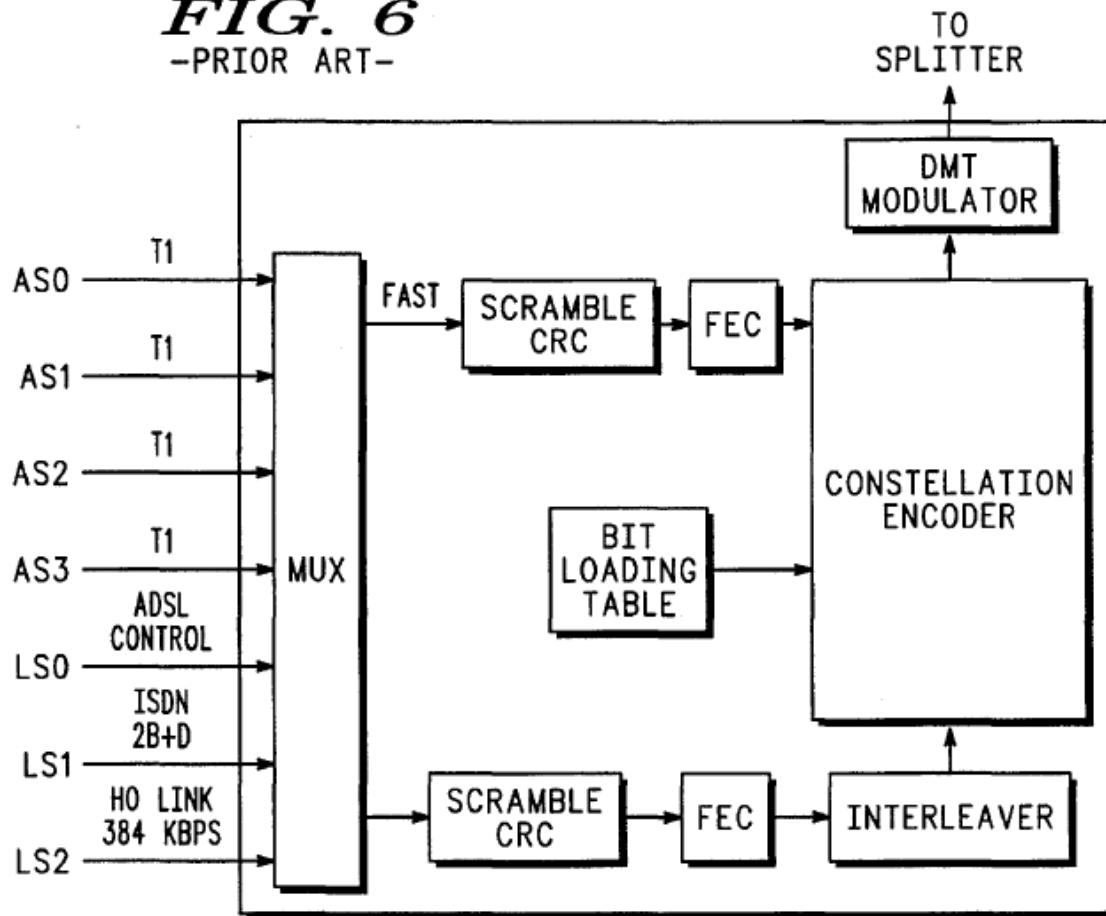
F. Obviousness over Grube
(Claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51)

Petitioner contends claims 1, 2, 4, 8–12, 16, 18–20, 22, 26–30, 43–45, and 48–51 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the teachings of Grube. Pet. 2, 11–12, 59–95.

1. Grube

Grube relates to a communication system infrastructure, and it describes a configuration of an ADSL transmitter in Figure 6, reproduced below. Ex. 1005, 1:8–10, 4:43–44.

FIG. 6
-PRIOR ART-

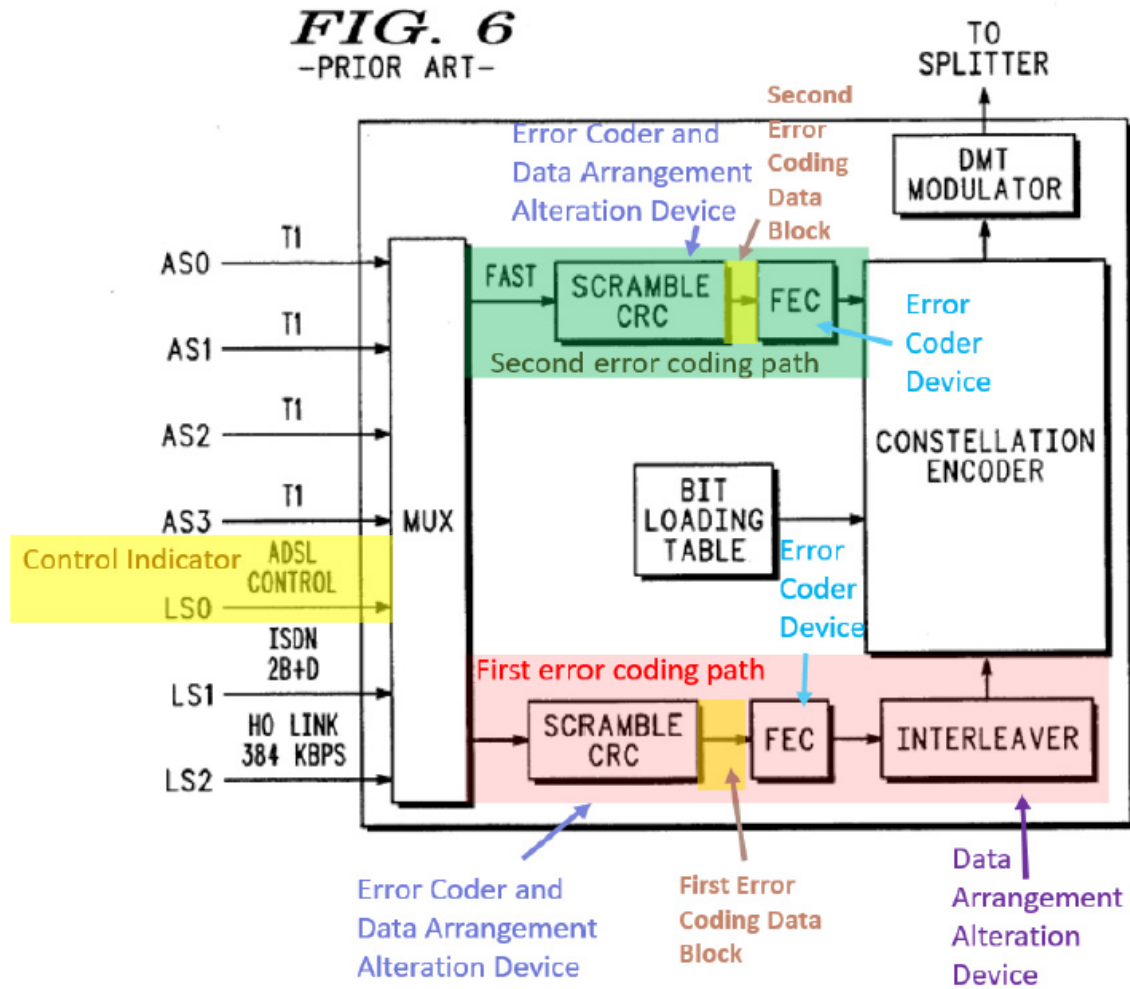


Grube's Figure 6 illustrates the transmit portion of an ADSL transceiver, and it depicts a fast path and an interleave path. Ex. 1005, 3:57-4:3.

2. Claim 1

a. First and second error coding paths

With its obviousness analysis, Petitioner provides an annotated version of Grube's Figure 6, which is reproduced below.



In this annotated version of Figure 6 from Grube, Petitioner identifies components that it contends disclose various components of the circuit of claim 1. Pet. 61. Grube discloses:

FIG. 6 illustrates the transmit portion of the ADSL transceiver. As shown, the ADSL transmitter includes a multiplexer which receives a plurality of inputs via TI links, ADSL control, an ISDN connection, and an HO link. Based on the ADSL control, the multiplexer provides one of the inputs to a constellation encoder via a fast path or an interleave path. The fast path includes a scramble cyclic redundancy check (CRC) block which is coupled to a forward error correction (FEC) block. The interleave path includes a scramble CRC, a forward error correction block, and an interleave block. The path selected

depends on the level of burst error correction needed. If less error correction is needed, the fast path is selected, otherwise the interleave path is selected.

Ex. 1005, 3:57–4:3.

Petitioner identifies the “interleave path” of Grube’s Figure 6 as the claimed “first error coding path” and the “fast path” as the claimed “second error coding path.” Pet. 60–64. Petitioner contends that the CRC and FEC blocks in Grube’s Figure 6 are error coding devices. *Id.* at 61–63. Petitioner acknowledges that “Grube lacks details on the error coding performed and fails to disclose that the error coding devices generate an ‘error coding data block,’” and, relying on the testimony of Dr. Tredennick, Petitioner argues that “ADSL CRC algorithms were well-known to generate a cyclic redundancy check code and ADSL FEC algorithms were well-known to generate a forward error correction code.” *Id.* at 61–62 (citing, *inter alia*, Ex. 1003 ¶ 213). Petitioner contends, therefore, that a person of ordinary skill in the art “would have found it obvious that Grube’s ‘scramble CRC’ generates CRC code using CRC algorithm and Grube’s FEC generates FEC code using FEC algorithm.” *Id.* at 62, 63 (citing Ex. 1005, 3:57–4:3; Ex. 1003 ¶¶ 213, 217). According to Petitioner, either the CRC code or the FEC code teaches an “error coding data block.” *Id.* at 62, 63. Petitioner contends the fast and interleave paths are selected based on the ADSL control depicted in Figure 6. *Id.* at 64–65 (citing Ex. 1005, 3:57–4:3). Petitioner, therefore, contends Grube’s ADSL control teaches the claimed “control indicator.” Pet. 64–65.

Although Patent Owner does not provide specific arguments regarding these particular limitations of claim 1, the burden remains on Petitioner to

demonstrate unpatentability. For the reasons explained below, we are persuaded by Petitioner's arguments and evidence.

Dr. Tredennick testifies that CRC codes and FEC codes, which are generated by CRC and FEC devices, respectively, teach error coding data blocks. Ex. 1003 ¶¶ 213, 217. Based on this testimony and Grube's disclosure of cyclic redundancy check (CRC) and forward error correction (FEC) devices in each path, we find Grube teaches "a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding" and "a second error coding path adapted to selectively create a second error coding data block in accordance with a second error coding."

Figure 6 depicts an input labeled "ADSL control," and Grube explains that, "[b]ased on the ADSL control, the multiplexer provides one of the inputs to a constellation encoder via a fast path or an interleave path." Ex. 1005, 3:60–63. Thus, Grube teaches that "the first error coding path and the second error coding path [are] selected as a function of a control indicator," specifically "ADSL control."

b. Data arrangement alteration

Petitioner further argues, citing the testimony of Dr. Tredennick, that the "Scramble CRC" device in each path and the "Interleaver" device in the Interleave path are data arrangement alteration devices. Pet. 65–66 (citing, *inter alia*, Ex. 1003 ¶¶ 222–226). As to the scrambler, Petitioner argues that, "although Grube lacks details on the scrambling performed by its 'Scramble CRC,' ADSL scramble algorithms were well-known to scramble (i.e., re-order/re-arrange) bits of data in a data block." Pet. 65 (citing Ex. 1003 ¶ 223; Ex. 1004, 25, 37–38; Ex. 1012 ¶ 27; Ex. 1013, 4:61–5:6, 10:23–38,

13:59–14:2; Ex. 1018, 149–151, 518–521). Petitioner and its declarant, Dr. Tredennick, do not provide an explanation for any of the cited references, with the exception of the ADSL scrambler, which is discussed in the ADSL anticipation ground. As discussed above in our analysis of the ADSL anticipation ground, we are not persuaded ADSL’s scrambler describes a “data arrangement alteration device.” Because Petitioner has not provided any further explanation as to how scrambling is performed in the cited references, we are not persuaded by Petitioner’s contention that Grube’s disclosure of a scramble CRC device teaches a “data arrangement alteration device.”

Grube, however, also discloses an “interleaver” in the interleaved path. Ex. 1005, 3:57–4:3, Fig. 6. Petitioner contends that “Grube similarly lacks details on its ‘interleaver’” but argues that “ADSL interleaving was well-known to interleave (i.e., re-order/re-arrange) bits of data in a data block.” Pet. 65–66 (citing, *inter alia*, Ex. 1003 ¶ 224; Ex. 1004, 11, 25, 39–40). According to Petitioner, “[b]y changing the arrangement of the data through interleaving, a [person of ordinary skill in the art] would have found it obvious that Grube’s ‘interleaver’ performs ‘data arrangement alteration.’” Pet. 66. Patent Owner refers to its arguments with respect to ADSL and argues that ADSL’s interleaver teachings do not support Petitioner’s contention that Grube’s interleaver alters the arrangement of a data block. PO Resp. 49 (citing PO Resp. §§ VI.A.1 and VII).

As discussed above in the ADSL anticipation ground, we disagree with Patent Owner’s contention that ADSL’s interleaving operation does not describe data arrangement alteration. See Section II.D.2.b.i above. Grube discloses that the transceiver depicted in Figure 6 is an “ADSL transceiver.”

Ex. 1005, 3:57–58, 4:43–44. Thus, we agree with Petitioner that a person of ordinary skill in the art would have understood that Grube’s disclosure of an ADSL interleaver teaches a device that alters the arrangement of data, consistent with the disclosure of interleaving in ADSL. Ex. 1003 ¶ 224 (citing, *inter alia*, Ex. 1004, 11, 25, 39–40). We find, therefore, that Grube’s disclosure of an ADSL interleaver in the interleave path teaches “at least the first error coding path comprising a data arrangement alteration device.”

c. Determination of unpatentability of claim 1

Although Petitioner has not shown Grube’s scrambler teaches a “data arrangement alteration device,” Petitioner has shown Grube’s interleaver teaches this subject matter. As discussed above, we find Grube teaches all of the limitations of claim 1. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 1 of the ’344 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

3. Independent Claim 43

Independent claim 43 is directed to “[a] method of creating an error coding data block for a first data block” and recites “receiving the first data block” before reciting method steps that correspond to the limitations of claim 1. Petitioner contends Grube’s ADSL transceiver receives the first data block. Pet. 92 (citing Ex. 1005, 3:57–4:3; Ex. 1003 ¶ 299). For the remaining limitations of claim 43, Petitioner refers to its analysis of the limitations of claim 1 reciting similar subject matter. Pet. 92–94.

Patent Owner relies on the same arguments for claim 43 that it raises for claim 1, namely that Grube does not teach data arrangement alteration.

PO Resp. 48–50. Nonetheless, the burden remains on Petitioner to prove unpatentability.

We are persuaded by Petitioner’s contentions that Grube teaches the subject matter of claim 43. We find Grube teaches “receiving the first data block” based on Grube’s disclosure that “the ADSL transmitter includes a multiplexer which receives a plurality of inputs via TI links, ADSL control, an ISDN connection, and an HO link.” Ex. 1005, 3:58–60; Fig. 6. Claim 43 recites “at least the step of selectively performing the first error coding comprises the step of performing a data arrangement alteration algorithm.” As discussed above with respect to claim 1, we find Grube discloses an interleaver that alters the arrangement of data, and, therefore, we find Grube teaches “performing a data arrangement alteration algorithm” in the interleaved path. *See* Section II.F.2.b above. For the reasons discussed above with respect to similar limitations of claim 1, we find Grube teaches the “selectively performing” steps of claim 43 and also describes that the first and second error coding data blocks are “selectively created as a function of a control indicator.” *See* Section II.F.2.a above.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 43 of the ’344 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

4. Dependent Claims 2 and 44

These claims require the same data arrangement alteration to be performed for the first and second error codings. Petitioner relies on the scramble CRC device in each of Grube’s two paths to show that the same data arrangement alteration algorithm is performed in both paths. Pet. 66–

69, 94. As discussed above with respect to claim 1, Petitioner has not shown Grube's scramble CRC device alters the *arrangement* of data, as required by claim 1. *See* Section II.F.2.b above. Although Grube's interleaver teaches a data arrangement alteration device, the interleaver is only in one of the two paths in Grube.

Thus, Petitioner has not shown claims 2 and 44 are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

5. Dependent Claims 4 and 45

These claims require the same error coding algorithm to be performed for the first and second error codings. Petitioner argues a person of ordinary skill in the art would have found using the same CRC and FEC algorithms in both paths to be obvious. Pet. 69–71 (citing Ex. 1005, 3:57–4:3; Ex. 1003 ¶¶ 234–241). Petitioner contends that a person of ordinary skill in the art “would have selected the same CRC and FEC algorithms because doing so would simplify the design and allow for reuse of the same type of CRC and FEC devices in each path.” Pet. 70 (citing Ex. 1003 ¶ 239; Ex. 1015, 786; Ex. 1011 ¶ 42). We are persuaded by Petitioner's contentions, as supported by the testimony of Dr. Tredennick. Ex. 1003 ¶¶ 238–240. For example, Dr. Tredennick testifies that “[u]sing the same type of circuit device ‘simplify[ies] the manufacturing process.’” Ex. 1003 ¶ 239 (alteration in original) (quoting Ex. 1015, 786). We credit Dr. Tredennick's testimony, and we find that a person of ordinary skill in the art would have been motivated to use the same CRC and FEC devices in both paths. Ex. 1003 ¶¶ 238–240.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that

claims 4 and 45 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

6. *Dependent Claim 8*

Claim 8 recites,

The circuit as claimed in claim 1, wherein the data arrangement alteration device is adapted to create a second data block, comprising a given number of data in a second arrangement, on the basis of the first data block comprising the given number of data in a first arrangement, in accordance with a data arrangement alteration algorithm.

Petitioner argues the subject matter of claim 8 would have been obvious based on Grube's disclosure of interleaving. Pet. 72 (citing, *inter alia*, Ex. 1003 ¶ 246; Ex. 1004, 11, 25, 39–40). Patent Owner argues ADSL's interleaving "do[es] not disclose that a second data block created on the basis of a first data block would have the same given number of data," and, therefore, Patent Owner argues that Petitioner's contentions as to Grube, which cite to ADSL's interleaver disclosures, are insufficient. PO Resp. 53.

As discussed above, we disagree with Patent Owner's interpretation that claim 8 requires the same number of data in the first and second data blocks. See Section II.B.2.b above. Rather, the claim language encompasses first and second data blocks of different sizes in which the second data block includes at least "the given number of data" and that given number of data is in a different arrangement from the first data block.

As discussed with respect to claim 1, Grube's disclosure of an ADSL interleaver teaches a device that alters the arrangement of data, consistent with the disclosure of interleaving in ADSL. Dr. Tredennick cites ADSL's disclosure of interleaving and testifies,

With this type of interleaving, a [person of ordinary skill in the art] would have found it obvious that the second data block comprises the given number of data in a second arrangement, with the second data block being created “on the basis of the first data block comprising the given number of data in a first arrangement.”

Ex. 1003 ¶ 246 (citing, *inter alia*, Ex. 1004, 11, 25, 39–40). We credit Dr. Tredennick’s testimony because, as discussed in the ADSL anticipation ground, although the output of the interleaver may include additional data, there are still a “given number of data” from the first data block that end up in a different arrangement in a second data block. As discussed above, Grube discloses that the transceiver depicted in Figure 6 is an “ADSL transceiver” (Ex. 1005, 3:57–58, 4:43–44), and, thus, Grube discloses an ADSL interleaver. We are persuaded, therefore, that a person of ordinary skill in the art would have found the subject matter of claim 8 obvious based on the teachings of Grube.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 8 of the ’344 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

7. *Dependent Claims 9 and 48*

Claim 9 depends from claim 1 and recites that “an input of the circuit is a parallel input which may receive several data at the same time.”

Claim 48 depends from claim 43 and recites that “receiving the first data block comprises receiving several data at the same time.” Petitioner argues that a person of ordinary skill in the art would have understood inputs AS0–AS3 in Grube’s Figure 6 are parallel inputs that are received by the multiplexer at the same time. Pet. 73–74 (citing Ex. 1005, 3:57–4:3, Fig. 6;

Ex. 1003 ¶¶ 248–250). Dr. Tredennick provides similar testimony in support of Petitioner’s contention. Ex. 1003 ¶¶ 248–250.

We are persuaded by Petitioner’s arguments and evidence. Based on Grube’s depiction of parallel inputs in Figure 6 and based on the testimony of Dr. Tredennick, we find a person of ordinary skill in the art would have understood Grube as teaching parallel input through which data in a data block are received at the same time.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claims 9 and 48 of the ’344 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

8. Dependent Claims 10, 11, 49, and 50

Claims 10 and 49 recite an error detection or error correction algorithm as the error coding algorithm. Claims 11 and 50 recite that the error coding algorithm is a cyclic redundancy code algorithm. Petitioner cites Grube’s disclosure of “cyclic redundancy check (CRC) block” and “forward error correction (FEC) block” and, relying on the testimony of Dr. Tredennick, argues that CRC and FEC are error detection and error correction algorithms, respectively. Pet. 74 (citing Ex. 1005, 3:57–4:3; Ex. 1003 ¶¶ 251–254), 95. Petitioner also argues that Grube’s CRC block performs a cyclic redundancy code algorithm. Pet. 74–75 (citing Ex. 1005, 3:57–4:3; Ex. 1003 ¶¶ 255–258), 95.

We are persuaded by Petitioner’s arguments and evidence, and we find Grube’s CRC and FEC blocks teach error detection and error correction algorithms, respectively. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of

the evidence that claims 10, 11, 49, and 50 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

9. Dependent Claims 12 and 51

As to these claims' recitation that the control indicator depends on an operating mode, Petitioner cites Grube's disclosure that the selection between the fast and the interleave path "depends on the level of burst error correction needed." Ex. 1005, 3:67–4:1, *cited in* Pet. 75. Grube explains that, "[i]f less error correction is needed, the fast path is selected, otherwise the interleave path is selected." Ex. 1005, 4:1–3, *cited in* Pet. 75. Thus, Petitioner argues that ADSL control, which teaches the "control indicator," depends on the error correction mode needed. Pet. 75.

We are persuaded by Petitioner's arguments and evidence, and we find Grube teaches ADSL control depends on the error correction mode. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claims 12 and 51 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

10. Independent Claim 16

Claim 16 is an independent claim directed to a "system" having "a processor," "a memory," and "a circuit coupled between the processor and the memory, the circuit for creating an error coding data block for a first data block, the circuit comprising" the first and second error coding paths as recited in claim 1. Petitioner argues that Grube teaches a "system" in Figure 8, an annotated version of which is reproduced below.

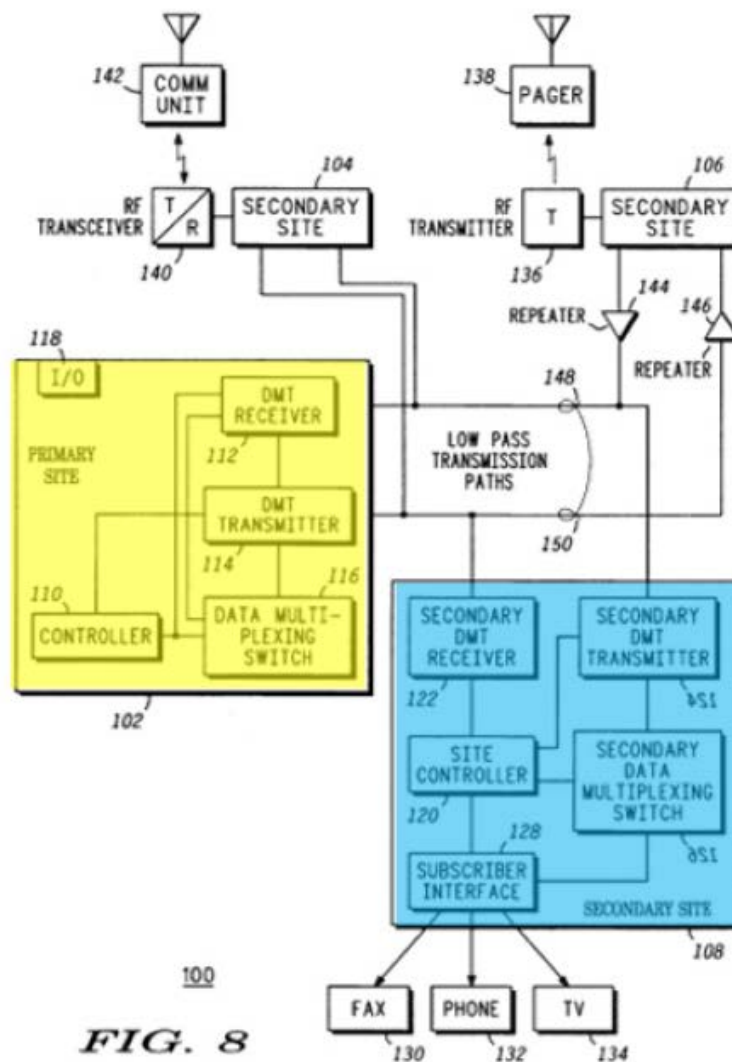


FIG. 8

Pet. 76. In this annotated version of Grube's Figure 8, Petitioner identifies in yellow primary site 102 and in blue secondary site 108. Pet. 75–76. Petitioner argues primary site 102's processor 172 teaches “a processor.” Pet. 76–77 (citing Ex. 1005, 9:62–10:6, Fig. 10; Ex. 1003 ¶ 264). Petitioner further argues memory 190 at secondary site 108 teaches “a memory.” Pet. 77–79 (citing Ex. 1005, 12:23–41, Fig. 11; Ex. 1003 ¶¶ 265–266).

As to claim 16's recitation of the circuit comprising the first and second error coding paths as recited in claim 1, Petitioner relies on DMT transmitters in primary site 102 and secondary site 108 and refers to its

contentions for claim 1. Pet. 82–84 (citing Ex. 1005, 3:57–4:3, 8:16–37, 9:62–13:45, 39:25–30, 40:19–22, 43:41–44:35, 45:54–56, 46:45–47:5, Figs. 8, 10, 11, 36, 42; Ex. 1003 ¶¶ 207–209, 270–276). Citing Grube’s disclosure that “[t]he present invention contemplates using the ADSL system techniques” (Ex. 1005, 39:26–28), Petitioner argues that a person of ordinary skill in the art “would have found it obvious to use the ADSL transmitter shown in Grube’s FIG. 6 for DMT transmitters.” Pet. 82–83 (citing Ex. 1005, 8:16–37, 9:62–13:45, 39:25–30, 40:19–22, 43:41–44:35, 45:54–56, 46:45–47:5, Figs. 8, 10, 11, 36, 42; Ex. 1003 ¶¶ 270–271).

As to claim 16’s recitation that the circuit is “coupled between the processor and the memory,” Petitioner argues that processor 172 in primary site 102 is connected to memory 190 in secondary site 108 via a path that includes data bus 176, data multiplexing switch 116, and DMT transmitter 114 at primary site 102 connected to DMT receiver 122 at secondary site 108 via outbound twisted pair 150, as shown in Figures 10 and 11. Pet 79–81 (citing Ex. 1005, 9:62–13:46, Figs. 10, 11; Ex. 1003 ¶¶ 267–269).

Patent Owner argues that the elements identified by Petitioner between processor 172 in primary site 102 and memory 190 in secondary site 108 would not have been considered a circuit by a person of ordinary skill in the art. PO Resp. 53–54 (citing Ex. 2002 ¶¶ 94–95). Dr. Przybylski testifies as follows:

As the primary and secondary sites [of Grube] are described as being physically and logically separate from each other, a person of ordinary skill would not consider individual portions of each to be part of a single “circuit” without some unifying aspect to motivate such a conceptualization. None exists in this case.

Ex. 2002 ¶ 95. Patent Owner argues that, “even if a DMT transmitter 114 of Grube has the elements of ADSL technology, that DMT transmitter 114 is not in a circuit coupled between the alleged processor and memory as recited in claim 16.” PO Resp. 54.

Dr. Przybylski testifies that there must be “some unifying aspect to motivate such a conceptualization” of physically separate components being part of the same “circuit.” Ex. 2002 ¶ 95. Dr. Tredennick explains how the components in Grube communicate with each other to thereby make a circuit. Ex. 1003 ¶¶ 267–269. Petitioner is not merely alleging that “individual portions” of primary site 102 and secondary site 108 form a circuit, as suggested by Dr. Przybylski. *See* Ex. 2002 ¶ 95. Rather, Petitioner identifies the paths by which primary site 102 and secondary site 108 communicate, including the components in those paths. *See* Pet. 79–81. Referring to Figure 8, Grube discloses that “communication system 100 includes a primary site 102, a plurality of secondary sites 104–108 *interoperably coupled to the primary site via* at least one inbound low pass transmission pass 148 and *at least one outbound low pass transmission path 150.*” Ex. 1005, 8:17–21 (emphases added). Petitioner identifies path 150 in Figures 10 and 11 as connecting DMT transmitter 114 in primary site 102 and DMT receiver 122 in secondary site 108. Pet. 80–81 (citing Ex. 1005, 12:23–13:46, Figs. 10, 11). Grube discloses that DMT transmitter 114 in primary site 102 “transmits the data in the carrier channels of the outbound low pass transmission path 150.” Ex. 1005, 11:42–45. Grube discloses that, at secondary site 108, “DMT receiver 122 receives information from an outbound twisted pair 150 and either places that information within the memory 190 or places it on the data bus 196.”

Ex. 1005, 12:33–36. Thus, Grube’s disclosure of a communication connection between primary site 102 and secondary site 108 describes a “unifying aspect” (Ex. 2002 ¶ 95) by which the paths identified by Petitioner form a “circuit.” Thus, we agree with Petitioner that identified components form a circuit. *See* Pet. 79–81.

We are persuaded that Grube’s processor 172 and memory 190 teach, respectively, “a processor” and “a memory,” as recited in claim 16. Based on Grube’s disclosure that “[t]he present invention contemplates using the ADSL system techniques” (Ex. 1005, 39:26–28) and based on Dr. Tredennick’s testimony (Ex. 1003 ¶ 271), we are persuaded that a person of ordinary skill in the art “would have found it obvious to use the ADSL transmitter shown in Grube’s FIG. 6 for DMT transmitters.” *See* Pet. 82–83. For the reasons explained for claim 1, we find Grube’s DMT transmitter in the circuit identified by Petitioner (*see id.* at 79–81) teaches a “circuit for creating an error coding data block for a first data block, the circuit comprising” the first and second error coding paths as recited in claim 1.

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 16 of the ’344 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

11. Dependent Claim 18

Claim 18 recites,

The system as claimed in claim 16, wherein the circuit is adapted to read out the information of the first data block along with the error coding data block in a reading operation; and to perform, by means of the error coding data block, an error detection or error correction for read-out information of the first data block.

Petitioner asserts that Grube's DMT transmitter 114 performs CRC and FEC error coding before transmitting data to DMT receiver 122 at secondary site 108. Pet. 84–85 (citing Ex. 1005, 7:1–15, 9:62–12:23, 43:60–65; Ex. 1003 ¶¶ 277–280). Petitioner argues that DMT receiver 122 at secondary site 108 receives and reads the transmitted DMT symbols comprising the data and error coding blocks provided by the transmitter's CRC and FEC operations. Pet. 85 (citing Ex. 1005, 7:1–15, 9:62–13:46, 43:41–44:20, 46:45–47:5; Ex. 1003 ¶¶ 277–278). As to the claimed error detection or error correction, Petitioner argues a person of ordinary skill would have found it obvious to use the CRC and FEC error coding data blocks for error detection and correction because that is the purpose of such error coding data blocks. Pet. 86 (citing Ex. 1003 ¶¶ 281–285).

We are persuaded by Petitioner's arguments and evidence. As discussed for claim 16, we are persuaded that a person of ordinary skill in the art “would have found it obvious to use the ADSL transmitter shown in Grube's FIG. 6 for DMT transmitters.” See Pet. 82–83. Grube's ADSL transmitter has CRC and FEC devices, and we agree that a person of ordinary skill in the art would have found it obvious that these devices are used for error detection and correction because this is their purpose, as Dr. Tredennick testifies. Ex. 1003 ¶ 282 (testifying that “the purpose of CRC/FEC blocks is for error detection/correction”). Grube confirms that ADSL transmitters perform error correction, stating, “[a]s an alternative to incorporating error correction into the data formatter 806, the error correction within the ADSL transmitter 852 could be used.” Ex. 1005, 44:13–15, *cited in* Pet. 85, 86. Thus, we find Grube teaches that “the circuit is adapted to read out the information of the first data block along with the

error coding data block in a reading operation” and is adapted to “to perform, by means of the error coding data block, an error detection or error correction for read-out information of the first data block.”

Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 18 of the ’344 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

12. Claims 19, 20, 22, and 26–30

Petitioner’s contentions as to claim 19 suffer from the same inadequacies we discuss with respect to the anticipation ground based on ADSL. *See* Section II.D.10 above. In particular, Petitioner relies on the scrambler and interleaver in Grube’s interleave path to teach “at least the first means for performing the first error coding comprising a means for performing a data arrangement alteration algorithm.” Pet. 89–90. For the reasons discussed for claim 1, Petitioner has not established that Grube’s scrambler is a data arrangement alteration device as described in the ’344 patent and, therefore, has not shown that Grube’s scrambler teaches the structure of data arrangement alteration devices 122, 132, and 222. Grube shows its interleaver is located after the error coders in Figure 6, similar to the arrangement of devices in ADSL. *Compare* Ex. 1005, Fig. 6, *with* Ex. 1004, Fig. 3. As discussed in the ADSL anticipation ground, we agree with Patent Owner that, in first error coding path 120, which we identified as the corresponding structure for “means for selectively performing a first error coding so as to create a first error coding data block,” the data arrangement alteration device is always located in front of the error coder and outputs data to the error coder. Ex. 1001, 3:27–34, 3:57–4:3, 5:53–64,

Figs. 1A, 1E. Petitioner's identification of Grube's interleaver located after the error coders does not show that Grube teaches the same structure as first error coding path 120 in the '344 patent. Furthermore, Petitioner does not provide argument or evidence demonstrating that Grube's interleave path, which performs data arrangement alteration after error coding, performs the claimed function in substantially the same way to achieve substantially the same result as first error coding path 120. Thus, Petitioner has not shown that Grube's interleave path teaches structure equivalent to first error coding path 120 in the '344 patent. Petitioner, therefore, has not proven, by a preponderance of the evidence, that claim 19 is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

Claims 20, 22, and 26–30 incorporate the “means for selectively performing a first error coding so as to create a first error coding data block” limitation of independent claim 19, and, therefore, Petitioner has not proven, by a preponderance of the evidence, that these claims are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Grube.

III. CONCLUSION

For the reasons discussed above, we determine Petitioner has proven, by a preponderance of the evidence, that (1) claims 1, 4, 8–12, 43, 45, and 48–51 are unpatentable under 35 U.S.C. § 102(b) over ADSL; (2) claims 16 and 18 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of ADSL and Voith; and (3) claims 1, 4, 8–12, 16, 18, 43, 45, and 48–51 are unpatentable under 35 U.S.C. § 103(a) over Grube. Petitioner, however, has not proven, by a preponderance of the evidence, that claims 2, 19, 20, 22, 26–30, and 44 are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1, 4, 8–12, 16, 18, 43, 45, and 48–51 of the '344 patent have been shown to be unpatentable; and

FURTHERED ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01346
Patent 8,161,344 B2

PETITIONER:

Jeremy Monaldo
W. Karl Renner
David M. Hoffman
FISH & RICHARDSON P.C.
jjm@fr.com
axf-ptab@fr.com
hoffman@fr.com

PATENT OWNER:

Matthew Phillips
Derek Meeker
Kevin Laurence
LAURENCE & PHILLIPS IP LAW LLP
mphillips@lpiplaw.com
dmeeker@lpiplaw.com
klaurence@lpiplaw.com

Bryan Richardson
WiLAN INC.
brichardson@wilan.com