

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01415
Patent 6,208,574 B1

Before JAMESON LEE, KEVIN F. TURNER, and
MATTHEW J. McNEILL, *Administrative Patent Judges*.

McNEILL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

On May 12, 2017, Petitioner, Samsung Electronics Co. Ltd., filed a Petition (Paper 1, “Pet.”) to institute *inter partes* review of claims 4–18 and 21–27 of U.S. Patent No. 6,208,574 B1 (Ex. 1001, “the ’574 patent”). In an initial decision, we instituted *inter partes* review of each of the challenged claims. Paper 6 (“Dec. Inst.”).

ProMOS Technologies Inc. (“Patent Owner”) filed a Patent Owner Response (Paper 10, “PO Resp.”), and Petitioner filed a Reply (Paper 12, “Reply”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued under 35 U.S.C. § 318(a). We determine that Petitioner has shown by a preponderance of the evidence that claims 4–18 and 21–27 of the ’574 patent are unpatentable.

B. Related Matters

Petitioner concurrently filed a Petition challenging claims 1–3 and 30–37 of the ’574 patent in IPR2017-001414. Pet. 1. Petitioner identifies U.S. Patent No. 6,088,270 (“the ’270 patent”) as related to the ’574 patent. Pet. 2. Petitioner indicates that the ’270 patent is the subject of *inter partes* review in IPR2017-00036. *Id.*

Petitioner indicates that Patent Owner asserted the ’574 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co.*, No. 1:16-cv-00335-SLR-SRF (D. Del.). Pet. 1. Petitioner indicates Patent Owner has also asserted the following patents in that action: U.S. Patent Nos. 6,069,507; 6,172,554; 6,562,714; 7,375,027; and 6,559,044. *Id.* Petitioner concurrently filed IPR petitions challenging the other asserted

patents in the following *inter partes* review proceedings: IPR2017-01412, IPR2017-01413, IPR2017-01416, IPR2017-01417, IPR2017-01418, and IPR2017-01419. *Id.*

Petitioner also filed several IPR petitions involving patents asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Pet. 1–2. Petitioner identifies the following *inter partes* review proceedings for the patents involved in that suit: IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. *Id.*

C. The '574 Patent

The '574 patent relates to sense amplifiers in integrated circuit memories. Ex. 1001, 1:9–11. Integrated circuit memories often include a large number of memory cells set forth in a memory array. *Id.* at 1:14–15. Memory arrays are often organized into rows and columns. *Id.* at 1:35–36. Rows represent the memory cells located along a word line. *Id.* at 1:36–37. Columns are organized perpendicularly to the rows and represent the memory cells located along a bit line. *Id.* at 1:37–40. Generally, each column is connected to a sense amplifier. *Id.* at 1:40–41. In a large memory cell with thousands of columns and rows, the voltage that reaches sense amplifiers at different ends of the array may be appreciably different as a result of resistance along the lines, causing inefficient or slow operation. *Id.* at 2:15–39. The '574 patent relates to additional circuitry that may be connected to the sense amplifiers to alleviate these issues. *Id.* at 4:61–5:39.

One embodiment of the '574 patent is represented in Figure 5, which is reproduced below.

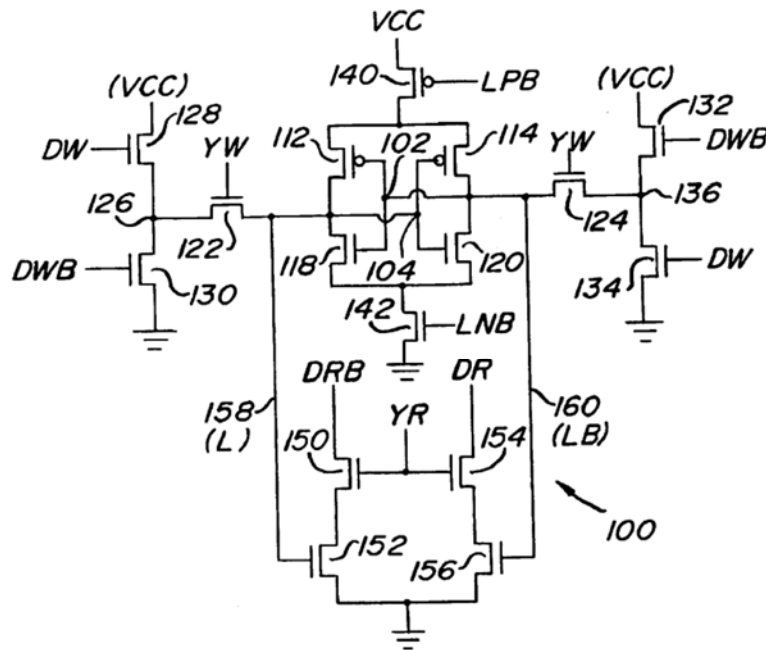


FIG. 5

Figure 5 depicts sense amplifier 100 having a latch formed by transistors 112, 114, 118, and 120. *Id.* at 6:6–9. Node 102 is coupled to the gate electrodes of P-channel transistor 112 and N-channel transistor 118. Node 102 is also coupled to the source-drain path of pass transistor 124. *Id.* at 6:28–31. Node 104 is coupled to the gate electrodes of P-channel transistor 114 and N-channel transistor 120. *Id.* at 6:9–13. Node 104 is also coupled to the source-drain path of pass transistor 122. *Id.* at 6:28–31. Pass transistors 122 and 124 are driven by column write select signal YW. *Id.* at 6:15–16.

Transistor 122 is coupled to node 126 between the source of local data write driver transistor 128 and the drain of local data write driver transistor 130. *Id.* at 6:32–35. Transistors 128 and 130 are N-channel transistors having their source-drain paths coupled in series. *Id.* at 6:35–36. The drain of transistor 128 is coupled to VCC and the source of transistor 130 is

coupled to ground. *Id.* at 6:36–38. Data write signal DW is coupled to the gate electrode of transistor 128, and its complement DWB is coupled to the gate electrode of transistor 130. *Id.* at 6:38–40. Transistors 132 and 134 on the opposite side of sense amplifier 100 have a similar arrangement, though DW and DWB are applied oppositely. *Id.* at 6:40–47.

Figure 5 also depicts local sense amplifier drive transistors 140 and 142. *Id.* at 7:16–18. Transistor 140 is coupled to the source electrodes of transistors 112 and 114. *Id.* at 6:53–55. The source electrode of transistor 140 is coupled to VCC (or LATCHP). *Id.* at 6:55–56. The gate of transistor 140 is coupled to LPB, which is the logical complement of LATCHP. *Id.* at 6:56–57. Transistor 142 is similarly configured with N-channel transistors 118 and 120, but the gate electrode of transistor 142 is coupled to signal LNB, the logical complement of LATCHN. *Id.* at 6:59–65.

The lower portion of Figure 5 also depicts a local column read amplifier comprising N-channel transistors 150, 152, 154, and 156. *Id.* at 6:66–7:1. The source-drain paths of transistors 150 and 152 are coupled in series, and the drain electrode of transistor 150 receives signal DRB, the logical complement of a data read signal DR. *Id.* at 7:1–4. The gate electrode of transistor 150 is coupled to column read signal Y_R. *Id.* at 7:7–8. The source electrode of transistor 152 is coupled to ground. *Id.* at 7:4–5. The gate electrode of transistor 152 is coupled to node 104. *Id.* at 7:5–7.

The source-drain paths of transistors 154 and 156 are similarly configured, being coupled in series between data read signal DR and ground on the right side of the figure. *Id.* at 7:8–10. The gate electrode of transistor 156 is coupled to node 102. *Id.* at 7:11–13.

Petitioner notes that the '574 patent claims priority to an earlier application filed on November 12, 1992. Ex. 1001, at [62]. As discussed below, Petitioner establishes that the asserted references qualify as prior art assuming that November 12, 1992, is the priority date of the '574 patent. *See* Pet 4.

Claim 4 of the '574 patent is independent and reproduced below:

4. A sense amplifier arrangement for an integrated circuit memory comprising, for each of a plurality of sense amplifiers:

a sense amplifier latch circuit having a pair of nodes to which respective bit lines may be coupled;

a local column read amplifier responsively coupled to the sense amplifier, and receiving at least one data read signal; and

a local data write driver circuit coupled to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes.

Ex. 1001, 13:46–58.

D. Evidence Relied Upon

Petitioner relies on the following prior art:

Japanese Patent Application Publication No. S58-128087, published July 30, 1983 (Ex. 1007, “Inoue”);¹

UK Patent Application Publication No. G.B. 2246005A, published January 15, 1992 (Ex. 1008, “Min”);

¹ Petitioner relies on a certified English translation of Inoue. Exhibit 1007 includes an English language version of Inoue (pages 1–6), the Japanese language version of Inoue (pages 7–10), a declaration certifying the English translation (page 11), and a certified correction to the translation (page 12). Our citations refer to the certified English translation of Inoue (pages 1–6 of Exhibit 1007).

Hamade, U.S. Patent No. 5,323,349, filed August 28, 1992, issued June 21, 1994 (Ex. 1009, “Hamade”); and

Ogawa, U.S. Patent No. 5,293,347, filed December 30, 1991, issued March 8, 1994 (Ex. 1010, “Ogawa”).

Petitioner also relies upon the testimony of Dr. R. Jacob Baker, Ph.D. Ex. 1002.

E. The Asserted Ground

Petitioner asserts the following grounds of unpatentability:

References	Basis	Claims Challenged
Inoue, Min, and Hamade	§ 103(a)	4–10, 14–17, 21–27
Inoue, Min, Hamade, and Ogawa	§ 103(a)	11–13, 18

II. ANALYSIS

A. Claim Construction

The ’574 patent has expired. We review expired patent claims according to the standard applied by the district courts. *See In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). Specifically, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

In our Institution Decision, we adopted Petitioner’s proposal (*see* Pet. 12–13) to construe the limitation “local data write driver circuit” in claims 1, 4, and 30 to mean “a data write driver circuit that is associated with only one

latch circuit.” Dec. Inst. 8–10. We were persuaded by Petitioner’s evidence from the specification of the ’574 patent that local write driver circuits are connected to or associated with a single latch circuit. *Id.* at 9 (citing Ex. 1001, 4:61–63, 5:29–36, 6:5–13, 7:15–16, 11:25–31, Fig. 5). We also were persuaded that Petitioner’s proposed construction was consistent with arguments made by the patentee during prosecution. *Id.* at 9–10 (citing Ex. 1006, 274; Ex. 1005, 166–68). We also determined that Petitioner’s proposal was consistent with the Board’s prior construction from an *ex parte* appeal of the application that matured into the related ’270 patent, where “local” was defined as having “a definite spatial form or location.” *Id.* at 8–9.

In its Response, Patent Owner does not dispute that “a local write driver circuit” is disclosed by the cited prior art combination under any asserted construction, including Petitioner’s proposed construction and the *ex parte* appeal construction proposed by Patent Owner. PO Resp. 6. Instead, Patent Owner argues “the resolution of the parties’ claim construction dispute is immaterial to the questions of [unpatentability] presented to the Board, [so] there is no need to construe [this] term[.]” *Id.* at 7. Patent Owner characterizes this claim construction issue as being “relevant only to infringement issues before the district court,” such that any construction we adopt would amount to an advisory opinion. *Id.* at 6. Thus, Patent Owner argues we should withdraw our preliminary claim construction of “local write driver circuit,” or adopt the Board’s earlier construction from the *ex parte* appeal. *Id.* at 7–13.

In its Reply, Petitioner urges us to maintain the construction from our Institution Decision because “there is a dispute between the parties as to the

proper construction of [this] term[.]” *See* Reply 2. Petitioner asserts the evidence of record supports our preliminary construction. *Id.* at 2–6.

We are persuaded by Patent Owner’s arguments. Whether the prior art teaches a “local write driver circuit” is not disputed in this proceeding. *See* PO Resp. 6. Because Patent Owner did not file a Preliminary Response, as is its right,² we construed “local write driver circuit” in our Institution Decision anticipating that this construction might affect the outcome of this case. Now that we have the benefit of Patent Owner’s positions from its Response, we see no reason to explicitly construe the term. Importantly, our reviewing court has stated that “claim terms need only be construed ‘to the extent necessary to resolve the controversy.’” *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). In the absence of any controversy about Petitioner’s unpatentability contentions for a “local write driver circuit,” we determine that no construction is necessary.

In our Institution Decision, we also adopted Petitioner’s proposed construction (*see* Pet. 16–21) for the limitation “local column read amplifier” in claims 1, 4, and 30. Dec. Inst. 10. However, for the same reasons as discussed above for “local data write driver circuit,” we determine that neither this limitation, nor any other terms, requires explicit construction.

² Patent Owner is not required to file a Preliminary Response. *See* 37 C.F.R. § 42.107(a) (“The patent owner *may* file a preliminary response to the petition”) (emphasis added).

B. Level of Ordinary Skill in the Art

As to the level of ordinary skill in the art, Petitioner states:

A person of ordinary skill in the art at the time of the alleged invention of the '574 patent ('POSITA') would have had at least a Bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in design of semiconductor memory circuits.

Pet. 5. Petitioner also states that "[m]ore education can supplement practical experience and vice versa." *Id.* at 5. Petitioner's position is supported by Dr. Baker's testimony (Ex. 1002 ¶ 20) and is not disputed by Patent Owner. We find Petitioner's proposed level of skill vague because it relies on the qualifier "at least." The qualifier makes the range of education and the range of working experience unacceptably broad. We adopt Petitioner's articulation of the level of ordinary skill in the art, as we credit the declaration of Dr. Baker (Ex. 1002 ¶ 20), but without inclusion of the qualifier "at least."

C. Ground 1: Alleged Obviousness of Claims 4–10, 14–16, and 21–27 over Inoue, Min, and Hamade

We have reviewed the arguments and evidence presented by Petitioner and Patent Owner. Petitioner has shown by a preponderance of the evidence that claims 4–10, 14–16, and 21–27 would have been obvious over Inoue, Min, and Hamade.

1. *Inoue*

Inoue is a Japanese patent application publication directed to "a semiconductor device that consumes only a small amount of transient power when writing to a flip-flop." Ex. 1007, 3. Figure 6 of Inoue is reproduced below.

第 6 図

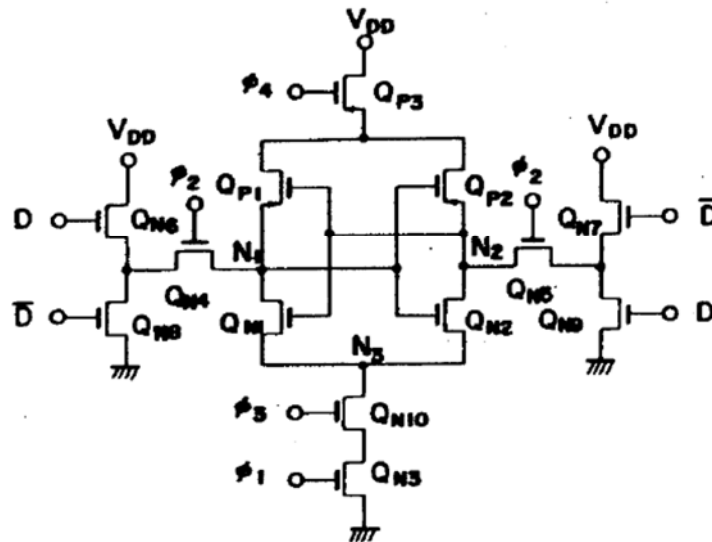


Figure 6 depicts a CMOS flip-flop circuit having supply terminals V_{DD} , nodes N_1 – N_3 , N-channel transistors Q_{N1} – Q_{N10} , P-channel transistors Q_{P1} – Q_{P3} , and clocks ϕ_1 – ϕ_4 . *Id.* at 3–4. D and $\bar{D}$ are input terminals. *Id.* at 4. The circuit in Figure 6 may be applied to a sense amplifier in a dynamic memory, wherein nodes N_1 and N_2 correspond to bit lines and transistors Q_{N6} – Q_{N9} correspond to the output stage for the data input buffer. *Id.*

We agree with Petitioner (Pet. 4) that Inoue qualifies as prior art under at least 35 U.S.C. § 102(b)³ because Inoue’s publication date of July 30, 1983, is more than one year before the earliest possible priority date for the ’574 patent, which is November 12, 1992. *See* Ex. 1001, at [62]; Ex. 1007, at [43].

³ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Because the priority date of the ’270 patent is before the effective date of the applicable AIA amendments, the pre-AIA versions of 35 U.S.C. §§ 102 and 103 apply.

2. *Min*

Min is a United Kingdom patent application publication directed to a sense amplifier driving circuit for controlling sense amplifiers of a high-density semiconductor memory device. Ex. 1008, Abstract. Figure 3B of Min is reproduced below.

FIG. 3B

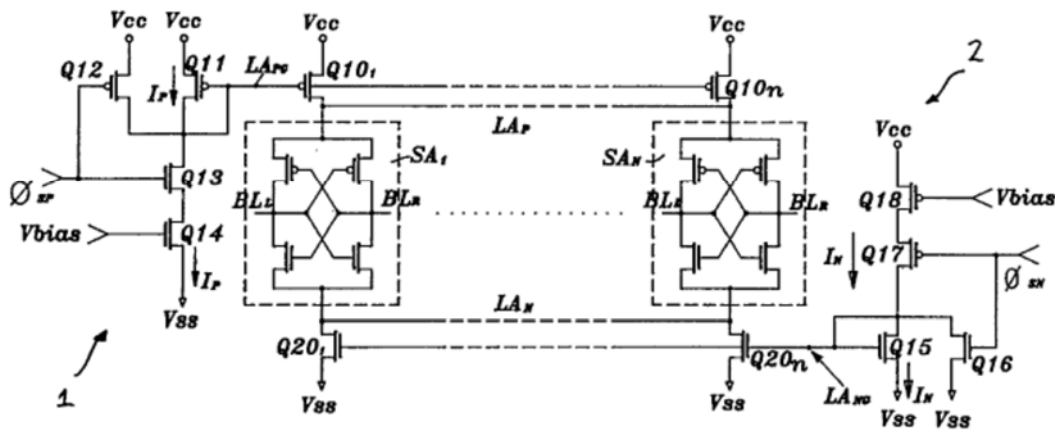


Figure 3B depicts a memory device with a plurality of sense amplifiers SA₁–SA_N. Ex. 1008, 1:4–8, Fig. 3B. Each sense amplifier is coupled to a bit line pair (BL_L and BL_R). Ex. 1008, 2:5–15, Fig. 3B. Each sense amplifier is also coupled to a positive power supply (V_{CC}) via driving transistor Q10_i and to ground (V_{SS}) via driving transistor Q20_i. *Id.* at 21:1–13, Fig. 3B. Min discloses a common driving signal from driving transistors Q10_i and Q20_i. Ex. 1008, Fig. 3B.

We agree with Petitioner (Pet. 4) that Min qualifies as prior art under at least 35 U.S.C. § 102(a) because Min’s publication date of January 15, 1992, is before the earliest possible priority date for the ’574 patent, which is November 12, 1992. *See* Ex. 1001, at [62]; Ex. 1008, at [43].

3. Hamade

Hamade discloses a semiconductor memory device. Ex. 1009, 1:8–9. Figure 1 of Hamade is reproduced below.

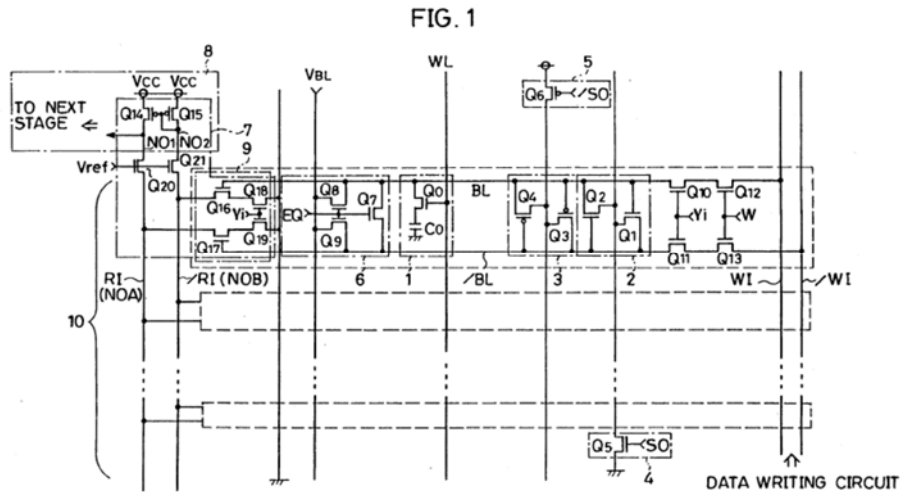


Figure 1 illustrates a “main part” of the device, depicting a pair of bit lines BL and /BL and their associated circuitry. *Id.* at 3:1–5, 7:10–13, Fig. 1. Each bit line pair is associated with n-type sense amplifier 2 and p-type sense amplifier 3. *Id.* at 1:47–52, 7:4–13, Fig. 1. Drive circuit 9, which includes transistors Q₁₆–Q₁₉, is provided for each bit line pair. *Id.* at 7:14–19, Fig. 1. Drive circuit 9 “amplifies the potentials of the associated bit lines.” *Id.* Drive circuit 9 “operate[s] to amplify the potentials on bit lines BL and /BL during a read operation, and allow[s] one of read only data lines RI and /RI to be discharged to ground during a read operation.” Pet. 29. We agree with Petitioner (Pet. 4) that Hamade qualifies as prior art under at least 35 U.S.C. § 102(e) because Hamade’s filing date of August 28, 1992, is before the earliest possible priority date for the ’574 patent, which is November 12, 1992. *See* Ex. 1001, at [62]; Ex. 1009, at [22], [45].

4. *Independent claim 4*

Claim 4 recites, “[a] sense amplifier arrangement for an integrated circuit memory comprising.” Petitioner asserts that Inoue discloses this feature. Pet. 17.

In particular, Petitioner asserts “*Inoue* discloses ‘a semiconductor device’ comprising a sense amplifier with a flip-flop circuit. The circuit in figure 6 of *Inoue* is for a sense amplifier in a dynamic memory.” *Id.* (citations omitted). Petitioner further asserts an ordinarily skilled artisan “would have understood that ‘dynamic memory’ in *Inoue* refers to a dynamic random access memory (DRAM), which is an integrated circuit memory.” *Id.* Dr. Baker’s testimony supports Petitioner’s assertions. Ex. 1002, ¶ 68. We find Dr. Baker’s testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that Inoue discloses “[a] sense amplifier arrangement for an integrated circuit memory comprising.”

Claim 4 further recites “for each of a plurality of sense amplifiers: a sense amplifier latch circuit having a pair of nodes to which respective bit lines may be coupled.” Petitioner asserts that Inoue in combination with Min discloses this limitation. Pet. 17–27.

Inoue discloses a “semiconductor device” in a “dynamic memory.” Ex. 1007, 3–4. Inoue discloses an embodiment, illustrated by Figure 6, with multiple sense amplifiers, where each comprises a CMOS “F/F” or “latch” that includes a pair of internal nodes “N₁ and N₂ correspond[ing] to bit lines.” Ex. 1007, 4. However, Petitioner concedes that Inoue does not

expressly disclose a plurality of sense amplifiers or a plurality of bit line pairs corresponding to such sense amplifiers. Pet. 20.

Min discloses a semiconductor memory device with a plurality of sense amplifiers SA_1-SA_N . Ex. 1008, 1:4–8, Fig. 3B. Each sense amplifier is coupled to a bit line pair (BL_L and BL_R). Ex. 1008, 2:5–15, Fig. 3B. Each sense amplifier is also coupled to a positive power supply (V_{CC}) via driving transistor $Q10_i$ and to ground (V_{SS}) via driving transistor $Q20_i$. Ex. 1008, 21:1–13, Fig. 3B. Min discloses a common driving signal from driving transistors $Q10_i$ and $Q20_i$. Ex. 1008, Fig. 3B.

Petitioner asserts an ordinarily skilled artisan “would have been motivated to implement *Inoue*’s figure 6 circuit in a multi-column memory system to create a dynamic memory having a plurality of bit line pairs with each of bit line pairs coupled to a respective sense amplifier.” Pet. 21. Specifically, Petitioner asserts an ordinarily skilled artisan would have been motivated to implement *Inoue*’s circuitry of Figure 6 to implement a multi-column DRAM with multiple sense amplifiers as taught by Min because practical DRAMs had multiple columns. Pet. 22. Petitioner further asserts an ordinarily skilled artisan would have found it beneficial to use common drive signals for the drive transistors as set forth in Min to reduce the amount of circuitry and, therefore, chip area, when compared to separate clock signals for each latch circuit. Pet. 24. Dr. Baker’s testimony supports these assertions. Ex. 1002, ¶¶ 34–37, 73, 77. We find Dr. Baker’s testimony on this point persuasive and afford it substantial weight.

Petitioner further asserts modifying *Inoue*’s apparatus to use a plurality of sense amplifiers and a plurality of bit line pairs as set forth in Min would have been straightforward for an ordinarily skilled artisan

because Inoue's Figure 6 embodiment describes a single sense amplifier with a single bit line pair and Min discloses a plurality of sense amplifiers, each coupled to respective bit line pairs. Pet. 24–25. According to Petitioner, an ordinarily skilled artisan would have understood how to incorporate Inoue's sense amplifier into Min's multi-column memory. *Id.* at 25. Petitioner asserts such a combination would have been a predictable combination of known components according to known methods, and would have been consistent with working DRAM features. *Id.* at 25–26. Dr. Baker's testimony supports these assertions. Ex. 1002, ¶¶ 74, 78. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight.

In an obviousness analysis, there must be articulated reasoning with a rational underpinning to support a conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Petitioner has articulated reasoning with a rational underpinning to support applying Inoue's sense amplifier to a practical multi-column memory because working DRAMs use multi-column arrangements and Min's common driving signals for multiple sense amplifiers and their corresponding bit line pairs would help reduce the amount of circuitry in such a memory, thereby reducing the chip area. Dr. Baker's testimony amply supports this rationale. Ex. 1002, ¶¶ 72–77. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations.

Thus, we are persuaded that the combination of Inoue and Min discloses “for each of a plurality of sense amplifiers: a sense amplifier latch circuit having a pair of nodes to which respective bit lines may be coupled”

and that an ordinarily skilled artisan would have been motivated to combine the teachings of Inoue and Min as proposed by Petitioner.

Claim 4 further recites “a local column read amplifier responsively coupled to the sense amplifier, and receiving at least one data read signal.” Petitioner concedes “[t]he combined *Inoue-Min* system does not expressly disclose this feature.” Pet. 27. However, Petitioner asserts that the Inoue-Min system in combination with Hamade discloses this limitation. Pet. 27–35.

Hamade discloses a semiconductor memory device. Ex. 1009, 1:7–9. Figure 1 of Hamade is shown below.

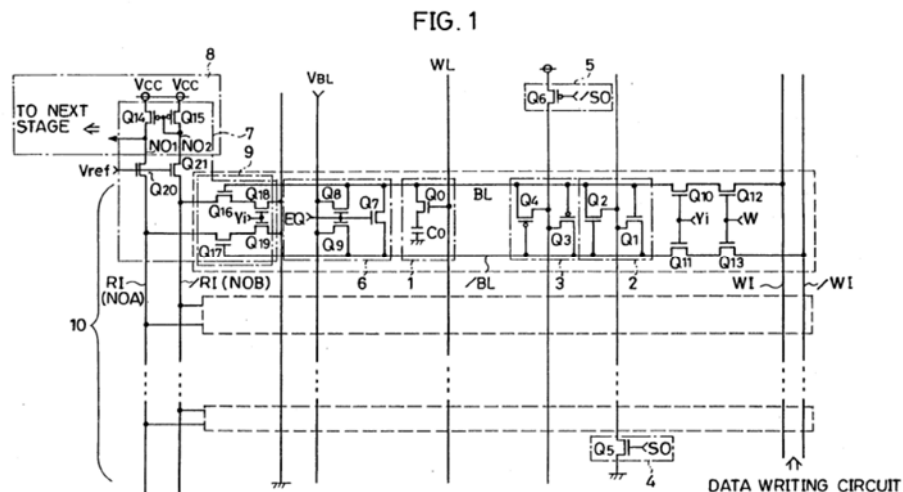


Figure 1 illustrates a “main part” of such a device and depicts a pair of bit lines BL and /BL and their associated circuitry. *Id.*, 3:1–5, 7:4–12, Fig. 1. Each bit line pair is associated with n-type sense amplifier 2 and p-type sense amplifier 3. *Id.*, 1:47–52, 7:4–13, Fig. 1. Dr. Baker testifies that an ordinarily skilled artisan would understand that, collectively, these sense amplifiers form a latch similar to the latch in Inoue’s Figure 6. Ex. 1002, ¶ 86.

Hamade further discloses a drive circuit 9 comprised of transistors Q₁₆–Q₁₉ is provided for each bit line pair. Ex. 1009, 7:14–19, Fig. 1. Drive circuit 9 “amplifies the potentials of the associated bit lines.” *Id.* Petitioner asserts an ordinarily skilled artisan would have understood drive circuit 9 to constitute a “column read amplifier” as claimed because drive circuit 9 “operate[s] to amplify the potentials on bit lines BL and /BL during a read operation, and allow[s] one of read only data lines RI and /RI to be discharged to ground during a read operation.” Pet. 29 (citing Ex. 1009, 3:61–4:10, 8:8–31, 8:52–54). Petitioner asserts “drive circuit 9 is provided for each *column* because it is provided for each bit line pair (Ex. 1009, 7:22–23), which is “related to memory cells in one *column* of the memory cell array.” (*Id.*, 1:36–39 (emphasis added), 7:4–9.).” Pet. 29. Petitioner asserts the drive circuit 9 “would receive signals on read only data lines RI and /RI (‘receiving at least one data read signal’) in the combined system.” *Id.* at 32–33 (citing Ex. 1009, 7:35–39, Fig. 1). Dr. Baker’s testimony supports these assertions. Ex. 1002, ¶ 87; *see also id.* ¶¶ 82–95. We find Dr. Baker’s testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses “a local column read amplifier responsively coupled to the sense amplifier, and receiving at least one data read signal.”

Petitioner further asserts an ordinarily skilled artisan would have been motivated to combine the Inoue-Min system with Hamade’s drive circuit at each column because Hamade discloses that drive circuit 9 is provided for each bit line pair. Pet. 29. Petitioner asserts an ordinarily skilled artisan would have known how to assemble and implement all of the relevant

circuitry into the combined system without undue experimentation. *Id.* Petitioner asserts an ordinarily skilled artisan would have looked to Hamade to modify the Inoue-Min system because the combined Inoue-Min system does not disclose read circuitry that would typically be found in a practical DRAM. *Id.* at 34. According to Petitioner, the combined Inoue-Min-Hamade system would allow “fast reading of the data carried by the bit lines.” *Id.* Petitioner asserts the combination would use known components according to known methods to yield predictable results. *Id.* at 34–35.

Patent Owner asserts an ordinarily skilled artisan would not combine Hamade with the Inoue-Min system because the combined system would consume more power, which is contrary to Inoue’s express goal of providing a circuit that consumes a small amount of power when sensing. PO Resp. 14, 17–18 (citing Ex. 1007, 3; Ex. 2001 ¶¶ 44–45; Ex. 2003, 75:12–16, 76:5–9, 107:8–108:1). Patent Owner asserts Hamade’s high-speed read amplifier uses at least four additional transistors with each bit line pair, increasing current consumption and power requirements compared to a system with a global data path. *Id.* at 14–16 (citing Ex. 1009, 1:8–15, 3:5–7, 7:17–19, 9:55–58; Ex. 2001, ¶¶ 48–51).

In an obviousness analysis, there must be articulated reasoning with a rational underpinning to support a conclusion of obviousness. *In re Kahn*, 441 F.3d at 988. Petitioner has articulated reasoning with a rational underpinning to support applying Hamade’s drive circuit 9 to the combined Inoue-Min system, namely adding the drive circuit would allow “fast reading of the data carried by the bit lines.” Pet. 34. Dr. Baker’s testimony amply supports this rationale. Ex. 1002 ¶¶ 84–99. For example, Dr. Baker testifies an ordinarily skilled artisan would have been motivated to modify

the combined Inoue-Min system to implement Hamade's drive circuit 9 because Hamade discloses that drive circuit 9 is provided for each bit line pair. *Id.* ¶ 90 (citing Ex. 1009, 7:17–18). Dr. Baker testifies an ordinarily skilled artisan would have looked to Hamade to augment and improve the capabilities of the combined Inoue-Min system because Hamade teaches circuitry and functionality applicable to a column of memory such as in the combined Inoue-Min system. *Id.* ¶¶ 97–98. Dr. Baker testifies an ordinarily skilled artisan would have recognized that the combined Inoue-Min system does not disclose read circuitry for reading data carried by bit lines that would typically be found in a practical DRAM, and Hamade discloses such circuitry for reading data at a high rate of speed. *Id.* ¶ 97. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight.

Patent Owner's argument that adding Hamade's drive circuit to the combined Inoue-Min system would defeat the intended purpose of Inoue is unpersuasive for two reasons. First, adding Hamade's drive circuit to the combined Inoue-Min system would not affect Inoue's circuitry that achieves the desired decrease in power consumption. Specifically, Inoue teaches disabling transistors Q_{P3} and Q_{N10} to reduce power consumption during a write operation. Ex. 1013, 116:24–118:3. Inoue teaches that conventional prior art circuits do not have these transistors. *Id.* Petitioner's proposed combination would not modify this portion of Inoue's circuitry, maintaining the reduced power consumption achieved by Inoue's teachings. *See* Reply 9–10. Thus, the proposed combination does not defeat the intended purpose of Inoue because it maintains the circuitry that achieves the desired decrease in power consumption.

Second, even if adding Hamade’s drive circuit to the combined Inoue-Min system caused additional power consumption, an ordinarily skilled artisan may embrace this tradeoff to achieve the speed increase taught by Hamade. The test for obviousness is not whether the goals and objectives of every prior art reference can be accomplished by a proposed combination of prior art teachings. Rather, an ordinarily skilled artisan may be motivated to pursue the desirable properties taught by one prior art reference even if that means foregoing the benefits taught by another prior art reference. *See In re Urbanski*, 809 F.3d 1237, 1244 (Fed. Cir. 2016); *see also Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (“[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.”). This is particularly true where, as here, the claims at issue do not require the benefit that is arguably lost in the combination. *See id.* Indeed, a prior art reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect. *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985). The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned, as they are a part of the literature and are relevant for all they contain. *In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) (citing *In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968)).

Thus, we are persuaded that the combination of Inoue, Min, and Hamade discloses “a local column read amplifier responsively coupled to the sense amplifier, and receiving at least one data read signal” and that an

ordinarily skilled artisan would have been motivated to combine the teachings of Inoue, Min, and Hamade as proposed by Petitioner.

Claim 4 further recites “a local data write driver circuit coupled to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes.” Petitioner asserts that the combined Inoue-Min-Hamade system discussed above discloses this limitation. Pet. 35–41. In particular, Petitioner asserts Q_{N6} and Q_{N8} form one “local data write driver circuit” on the left side of Inoue’s Figure 6 and Q_{N7} and Q_{N9} form a second “local data write driver circuit” on the right side of the figure. *Id.* at 35–36. Each of these data write driver circuits is only associated with the sense amplifier depicted in Figure 6. Dr. Baker’s testimony supports Petitioner’s assertions. Ex. 1002 ¶ 100. We find Dr. Baker’s testimony on this point persuasive and afford it substantial weight.

Petitioner further asserts each latch circuit is coupled to only one pair of data write driver circuits and, therefore, each data write driver circuit is a “local data write driver circuit.” Pet. 37–38. Dr. Baker’s testimony supports Petitioner’s assertion. Ex. 1002, ¶ 102. We find Dr. Baker’s testimony on this point persuasive and afford it substantial weight.

Petitioner further asserts:

Each of the local data write driver circuits at each column in the combined *Inoue-Min-Hamade* system would have been coupled to (1) receive data at their gate terminals D and $\bar{D}$ (“receive write data”) during a write operation at a gate electrode of a transistor Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} (“a transistor in said data write driver circuit”) in said data write driver circuit, and (2) apply a signal corresponding to a level ‘H’ or ‘L’ (“apply a signal”) based upon receiving data D or $\bar{D}$ (“based upon receiving said

write data”) to node N1 or N2 of the latch circuit (“one of said latch circuit nodes”) (red below). (Ex.1007, FIG. 6; Ex.1002, ¶103.)

Pet. 38–39. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses “a local data write driver circuit coupled to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes.”

On these bases, Petitioner submits that the proposed combination of Inoue, Min, and Hamade discloses claim 4. Petitioner has shown, by a preponderance of the evidence, that (1) the combination of Inoue, Min, and Hamade discloses the subject matter of claim 4 in the arrangement as required by the claim; and (2) Petitioner provides sufficient reasons about why an ordinarily skilled artisan would have combined the teachings of Inoue, Min, and Hamade. Thus, for the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 4 is unpatentable as obvious over Inoue, Min, and Hamade.

5. *Dependent claims 5–10, 14–17, and 21–27*

Each of claims 5–10, 14–17, and 21–27 directly or indirectly depends from claim 4. In the Petition, Petitioner accounts for the added limitation of claim 5 relative to base claim 4. Pet. 41–43. Petitioner also accounts for the added limitation of claim 6 relative to base claim 5. *Id.* at 44–46. Petitioner accounts for the added limitations of claims 7 and 8 relative to base claim 4. *Id.* at 46–50. Petitioner also accounts for the added limitations of claim 9

relative to base claim 8 and claims 10 and 14 relative to base claim 9. *Id.* at 50–57.

Petitioner accounts for the added limitations of claim 15 relative to base claim 14 and claim 16 relative to base claim 15. *Id.* at 55–63. Petitioner also accounts for the added limitations of claim 17 relative to base claim 16. *Id.* at 93–95. Petitioner also accounts for the added limitations of claim 18 relative to base claim 17. *Id.* at 96–100. Petitioner also accounts for the added limitations of claim 21 relative to base claim 4 and claim 22 relative to base claim 21. *Id.* at 63–65. Petitioner accounts for the added limitations of claim 23 relative to base claim 22 and claim 24 relative to base claim 23. *Id.* at 65–68. Petitioner accounts for the added limitations of claim 25 relative to base claim 24, claim 26 relative to base claim 25, and claim 27 relative to base claim 24. *Id.* at 68–70.

Each of Petitioner’s positions set forth above are supported by the testimony of Dr. Baker. Ex. 1002 ¶¶ 107–110 (claim 5), ¶¶ 111–112 (claim 6), ¶¶ 113–114 (claim 7), ¶¶ 115–117 (claim 8), ¶¶ 26–33, 118–121 (claim 9), ¶¶ 122–125 (claim 10), ¶¶ 126–127 (claim 14), ¶¶ 128–129 (claim 15), ¶¶ 130–131 (claim 16), ¶¶ 197–199 (claim 17), ¶¶ 201–208 (claim 18), ¶¶ 132–133 (claim 21), ¶¶ 134–136 (claim 22), ¶¶ 137–138 (claim 23), ¶¶ 140–142 (claim 24), ¶ 143 (claim 25), ¶¶ 144–145 (claim 26), and ¶ 146 (claim 27).

Patent Owner has provided no counterargument to Petitioner’s arguments and assertions about the obviousness of claims 5–10, 14–16, and 21–27 over Inoue, Min, and Hamade. We are persuaded that Petitioner has adequately accounted for the limitations added by each of claims 5–10, 14–18, and 21–27, and that Petitioner has shown how the combination satisfies

each of the dependent claims. Petitioner has shown, by a preponderance of the evidence, that each of claims 5–10, 14–16, and 21–27 is unpatentable as obvious over Inoue, Min, and Hamade.

D. Ground 2: Alleged Obviousness of Claims 11–13 and 18 over Inoue, Min, Hamade, and Ogawa

1. Ogawa

Ogawa is a U.S. patent directed to “a semiconductor memory device that carries out pipe line processing in page mode.” Ex. 1010, 1:10–12.

Figure 2 of Ogawa is reproduced below.

FIG. 2

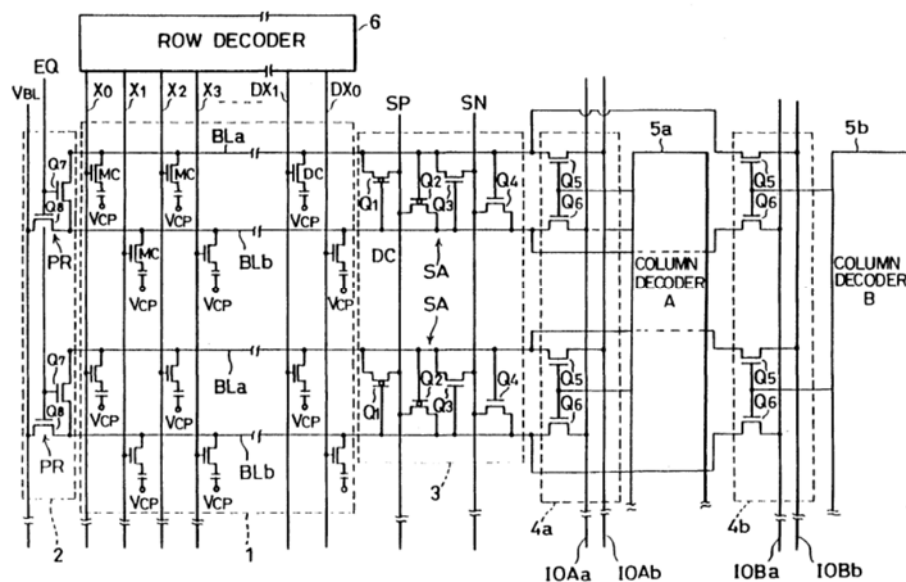


Figure 2 is a circuit diagram of the peripheral circuit of memory cell array 1, which has memory cells arranged in a matrix of rows and columns. *Id.* at 1:17–20, 8:16–18. “[A] plurality of bit line pairs BLa and BLb, and word lines X₀–X₃ crossing the bit line pairs are arranged in memory cell array 1.” *Id.* at 1:46–48. Sense amplifier 3 amplifies the potential difference appearing on a bit line pair. *Id.* at 1:22–24. Column decoders A and B (reference numerals 5a, 5b) select a desired bit line pair according to a

column address. *Id.* at 1:25–26, 7:59–64. Data buses IOAa and IOAb provide write data generated by write driver A (reference numeral 8a; *see* Fig. 5) to I/O control A (reference numeral 4a). *Id.* at 1:29–31, 1:62–66, 2:24–27, 7:67–8:4. Similarly, data buses IOBa and IOBb provide write data generated by write driver B (reference numeral 8b; *see* Fig. 5) to I/O control B (reference numeral 4b). *Id.* at 1:29–31, 1:62–66, 2:24–27, 7:67–8:4. Transistors Q₅ and Q₆, which are provided between the IO bus and the bit line pair, are connected to the gates of column decoders 5a and 5b. *Id.* at 1:66–68, 2:12–16, 2:21–24, 8:27–31.

We agree with Petitioner (Pet. 4) that Ogawa qualifies as prior art under at least 35 U.S.C. § 102(e) because Ogawa’s filing date is December 30, 1991, which is before the earliest possible priority date for the ’574 patent, November 12, 1992. *See* Ex. 1001, at [62]; Ex. 1010, at [22].

2. *Claim 11*

Claim 11 recites, “[t]he sense amplifier arrangement according to claim 10 wherein said write control signal is a column write signal.” Petitioner asserts the Inoue-Min-Hamade system combined with Ogawa discloses this limitation. Pet. 71–75.

Petitioner asserts Ogawa discloses a conventional memory writing technique where a column decoder decodes a provided column address and selects a desired bit line pair for writing data by turning on pass transistors corresponding to that bit line pair. Pet. 71–72 (citing Ex. 1010, 1:18–19, 1:24–27, 3:1–13, Figs. 2, 12). Petitioner asserts Ogawa modifies this conventional technique by providing two column decoders (5A and 5B in Fig. 2) instead of one. *Id.* at 72–73 (citing Ex. 1010, 8:16–36, Fig. 2). Petitioner asserts an ordinarily skilled artisan would have understood that

Ogawa's signal provided from the column decoder to a pass transistor is a "column write signal" as recited in claim 11. *Id.* at 73. Dr. Baker's testimony supports these assertions. Ex. 1002, ¶¶ 148–156. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight.

Petitioner also asserts that it would have been obvious to an ordinarily skilled artisan to implement the Inoue-Min-Hamade write control clock for each column as a column write signal as taught in Ogawa because Ogawa discloses how to operate a dynamic memory with multiple rows and columns, a typical arrangement for memory cells in dynamic memory as disclosed in Min and Hamade. Pet. 73–74 (citing Ex. 1008, Fig. 3B; Ex. 1009, Fig. 1; Ex. 1002, ¶ 155). Petitioner alleges such a modification would provide the benefit of allowing a column of memory cells and would have allowed Inoue's Figure 6 circuit to be implemented in a dynamic memory with many memory cells. *Id.* at 74–75. Petitioner asserts this would have been a combination of known elements using known methods to yield predictable results. *Id.* at 75.

Patent Owner argues Petitioner relies on two separate embodiments from Ogawa—a prior art embodiment shown in Figure 12 and Ogawa's invention shown in Figure 2. PO Resp. 18 (citing Pet. 71). First, Patent Owner argues an ordinarily skilled artisan would not have combined the prior art embodiment taught by Ogawa with the Inoue-Min-Hamade system because Ogawa teaches away from such a combination. *Id.* at 19–20.

A teaching away requires a reference to actually criticize, discredit, or otherwise discourage the claimed solution. *See In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004) ("The prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives

because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed.”). Merely teaching an alternative or equivalent method does not teach away from the use of a claimed method. *See In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012) (citations omitted); *In re Dunn*, 349 F.2d 433, 438 (CCPA 1965). Describing a prior art teaching as “inferior” also does not by itself constitute a teaching away from using the teaching, as long as the material was taught in the prior art as “usable” and had “been used” for the stated purpose. *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994).

Patent Owner’s teaching away argument is not persuasive because Ogawa does not criticize, discredit, or discourage the claimed solution. Instead, Ogawa teaches a prior art embodiment that used a single column decoder may be improved by adding an additional column decoder. Ex. 1010, 5:23–48. “A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit, or otherwise discourage’ investigation into the invention claimed.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (quoting *In re Fulton*, 391 F.3d at 1201). Also, an ordinarily skilled artisan may be motivated to pursue the desirable properties taught by one prior art reference even if that means foregoing the benefits taught by another prior art reference. *See In re Urbanski*, 809 F.3d at 1244; *see also Medichem*, 437 F.3d at 1165 (“[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.”). This is particularly true where, as here, the claims at issue do not require the benefit that is arguably lost in the combination. *See id.*

Second, Patent Owner argues an ordinarily skilled artisan would not have been motivated to combine Ogawa's invention with the Inoue-Min-Hamade system because Ogawa's invention consumes greater power, running counter to the express goals for Inoue. PO Resp. 18. In particular, Patent Owner argues Ogawa teaches splitting a memory array into two halves for pipe line processing and adding additional global column circuitry to the circuit. *Id.* at 20–21 (citing Ex. 1010 8:21–31; Ex. 2001 ¶¶ 44–45, 52–53). Patent Owner argues the prior art embodiment in Ogawa uses a single column decoder, and Ogawa criticizes and discourages using this single column decoder because it is too slow. *Id.* at 20 (citing Ex. 1010, 5:23–58). Patent Owner argues this adds transistors to the design, increasing power consumption. *Id.* at 21. Patent Owner argues, similar to the argument regarding Hamade above, that an ordinarily skilled artisan would not have been motivated to increase the power consumption of the circuit because this undermines the purpose of Inoue. *Id.* at 22.

In an obviousness analysis, there must be articulated reasoning with a rational underpinning to support a conclusion of obviousness. *In re Kahn*, 441 F.3d at 988. Petitioner has articulated reasoning with a rational underpinning to support implementing the Inoue-Min-Hamade write control clock for each column as a column write signal as taught in Ogawa because such an arrangement would allow Inoue's Figure 6 circuit to be implemented in a dynamic memory with many memory cells. Pet. 73–75.

Dr. Baker's testimony supports Petitioner's assertions. Ex. 1002, ¶¶ 154–156. For example, Dr. Baker testifies an ordinarily skilled artisan would have looked to Ogawa to "refine or improve the combined Inoue-Min-Hamade system, because Inoue discloses that its figure 6 circuit

configuration may be applied to a sense amplifier in dynamic memory and Ogawa teaches how to operate a dynamic memory with multiple rows and columns of memory cells.” *Id.* ¶ 154. Dr. Baker testifies that in the early 1990s, a typical way to arrange memory cells in dynamic memory was by columns and rows, and an ordinarily skilled artisan would have looked to Ogawa for details regarding implementing a column decoder in such an arrangement. *Id.* ¶ 155. Dr. Baker also testifies an ordinarily skilled artisan would have recognized that modifying the write control clock in the combined Inoue-Min-Hamade system to be a column write signal as taught by Ogawa’s decoder would have been a necessary change to enable Inoue’s circuit to be implemented in a dynamic memory with many memory cells. *Id.* ¶ 155. We find Dr. Baker’s testimony on this point persuasive and afford it substantial weight.

Patent Owner’s argument that implementing the Inoue-Min-Hamade write control clock for each column as a column write signal as taught in Ogawa would defeat the intended purpose of Inoue is unpersuasive for two reasons. First, implementing the write control clock for each column would not affect Inoue’s circuitry that achieves the desired decrease in power consumption. Specifically, Inoue teaches disabling transistors Q_{P3} and Q_{N10} to reduce power consumption during a write operation. Ex. 1013, 116:24–118:3. Inoue teaches that conventional prior art circuits do not have these transistors. *Id.* Petitioner’s proposed combination would not modify this portion of Inoue’s circuitry, maintaining the reduced power consumption achieved by Inoue’s teachings. *See* Reply 24–25. Thus, the proposed combination does not defeat the intended purpose of Inoue because it

maintains the circuitry that achieves the desired decrease in power consumption.

Second, even if implementing the Inoue-Min-Hamade write control clock for each column as a column write signal as taught in Ogawa caused additional power consumption, an ordinarily skilled artisan may embrace this tradeoff to achieve the benefit of implementing the circuit in a dynamic memory with many memory cells. The test for obviousness is not whether the goals and objectives of every prior art reference can be accomplished by a proposed combination of prior art teachings. Rather, an ordinarily skilled artisan may be motivated to pursue the desirable properties taught by one prior art reference even if that means foregoing the benefits taught by another prior art reference. *See In re Urbanski*, 809 F.3d 1237, 1244 (Fed. Cir. 2016); *see also Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (“[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.”). This is particularly true where, as here, the claims at issue do not require the benefit that is arguably lost in the combination. *See id.* Indeed, a prior art reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect. *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985). The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned, as they are a part of the literature and are relevant for all they contain. *In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) (citing *In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968)).

Thus, we are persuaded that the combination of Inoue, Min, Hamade, and Ogawa discloses “[t]he sense amplifier arrangement according to claim 10 wherein said write control signal is a column write signal” and that an ordinarily skilled artisan would have been motivated to combine the teachings of Inoue, Min, Hamade, and Ogawa as proposed by Petitioner.

On these bases, Petitioner submits that the proposed combination of Inoue, Min, Hamade, and Ogawa discloses claim 11. Petitioner has shown, by a preponderance of the evidence, that (1) the combination of Inoue, Min, Hamade, and Ogawa discloses the subject matter of claim 11 in the arrangement as required by the claim; and (2) Petitioner provides sufficient reasons about why an ordinarily skilled artisan would have combined the teachings of Inoue, Min, Hamade, and Ogawa. Thus, for the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 11 is unpatentable as obvious over Inoue, Min, Hamade, and Ogawa.

3. *Dependent claims 12, 13, and 18*

Claim 13 depends from claim 12, which depends from claim 11. Claim 18 depends from claim 17, which depends indirectly from claim 4. In the Petition, Petitioner accounts for the added limitation of claim 12 relative to base claim 11. Pet. 75. Petitioner also accounts for the added limitation of claim 13 relative to base claim 12. *Id.* at 76. Petitioner also accounts for the added limitation of claim 18 relative to base claim 17. *Id.* at 96–100. Petitioner’s positions regarding claims 12, 13, and 18 are supported by the testimony of Dr. Baker. Ex. 1002 ¶ 157 (claim 12), ¶ 158 (claim 13), ¶¶ 201–208 (claim 18).

Patent Owner has provided no counterargument to Petitioner’s arguments and assertions about the obviousness of claims 12, 13, and 18

over Inoue, Min, Hamade, and Ogawa. We are persuaded that Petitioner has adequately accounted for the limitations added by each of claims 12, 13, and 18, and that Petitioner has shown how the combination satisfies each of the dependent claims. Petitioner has shown, by a preponderance of the evidence, that each of claims 12, 13, and 18 is unpatentable as obvious over Inoue, Min, Hamade, and Ogawa.

III. CONCLUSION

Petitioner has shown, by a preponderance of the evidence, that claims 4–18 and 21–27 are unpatentable under 35 U.S.C. § 103(a) as obvious over Inoue, Min, Hamade, and Ogawa.

IV. ORDER

It is

ORDERED that claims 4–18 and 21–27 of the '574 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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