

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01416
Patent 6,172,554 B1

Before JAMESON LEE, KEVIN F. TURNER, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

TURNER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition for *inter partes* review of claims 1–3, 14–16, 22, and 28–36 of U.S. Patent No. 6,172,554 B1 (Ex. 1001, “the ’554 Patent”). Paper 1 (“Pet.”). We instituted review of all claims 1–3, 14–16, 22, and 28–36 on all grounds asserted in the Petition. Paper 7 (“Dec. on Inst.”). ProMOS Technologies Inc. (“Patent Owner”) filed a Patent Owner Response.¹ Paper 12. In response thereto, Petitioner filed a Reply. Paper 15. Oral hearing was held on August 16, 2018. A copy of the transcript for the oral hearing has been entered as Paper 22.

We determine that Petitioner has shown by a preponderance of the evidence that each of claims 1–3, 14–16, 22, and 28–36 is unpatentable.

A. *Related Matters*

The parties inform us that the challenged patent is the subject of a district court proceeding in the District of Delaware, captioned *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:16-cv-00335-SLR (D. Del.). Pet. 1, Paper 4. In that action, Patent Owner has asserted other patents against Petitioner, and Petitioner has filed *inter partes* review petitions against those other patents in IPR2017-01412, IPR2017-01413, IPR2017-01414, IPR2017-01415, IPR2017-01417, IPR2017-01418, and IPR2017-01419. *Id.*

Petitioner also identifies these *inter partes* review proceedings, initiated by petitions filed by Petitioner, as involving additional patents

¹ Patent Owner also filed a declaration of Mr. Dhaval Brahmbhatt in support of the Patent Owner Response (PO Resp.). Ex. 2001.

asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:15-cv-00898-SLR-SRF (D. Del.): IPR2017-00032; IPR2017-00033; IPR2017-00035; IPR2017-00036; IPR2017-00037; IPR2017-00038; IPR2017-00039; and IPR2017-00040. Pet. 1–2.

B. The '554 Patent

The '554 Patent is titled “Power Supply Insensitive Substrate Bias Voltage Detector Circuit.” Ex. 1001, [54]. The patent issued on January 9, 2001 from an application filed on September 24, 1998. *Id.* at [45], [22]. The patent is directed to “a circuit provid[ing] a bias voltage V1 which is substantially insensitive to variations of a power supply voltage powering the circuit.” *Id.* at Abstract, 1:6.

The '554 Patent discloses that voltage generating circuits known as back-bias generators may be used in semiconductor devices which require the substrate region to be biased to a predetermined voltage, such as in dynamic random access memories (DRAM), where the substrate region is negatively biased to prevent the DRAM cells from losing stored information. Ex. 1001, 1:8–15. Such a back-bias generator includes a voltage multiplier circuit, commonly referred to as charge pump, for providing the negative Back-Bias Voltage (V_{BB}), and usually includes a V_{BB} detector circuit, which regulates the charge pump such that V_{BB} is maintained as close to a target V_{BB} value as possible. *Id.* at 1:15–21. The detector circuit constantly senses the V_{BB} voltage level, and if V_{BB} becomes more negative than the target V_{BB} , the detector circuit turns off the charge pump thereby allowing V_{BB} to drift back to the target V_{BB} ; and if V_{BB} becomes less negative than the target

V_{BB} , the detector circuit turns on the charge pump to pump V_{BB} back to the target V_{BB} . *Id.* at 1:22–28.

A conventional V_{BB} detector circuit 17 is illustrated in Figure 1, reproduced below, along with Figure 3A illustrating an alternative, conventional V_{BB} detector circuit 37.

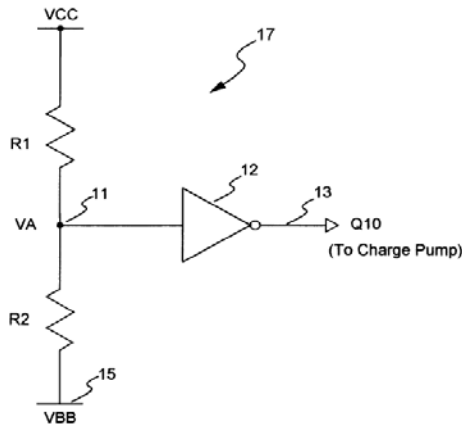


FIG. 1
(Prior Art)

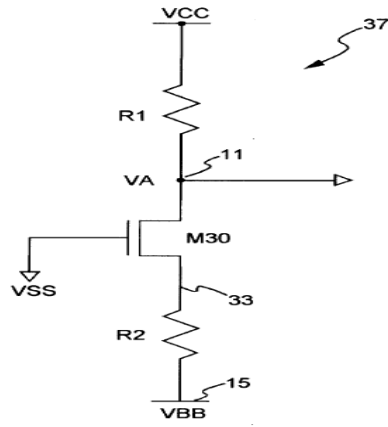


FIG. 3A
(Prior Art)

The conventional V_{BB} detector circuit 17, in Figure 1, has serially connected resistors R1 and R2 coupled between the power supply V_{CC} and V_{BB} terminal 15, where V_{CC} is provided by a power supply external to the device, and V_{BB} is generated internally by a charge pump, which is not shown. *Id.* at 1:29–33. Inverter 12 has its input terminal connected to node 11 which is the node between R1 and R2, and its output connected to the charge pump. *Id.* at 1:33–37.

Resistors R1 and R2 are selected so that the voltage V_A equals the trip point of inverter 12, such that if the charge pump causes V_{BB} to become more negative than the target value, V_A drops below the trip point of inverter 12, causing Q10 to go high. *Id.* at 1:43–49. The high level at Q10 turns off the charge pump, allowing V_{BB} to increase back to the target value. *Id.* Alternatively, if V_{BB} becomes less negative than the target V_{BB} , V_A rises

above the trip point of inverter 12, causing Q10 to go low, which turns on the charge pump causing V_{BB} to become more negative. *Id.* at 1:49–54.

In Figure 3A (not reproduced here), the '554 Patent depicts another prior art detector circuit 37 that prevents V_{BB} from becoming positive. Circuit 37 is identical to circuit 17 of Figure 1 except that NMOS transistor M30 is connected between node 11 and R2, where that transistor causes the charge pump to turn on and pump V_{BB} to a more negative voltage. *Id.* at 2:29–37, Fig. 3A.

The '554 Patent details that the conventional circuits have drawbacks, including that V_{BB} varies with changes to V_{CC} , such that higher voltages can result in increases in junction leakage. *Id.* at 1:55–67. Also, the conventional circuits may not prevent V_{BB} from becoming positive, which can damage the device. *Id.* at 2:23–28. Because of these drawbacks, the '554 Patent discloses embodiments of V_{BB} detector circuits wherein V_{BB} is made insensitive to V_{CC} variations, and also wherein the range of possible V_{BB} values is increased without compromising power consumption. *Id.* at 2:56–59. Figures 4A and 5A are reproduced below:

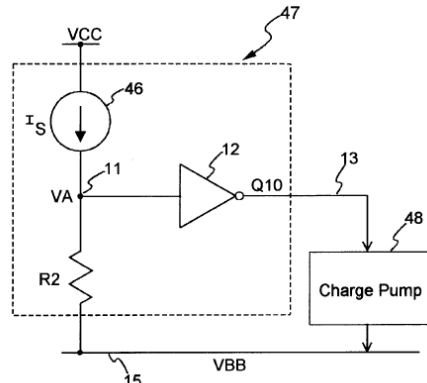


FIG. 4A

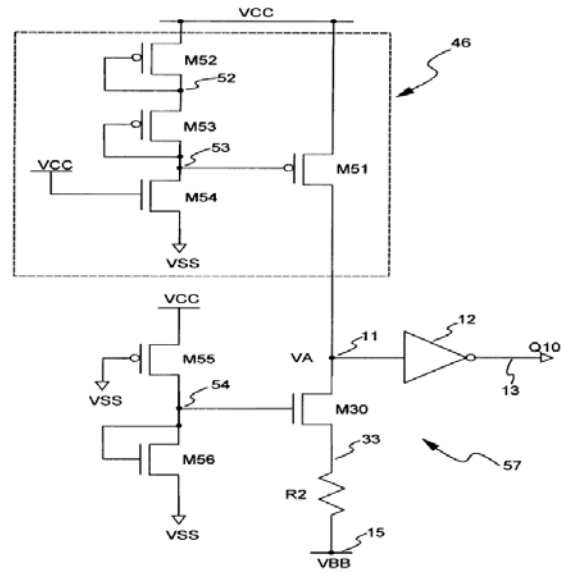


FIG. 5A

Figure 4A shows a voltage detector circuit 47 where the resistor R1 of Figure 1 is replaced with a power-supply-voltage-insensitive current source 46 connected between V_{CC} and node 11. *Id.* at 3:45–57. Resistor R2 is connected between node 11 and V_{BB} terminal 15. *Id.* Inverter 12 has its input terminal connected to node 11 and its output terminal represents the output terminal Q10, which is connected to an input terminal 13 of a charge pump 48. *Id.* Figure 5A illustrates another V_{BB} detector circuit 57 with transistors M51, M52, M53, and M54 collectively implementing a constant current source 46. *Id.* at 4:18–21.

C. Illustrative Claims

Petitioner challenges claims 1–3, 14–16, 22, and 28–36 of the '554 Patent, of which claims 1, 15, 22, and 30 are independent. Pet. 1. Claims 1 and 22 are illustrative of the subject matter of the challenged claims and read as follows:

1. A circuit for providing a bias voltage V1 which is substantially insensitive to variations of a power supply voltage powering the circuit, the circuit comprising:

a detector circuit for generating a signal from the power supply voltage and the bias voltage V1, wherein said signal is substantially insensitive to variations in the power supply voltage while being responsive to the bias voltage V1; and

a voltage generator for generating the bias voltage V1 on an output terminal, wherein the voltage generator is responsive to said signal such that the detector circuit and the voltage generator are operable to maintain the bias voltage V1 at a substantially constant value over power supply voltage variations;

wherein the detector circuit comprises:

a bias circuit for biasing a first node to a node voltage, the bias circuit receiving the power supply voltage and the bias voltage V1; and

a sensing circuit for generating said signal in response to the node voltage at the first node;

wherein the power supply voltage is provided across a power supply terminal and a reference terminal, and the bias circuit comprises:

a current source connected between the power supply terminal and the first node, the current source being substantially insensitive to power supply voltage variations; and

a resistor connected between the first node and the output terminal of the voltage generator circuit;

wherein the current source comprises a first transistor connected between the power supply terminal and the first node, the first transistor being biased such that a current through the first transistor is substantially insensitive to power supply voltage variations;

wherein the gate to source voltage of the first transistor is made substantially insensitive to power supply voltage variations;

wherein the first transistor is a field effect transistor biased in the saturation mode;

wherein the sensing circuit comprises an inverter having an input terminal connected to the first node, the inverter possessing a trip point which is substantially insensitive to power supply voltage variations, whereby the bias voltage V1 is obtained when the node voltage and the trip point of the inverter are substantially the same.

22. A circuit comprising:

a voltage generator for generating a bias voltage V1; and

a detector circuit for detecting the bias voltage V1 and regulating the voltage generator to maintain the bias voltage V1 at a substantially constant negative level, the detector circuit allowing the bias voltage V1 to get arbitrarily close to the ground voltage but not allowing the bias voltage V1 to become positive.

Ex. 1001, 6:23–7:3, 8:67–9:7.

D. Instituted Grounds of Unpatentability

We instituted a trial based on the asserted grounds of unpatentability (“grounds”) set forth in the table below, relying on the declaration testimony of Dr. R. Jacob Baker (Ex. 1002). Dec. on Inst. 29.

Reference(s)	Basis	Challenged Claim(s)
Ito ²	§ 102(e)	22
Ito and Kim ³	§ 103	28 and 29
Park ⁴ and Baker ⁵	§ 103	1–3, 14–16, 30, 31, and 36
Park, Baker, and Tsukada ⁶	§ 103	32–34
Park, Baker, and Young ⁷	§ 103	35

II. ANALYSIS

A. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference.

Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1369 (Fed. Cir. 2008);

Karsten Mfg. Corp. v. Cleveland Golf Co., 242 F.3d 1376, 1383 (Fed. Cir.

2001). While the elements must be arranged in the same way as is recited in

² U.S. Patent No. 5,744,998, filed Dec. 3, 1996, issued Apr. 28, 1998 (Ex. 1005, “Ito”).

³ U.S. Patent No. 5,602,506, issued Feb. 11, 1997 (Ex. 1006, “Kim”).

⁴ U.S. Patent No. 5,886,567, filed July 9, 1997, issued Mar. 23, 1999 (Ex. 1007, “Park”).

⁵ R. Jacob Baker et al., CMOS Circuit Design, Layout, and Simulation, (Stuart K. Tewksbury ed., IEEE Press 1997) (Ex. 1008, “Baker”).

⁶ U.S. Patent No. 5,818,290, filed Feb. 14, 1996, issued Oct. 6, 1998 (Ex. 1009, “Tsukada”).

⁷ U.S. Patent No. 4,710,647, issued Dec. 1, 1987 (Ex. 1012, “Young”).

the claim, “the reference need not satisfy an *ipsissimis verbis* test.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990)). Thus, identity of terminology between the prior art reference and the claim is not required. “A reference anticipates a claim if it discloses the claimed invention ‘such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.’” *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995). That means prior art references must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Also, “it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁸ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Consideration of the *Graham* factors “helps inform the ultimate obviousness

⁸ We note that neither party has submitted or discussed secondary considerations with respect to any obviousness ground.

determination.” *Apple v. Samsung Elecs. Co.*, 839 F.3d 1034, 1048 (Fed. Cir. 2016) (en banc), *cert. denied*, 2017 WL 948834 (U.S. Nov. 6, 2017).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

Thus, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. We analyze the challenges presented in the Petition in accordance with the above-stated principles.

B. Level of Ordinary Skill

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner proposes that a person of ordinary skill in the art at the time of the alleged invention of the ’554 Patent would have had “at least a

bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design.” Pet. 5–6 (citing Ex. 1002 ¶ 20). Patent Owner does not address the level of ordinary skill in its Patent Owner Response, but its declarant, Mr. Brahmhatt, indicates that he has adopted and applied Petitioner's level of ordinary skill in the art for purposes of his testimony. See Ex. 2001 ¶ 23.

Based on the current record, we are concerned that Petitioner's articulation contains no upper bounds, i.e., “at least a bachelor's degree,” such that the level of ordinary skill proposed by Petitioner is not sufficiently specific. As such, we adopt the definition provided by Petitioner with minor variations: “a person having ordinary skill in the relevant art at the time of invention is a person with a Bachelor's of Science degree in electrical engineering or a similar field, and two to three years of experience in integrated circuit design.”

Additionally, we determine that the level of ordinary skill in the art is reflected by the prior art of record. See *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Claim Construction

Petitioner pointed out that the '554 Patent was set to expire on “September 24, 2018, i.e., during the pendency of the instituted proceeding” and contends that the challenged claims should be construed under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Pet. 10. We agree and determine that the instant patent expired on that date. Under the *Phillips* standard, claim terms are given their ordinary and customary meanings, as would be understood by a person of

ordinary skill in the art, having taken into consideration the language of the claims, the specification, and the prosecution history of record.

In the Decision on Institution, we acknowledged that Petitioner did not propose an express construction for any claim terms. Dec. on Inst. 12 (citing Pet. 11). In its Response, Patent Owner likewise does not propose explicit claim constructions for any claim terms, and its declarant, Mr. Brahmbhatt, indicates that he has assumed “that the claim terms have their ordinary customary meaning and that there are no specific constructions that I am to apply.” See PO Resp.; Ex. 2001 ¶ 24. As such, we determine that no claim terms require express construction and we apply the ordinary and customary meanings for all claim terms, as would have been understood by a person of ordinary skill in the art.

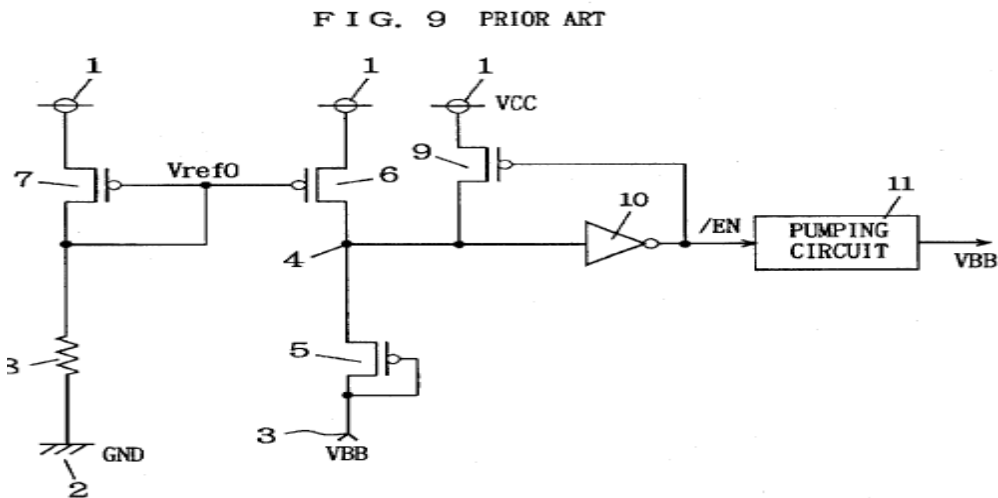
D. Anticipation by Ito

Petitioner contends that claim 22 is unpatentable under 35 U.S.C. § 102(e) as anticipated by Ito. Pet. 3, 12–18. Relying in part on the testimony of Dr. Baker and numerous citations to the reference, Petitioner explains how Ito discloses all of the claim limitations. *Id.* at 12–18. Patent Owner disputes these contentions and raises specific arguments that Ito fails to teach all of the elements of independent claim 22. PO Resp. 7–11. We first review Ito, discuss Petitioner’s contentions with respect to the claim, and consider Patent Owner’s counter-arguments.

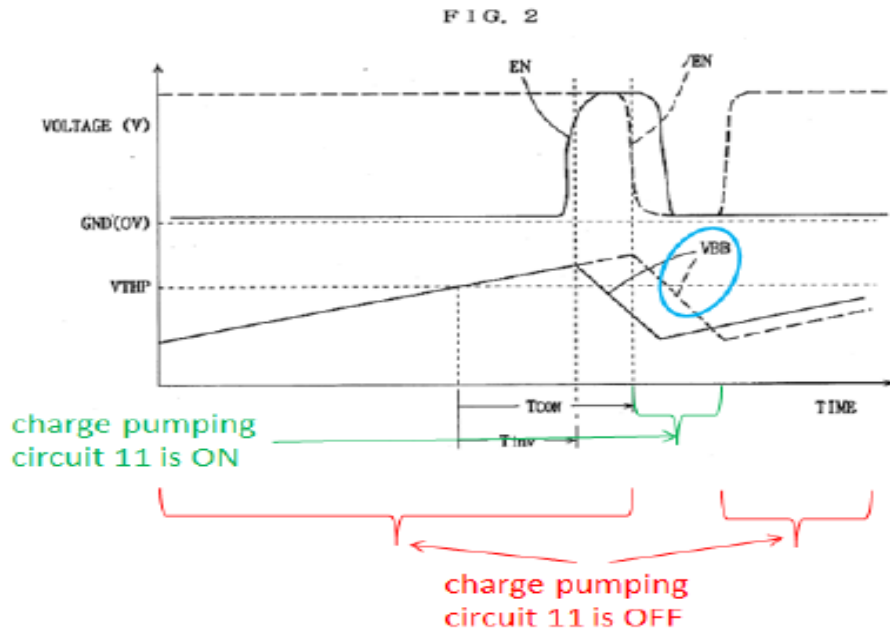
1. Disclosure of Ito

Ito relates to a substrate voltage detecting circuit for detecting a substrate voltage in a semiconductor memory device, such as a DRAM, and activating a substrate voltage generation circuit. Ex. 1005, 1:6–12. An

embodiment of that substrate voltage detecting circuit is illustrated in Figure 9, reproduced below:



Ito describes that its charge pumping circuit 11 generates a negative substrate voltage VBB that is supplied to the semiconductor substrate. *Id.* at 1:15–22. The substrate voltage detecting circuit is connected to charge pumping circuit 11 in order to retain the substrate voltage VBB at a prescribed level.” *Id.* at 1:15–22, Fig. 9. When VBB is detected as more negative than the negative threshold voltage of PMOS transistor 5, the enable signal (/EN) is generated high such that the charge pumping circuit is off. *Id.* at 1:38–45. When VBB is detected as higher than the threshold voltage VTHP, the /EN signal is generated low such that the charge pumping circuit is turned on to pull VBB more negative. *Id.* at 1:50–57. This behavior of the circuit is illustrated in Figure 2 of Ito, reproduced below, with Petitioner’s annotations:



Pet. 15 (citing Ex. 1005, Fig. 2). In this annotated version of Ito's Figure 2, Petitioner shows VBB in blue, and ON and OFF time periods for charge pumping circuit 11 corresponding to dotted line VBB in green and red, respectively. *Id.*

2. Petitioner's Contentions Regarding Claim 22

With respect to independent claim 22, Petitioner addresses the disclosure of Ito, as discussed above. Pet. 12–18. Petitioner also contends that certain elements of claim 22 are equivalent to portions of Ito. *Id.* We discuss each in turn below.

Petitioner asserts that a person of ordinary skill in the art would have understood that VBB refers to a back bias voltage, where that voltage is supplied to the semiconductor substrate. *Id.* at 13 (citing Ex. 1002 ¶ 69). We determine that this is correct based on the background disclosure in the '554 Patent, discussed above. Petitioner also asserts that because VBB is maintained at a "prescribed level" below a negative VTHP, Ito discloses

maintaining VBB “at a substantially constant negative level,” as claimed. *Id.* at 16–17 (citing Ex. 1005, 1:15-21, 29; Ex. 1002 ¶ 76).

Additionally, Petitioner asserts that, as shown in the annotated Figure 2 of Ito, the dotted line version of VBB, which corresponds to the prior art noted in Ito, becomes less negative (closer to 0V) than the threshold voltage V_{THP} , thus the detector circuit allows substrate voltage VBB to get arbitrarily close to the level indicated in Figure 2 as “GND (0V),” without allowing the voltage to become positive. *Id.* at 17–18 (citing Ex. 1005, Fig. 2; Ex. 1002 ¶ 77). We determine that Petitioner’s interpretations of Ito are persuasive.

3. *Patent Owner’s Arguments Regarding Claim 22*

Patent Owner argues that claim 22 is not anticipated by Ito because Ito does not teach a detector circuit “allowing the bias voltage V_1 to get arbitrarily close to the ground voltage.” PO Resp. 7–11. Patent Owner argues that claim 22 was allowed over “Applicants’ prior art Fig. 3A,” and Figure 9 of Ito, relied upon in the ground of unpatentability, is identical, in relevant portion, to that prior art figure and suffers from the same problem. *Id.* at 7–9 (citing Ex. 1001, Fig. 3A; Ex. 1004, 81–82, 86–87; Ex. 1005, Fig. 9). Patent Owner also argues that the ’554 Patent “improved upon and disclaimed” the prior art illustrated in Figures 3A and 3B of the ’554 Patent. *Id.* at 10.

Patent Owner also argues that behavior of the circuit illustrated in Figure 2 of Ito occurs only because of delay in the circuit, and “is not a design for getting ‘arbitrarily close to the ground voltage.’” PO Resp. 10–11 (citing Ex. 2003, 20:16–21:5; Ex. 2001 ¶¶ 27–31, 44–47). Patent Owner also argues that such a delay would exist in any detector circuit, including

the circuit in prior art Figure 3A, and Ito states that this delay is undesirable and counter to the purposes of Ito to reduce delay. *Id.* at 11 (citing Ex. 1005, 2:5–10, 2:13–15, 5:15–17; Ex. 2003, 24:18–21, 25:10–17).

Petitioner replies that Patent Owner does not dispute that Ito discloses all of the features of claim 22, save one, and that the evidence demonstrates that Ito discloses that feature. Pet. Reply 3. Petitioner points out, as discussed above, that Figure 2 of Ito shows that the peak of VBB is less negative than threshold voltage VTHP and “arbitrarily close to the ground voltage,” such that Patent Owner cannot contest that Ito’s detector meets the limitations of claim 22. *Id.* at 4–5. Petitioner also argues that claim 22 does not recite that “the designed target value of VBB to be close to 0V,” but rather recites that the bias voltage is allowed to get arbitrarily close to ground. *Id.* at 6 (citing PO Resp. 8). Petitioner also argue that why or how VBB, in Ito, gets closer to ground than the threshold voltage “is irrelevant to the anticipation analysis.” *Id.* at 7–8. Petitioner also distinguishes Ito from the prior art Figures 3A and 3B of the ’554 Patent. *Id.* at 8–11.

We agree with Petitioner. Although Patent Owner cites to the testimony of its declarant, Mr. Brahmhatt, we do not find persuasive his testimony that the “claim element requiring the bias voltage to be ‘arbitrarily close to the ground voltage’ is not met by the Ito design which unintentionally, uncontrollably, and undesirably (per Ito) rises above – VTHP.” The intent, control, and desirability of the detector’s function in Ito is irrelevant to anticipation. *See State Contracting & Eng’g Corp. v. Condotte America, Inc.*, 346 F.3d 1057, 1068 (Fed. Cir. 2003) (A reference may be directed to an entirely different problem than the one addressed by the inventor and still be anticipatory); *Celeritas Technologies Ltd. v.*

Rockwell Intern. Corp., 150 F.3d 1354, 1361 (Fed. Cir. 1998) (Prior art that teaches away from the claimed invention can anticipate the claims based on what it discloses). Based on the disclosed function of the detector circuit in Ito, we determine that it meets the limitations recited in claim 22.

Additionally, Petitioner points out differences between the prior art Figures 3A and 3B of the '554 Patent and the detector circuit of Ito (Pet. Reply 8 n.2), and argues that Patent Owner's arguments before the Examiner are also distinguishable. *Id.* at 8–9. Petitioner points out that Patent Owner argued during prosecution of the instant patent that “M30 also prevents VBB from becoming closer to 0V than the threshold voltage V_{TN} of transistor M30 [per Fig. 3A],” which is distinguishable from Ito, because VBB crosses the transistor threshold voltage in Ito. *Id.* at 9–10 (citing Ex. 1004, 81–82; Ex. 1005, Fig. 2). In other words, in the acknowledged prior art, the dynamic range of VBB was limited to $-V_{TN}$ at the top end (see Ex. 1001, Fig. 3B), whereas the demonstrated functioning of the detector in Ito has no such apparent limit. *Id.* As such, we agree with Petitioner that any disclaimer of Figures 3A and 3B, in the context of the prosecution of claim 22, would not necessarily be effective in distinguishing claim 22 from Ito.

4. Conclusion

We have reviewed Petitioner's explanations and supporting evidence as to how Ito teaches all of the elements of claim 22, and we agree with Petitioner's analysis and we do not agree with Patent Owner's arguments. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the subject matter of claim 22 is anticipated by Ito.

E. Obviousness over Ito and Kim

Petitioner contends that claims 28 and 29 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ito and Kim. Pet. 3, 18–23. Petitioner, relying on citations to the references and declaration testimony of Dr. Baker, sets forth how the references purportedly would have conveyed the claim limitations and provides purported reasoning for combining the teachings of the references. *Id.* at 18–23. Patent Owner does not specifically raise arguments against this ground, other than the prior arguments raised against Ito in the anticipation ground. *See* PO Resp. 11–12.

Claims 28 and 29 further recite that the bias voltage V1 biases a P-type region, forming a junction with an N-type region, and making the junction reversed biased, and that the circuit is a DRAM device, respectively, with claim 29 dependent on claim 28. Ex. 1001, 9:31–36. As discussed above, Ito discloses its substrate voltage detecting circuit for use with a DRAM device. Petitioner acknowledges that Ito does not provide express details about biasing junctions, but asserts that Kim discloses biasing in the general context of a memory device. Pet. 18–19.

Kim discloses a back bias voltage generator for generating a back bias voltage (VBB) having a constant level, where that voltage is applied to the substrate of a memory device. Ex. 1006, 1:6–12, 4:6–15. Kim illustrates that memory devices include transistors, with each transistor having a P-type substrate to which the back bias voltage VBB is applied, and being in contact with “N+ diffusion region having a drain for inputting the voltage Vpp.” *Id.* at Fig. 6, 4:6–15.

Petitioner alleges that it would have been obvious for one of ordinary skill in the art to have used Ito’s substrate voltage VBB to reverse bias the

junction of Kim. Pet. 20–21. Petitioner asserts that one of ordinary skill in the art would have been motivated to make this combination because both references are directed to generating back bias voltages, both references disclose using such a back bias voltage to bias the substrate for a memory device, and the person of ordinary skill would have known to include transistors, as illustrated in Kim, in DRAM devices, as described in Ito. *Id.* Petitioner makes additional arguments applying the obviousness legal principles from *KSR*. *Id.* at 22.

In its Patent Owner Response, Patent Owner does not address separately whether the combined teachings of the references account for the limitations recited in dependent claims 28 and 29. *See* PO Resp. 11–12. Instead, Patent Owner argues that Kim does not cure the deficiencies of Ito. *Id.* As discussed above, however, we do not agree with Patent Owner’s arguments against the anticipation of claim 22 by Ito.

We have reviewed Petitioner’s explanations and supporting evidence as to how the proffered combination teaches the limitations of claims 28 and 29, as well as its explanations as to how one of ordinary skill in the art would have combined Ito and Kim, and we agree with Petitioner’s analysis. *See* Pet. 18–23. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the subject matter of dependent claims 28 and 29 would have been obvious over the combined teachings of Ito and Kim.

F. Obviousness over Park and Baker

Petitioner contends that claims 1–3, 14–16, 30, 31, and 36 are unpatentable under 35 U.S.C. § 103(a) as obvious over Park and Baker. Pet. 3, 23–73. Petitioner, relying on citations to the references and declaration testimony of Dr. Baker, sets forth how the references would have

conveyed the claim limitations and provides reasoning for combining the teachings of the references. *Id.* at 23–73. Patent Owner disputes these contentions and raises specific arguments that the combination of Park and Baker fails to teach or suggest all of the elements of claims 1–3, 14–16, 30, 31, and 36. PO Resp. 12–18. We first review the cited references, discuss Petitioner’s contentions with respect to the subject claims, and consider Patent Owner’s counter-arguments.

1. *Disclosure of Park*

Park is directed to a back bias voltage level detector. Ex. 1007, Abstract. The back bias voltage level detector generates oscillator enable signal OSCEN, such that when OSCEN becomes a high, back bias voltage oscillator 2, as shown in Figure 1, outputs pulse OSC, and OSC is inputted to back bias voltage pump 3, which in turn generates the back bias voltage V_{BB} . *Id.* at 4:58–5:45, 5:26–28, 40–45, Fig. 1. A block diagram of a conventional back bias voltage generator and a circuit diagram of the back bias voltage level detector are illustrated in Figures 1 and 5, respectively, reproduced below:

FIG. 1
CONVENTIONAL ART

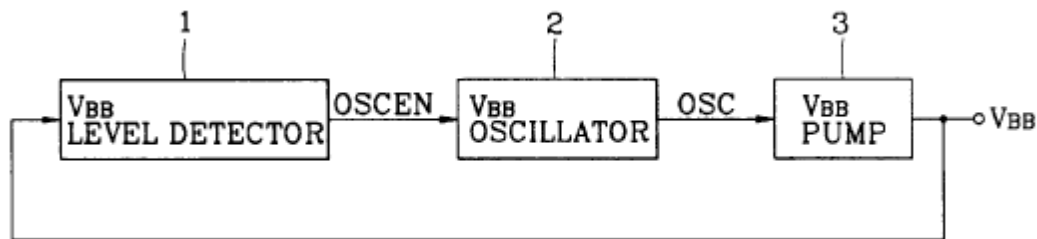


FIG. 5

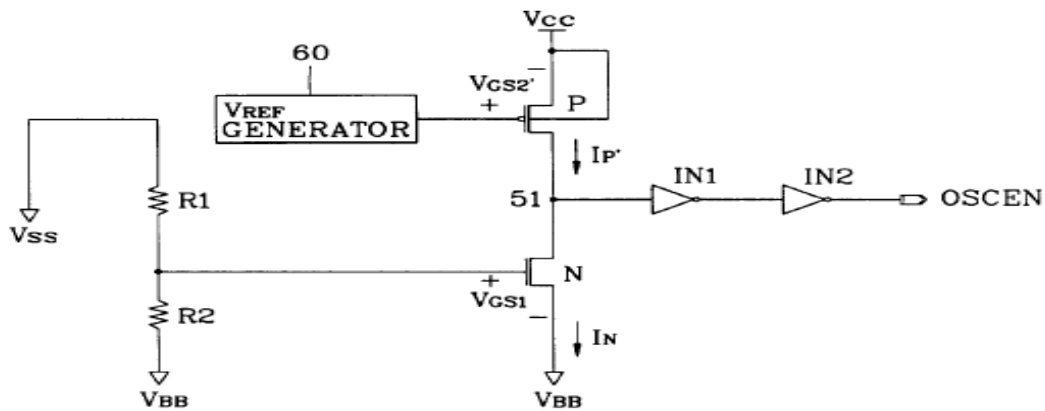


Figure 1 of Park depicts a block diagram of a conventional back bias voltage generator and Figure 5, depicts a circuit diagram of the back bias voltage level detector. Park discloses that signal OSCEN is generated from a current $I_{p'}$ supplied by V_{CC} through transistor P. *Id.* at 4:58–5:45, Fig. 5. Park also discloses that when the absolute value of the back bias voltage V_{BB} is increased, node 51 becomes low, which is in turn used by inverter IN1 to generate a high or low output. *Id.* at 5:33–39, Fig. 5. Park also discloses that “[s]ince the difference $V_{CC}-V_{REF}$ is constant, it is possible to obtain constant current $I_{p'}$ irrespective of the external voltage V_{CC} .” *Id.* at 5:12–14. Similarly, current I_N is also substantially insensitive to variations in V_{CC} because I_N depends on V_{GS1} , which is the difference between the gate voltage of NMOS pull-down transistor N and V_{BB} . *Id.* at 5:18–20, Fig. 5. Park also discloses that the gate to source voltage V_{GS2} of the PMOS pull-up transistor P is made substantially insensitive to variations in the external voltage V_{CC} . *Id.* at 4:60, 4:66–5:4, Fig. 5.

Park’s back bias voltage level detector includes reference voltage generator 60, PMOS pull-up transistor P, resistor divider R1/R2, and NMOS pull-down transistor N for biasing node 51 to a voltage. *Id.* at 4:66–5:39,

Fig. 5. Inverters IN1 and IN2 generate the oscillation enable signal OSCEN in response to the node voltage at node 51. *Id.* at 5:24–27, 5:39–41, Fig. 5. V_{CC} supplies power to the reference voltage generator 60 across from ground voltage V_{SS} . *Id.* at 4:46–47, Fig. 6.

Figure 8 of Park is reproduced below:

FIG. 8

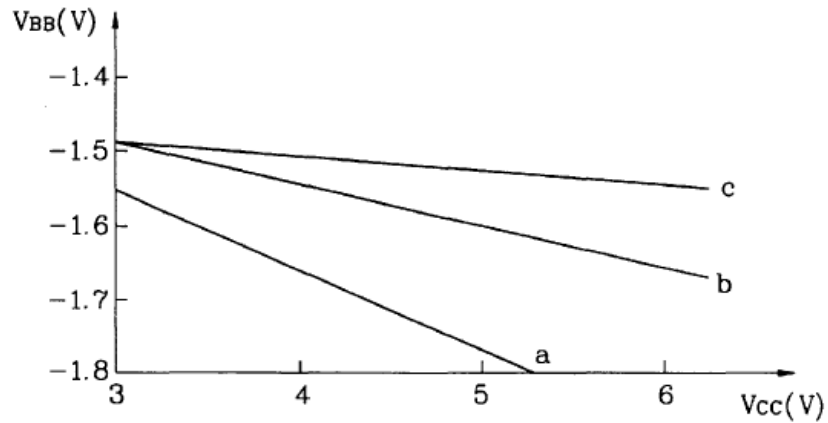


Figure 8 depicts a graph of the output of V_{BB} versus V_{CC} . Park discloses that output c of Figure 8 has more stable back bias voltage, V_{BB} , level with respect to the variation of the external voltage V_{CC} “compared to the conventional circuits.” *Id.* at 5:12–14, 6:32–35. Park also discloses that “even if the external voltage V_{CC} is varied . . . the back bias voltage V_{BB} is stable.” *Id.* at 6:39–42.

2. Disclosure of Baker

Baker is a textbook directed to CMOS circuit design and layout. Ex. 1008. Baker discusses the functions of inverters and details regarding the trip point of an inverter, referred to as a “switching point.” *Id.* at 204–05. Figure 11.1 of Baker is reproduced below:

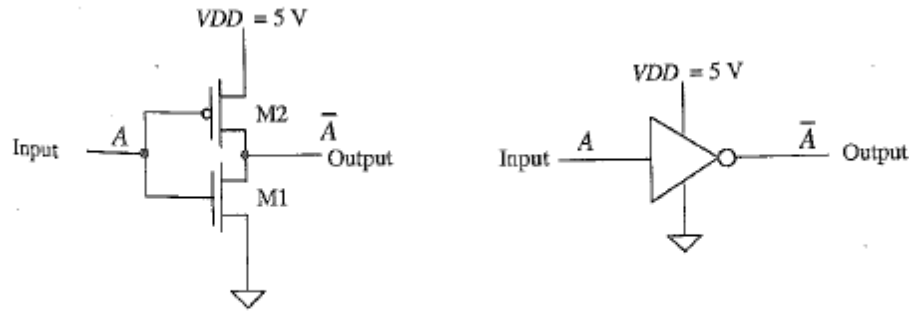


Figure 11.1 The CMOS inverter, schematic, and logic symbol.

Id. at 201. Figure 11.1 of Baker depicts the CMOS inverter schematic and its symbol logic. Transistors M1 and M2 are a PMOS “pull up transistor” and an NMOS “pull down transistor,” respectively. *Id.* at 151, 201. As illustrated, the source of transistor M1 is connected to ground and its drain is connected to a node labeled “Output.” *Id.* at Fig. 11.1. Transistor M2 has its drain connected to the output node and the drain of transistor M1, in effect coupling the transistors. See Ex. 1002 ¶ 192.

Baker also discloses the following equation (11.4) for the switching point of an inverter comprising an NMOS transistor and a PMOS transistor:

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

where β_n and β_p are transconductance parameters of the NMOS and PMOS transistors, respectively, in the inverter, V_{THN} and V_{THP} are threshold voltages of the NMOS and PMOS transistors, respectively, and VDD is the power supply voltage. Ex. 1008, 205.

3. *Petitioner's Contentions Regarding Claims 1, 15, and 30*

With respect to independent claims 1, 15, and 30, Petitioner addresses the disclosures of Park and Baker, as discussed above. Pet. 23–52, 57–70. Petitioner also contends that certain aspects of claims 1, 15, and 30 are obvious over the cited references and proffers motivation to combine the references. *Id.* We discuss each independent claim in turn below.

With respect to claim 1, Petitioner asserts that a person of ordinary skill in the art would have recognized that while the OSCEN signal in the circuit of Figure 5 of Park is quite insensitive to power supply variations, the switching or “trip” point of inverter IN1 is a factor that could contribute to some power supply sensitivity for OSCEN. *Id.* at 30 (citing Ex. 1002 ¶¶ 98–103). Petitioner acknowledges that Park does not disclose that the “trip” point of inverter IN1 is substantially insensitive to variations in V_{CC} , but cites to Baker based on details provided regarding inverters, discussed above. *Id.* at 30–31. Based on Baker’s equation 11.4, Petitioner asserts that a person of ordinary skill in the art would have recognized that the trip point will be “substantially insensitive” to variations in V_{DD} if β_n is set much larger than β_p by sizing the NMOS and PMOS transistors of the inverter suitably, which was a task allegedly within the capability and skill of an ordinary artisan at the time of the invention. *Id.* at 31–32 (citing Ex. 1002 ¶¶ 108–109). Petitioner asserts that in view of Baker, one of ordinary skill in the art would have been motivated to configure Park’s circuit to have its trip point be substantially insensitive to power supply voltage variations, in keeping with Park’s overall objective of “constantly maintaining a back bias voltage with respect to the variation of an external voltage.” *Id.* at 32 (quoting Ex. 1007, 3:45–57; Ex. 1002 ¶ 110). Petitioner raises additional

reasons to combine Park and Baker. *Id.* at 32–34. Notwithstanding Patent Owner’s arguments, discussed below, we determine that Petitioner has demonstrated that it would have been obvious to optimize Park’s circuit based on the teachings of Baker.

Petitioner also asserts that a person of ordinary skill in the art would have understood that the external voltage V_{CC} in Park is provided across the V_{CC} terminal and V_{SS} terminal because the external voltage V_{CC} can be measured across the V_{CC} terminal and V_{SS} terminal. *Id.* at 41 (citing Ex. 1002 ¶ 124). In addition, Petitioner alleges that in the context of “a resistor connected between the first node and the output terminal of the voltage generator circuit,” recited in claim 1, a person of ordinary skill in the art would have understood that the NMOS pull-down transistor N of Park acts as a resistor between node 51 and the back bias voltage V_{BB} . *Id.* at 46 (citing Ex. 1002 ¶ 131; Ex. 1001, 3:50–51). Notwithstanding Patent Owner’s arguments, discussed below, we determine that the various inferences and creative steps noted by Petitioner with respect to Park and Baker would have been within the understanding of persons of ordinary skill in the art.

Claim 1 also recites that “the first transistor is a field effect transistor biased in the saturation mode.” Petitioner argues that a person of ordinary skill in the art would have understood that for a constant current I_P provided by PMOS pull-up transistor P, in Park, transistor P is biased in the saturation mode based on the disclosure of Baker. *Id.* at 48–49 (citing Ex. 1002 ¶¶ 137–138; Ex. 1008, 96). Notwithstanding Patent Owner’s arguments, discussed below, we determine that Petitioner has demonstrated that this

would have been within the understanding of persons of ordinary skill in the art.

With respect to independent claim 15, Petitioner generally relies on its discussion of claim 1 in view of Park and Baker. Pet. 57–62. Petitioner emphasizes that a person of ordinary skill in the art would have understood that Park discloses generating signal OSCEN “on an output terminal” of the back bias voltage level detector. *Id.* at 59 (citing Ex. 1002 ¶ 156; Ex. 1007, Fig. 5). Additionally, claim 15 recites “preventing the bias voltage V1 from exceeding a predesignated voltage.” Petitioner argues that a person of ordinary skill in the art would have understood that

the back bias voltage V_{BB} at which ‘node 51 becomes the high electric potential’ is at or near the maximum voltage to which V_{BB} can rise, because once V_{BB} reaches the voltage at which node 51 becomes a ‘high’ voltage, OSCEN becomes a high electric potential and voltage pump 3 begins to start pumping negative charge to the substrate to decrease V_{BB} .

Id. at 60–61 (citing Ex. 1002 ¶ 156; Ex. 1007, 5:18–32). Notwithstanding Patent Owner’s arguments, discussed below, we determine that Petitioner has demonstrated that this would have been within the understanding of persons of ordinary skill in the art.

With respect to claim 30, that claim additionally requires an “integrated circuit” comprising the circuit C1, the integrated circuit comprising a semiconductor region, and the bias voltage V1 provided by the circuit C1 biases the semiconductor region. Petitioner argues that a person of ordinary skill in the art would have understood that Park’s voltage pump biases the substrate, and that an integrated circuit is formed on semiconductor material such as the substrate. *Id.* at 64 (citing Ex. 1002 ¶¶ 171–173). Additionally, Petitioner argues that a person of ordinary skill

in the art would have understood based on the disclosure of Park that “the back bias voltage oscillator 2 and back bias voltage pump 3 (collectively, ‘voltage generator’) turn on and off in response to an output signal of inverter IN1 (‘inverter’). *Id.* at 70 (citing Ex. 1002 ¶ 187). Notwithstanding Patent Owner’s arguments, discussed below, we determine that Petitioner has demonstrated that this would have been within the understanding of persons of ordinary skill in the art.

4. *Patent Owner’s Arguments Regarding Claims 1, 15, and 30*

Patent Owner argues that the independent claims recite a “trip point which is substantially insensitive to power supply variations,” which is taught by neither Park nor Baker. PO Resp. 12–16. Patent Owner points out that the Specification of the ’554 Patent details that this requires a non-standard inverter design that achieves an unbalanced output. *Id.* at 12–13 (citing Ex. 1001, 4:7–17, 5:10–18; Ex. 2001 ¶¶ 40–42, 48–51). Patent Owner continues that Petitioner relies on Baker to adjust values to obtain the proper range of switching point values, but “nothing in . . . Baker . . . tells a person of skill in the art to select the specific values necessary to provide the claims structure.” *Id.* at 13 (citing Ex. 2001 ¶¶ 40–42, 48–51). Because of this, Patent Owner argues that Petitioner relies solely on “common sense” for one of ordinary skill in the art to manipulate Baker’s formula to meet the claim limitation, which is insufficient to meet its burden. *Id.* at 14–15 (citing Pet. 30–34).

Patent Owner also notes that, during the deposition of Dr. Baker, he referenced a homework problem in Baker as support for his analysis. PO Resp. 14 n.1 (citing Ex. 2003, 62:22–63:3). Patent Owner argues that we should disregard this disclosure as it was not included in the Petition, and

because the homework problem does not suggest to one of ordinary skill in the art to modify the trip point in order to make the inverter substantially insensitive to power supply voltage variations. *Id.* Instead, Patent Owner contends the problem merely asks students to design an inverter having arbitrary transistor values, without explaining the significance of doing so or that the result would affect the output's sensitivity to varying power supply voltages. *Id.* (citing Ex. 2001 ¶¶ 42, 51).

Petitioner replies that Patent Owner is only considering the references individually, and Baker, through its homework problem, describes “an inverter with V_{SP} approximately equal to V_{THN} ,” which is an inverter having a trip point that is substantially insensitive to power supply variations. Pet. Reply 11–12 (citing Ex. 1002 ¶ 108; Ex. 1008, 229). Petitioner points out that Patent Owner's declarant, Mr. Brahnhatt, has acknowledged that when the “ V_{SP} ” of an inverter is approximately equal to “ V_{THN} ,” the trip point of the inverter is substantially insensitive to power supply variations. *Id.* at 12 (citing Ex. 1015, 37:15–21, 67:25–68:6). Petitioner also identifies that the homework problem of Baker was cited in Dr. Baker's declaration, which was cited in the Petition. *Id.* at 13 (citing Ex. 1002 ¶ 108; Pet. 32). As such, we do not agree with Patent Owner that the homework problem of Baker should be disregarded. See PO Resp. 14 n.1. Petitioner also argues that Patent Owner has failed to address the “extensive evidence submitted by Petitioner demonstrating that a [person of ordinary skill in the art] would have been motivated to” modify Park's inverter such that it has a stable trip point. *Id.* at 14–15.

We agree with Petitioner. We determine that Petitioner, in the Petition, explained that one of ordinary skill in the art would have

understood that the trip point would be substantially insensitive to variations in VDD based on the parameters set in Baker. *See* Pet. 31–32. The Petitioner and Dr. Baker provide a reasoned explanation for why the subject limitation, i.e., a “trip point which is substantially insensitive to power supply variations,” is disclosed and suggested by Baker, and why one would have been motivated to configure the inverter in Park to have a stable trip point, per Baker. *Id.* Further, we reaffirm our determination that one of ordinary skill in the art would have been motivated to configure Park’s circuit to have its trip point be substantially insensitive to power supply voltage variations, in keeping with Park’s overall objective of “constantly maintaining a back bias voltage with respect to the variation of an external voltage.” Dec. on Inst. 21–22 (citing Pet. 32; Ex. 1007, 3:45–57; Ex. 1002 ¶ 110).

We further agree with Petitioner that Patent Owner’s assertions—that the Specification of the ’554 Patent is designed to achieve an unbalanced output and present a unique circuit design—rely wholly on the testimony of Mr. Brahmhatt, who does not identify the location of these alleged teachings in ’554 Patent. Pet. Reply 14. Although the testimony of Mr. Brahmhatt details what “typical inverter design” dictates (Ex. 2001 ¶¶ 42, 48), we are not persuaded that the ’554 Patent explicitly discloses a design to achieve an unbalanced output or a design which is “unique;” a detector circuit with VBB being insensitive to VCC variations is discussed, but its uniqueness or unbalanced output are not discussed. *See* Ex. 1001 2:39–4:21. Additionally, even if such a design is conveyed in the disclosure, that does not mean it must be read into any claim that does not require it.

Further, we also disagree with Patent Owner that Petitioner relies solely on “common sense” for one of ordinary skill in the art to manipulate Baker’s formula to meet the claim limitation. *See* PO Resp. 14–15. As discussed above, we determine that Baker, through its homework problem, describes “an inverter with V_{SP} approximately equal to V_{THN} ,” which is an inverter having a trip point that is substantially insensitive to power supply variations. We determine that not all material relied on by expert must be expressly identified and discussed in the Petition itself. We further determine that it is sufficient that the testimony of the expert, cited by Petitioner, relies on it. Given the explicit disclosure in Baker, and the motivation to incorporate the parameters of Baker into Park, we determine that Petitioner relies on more than mere common sense for the combination of Park and Baker. *See* Pet. 31–32.

With respect to independent claims 1 and 15, Patent Owner also argues that those independent claims require that the bias voltage be “substantially insensitive” to power supply variations, which is not taught or suggested by Park or Baker. PO Resp. 16. Patent Owner points to Figure 8 of Park, specifically “line c,” that Patent Owner argues has a slope, which “reflects a dependence of VBB on VCC voltage variations. *Id.* at 17 (citing Ex. 2001 ¶¶ 37–38, 52–54).

Petitioner replies that independent claims 1 and 15 “do not require the bias voltage to be ‘completely insensitive’ to power supply voltage variations,” and Patent Owner has not presented any indication as to the degree of insensitivity that is required for something to be “substantially insensitive.” Pet. Reply 25. Additionally, Petitioner argues that Patent Owner ignores the explicit disclosure of Park that provides: “[a]lthough the

present invention is suitable for a wide scope of applications, it is particularly suitable for constantly maintaining a back bias voltage with respect to the variation of an external voltage.” *Id.* at 25–26 (citing Ex. 1007, 1:10–13).

We agree with Petitioner. Independent claims 1 and 15 do not recite a complete insensitivity to variations in the power supply, only that bias voltage be “substantially insensitive” to power supply variations. A completely horizontal line, if so provided in Figure 8 of Park, would indicate an insensitivity of VBB with respect to VCC. A “substantially insensitive” line could have some type of slope, to contrast it with the horizontal or completely insensitive line. Further, neither Patent Owner nor the ’554 Patent provides further definition of “substantially insensitive” so that it can be distinguished from Park, especially when Park touts its back bias voltage as being maintained constant even with variations in the external voltage. *See* Ex. 1007, 1:10–13. As such, we do not agree with Patent Owner’s arguments distinguishing claims 1 and 15 from Park.

5. *Petitioner’s Contentions Regarding Claims 2, 3, 14, 16, 31, and 36*

With respect to dependent claims 2, 3, 14, 16, 31, and 36, Petitioner addresses the disclosures of Park and Baker, as discussed above. Pet. 52–57, 63, 70–73. Petitioner also contends that certain aspects of those dependent claims would have been obvious over the cited references and posits reasons to combine the references to meet the specific recitations of those dependent claims. *Id.* Patent Owner does not expressly address the subject matter of these dependent claims. *See* PO Resp. We discuss those claims below.

Claims 2 and 16 recite that inverter comprises a “pull up transistor” and a “pull down transistor,” with the pull down transistor size being

substantially larger than the pull up transistor size. Claim 31 recites first and second transistors connected in series with a similar differential size limitation for the transistors as recited in claims 2 and 16. Petitioner argues that a person of ordinary skill in the art would have been motivated to implement Park's inverter with Baker's pull up and pull down transistors because it "was a well-known, standard CMOS implementation of an inverter," and would have been well within the capability of an ordinary artisan. *Id.* at 52–55 (citing, *inter alia*, Ex. 1002 ¶ 146; Ex. 1008, 201, Fig. 11.1). With respect to the transistor size differential, Petitioner argues that a person of ordinary skill in the art would have been motivated to configure the size of the NMOS transistor of inverter IN1 to be much larger than the size of the PMOS transistor of inverter IN1 in order for inverter IN1 to have an inverter trip point that is substantially insensitive to variations in the external voltage V_{CC} , as discussed above. *Id.* at 55–56 (citing Ex. 1002 ¶¶ 147–148). We determine that, in light of Petitioner's cited teachings from Park and Baker, persons of ordinary skill in the art would have known to combine the references and would have been motivated to do so for the reasons provided in the Petition.

Claim 3 recites that the first transistor is a PMOS transistor with its gate biased to a voltage equal to the power supply voltage minus a predesignated voltage. Petitioner points out that Park discloses that transistor P is a PMOS pull up transistor, with reference voltage V_{REF} connected to the gate thereof, where V_{REF} is set to the power supply voltage V_{CC} minus a constant voltage. *Id.* at 56 (citing Ex. 1007, 4:66–5:2, 5:11, Fig. 5; Ex. 1002 ¶ 151).

Claim 14 recites that the resistor is implemented using a MOS transistor, or a strip of polysilicon, or a strip of diffusion. As discussed above, Petitioner points out that Park discloses that the NMOS pull down transistor N is implemented using a NMOS transistor N. *Id.* at 57 (citing Ex. 1002 ¶ 152).

Claim 36 recites that “the current source comprises a transistor connected between the power supply terminal and the node,” and the transistor is “a field effect transistor biased in the saturation mode.” As discussed above, Petitioner has demonstrated the obviousness of such features in the context of discussing claims 1 and 15.

As such, with respect to dependent claims 2, 3, 14, 16, 31, and 36, Petitioner, we have reviewed Petitioner’s explanations and supporting evidence as to how the proffered combination teaches the limitations of those dependent claims, as well as its explanations as to how one of ordinary skill in the art would have combined Park and Baker, and we agree with Petitioner’s analysis. *See* Pet. 52–57, 63, 70–73. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the subject matter of dependent claims 2, 3, 14, 16, 31, and 36 would have been obvious over the combined teachings of Park and Baker.

6. Conclusion

Accordingly, we determine that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claims 1–3, 14–16, 30, 31, and 36 are unpatentable under 35 U.S.C. § 103(a) as obvious over Park and Baker.

G. Obviousness over Combinations of Park, Baker, Tsukada, and Young

Petitioner contends that claims 32–35 are unpatentable under 35 U.S.C. § 103(a) as obvious over combinations of Park, Baker, Tsukada, and Young. Pet. 3, 74–82. Specifically, Petitioner asserts that claims 32–34 would have been obvious over Park, Baker, and Tsukada, and that claim 35 would have been obvious over Park, Baker, and Young. *Id.* Petitioner, relying on citations to the references and declaration testimony of Dr. Baker, sets forth how the references would have conveyed the claim limitations and provides reasoning for combining the teachings of the references. *Id.* at 74–82.

Patent Owner argues that Tsukada and Young do not cure the deficiencies of Park and Baker, discussed above, the combinations including Tsukada and Young also fail to render claims 32–35 obvious. PO Resp. 18–19. As discussed above, however, we do not agree with Patent Owner’s arguments against the combination of Park and Baker.

Claims 32–35 are dependent claims reciting that a bias voltage is applied to a silicon substrate region in which memory cells reside (claims 32 and 35 each of which depends from claim 30); that the device is a DRAM (claim 33 depending from claim 32); that the bias voltage is less than or equal to 0 volt (claim 34 depending from claim 32); and that the bias voltage is applied to a well region of the substrate having opposite conductivity type (claim 35). Ex. 1001, 10:5–20. With respect to claims 33 and 34, Petitioner asserts that the system of Park and Baker discloses its use with a DRAM and that its back bias voltage is less than or equal to zero volts, as discussed above. Pet. 78–79.

Petitioner acknowledges that the combined system of Park and Baker does not disclose the application of its back bias voltage to a silicon substrate in which memory cells reside, and thus cites to Tsukada. *Id.* at 74. Tsukada is directed to a bias voltage controlling apparatus, and illustrates a conventional stacked-capacitor type DRAM cell, formed from a P-type silicon substrate. Ex. 1009, Abstract, 2:46–49, Fig. 1A. As illustrated in Figure 1A of Tsukada, the substrate has a bias voltage, V_{BB} , applied thereto through a bias voltage controlling apparatus. *Id.* at 2:62–64, Fig. 1A.

With respect to claim 32, Petitioner asserts that although a single DRAM cell is illustrated in Figure 1A, Tsukada discloses a device with multiple cells, and a person of ordinary skill in the art would have understood that Tsukada's substrate houses multiple DRAM cells. Pet. 75–76 (citing Ex. 1009, 4:18–25; Ex. 1002 ¶ 202). Additionally, Petitioner asserts that a person of ordinary skill in the art would have recognized that the combined Park-Baker system would provide a back bias voltage V_{BB} that is usable for biasing Tsukada's substrate because it would have constituted a combination of known components according to known methods to achieve the predictable result of controlled substrate biasing. *Id.* at 76–78 (citing Ex. 1002 ¶¶ 204–206).

We have reviewed Petitioner's explanations and supporting evidence as to how the proffered combination teaches the limitations of claim 32, as well as its explanations as to how one of ordinary skill in the art would have combined Park, Baker, and Tsukada, and we agree with Petitioner's analysis. Also, as discussed above, the elements of claims 33 and 34 are disclosed by the combination of Park and Baker. Pet. 78–79. As such, we determine that Petitioner has demonstrated by a preponderance of the

evidence that the subject matter of claims 32–34 is rendered obvious over the combination of Park, Baker, and Tsukada.

With respect to claim 35, Petitioner acknowledges that the combined Park-Baker system does not disclose the memory device having well regions, so Petitioner cites to Young. Pet. 79–80. Young is directed to a charge pump circuit for biasing an N well of a memory array. Ex. 1012, Abstract. Young details that memory cells could be formed from wells of P-type conductivity in an N-type silicon substrate, and that those wells could be biased by a negative voltage. *Id.* at 1:14–21. Petitioner asserts that it would have been obvious for one of ordinary skill in the art to use the bias circuit of Park-Baker to bias a P-well in a memory array, like Young. Pet. 81. Petitioner also asserts that a person of ordinary skill in the art would have been motivated to make this combination because it constitutes a mere combination of known elements, according to known methods, to achieve predictable results. *Id.*

We have reviewed Petitioner’s explanations and supporting evidence as to how the proffered combination teaches the limitations of claim 35, as well as its explanations as to how one of ordinary skill in the art would have combined Park, Baker, and Young, and we agree with Petitioner’s analysis. As such, we determine that Petitioner has demonstrated by a preponderance of the evidence that the subject matter of claim 35 is rendered obvious over the combination of Park, Baker, and Young.

III. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence that (1) claim 22 is anticipated by Ito under 35 U.S.C. § 102(e); (2) claims 28

and 29 are unpatentable over Ito and Kim under 35 U.S.C. § 103; (3) claims 1–3, 14–16, 30, 31, and 36 are unpatentable over Park and Baker under 35 U.S.C. § 103; (4) claims 32–34 are unpatentable over Park, Baker, and Tsukada under 35 U.S.C. § 103; and (5) claim 35 is unpatentable over Park, Baker, and Young under 35 U.S.C. § 103.

IV. ORDER

It is

ORDERED that each of claims 1–3, 14–16, 22, and 28–36 of U.S. Patent No. 6,172,554B1 is unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01416
Patent 6,172,554 B1

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