

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01417
Patent 7,375,027 B2

Before JAMESON LEE, KEVIN F. TURNER, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

LEE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Petitioner¹ filed a Petition (Paper 1, “Pet.”) to institute *inter partes* review of claims 1–10 of U.S. Patent No. 7,375,027 B2 (Ex. 1001, “the ’027 patent”). We instituted review of claims 1–10 on all grounds asserted in the Petition. Paper 7 (“Decision on Institution”). Patent Owner² filed a Patent Owner Response.³ Paper 13. Petitioner filed a Reply.⁴ Paper 20. Oral hearing was held on August 16, 2018. A copy of the transcript for the oral hearing has been entered as Paper 32.

We determine that Petitioner has shown by a preponderance of the evidence that each of claims 1–10 is unpatentable.

B. Related Matters

Both Petitioner and Patent Owner have identified the following action as involving the ’027 patent: *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:16-cv-00335-SLR (D. Del.). Pet. 1; Paper 4. Petitioner identifies these *inter partes* review proceedings between the parties that involve other patents: IPR2017-00032; IPR2017-00033; IPR2017-00035; IPR2017-00036; IPR2017-00037; IPR2017-00038;

¹ Samsung Electronics Co., Ltd.

² ProMOS Technologies, Inc.

³ Patent Owner also filed a declaration of Mr. Ron Maltiel in support of the Patent Owner Response. Ex. 2002.

⁴ Patent Owner filed a Motion for Observations on Cross-Examination. Paper 26. Petitioner filed a Response to Patent Owner’s Motion for Observations on Cross-Examination. Paper 28. We have considered both submissions.

IPR2017-00039; and IPR2017-00040. Pet. 1–2. Patent Owner additionally identifies these *inter partes* review proceedings between the parties that involve other patents: IPR2017-01412, IPR2017-01413, IPR2017-01414, IPR2017-01415, IPR2017-01416, IPR2017-01418, and IPR2017-01419. Paper 4.

C. The '027 Patent

The '027 patent is directed to the field of manufacturing semiconductor devices, and more particularly to opening a contact via to a surface of a material in a semiconductor device. Ex. 1001, 1:6–9. The '027 patent explains that a problem with preexisting methods of opening a contact via to a surface of a material in a semiconductor device is that the semiconductor material at the bottom of the contact via is etched twice, thus subjecting that material to damage. *Id.* at 1:13–30. Specifically, the '027 patent describes that in the prior art, a first etching step is applied which goes through a photoresist layer down to the surface of the semiconductor material, subjecting the surface to the effects of etching once. *Id.* at 1:19–21. After the first etching step, a liner material is applied to the via and the surface of the semiconductor material within the via. *Id.* at 1:21–23. Then, an anisotropic etching step is performed to remove the liner material at the bottom of the aperture, which has the undesirable effect of subjecting the surface of the semiconductor material within the via to the effects of etching a second time. *Id.* at 1:23–37.

The '027 patent discloses a method of providing a contact via to a surface of a material that avoids the damaging effects of the second etching step in prior art techniques. *Id.* at 1:38–48. Specifically, the '027 patent describes:

In one aspect of the invention, a contact via to a surface of a material is performed by forming a first dielectric layer on the surface, forming a second dielectric layer on the first dielectric layer, providing a first aperture which extends from a surface of the second dielectric layer toward the contact surface area of the material for a distance which is less than a combined thickness of the first and second dielectric layers. Next, a third dielectric layer is provided covering a surface of the aperture and an exposed surface of the first dielectric layer. A portion of the third dielectric layer and a portion of the first dielectric layer are removed to expose a portion of the contact surface area of the material.

Id. at 1:48–59.

Of all challenged claims, claim 1 is the only independent claim.

Claim 1 is reproduced below:

1. A method of providing a contact via to a surface of a substrate, the method comprising:
 - forming a first dielectric layer on the surface;
 - forming a second dielectric layer on the first dielectric layer;
 - providing a first aperture which extends from a surface of the second dielectric layer toward the surface of the substrate for a distance which is less than a combined thickness of the first and second dielectric layers;
 - providing a third dielectric layer covering a surface of the first aperture and an exposed surface of the first dielectric layer; and
 - removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.

Ex. 1001, 4:17–32.

Notably, in the “providing a first aperture” step, the aperture does not extend all the way to the surface of the substrate because it starts at the

surface of the second dielectric layer and extends for a distance that is less than the combined thickness of the first and second dielectric layers. The surface of the substrate is not exposed until the step of “removing a portion of the third dielectric layer and a portion of the first dielectric layer.”

Figure 3 of the '027 patent is reproduced below:

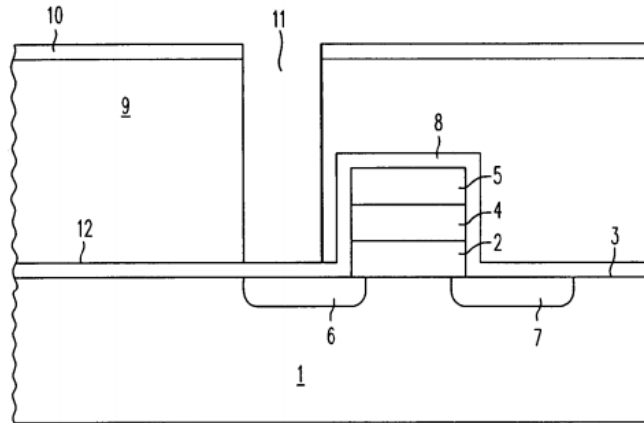


Figure 3 illustrates a cross-section of the semiconductor structure in the midst of contact via formation. Ex. 1001, 2:19–27. Protective layer 8 constitutes a first dielectric layer. *Id.* at 2:55–57. Reference numeral 9 designates a second dielectric layer that has been applied over first dielectric layer 8. *Id.* at 2:66–67. Initial via 11 has been etched through second dielectric layer 9 but does not extend through to the surface of semiconductor substrate 1. *Id.* at 3:3–6.

Figure 5 of the '027 patent is reproduced below:

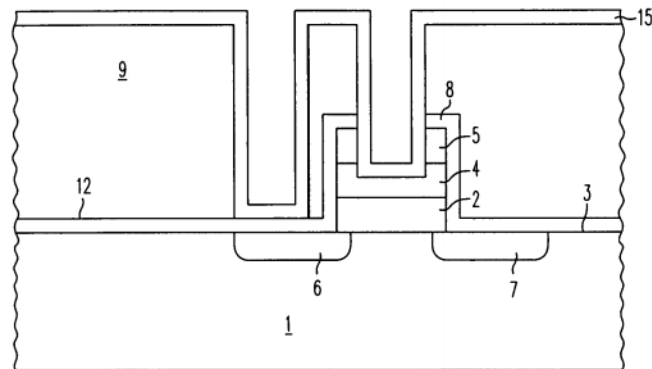


FIG. 5

Figure 5 illustrates the deposition of third dielectric layer 15 over the initial aperture and the exposed surface of the first dielectric layer. *Id.* at 2:30–32; 3:35–45.

Figure 6 of the '027 patent is reproduced below:

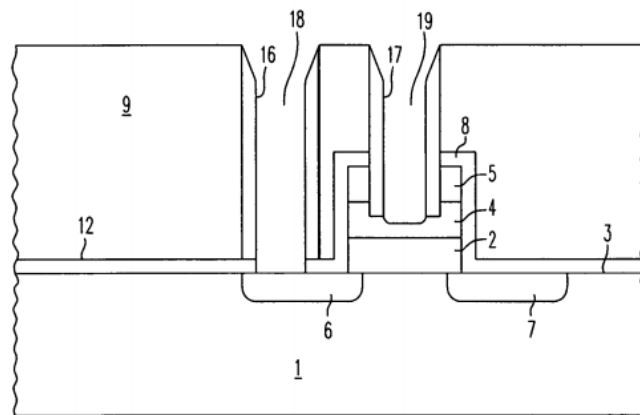


FIG. 6

Figure 6 illustrates the results of an anisotropic etching step that completes the contact via by removing the portion of third dielectric layer 15 that sits atop dielectric layer 9 and the portion of dielectric layer 15 that sits atop first dielectric layer 8. *Id.* at 3:46–50. In addition, the portion of first dielectric layer 8 that covers source region 6. *Id.* at 3:50–53. Contact via 18, extending to the surface of substrate 1, has been formed. *Id.* at 3:58–60.

D. Evidence Relied Upon by Petitioner

Petitioner relies on the following references⁵:

Reference		Date	Exhibit
Koyama	U.S. Pat. Pub. 2003/0049920 A1	March 13, 2003	Ex. 1005
Ngo	U.S. Pat. No. 6,060,393	May 9, 2000	Ex. 1012
Ono	Jap. Pat. App. Pub. H10-144788	May 29, 1998	Ex. 1009 ⁶
Cronin	U.S. Pat. No. 5,654,238	Aug. 5, 1997	Ex. 1008

Petitioner also relies on the Declarations of Gary Rubloff, Ph.D.
(Exs. 1002, 1026).⁷

E. The Asserted Grounds

Petitioner asserts the following grounds of unpatentability (Pet. 3–4):

Claim(s) Challenged	Basis	Reference(s)
1, 2, 4, 6–8, and 10	§ 102(b)	Ono
3 and 5	§ 103(a)	Ono and Ngo
9	§ 103(a)	Ono and Cronin
1, 2, 4, 6–8, and 10	§ 102(b)	Koyama
3 and 5	§ 103(a)	Koyama and Ngo
9	§ 103(a)	Koyama and Cronin

⁵ The application leading to the '027 patent was filed on October 12, 2004 and does not claim priority to any earlier application. Ex. 1001, [22].

⁶ Exhibit 1009 includes Ono (pages 9–16), an English translation of Ono (pages 1–8), and an affidavit certifying the translation (page 17). Pet. 3 n.1.

⁷ Exhibit 1026 was filed in support of Petitioner's Reply.

II. ANALYSIS

A. The Law on Anticipation and Obviousness

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference.

Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged in the same way as is recited in the claim, “the reference need not satisfy an *ipsissimis verbis* test.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990)). Identity of terminology between the anticipatory prior art reference and the claim is not required. “A reference anticipates a claim if it discloses the claimed invention ‘such that a skilled artisan could take its teachings in *combination with his own knowledge of the particular art and be in possession of the invention.*’” *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995). Prior art references must be “‘considered together with the knowledge of one of ordinary skill in the pertinent art.’” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Also, “it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968). As the Court of Appeals for the Federal Circuit recently explained, the dispositive question for anticipation is whether one skilled in the art would reasonably understand or infer from a prior art reference that every claim element is disclosed in that reference. *Eli Lilly v. Los Angeles Biomedical Research Inst.*, 849 F.3d 1073, 1074–1075 (Fed. Cir. 2017).

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). One seeking to establish obviousness must articulate sufficient reasoning to support the conclusion of obviousness. *See In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner . . . must . . . articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007))).

B. Level of Ordinary Skill in the Art

Petitioner proposes that a person of ordinary skill in the art at the time of the alleged invention of the ’027 patent “would have had a master’s degree or higher in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and three to four years of experience in the design and fabrication of semiconductor devices. (Ex. 1002, ¶¶ 19-20.)” Pet. 4–5 (footnote omitted).

Patent Owner states, however,

Patent Owner believes a Bachelor’s degree in a field relating to the semiconductor manufacturing process like materials science, physics, chemistry, or other related subjects, along with at least four to five years of experience in the field, would meet the level of ordinary skill in the art.

PO Resp. 17 (*see also* the testimony of Mr. Ron Maltiel (Ex. 2002 ¶ 19)).

We find Petitioner’s proposal vague in its reliance on the term “or higher” to describe the level of education. This qualifier introduces a range

that is too broad to provide a meaningful indication of what knowledge and skills would have been possessed by one with ordinary skill in the art. The same is true with Patent Owner's use of the qualifier "at least" with regard to the amount of work experience.

By definition, the level of ordinary skill is less than that of an expert. A "master degree or higher" is an advanced degree. Without Petitioner explaining why the level of "ordinary skill" is reflected by an advanced degree, and where Patent Owner disputes that an advanced degree reflects the level of ordinary skill, we are not persuaded by Petitioner's articulation of the level of ordinary skill. Therefore, with regard to the education level of ordinary skill, we credit the testimony of Mr. Maltiel (Ex. 2002 ¶ 19) over the testimony of Dr. Rubloff (Ex. 1002 ¶ 19). However, we find Patent Owner's reference to experience in any related field to be too general, and we credit Dr. Rubloff's testimony over that of the testimony of Mr. Maltiel insofar as the level of experience is concerned. We also eliminate the qualifier "at least" to eliminate vagueness.

For the foregoing reasons, we find the level of ordinary skill is reflected by a bachelor's degree in a field relating to a semiconductor manufacturing process like materials science, physics, chemistry, or other related subjects, along with three to four years of experience in the design and fabrication of semiconductor devices.

C. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2016); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016).

Consistent with that standard, claim terms are generally given their ordinary and customary meaning, as would have been understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). There are, however, two exceptions to that rule: “(1) when a patentee sets out a definition and acts as his own lexicographer,” and “(2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comp. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

It is likewise not enough [for disavowal] that the only embodiments, or all of the embodiments, contain a particular limitation. We do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that. To constitute disclaimer, there must be a clear and unmistakable disclaimer.

Id. at 1366–67; *see also EPOS Techs. Ltd. v. Pegasus Techs. Ltd.*, 766 F.3d 1338, 1341 (Fed. Cir. 2014).

If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). Disavowal can be effectuated by language in the specification or the prosecution history. *Poly-America, L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016). “In either case, the standard for disavowal is exacting, requiring clear and unequivocal evidence that the claimed invention includes or does not include a particular feature.” *Id.* Neither party contends that the Specification of the ’027 patent specially defined any term or that the inventors of the ’027 patent acted as their own lexicographer. We have no reason to determine otherwise.

“In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.”

DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc., 469 F.3d 1005, 1014 (Fed. Cir. 2006). However, claim construction does not mean importing limitations into the claims in the name of construction, if the limitations are not otherwise there. As the Federal Circuit explained,

It is a “bedrock principle” of patent law that “the claims of a patent define the invention to which the patentee is entitled the right to exclude.” *Innova*, 381 F.3d at 1115; *see also Vitronics*, 90 F.3d at 1582 (“we look to the words of the claims themselves . . . to define the scope of the patented invention”); *Markman*, 52 F.3d at 980 (“The written description part of the specification itself does not delimit the right to exclude. That is the function and purpose of claims.”). . . . Because the patentee is required to “define precisely what his invention is,” the [Supreme Court] explained, it is “unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its terms.” *White v. Dunbar*, 119 U.S. 47, 52, 7 S.Ct. 72, 30 L.Ed. 303 (1886); *see also Cont’l Paper Bag Co. v. E. Paper Bag Co.*, 210 U.S. 405, 419, 28 S.Ct. 748, 52 L.Ed. 1122 (1908) (“the claims measure the invention”); *McCarty v. Lehigh Valley R.R. Co.*, 160 U.S. 110, 116, 16 S.Ct. 240, 40 L.Ed. 358 (1895) (“if we once begin to include elements not mentioned in the claim, in order to limit such claim . . . , we should never know where to stop”); *Aro Mfg. Co. v. Convertible Top Replacement Co.*, 365 U.S. 336, 339, 81 S.Ct. 599, 5 L.Ed.2d 592 (1961) (“the claims made in the patent are the sole measure of the grant”).

Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed. Cir. 2005).

Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1.

“forming a first dielectric layer on the surface”

Independent claim 1 recites a step of “forming a first dielectric layer on the surface.” Ex. 1001, 4:19. The term “the surface” draws antecedent basis from “a surface of a substrate” as recited in the preamble of claim 1. *Id.* at 4:17–18. According to Petitioner, nothing in the language of the claims or the specification of the ’027 patent requires formation of layers “on the surface” to be interpreted to mean formation of a layer “directly on the surface of the substrate, and thus depositing a layer on the surface of the substrate does not necessarily require depositing a layer directly on the surface of the substrate. Pet. 24–25. Patent Owner asserts, however, that “forming a first dielectric layer on the surface” should be construed to require that the first dielectric layer be formed “*directly on* the substrate surface.” PO Resp. 10 (emphasis added).

We need not determine whether forming a layer “directly on” the surface of the substrate is required by the claim, because even assuming that a layer must be formed “directly on” the substrate surface, Petitioner has shown that the prior art in each alleged ground of unpatentability discloses forming a first dielectric layer “directly on” the surface of a substrate. Nevertheless, because Patent Owner contends, to the contrary, that the prior art does not disclose any dielectric layer formed “directly on” the surface of a substrate, we resolve the issue of claim construction to provide an alternate answer to Patent Owner’s arguments. For reasons discussed below, we determine that the “directly on” restriction is not required under the rule of broadest reasonable interpretation. Patent Owner’s proposed construction is rejected.

The plain and ordinary meaning of “forming a dielectric layer on the surface” does not specify whether the layer is formed directly on the surface of the substrate, or indirectly on the surface of the substrate, i.e., with presence of some material between them. Thus, the plain and ordinary meaning of the phrase is sufficiently broad to cover both forming the layer directly on the surface and indirectly on the surface.⁸ Patent Owner does not represent that the inventors of the ’027 patent acted as their own lexicographer and redefined, in the Specification of the ’027 patent, the plain and ordinary meaning of any term, and we do not find any such special definition in the Specification. Also, Patent Owner does not identify any express disavowal in the Specification of the ’027 patent with regard to whether the first dielectric layer must be formed directly on the surface of the substrate, and we find none.

Although the only disclosed embodiment in the ’027 patent forms the first dielectric layer directly on the surface of the substrate, that does not constitute an express disavowal of forming the dielectric layer indirectly on the surface of the substrate. We must be careful not to read limitations from the specification into the claims. “It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (citations omitted).

Patent Owner argues that the prosecution history of the ’027 patent supports its proposed claim construction to require forming the first

⁸ The word “on” is generic and itself sets forth no requirement of a specific manner in which one object is deemed to be “on” another. One of the dictionary meanings of “on” is to indicate “a source of attachment or support.” *Merriam-Webster Online Dictionary* (November 14, 2018), <https://www.merriam-webster.com/dictionary/on> (Ex. 3001).

dielectric layer “directly on” the surface of the substrate. For reasons discussed below, we disagree.

Patent Owner argues that during prosecution of the '027 patent, the claims were amended “to make clear that the first dielectric layer is formed directly on the surface of the semiconductor substrate.” PO Resp. 10.

Patent Owner argues,

As filed, original claim 1 did not use the word “substrate”, instead using the word “material.” Thus, the preamble of claim one read: “a method of providing a contact via to a surface of a material, the method comprising.” Ex. 1004 ('027 File History) at p. 112. This claim was rejected as anticipated by U.S. Patent No. 6, 441,418 (“Shields” or the “'418 patent”). *Id.* at p. 119. To support the rejection, the examiner stated that “Shields et al. discloses forming a via including forming a first dielectric layer (16) on a surface

Shields discloses a method of forming a contact in an integrated circuit. Ex. 2005 ('418 patent) at Abstract. Shields, however, discloses that the first dielectric layer (etch stop layer 16) is “located intermediate first oxide layer 14 and second oxide layer 18.” *Id.* at 3:64–65. The first dielectric layer of Shields is thus not deposited on the surface of the substrate, but rather the surface of the oxide layer 14, as shown in Fig. 1 from Shields:

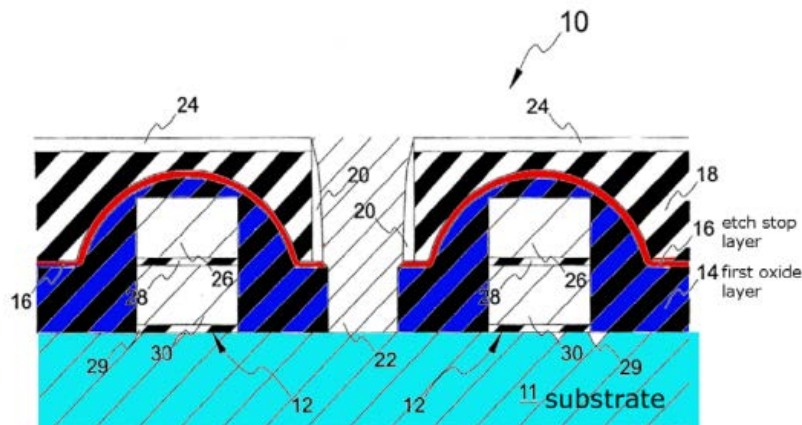


FIG. 1

Ex. 2005 ('418 patent) Figure 1 (annotated).

In response to the examiner's rejection of then pending claims 1–10, the claims of the '027 patent were amended as follows: [footnote omitted]

1. (Currently Amended) A method of providing a contact via to a surface of a ~~material~~ substrate, the method comprising:

forming a first dielectric layer on the surface;

forming a second dielectric layer on the first dielectric layer;

providing a first aperture which extends from a surface of the second dielectric layer toward the surface of the ~~material~~ substrate for a distance which is less than a combined thickness of the first and second dielectric layers;

providing a third dielectric layer covering a surface of the first aperture and an exposed surface of the first dielectric layer; and

removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate ~~material~~.

Ex. 1004 at p. 112.

After the amendment, claims 1–10 were allowed. As shown above, the only change to the claim was to replace the term “material” with “substrate.” In this case, given Shield's structure, the purpose of the amendment was to distinguish structures, such as Shields, where the etch stop was deposited on a previously deposited intermediate layer.

PO Resp. 11–13.

Patent Owner's explanation of the purpose and significance of the amendment, had it been presented by the patent applicant during the examination process, may well have constituted an express disavowal regarding forming the first dielectric layer directly or indirectly on the surface of the substrate. However, no such remarks appeared in the prosecution history. The patent applicant made no representation focused on

whether “directly on” is required. The characterization by Patent Owner, as noted above, is just one of many potential explanations that are consistent with the prosecution history.

The patent applicant merely stated “Shields does not disclose: ‘forming a first dielectric layer on the surface [of the substrate] . . . and removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.’”

Ex. 1004, 114. The generic explanation also is consistent with a position that Shields does not disclose forming a dielectric layer on the surface of the substrate, either directly or indirectly, or a position that Shields does not disclose removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the substrate.

Based on the generality of the patent applicant’s remark, we agree with Petitioner that a general allegation that a combination of limitations are not met by the prior art is insufficient to constitute a disclaimer or disavowal of claim scope with respect to whether the first dielectric layer has to be formed directly on the surface of the substrate. As we discussed above, “the standard for disavowal is exacting, requiring clear and unequivocal evidence that the claimed invention includes or does not include a particular feature.” *Poly-America*, 839 F.3d at 1136. To constitute disavowal, the disavowal must be clear and unmistakable. *See Thorner*, 669 F.3d at 1367. The generic remark of the patent applicant does not satisfy this standard. Patent Owner’s present characterization of the intent and significance of the patent applicant’s remark reflects hindsight characterization to yield a result that fits a desired litigation position, and is not adequately supported by the record.

Based on the foregoing, we find no disavowal of anything by the applicant for patent either in the Specification of the '027 patent or in the prosecution history with regard to whether the first dielectric layer must be formed “directly on” the surface of the substrate. To satisfy the recitation “forming a first dielectric layer on the surface,” the dielectric layer may be formed either directly or indirectly on the surface of the substrate. Direct contact between the first dielectric layer and the surface of the substrate is not required.

2.

“the first dielectric layer”

Independent claim 1 recites a step of “forming a first dielectric layer on the surface.” Ex. 1001, 4:19.

Petitioner reads “the first dielectric layer” onto a combination or composite of two layers in Ono, i.e., silicon oxide gate electrode coating insulation film 21 and semiconductor coating layer 22. Pet. 11; Ex. 1002 ¶ 60. Implicit in that position is that the “first dielectric layer” is not limited to a single layer to the exclusion of the presence of any internal sub-layer. Petitioner correctly states that because the plain meaning of “dielectric layer” is not limited to a single layer of a single material, there must be some special definition or express disavowal to limit the “first dielectric layer” to a single layer of a single material. We agree with Petitioner that the plain and ordinary meaning of “first dielectric layer” does not exclude internal

sub-layers,⁹ and that there is no special definition or disavowal to limit the claims by excluding internal sub-layers.¹⁰

Patent Owner asserts

[Petitioner’s reading of “first dielectric layer”] should be rejected, because it is inconsistent with the ’027 patent specification. Indeed, every mention of a “first dielectric layer” in the ’027 patent refers to a single layer made of one material such as silicon nitride, or silicon oxynitride. Ex. 1001 at 1:60–65, 2:1–3, 2:55–57, 3:54–60, Table 1. There is no disclosure, teaching, or suggestion in the ’027 patent that the first dielectric layer should be a multi-layer structure.

PO Resp. 14. The argument is misplaced. A properly construed claim may cover other embodiments even when only one embodiment is disclosed so long as the Specification does not expressly exclude such other embodiments. There is no such disclaimer or disavowal. For instance, the Specification does not state that the only embodiments covered by the claims

⁹ U.S. Patent 6,849,897 B2 (Ex. 1027), cited by Dr. Rubloff (Ex. 1026 ¶ 3), refers to a dielectric layer comprising multiple internal layers. Ex. 1027, 8:21–25. Also, as is noted by Dr. Rubloff (Ex. 1026 ¶ 3), Ono itself indicates that each of its semiconductor coating layer 22, interlayer insulation film 23, and mask layer 33 can include multiple sublayers of different materials. Ex. 1009 ¶ 47. We credit Dr. Rubloff’s testimony that the plain meaning of “layer” is not limited to a single layer of a single material, because the testimony is supported by the cited evidence. Ex. 1026 ¶ 3.

¹⁰ Neither party contends that the inventors of the ’027 patent acted as lexicographers and provided in the Specification a special definition for “dielectric material” or “first dielectric material” that would exclude internal sub-layers. We also find no such special definition in the Specification.

are those expressly described or suggested in the Specification, or that a dielectric layer necessarily excludes internal sub-layers.

Although the only disclosed embodiment in the '027 patent describes a first dielectric layer that is a layer comprised of just one material without internal sub-layers, that does not constitute an express disavowal of a dielectric layer including internal sub-layers of dielectric material. Patent Owner argues “[t]he fact that every reference, including Table 1, in the '027 patent refers to a ‘first dielectric layer’ as being a single layer requires a departure from ‘a first dielectric layer’ being construed as being ‘one or more’ layers.”¹¹ PO Resp. 15–16. We disagree.

We must be careful not to read limitations from the specification into the claims. “It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (citations omitted). “[I]f we once begin to include elements not mentioned in the claim, in order to limit such claim . . . , we should never know where to stop.” *McCarty*, 160 U.S. at 116. It is not enough that the only embodiments, or all of the embodiments, contain a particular limitation to limit a claim term beyond its ordinary meaning. *Aria Diagnostics, Inc. v. Sequenom, Inc.*, 726 F.3d 1296, 1301 (Fed. Cir. 2013). Even if a specification has only one embodiment, its claims will not be confined to that example unless the patentee has demonstrated a clear intention to limit the claim scope using words or

¹¹ It is not accurate for Patent Owner to state that the '027 patent refers to the “first dielectric layer” as a “single layer,” because the word “single” does not appear in the Specification. We treat the argument, more accurately, as that in the '027 patent each disclosed implementation of the first dielectric layer is a layer without internal sub-layers.

expression of manifest exclusion or restriction. *Id.* There is no such disavowal.

Patent Owner further argues

a person of ordinary skill in the art would understand from looking at claim 1 that each of the dielectric layers serve a different purpose and a specific function that requires that they be a distinct, single layer. Ex. 2002 at ¶¶ 37–42. The first dielectric layer serves as an etch stop for etching the layer above it. Ex. 1001 at 3:5–6. To avoid damage, the etch stop layer must be of a different material than the layer it is serving as an etch stop for. *Id.* This requires that the dielectric layers as taught in the '027 patent must be of a single layer. A person of ordinary skill in the art would know that using multiple layers of different materials to try and serve the function of the “first dielectric layer” disclosed in the '027 patent would not work, because different materials have different properties that [affect] the etch rate, selectivity, fabrication and, deposition of the materials. Ex. 2002 at 41–42; Ex. 2007 (Properties of SiO₂ and Si₃N₄ at 300K); Ex. 2008 (Silicon Nitride, Si₃N₄ Ceramic Properties); Ex. 1001 at Table 1. Accordingly, “the first dielectric layer” should be made of a single material.

PO Resp. 14–15.

We do not agree that one with ordinary skill in the art would regard as inoperative, in the context of the claimed invention, a first dielectric layer that is comprised of multiple sub-layers of dielectric material. Patent Owner does not specifically identify exactly what “would not work” based on the fact that “different materials have different properties that [affect] the etch rate, selectivity, fabrication and, deposition of the materials.”

With regard to actions about the first dielectric layer, claim 1, the only independent claim, recites only “forming a first dielectric layer on the surface,” and “removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the

substrate.” Patent Owner does not establish why either (1) the first dielectric layer cannot be formed on the surface of the substrate if the first dielectric layer includes internal sub-layers, or (2) a portion of the first dielectric layer cannot be removed to expose the surface of the substrate if the first dielectric layer includes internal sub-layers.

We have reviewed paragraphs 41 and 42 of the testimony of Mr. Ron Maltiel, Patent Owner’s declarant (Ex. 2002). Mr. Maltiel does not explain why the different properties of materials in internal sublayers of a dielectric layer would render the dielectric layer incapable of being either formed on the surface of the substrate or removed to expose the surface of the substrate. Mr. Maltiel also does not explain why the first dielectric layer would lose its ability to act as an “etch stop” for the layer immediately above it, if it were to be comprised of multiple internal sub-layers of dielectric material. For instance, Mr. Maltiel explains that “[i]n order to achieve the goal of serving as an etch stop, the etch stop layer must be of a different material than the layer it is serving as an etch stop for.” Ex. 2002 ¶ 41. That, however, does not limit the etch stop layer to a single layer without internal sub-layers. Layer 21 is beneath layer 22. Patent Owner does not explain why, if layer 22 acts as an etch stop for a layer above it, the combination of layers 21 and 22 still retains the same etch stop function despite the presence of layer 21 beneath layer 22.

Additionally, on cross-examination, Mr. Maltiel acknowledged that if a layer is effective as an etch stop for a layer above it, then generally the inclusion of another layer immediately beneath it would not cause the layer to stop working as an etch stop. Ex. 1025, 93:17–95:5. In that regard, Dr. Rubloff, Petitioner’s declarant, testified as follows:

This is because a composite layer made of two materials can effectively serve as an etch stop for the layer above it. For example, a composite layer having a silicon nitride layer on top of a silicon oxide layer would function as an effective etch stop for an overlying layer of silicon oxide. . . . Therefore, a composite layer of 21 and 22 can still effectively serve the function of an etch stop layer.

Ex. 1026 ¶ 5. We credit the testimony of Dr. Rubloff and the above-noted cross-examination testimony of Mr. Maltiel, which are consistent with each other.

Mr. Maltiel further testified that

[i]f one material has a different thermal expansion coefficient than the layer above it, during later fabrication a stress will be created between them when the device is raised to a higher temperature and then cooled down to room temperature. That stress can lead to the device failure due to cracking. In other cases, the appropriate stressed layer will impact the mobility of the transistor channel between the source and drain, which will improve the speed of the transistors.

Ex. 2002 ¶ 42. But this testimony does not explain why a first dielectric layer cannot be comprised of multiple sub-layers of dielectric material or establish that one of the multiple sub-layers necessarily would crack during the manufacturing process. Cracking merely is a possibility and the potential for cracking due to stress caused by different thermal expansion coefficients exists not simply for sub-layers within the first dielectric layer but also for all layers that are disposed next to each other.

Finally, even assuming, hypothetically, that a dielectric layer that includes multiple sub-layers “would not work” as an etch stop layer, which we do not find is the case, Patent Owner has shown why we must construe the claims to exclude multiple sub-layers in the dielectric layer when there is no disavowal in either the Specification or the prosecution history. We must

respect the language of the claims and not rewrite them in the name of claim interpretation. In *SRAM Corp.*, the Federal Circuit stated:

While SRAM strongly urges the court to interpret the claim to encompass the innovative precision indexing shifting feature it contends it has invented, *we are powerless to rewrite the claims and must construe the language of the claim at issue based on the words used.* *Hoganas AB v. Dresser Indus., Inc.*, 9 F.3d 948, 951 (Fed. Cir. 1993). In this case, the words are clear and the claim covers no more than the recited method of taking up lost motion and effecting a shift.

SRAM Corp. v. AD-II Eng'g, Inc., 465 F.3d 1351, 1359 (Fed. Cir. 2006) (emphasis added); see *K-2 Corp. v. Solomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999) (“Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee.”). “We do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that.” *Thorner*, 669 F.3d at 1366.

For the foregoing reasons, we agree with Petitioner that “the first dielectric layer” as recited in claim 1 may include internal sub-layers, and we reject Patent Owner’s contention that the “first dielectric layer” must be comprised of only a single layer without any sub-layer.

3.

“expose a portion of the surface of the substrate”

Claim 1 recites “removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.” Ex. 1001, 4:30–32. Petitioner did not, in the Petition, expressly construe “expose a portion of the surface of the substrate.” In the Decision on Institution (Paper 7), we did not expressly construe the phrase. Patent Owner argues:

This term should be given its plain and ordinary meaning, which is that the step must expose the surface of the silicon substrate. Samsung's construction, that this includes exposing a silicide layer on top of the substrate should be rejected because it is inconsistent with the prosecution history.

PO Resp. 16. There is no dispute between the parties that the phrase should be given its plain and ordinary meaning. Reply 10–11. Petitioner does not contend that the phrase can be met by exposing some other layer on top of the surface of the substrate but not exposing the surface of the substrate.¹²

Id. Consequently, there is no need for a specific construction.

D. Alleged Unpatentability of Claims
1, 2, 4, 6–8, and 10 as Anticipated by Ono

1. Ono

Ono is directed to a method for manufacturing semiconductor devices having contacts. Ex. 1009 ¶ 1. Ono describes certain problems in prior art manufacturing techniques, including “formation of a damage layer at the bottom of contacts,” “enlargement of the contact diameter during etching of the bottom of contacts,” and increases of “contact resistance” or “junction leakage current.” *Id.* at [57]. Ono explains:

The cause of [increases in contact resistance and junction leakage current] has been ascertained to be the presence of a layer containing oxygen and carbon, which is known as a so-called damage layer, in the contacts. Various methods of removing this damage layer have been reported at academic conferences and

¹² Petitioner's position is that the silicide layer in Koyama has chemically reacted with the silicon substrate such that the silicide has become a part of the surface of the substrate. Pet. 43–45, 50–51; Reply 11. Whether the silicide layer in Koyama has become a part of the surface of the substrate in Koyama is a factual question that we discuss later in this opinion.

the like, but mass production technology capable of completely removing damage layers has not been established.

Id. ¶ 3 (cited at Pet. 7). Ono also describes how the damage layer is formed:

The portion known as the damage layer is formed as a result of oxygen and carbon being driven into the substrate during etching of the interlayer insulation film having SiO₂ as the main component using a resist having carbon as the main component as the mask, and as a result of oxygen in the interlayer insulation film being driven into the substrate due to reverse sputtering being performed for native oxide film removal prior to embedding of conductors into the contact holes.

Id. ¶ 4 (cited at Pet. 7).

To solve the problem, Ono describes the following:

[A] semiconductor device manufacturing method characterized in that it comprises: *a step of forming a semiconductor coating layer which coats a semiconductor substrate*; a step of forming an interlayer insulation film which covers said semiconductor coating layer; a step of forming a mask layer on said interlayer insulation film; *a step of forming contact holes which penetrate said mask layer and said interlayer insulation film and reach said semiconductor coating layer*; a step of forming a side wall layer which coats at least the side walls of said contact holes; and *a step of etching said semiconductor coating layer to expose the surface of said semiconductor substrate*.

Id. ¶ 10 (emphases added) (cited at Pet. 6).

2. Claim 1

Claim 1 recites “[a] method of providing a contact via to a surface of a substrate.” Ex. 1001, 4:17–18. As is noted by Petitioner (Pet. 10), Ono discloses such a method. Ex. 1009 ¶¶ 1, 9, 10, 25–23 (cited at Pet. 10). Petitioner’s assertion also is supported by the testimony of Dr. Rubloff. Ex. 1002 ¶¶ 53–58.

Claim 1 further recites “forming a first dielectric layer on the surface.” Ex. 1001, 4:19. The term “the surface” draws its antecedent basis from the preamble of claim 1, which recites “a surface of a substrate.” Therefore, “the surface” refers to the surface of the substrate.

Ono's Figure 1(a) is reproduced below:

[FIG. 1]

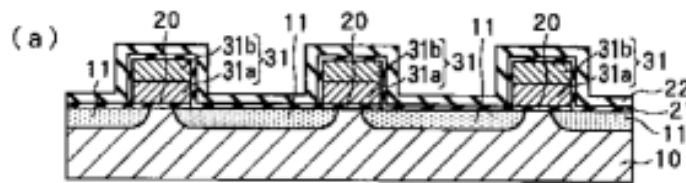


Figure 1(a) illustrates Ono's semiconductor device manufacturing method up to the step of forming a semiconductor coating layer. Ex. 1009 ¶ 49.

Ono describes:

Next, a silicon oxide gate electrode coating insulation film 21 is deposited through CVD over the entire surface to a thickness of approximately 20 nm, and on top of that, silicon nitride is deposited by CVD to approximately 40 nm to form a semiconductor coating layer 22, leading to the state of FIG. 1(a).

Id. ¶ 26 (cited at Pet. 11) (“CVD” stands for chemical vapor deposition; see Ex. 1002 ¶ 83).

Petitioner identifies the combined layers of (1) silicon oxide gate electrode coating insulation film 21 and (2) semiconductor coating layer 22 formed of silicon nitride as a dielectric layer satisfying the first dielectric layer of claim 1. Pet. 11. Dr. Rubloff testifies that both silicon oxide and silicon nitride are dielectric materials. Ex. 1002 ¶ 60 (cited at Pet. 11). Dr. Rubloff explains that because source and drain regions 11 are within the substrate, and because the surface of source and drain regions 11 is coplanar with the surface of the substrate, the surface of source and drain regions 11

is the same as the surface of semiconductor substrate 10. *Id.* ¶ 62.

Dr. Rubloff testifies that “the combination of the silicon oxide gate electrode coating insulation film 21 and semiconductor coating layer 22 is a ‘first dielectric layer,’ as claimed.” *Id.* ¶ 60.

Notwithstanding the contrary arguments of Patent Owner, which we discuss below, Petitioner has shown sufficiently that Ono discloses the step of “forming a first dielectric layer on the surface” of the substrate, and that the two layers 21 and 22 in Ono collectively constitute the “first dielectric layer.”¹³ Patent Owner makes these three arguments regarding the step of “forming a first dielectric layer on the surface”:

First, Ono does not disclose depositing a first dielectric layer directly on the substrate, as required by a proper construction of this term. Second, the combination of two separate layers 21 and 22 as described in Ono does not meet the proper construction of this term, which limits it to a single layer. Finally, even if a dual layer structure can be the first dielectric layer, which it should not be, the structure described by Ono is incompatible with the goals of the '027 patent, and cannot properly be considered a “first dielectric layer.”

PO Resp. 18.

We do not agree with any of Patent Owner’s above-identified arguments. First, as shown in Figure 1(a) of Ono, reproduced above, we

¹³ In its Reply, Petitioner alternatively argues that Ono’s layer 22 itself can serve as the claimed first dielectric layer. Reply 17–18. We recognize that the argument was made in response to Patent Owner’s assertion that layer 22 cannot itself be the first dielectric layer. PO Resp. 19. However, Patent Owner also noted, correctly, that Petitioner did not pursue that approach in the Petition. *Id.* We hold that the argument is a new argument first raised in the Reply but should have been presented in the Petition. It will not be considered.

find that the combination of layers 21 and 22 is disposed directly on the surface of substrate 10. Dr. Rubloff has testified that the surface of source and drain regions 11 is the same as the surface of substrate 10. *Id.* ¶ 62 (cited at Pet. 13). Patent Owner has not asserted that source and drain regions 11 are not a part of substrate 10. In any event, we have construed the “forming a first dielectric layer” limitation above such that the first dielectric layer need not be formed “directly on” the surface of the substrate. *See supra* § II.C.1. Second, as also discussed above in the claim construction analysis, we do not agree with Patent Owner that “first dielectric layer” must comprise of a single layer made of a single material without any sub-layer. *See supra* § II.C.2. Rather, as discussed above, we agree with Petitioner that “first dielectric layer” does not exclude the inclusion of internal sub-layers.

Third, Patent Owner argues that even if a two-layer structure can be “the first dielectric layer,” Ono’s layers 21 and 22 cannot be regarded as that first dielectric layer because “it would not function in the claimed process recited in the claims of the ’027 patent.” PO Resp. 20. Specifically, Patent Owner asserts “[t]he ’027 patent’s structure allows it to use only a single etch step for exposing a portion of the semiconductor substrate – unlike Samsung’s proffered bilayer from Ono. Ex. 1001 at 3:61–64; Ex. 2002 at ¶ 60.” *Id.* We reject Patent Owner’s argument for two reasons. The first is that none of the claims requires using only a single etch step, without sub-steps, to remove the first dielectric layer to expose the substrate.¹⁴ The

¹⁴ For instance, independent claim 1 recites only “removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.” Ex. 1001, 4:30–32.

second is that we do not agree that more than a single etch step to remove portions of Ono's layers 21 and 22 to expose the substrate, as explained below.

Patent Owner argues that layers 21 and 22 in Ono are made of different materials and thus have different etch rates, and that etching of layer 22 must slow down when it reaches the surface of layer 21. PO Resp. 21. Further, Patent Owner explains that “[a]ttempting to etch away 21, 22, and 25 in one step would be a much slower process and not well-controlled, and thus would never be employed in actual production.” *Id.* at 22. Patent Owner asserts that it is inefficient to etch away layers 21 and 22 in one step. *Id.* at 22–24. None of these assertions, even if true, adequately support the contention that a single etch step, without sub-steps, must be used to etch away Ono's layers 21 and 22. Patent Owner's arguments are directed to relative efficiency and what one with ordinary skill in the art might choose as the preferred approach to etching layers 21 and 22; they do not indicate a limitation on what can be done in a single etching step.

Patent Owner's declarant, Mr. Maltiel, testifies that “[a] person of ordinary skill in the art would know that to have a controllable production process, silicon nitride and silicon oxide need to be etched in separate steps.” Ex. 2002 ¶ 62. Yet Mr. Maltiel's underlying reasoning does not indicate a technical limitation on using a single etching step to etch Ono's layers 21 and 22. Rather, the reasoning establishes only what one with ordinary skill in the art would choose to do based on what is more efficient. For instance, Mr. Maltiel states: “Once the silicon nitride layer 22 of Ono is removed, the silicon oxide layer 21 is still present. Given the different etch rates of these materials, and the precision required in manufacturing semiconductor

devices, one would not use the same etchant to remove 21 as 22.” *Id.* But the testimony is silent on whether, when using the same etchant, the etching of layer 21 would continue after layer 22 is etched away.¹⁵ Also, that one with ordinary skill in the art would choose to use a single etchant does not mean using two etchants would be incapable of performing the task.

Patent Owner further argues that “[l]ayers 21 and 22 of Ono in combination do not disclose such a ‘first dielectric layer’ because the properties of these layers are such that they perform different functions. Ex. 1009 at ¶ 0026; Ex. 2002 at ¶¶ 61–66.” PO Resp. 20. We do not agree with this argument for several reasons. First, Patent Owner does not explain why a dielectric layer necessarily must perform one and only one function. Second, Patent Owner does not explain why one with ordinary skill in the art would regard as a requirement for a dielectric layer that it has completely uniform properties throughout its depth.¹⁶ Third, we are not persuaded that Ono’s layers 21 and 22 do not share in some functionalities even by Patent Owner’s own accounting.

For instance, Patent Owner asserts that Ono’s layer 21 serves the function of protecting the exposed surfaces and sides of the gate 31a, 31b,

¹⁵ To the extent, if any, that Patent Owner relies on this testimony to mean that layer 21 cannot be etched by the same etchant that etches layer 22, we do not credit it. We also do not credit Mr. Maltiel’s testimony that Ono’s layer 21 acts as an etch stop for layer 22. Ex. 2002 ¶ 59. Instead, we credit the testimony of Dr. Rubloff that “[a] person of ordinary skill in the art would have understood that etching does not stop at every layer, and, in many instances, an etch will etch through multiple layers even if the etch etches the multiple layers at different etch rates.” Ex. 1026 ¶ 12.

¹⁶ Note also that claim 1 does not specify any particular function to be performed by the first dielectric layer other than its composition.

and the sides of the gate insulation film 20, and also protects the source/drain diffusion region 11 from unwanted oxide growth that can occur by exposure to air. PO Resp. 21 n.2. Patent Owner does not explain, however, why layer 22 of Ono, laid immediately on top of layer 21, does not similarly provide the same function, even if it additionally provides other functions.

Instead, we credit this testimony of Dr. Rubloff:

I disagree that layers 21 and 22 serve such different functions that would not allow them to be considered as a “first dielectric layer.” Both these layers serve a common purpose of protecting the gate electrodes and source/drain regions as they can be seen covering these parts of the device. (*See, e.g.*, Ex. 1009 at FIG. 1(a), ¶ [0026].)

Ex. 1026 ¶ 14 (cited at Reply 14). We also credit Dr. Rubloff’s testimony that both layers 21 and 22 of Ono are made of dielectric material, Ex. 1002 ¶ 60 (cited at Pet. 11), and that the shared functionality of layers 21 and 22 supports the understanding that they collectively constitute a “first dielectric layer.” Ex. 2004, 119:12–120:2. Dr. Rubloff further testifies, persuasively, that both layers 21 and 22 cover the entire exposed surface when deposited, and that when portions of layer 22 are removed, the corresponding portions of layer 21 are removed as well. Ex. 2004, 106:13–22; 108:4–10; 118:9–15.

For the foregoing reasons, we determine that Ono discloses the step of “forming a first dielectric layer on the surface.”

Claim 1 further recites: “forming a second dielectric layer on the first dielectric layer.” Ex. 1001, 4:20–21. Petitioner has shown that Ono discloses this step. Specifically, Ono states: “Next, as shown in FIG. 1(b), interlayer insulation film 23 is formed over semiconductor coating layer 22, for example, by depositing BPSG to about 500 nm.” Ex. 1009 ¶ 27 (cited at

Next, anisotropic etching is performed along the mask layer 24, forming contact holes CH which penetrate through the interlayer insulation film 23. At this stage, *the semiconductor coating layer 22 is used as an etching stopper layer and etching is terminated once the surface of the semiconductor coating layer 22 has been exposed.*

Id. ¶ 27 (emphasis added) (cited at Pet. 18). Dr. Rubloff explains that the underlying gate insulating film 21 is not etched at all because coating layer 22 covers insulating film 21 and etching is terminated at the surface of semiconductor coating layer 22. Ex. 1002 ¶ 72 (cited at Pet. 19). This is supported by Ono's disclosure. Ex. 1009 ¶ 27 (cited at Pet. 18) (“[T]he semiconductor coating layer 22 is used as an etching stopper layer and etching is terminated once the surface of the semiconductor coating layer 22 has been exposed.”).

Petitioner explains that Ono discloses providing a contact hole (first aperture) in Figure 1(b) extending from a surface of the interlayer insulating film 23 (second dielectric layer) toward the surface of semiconductor substrate 10 for a distance that is less than a combined thickness of (1) the second dielectric layer, and (2) the semiconductor coating layer 22 and silicon oxide gate electrode coating insulation film 21 (collectively the “first dielectric layer”). Pet. 18 (citing Ex. 1009 ¶ 27). The explanation is supported by the above-quoted disclosure of Ono (Ex. 1009 ¶ 27), as well as by the testimony of Dr. Rubloff (Ex. 1002 ¶ 72). Thus, Petitioner has shown that Ono discloses the step of “providing a first aperture which extends from a surface of the second dielectric layer toward the surface of the substrate for a distance which is less than a combined thickness of the first and second dielectric layers.”

Claim 1 further recites: “providing a third dielectric layer covering a surface of the first aperture and an exposed surface of the first dielectric layer.” Ex. 1001, 4:27–29. Petitioner has shown that Ono discloses this step. Figure 1(c) of Ono is reproduced below:

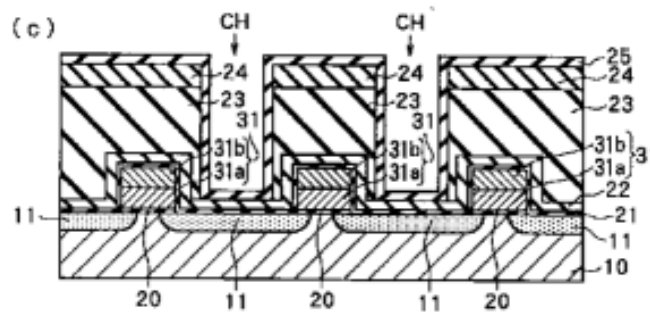


Figure 1(c) of Ono illustrates the process of Ono’s manufacturing method up to the step of forming a contact hole coating layer. Ex. 1009 ¶ 49.

Petitioner identifies layer 25 in Figure 1(c) as the third dielectric layer. Pet. 20. In that regard, Ono describes: “[T]he inside walls and bottom surfaces of the contact holes CH and the outside of the contact holes are coated, performing CVD of e.g., silicon nitride to approximately 40 nm to form a contact hole coating layer 25.” *Id.* ¶ 28 (cited at Pet. 20). Dr. Rubloff testifies that silicon nitride is a dielectric material. Ex. 1002 ¶ 74 (cited at Pet. 20).

As is evident from Figure 1(c), the contact hole coating layer covers aperture CH and the exposed surface of the combined layers of semiconductor coating layer 22 and silicon oxide gate electrode coating insulation film 21. Thus, we find that Ono discloses the step of “providing a third dielectric layer covering a surface of the first aperture and an exposed surface of the first dielectric layer.”

Claim 1 further recites: “removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.” Ex. 1001, 4:30–32. Petitioner has shown that Ono discloses this step. Figure 2(d) of Ono is reproduced below (cited at Pet. 21):

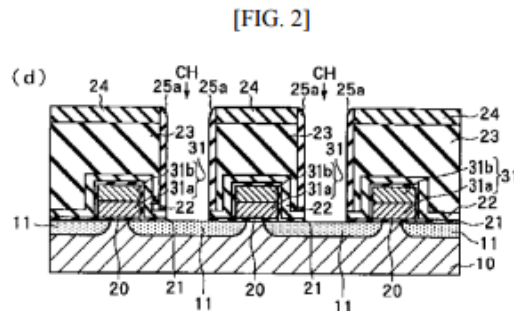


Figure 2(d) of Ono illustrates the process of Ono’s manufacturing method up to the step of forming a contact hole through which the semiconductor substrate is exposed. Ex. 1009 ¶ 49.

Ono describes:

Next, as shown in FIG. 2(d), anisotropic etching such as RIE (reactive ion etching) is performed to remove the contact hole coating layer 25, semiconductor coating layer 22 and gate electrode coating insulation film 21 corresponding to the bottom of contacts to expose the source/drain diffusion layer surface at the bottom of the contacts.

Id. ¶ 29 (cited by at Pet. 21–22). Dr. Rubloff testifies that the anisotropic etching step illustrated in Ono’s Figure 2(d) satisfies the claimed step of “removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.” Ex. 1002 ¶¶ 75–76 (cited at Pet. 21). For the foregoing reasons, we find that Ono discloses the step of “removing a portion of the third dielectric layer and a

portion of the first dielectric layer to expose a portion of the surface of the substrate.”

We have considered the arguments and evidence presented by Petitioner and all of the opposing arguments and evidence presented by Patent Owner. For the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 1 is anticipated by Ono.

3. Claims 2, 4, 6–8, and 10

For reasons discussed below, we find that Petitioner has established, by a preponderance of the evidence, that each of claims 2, 4, 6–8, and 10 is anticipated by Ono.

Claim 2 depends from claim 1 and further recites: “wherein forming a first dielectric layer on the surface comprises depositing a layer of silicon nitride on the surface.” Ex. 1001, 4:33–35. Ono discloses this added limitation because it states that silicon nitride is deposited by CVD to approximately 40 nm to form a semiconductor coating layer 22, leading to the situation depicted in Figure 1(a). Ex. 1009 ¶ 26 (cited at Pet. 24). Dr. Rubloff’s testimony supports this understanding and reading of Ono. Ex. 1002 ¶ 79 (cited at Pet. 24).

Petitioner argues that “nothing in the language of the claims or the specification of the ’027 patent requires the formation of layers ‘on the surface’ to be interpreted to mean formation ‘directly on the surface.’” Pet. 24. In the claim construction analysis above, we determined that “forming a first dielectric layer on the surface” does not require forming the first dielectric layer “directly on” the surface of the substrate. *See supra* § II.C.1. For similar reasons, we determine that “depositing a layer of

silicon nitride on the surface” does not require depositing the silicon nitride “directly on” the surface of the substrate.¹⁷

We do not read the depositing step so narrowly as to require that there cannot be another layer between the silicon nitride and the surface of the semiconductor substrate. Direct contact between the silicon nitride layer and the surface of the substrate is not required. Thus, Ono’s chemical vapor deposition of layer 22 over film 21—which is on the surface of substrate 10—satisfies “depositing a layer of silicon nitride on the surface.”

Accordingly, we find that Ono discloses the step of “depositing a layer of silicon nitride on the surface.” We determine that Petitioner has established, by a preponderance of the evidence, that claim 2 is anticipated by Ono.

Claim 4 depends from claim 2 and further recites: “wherein depositing a layer of silicon nitride comprises depositing the layer of silicon nitride using a chemical vapor deposition process.” Ex. 1001, 4:39–41. As discussed above in the context of claim 2, Ono discloses depositing a layer of silicon nitride on the surface of the semiconductor substrate by use of “CVD.” Ex. 1009 ¶ 26 (cited at Pet. 26). Dr. Rubloff testifies that a person of ordinary skill in the art would have readily understood that “CVD” as used by Ono means chemical vapor deposition. Ex. 1002 ¶ 83 (cited at Pet. 26). Patent Owner advances no argument for claim 4 separate from those it has advanced for independent claim 1, and we already have addressed and rejected those arguments within the analysis for claim 1.

¹⁷ Patent Owner advances no argument for claim 2 separate from those it has advanced for independent claim 1, and we already have addressed and rejected those arguments within the analysis for claim 1.

We find that Ono discloses “wherein depositing a layer of silicon nitride comprises depositing the layer of silicon nitride using a chemical vapor deposition process.” Petitioner has established, by a preponderance of the evidence, that claim 4 is anticipated by Ono.

Claim 6 depends from claim 1 and further recites: “wherein removing a portion of the third dielectric layer and the first dielectric layer to expose a portion of the surface of the material comprises performing an anisotropic etch process.” Ex. 1001, 4:47–50. We recognize, as Petitioner has pointed out (Pet. 27 n.7), that the term “the material” has no antecedent basis either within claim 6 itself or within base claim 1. However, because the term refers to material to be exposed by removal of the first dielectric layer, we understand the term as specifically identifying the surface of the substrate. We articulated this position in the Decision on Institution. Paper 7, 18. During trial, neither party objected to that understanding. Here, we have no reason to deviate from that understanding.

As cited by Petitioner (Pet. 27), Ono describes: “[A]s shown in FIG. 2(d), *anisotropic etching* such as RIE (reactive ion etching) is performed to remove the contact hole coating layer 25, semiconductor coating layer 22 and gate electrode coating insulation film 21 corresponding to the bottom of contacts to expose the source/drain diffusion layer surface at the bottom of the contacts.” Ex. 1009 ¶ 29 (emphasis added). Patent Owner advances no argument for claim 6 separate from those it has advanced for independent claim 1, and we already have addressed and rejected those arguments within the analysis for claim 1.

We find that Ono discloses “wherein removing a portion of the third dielectric layer and the first dielectric layer to expose a portion of the surface

of the material comprises performing an anisotropic etch process.”

Petitioner has established, by a preponderance of the evidence, that claim 6 is anticipated by Ono.

Claim 7 depends from claim 1 and further recites: “wherein forming a second dielectric layer on the first dielectric layer comprises forming a layer of silicon dioxide on the first dielectric layer.” Ex. 1001, 4:51–53. As discussed above, Petitioner identifies Ono’s interlayer insulating film 23 as the second dielectric layer. Ono describes interlayer insulating film 23 as comprising silicon oxide. Ex. 1009 ¶ 23 (cited at Pet. 28). Also as cited by Petitioner (Pet. 28), Ono also describes interlayer insulation film 23 as being formed by depositing BPSG to about 500 nm. *Id.* ¶ 27 (cited at Pet. 28).

Dr. Rubloff testifies that a person of ordinary skill in the art would have understood that silicon oxide is not stoichiometrically balanced and that, in the context of semiconductor fabrication techniques, the term “silicon oxide” is used to refer to “silicon dioxide” which is stoichiometrically balanced. Ex. 1002 ¶ 86 (cited at Pet. 28). Additionally, Dr. Rubloff testifies:

In my opinion, a person of ordinary skill in the art would have understood that *Ono*’s disclosure that the interlayer insulation film 23 being formed by depositing BPSG (*Id.* ¶ [0027]) discloses that the interlayer insulation film 23 is made of silicon dioxide. In particular, a person of ordinary skill in the art would have known that BPSG includes silicon dioxide because BPSG is a material including silicon dioxide doped with boron (B) and phosphorous (P). (Ex. 1010 (*Vaartstra*) at ¶¶ [0002], [0020], Ex. 1011 (*Li*) at ¶ [0050].)

Ex. 1002 ¶ 86 (footnote omitted) (cited at Pet. 28).

Patent Owner advances no argument for claim 7 separate from those it has advanced for independent claim 1, and we already have addressed and

rejected those arguments within the analysis for claim 1. Based on the above-noted testimony of Dr. Rubloff, we find that Ono discloses the limitation added by claim 7. Petitioner has established, by a preponderance of the evidence, that claim 7 is anticipated by Ono.

Claim 8 depends from claim 1 and further recites: “wherein providing the first aperture comprises performing an etch process.” Ex. 1001, 4:54–55. This step is disclosed by Ono. Ono describes that an anisotropic etching step is performed to form contact holes that penetrate through interlayer insulation film 23. Ex. 1009 ¶ 27 (cited at Pet. 29). Ono also describes that etching is terminated once the surface of the semiconductor coating layer 22 has been exposed. *Id.* Patent Owner advances no argument for claim 8 separate from those it has advanced for independent claim 1, and we already have addressed and rejected those arguments within the analysis for claim 1. Petitioner has established, by a preponderance of the evidence, that claim 8 is anticipated by Ono.

Claim 10 depends from claim 1 and further recites: “wherein removing a portion of the third dielectric layer and the first dielectric layer comprises performing a reactive ion etch.” Ex. 1001, 4:59–61. Ono’s manufacturing method satisfies this requirement. Specifically, as cited by Petitioner (Pet. 30), Ono identifies reactive ion etching as an example of the anisotropic etching step used to remove the contact hole coating layer 25 (third dielectric layer), and the semiconductor coating layer 22 and gate electrode coating insulating film 21 (together forming the first dielectric layer) to expose the source/drain diffusion layer surface at the bottom of the contact holes. Ex. 1009 ¶ 29.

Patent Owner advances no argument for claim 10 separate from those it has advanced for independent claim 1, and we already have addressed and rejected those arguments within the analysis for claim 1. Petitioner has established, by a preponderance of the evidence, that claim 10 is anticipated by Ono.

E. Alleged Unpatentability of Claims
3 and 5 as Obvious over Ono and Ngo

1. Ngo

Ngo is directed to a semiconductor device manufacturing process. Ex. 1012, 1:14–15. Specifically, the method includes the formation of a stop layer on the semiconductor substrate and a subsequent formation of an overlying dielectric layer. *Id.* at 2:54–62. Thereafter, a step is performed that forms a conductive path that extends through the two layers to the device. *Id.* at 3:1–4.

2. Claim 3

Claim 3 depends from claim 1 and further recites: “wherein forming a first dielectric layer on the surface comprises depositing a layer of silicon oxynitride on the surface.” Ex. 1001, 4:36–38. Ono by itself does not meet this limitation, because in Ono the first dielectric layer, as discussed above, includes silicon oxide gate electrode coating insulation film 21 and silicon nitride semiconductor coating layer 22. Pet. 11. Dr. Rubloff testifies, however, that “[a] person of ordinary skill in the art would have been motivated to modify *Ono* such that the semiconductor coating layer 22 is a silicon oxynitride film based on the teachings of *Ngo*.” Ex. 1002 ¶ 93 (cited at Pet. 31). Ngo describes depositing stop layer 22’, “for example silicon

oxynitride” on a semiconductor substrate. Ex. 1012, 6:12–15 (cited at Pet. 33).

With regard to that motivation, Dr. Rubloff testifies:

Ngo’s stop layer 22’ has a function similar to *Ono*’s silicon nitride semiconductor coating layer 22, i.e., to minimize “the possibility of etching into substrate 12 . . . [because] [w]ithout stop layer 22, the etching process would likely extend too far into substrate 12 which could damage existing structures therein and/or cause circuit failures.” (*Id.* at 2:7–18; *see also* Ex. 1009 at ¶ [0027].) Although *Ngo* does not specifically disclose the function of its [stop layer 22’, a person of ordinary skill in the art would have readily understood that the function of its stop layer 22’ is similar to the function of the stop layer 22 disclosed in *Ngo* with respect to a prior art embodiment (*e.g.*, *compare* Ex. 1012 at FIG. 1 (showing prior-art semiconductor device with stop layer 22) *with id.* at FIG. 2(b) (showing *Ngo*’s semiconductor device with stop layer 22’).)

Ex. 1002 ¶ 94 (cited at Pet. 32). Dr. Rubloff further explains:

Having looked to *Ngo*, a person of ordinary skill in the art would have been motivated to combine *Ono*’s teachings with *Ngo*’s teachings in this manner [using silicon oxynitride as the semiconductor coating layer 22 instead of silicon nitride] because silicon oxynitride was a well-known alternative to silicon nitride for use as an etch stop film during the formation of contact structures. For example, *Ngo* itself discloses that the stop layer 22 could be “silicon nitride or silicon oxynitride,” thereby suggesting that silicon nitride or silicon oxynitride could be used interchangeably as the material for forming the stop layer. (*Id.* at 4:57–60.)

Id. ¶ 96 (cited at Pet. 33). Dr. Rubloff additionally cites evidence that, in the semiconductor fabrication technical field, silicon nitride and silicon oxynitride were known to be interchangeable for purposes of forming etch stop films. *Id.* ¶ 96 & n.12 (citing Ex. 1006, 6:7–13, 6:48–50; Ex. 1007, 1:14–19; Ex. 1013, 6:21–26; Ex. 1014, 6:27–33).

Notwithstanding the contrary argument of Patent Owner, which we address below, Petitioner has presented persuasive reasoning with a rational underpinning to support that one with ordinary skill in the art would have modified Ono by using silicon oxynitride, instead of silicon nitride, as semiconductor coating layer 22.

Patent Owner advances the same argument for claim 3 that it asserted for independent claim 1. PO Resp. 26. We already have addressed and rejected those arguments within the analysis for claim 1. Patent Owner makes an additional argument for claim 3:

Ono is seeking to prevent formation of “a damage layer” [such] that [it] does not form readily due to carbon of the resist material and oxygen of the interlayer insulation film being driven into the contact holes during etching.” *Id.* at ¶ 0031. Moreover, Ono also states that “when a sputter layer is used for the connection holes, oxygen is also driven in due to so-called reverse sputtering, which is performed as a pretreatment. This sort of layer is difficult to remove, and is known to have an adverse effect on the properties of the contacts.” *Id.* at ¶ 0008. Ono further states that “in the semiconductor device manufacturing method of the present invention, it is preferable for the semiconductor coating layer, mask layer and side wall layer to have an etching selection ratio to the interlayer insulation film, and to substantially not contain carbon or oxygen.” *Id.* at ¶ 0015.

A person of ordinary skill in the art would thus be discouraged from using the silicon oxynitride of Ngo in place of Ono’s silicon nitride layer. They would understand that replacing silicon nitride with silicon oxynitride in this situation would only lead to more oxygen that could be driven into the substrate and lead to more, not less, damage of the substrate. Ex. 2002 at ¶¶ 67–69. Thus, a person of ordinary skill in the art would not look to combine Ono with Ngo because Ono specifically states that it wants to avoid excess oxygen from being driven into the substrate. Ex. 1009 at ¶ 0031.

PO Resp. 27–28. We do not agree with Patent Owner’s argument.

It is not the law on determining obviousness that only the best approach would be deemed obvious, and all inferior designs be regarded as nonobvious. Multiple approaches may be deemed obvious, even if one may be better than another. *See In re Cyclobenzaprine Hydrochloride Extended-Release Capsul Patent Litigation*, 676 F.3d 1063, 1070–71 (Fed. Cir. 2012) (“Where a skilled artisan merely pursues ‘known options’ from ‘a finite number of identified, predictable solutions,’ the resulting invention is obvious under Section 103.”). Key is the following statement from Ono:

[I]n the semiconductor device manufacturing method of the present invention, *it is preferable for the semiconductor coating layer, mask layer and side wall layer to have an etching selection ratio to the interlayer insulation film, and to substantially not contain carbon or oxygen.*

Ex. 1009 ¶ 15 (emphasis added) (cited at Pet. 20). Ono’s disclosure neither requires the semiconductor coating layer to be free of substantial oxygen, nor states that the semiconductor coating layer cannot perform its function if it contains substantial oxygen. Rather, the disclosure simply is that it is “preferred” for the semiconductor coating layer to substantially not contain oxygen. Obviousness is not determined on the basis of what is the most preferred among several acceptable approaches, choices, or techniques.

Furthermore, we disagree with Patent Owner’s argument that an ordinarily skilled artisan would have been discouraged from using oxynitride as the semiconductor coating layer. In order to support a case of teaching away, “a reference . . . [must] suggest[] that the developments flowing from its disclosures are unlikely to produce the objective of the applicant’s invention.” *Syntex (U.S.A) LLC v. Apotex, Inc.*, 407 F.3d 1371, 1380 (Fed. Cir. 2005) (citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Ono

does not describe that its semiconductor coating layer, if made of oxynitride, would be incapable of sufficiently preventing carbon of the resist material and oxygen of the interlayer insulation film from being driven into the contact holes. Notably, Mr. Maltiel, Patent Owner's declarant, has testified that oxynitride is a known barrier layer used to prevent oxidation of the layers it covers. Ex. 1025, 76:11–15.

For the foregoing reasons, we find that Petitioner has established, by a preponderance of the evidence, that claim 3 is unpatentable as obvious over the combined teachings of Ono and Ngo.

3. Claim 5

Claim 5 depends from claim 3 and further recites: “wherein depositing a layer of silicon oxynitride comprises depositing the layer of silicon oxynitride using a chemical vapor deposition process.” Ex. 1001, 4:42–45. Ono specifically discloses, for semiconductor coating layer 22 that is silicon nitride, depositing the silicon nitride layer by using a chemical vapor deposition process. Ex. 1009 ¶ 26 (cited at Pet. 35). In the context of claim 3, we have discussed why it would have been obvious to one with ordinary skill in the art, in light of Ngo's disclosure, to form Ono's semiconductor coating layer 22 with silicon oxynitride instead of silicon nitride. Ngo specifically discloses forming its silicon oxynitride layer in a “PECVD system.” Ex. 1012 ¶ 6:12–17 (cited at Pet. 36).

By “PECVD,” Ngo refers to plasma enhanced chemical vapor deposition. Ex. 1012, 3:4–7. Thus, Ngo discloses using chemical vapor deposition to deposit silicon oxynitride. Petitioner asserts that it would have been obvious to one with ordinary skill in the art to do the same in the combined method of Ono and Ngo, where a layer of silicon oxynitride has to

be deposited. Pet. 36. The assertion is supported by the testimony of Dr. Rubloff. In that regard, Dr. Rubloff testifies:

Indeed, the combined *Ono-Ngo* method would have led to the expected outcome of depositing silicon oxynitride as the semiconductor coating layer 22 in *Ono*, and therefore would have been predictable. In particular, the combined *Ono-Ngo* method would merely be a combination of known elements (forming the semiconductor coating layer 22 using silicon oxynitride in the combined *Ono-Ngo* contact hole formation method) using a known technique (PECVD, as disclosed by *Ngo* as well) to achieve the expected outcome of forming a semiconductor coating layer 22.

Ex. 1002 ¶ 100 (cited at Pet. 36).

Patent Owner advances the same argument for claim 5 that it asserted for claim 3. PO Resp. 26. We already have addressed and rejected those arguments within the analysis for claim 3.

For the foregoing reasons, we find that Petitioner has established, by a preponderance of the evidence, that claim 5 is unpatentable as obvious over the combined teachings of *Ono* and *Ngo*.

F. Alleged Obviousness of Claim 9
as Obvious over *Ono* and *Cronin*

1. *Cronin*

Cronin is directed to a method, in a semiconductor fabrication process, of maintaining a near vertical edge in a contact hole, without directional etching damage to the silicon substrate. Ex. 1008, 1:50–54.

Cronin describes:

[T]he invention provides for a method of etching vertical contact holes in a semiconductor device having an insulating layer of known thickness ‘X’ formed over a substrate, the method comprising the steps of: (1) forming a pattern image on the insulating layer; (2) forming a conformal layer on the pattern

image; (3) *etching the conformal layer by directional etching to produce sidewall spacers, each of width 'W' and having a vertical contact hole therebetween*, the etching continuing to the insulating layer to a depth equal to the thickness 'X' of the insulating layer minus the width 'W' of the sidewall spacer; and (4) isotropically removing the insulating layer to achieve a near vertical edge contact hole without directional etching damage to the substrate.

Id. at 1:61–2:7 (emphasis added).

2. Claim 9

Claim 9 depends from claim 8 and further recites: “wherein performing an etch process comprises performing a reactive ion etch process.” Ex. 1001, 4:56–58. In the context of claim 8 discussed above, “performing an etch process” refers to the etching that creates the first aperture. Petitioner acknowledges that Ono does not disclose that this etching is performed by way of a reactive ion etch process. Pet. 38. Petitioner, however, identifies Cronin as disclosing reactive ion etching when forming a first aperture during a contact structure fabrication process for a semiconductor device. *Id.* at 38–39. In that regard, Petitioner refers to Figure 3 of Cronin. *Id.* at 39. Figure 3 of Cronin is reproduced below:

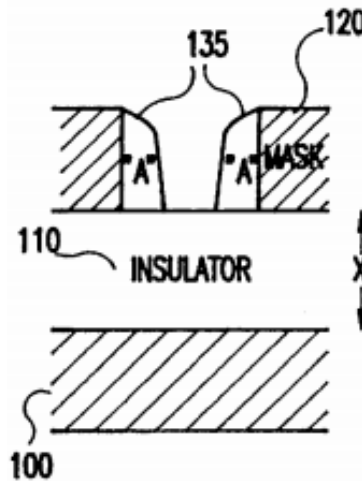


FIG.3

Figure 3 of Cronin illustrates a cross sectional view of a semiconductor device after it has been etched by reactive ion etching to form sidewall pacers 135. Ex. 1008, 2:27–28, 3:10–12.

Petitioner asserts:

In particular, “[a]s shown in FIG. 3, the conformal layer 130 is . . . directionally etched, **using a reactive ion etch (RIE)** for example, to form sidewall spacers 135.” (*Id.*, 3:11–13.) *Cronin*’s conformal layer 130 is a dielectric layer, as it is made from silicon oxide or silicon nitride. (*Id.*, 3:5-9.) As such, the conformal layer 130 penetrated to form the opening in *Cronin* is analogous to the interlayer insulating film 23 (also a dielectric) of *Ono* which is penetrated to form the contact hole CH in figure 1(b). (*Id.*, FIG. 3; Ex. 1009, ¶ [0027], FIG. 1(b).)

Pet. 39. This assertion is supported by the testimony of Dr. Rubloff. Ex. 1002 ¶ 107 (cited at Pet. 39). Dr. Rubloff further explains why one with ordinary skill in the art would have applied Cronin’s teaching to Ono:

In my opinion, a person having ordinary skill in the art would have looked to *Cronin* to refine the teachings of *Ono* because both references relate to semiconductor fabrication and

disclose the formation of contact holes and vias. Having looked to *Cronin*, a person of ordinary skill in the art would have been motivated to use RIE as the anisotropic etching technique to form the contact hole CH in figure 1(b) of *Ono*. For example, *Ono* itself recognizes RIE [reactive ion etch] as a type of anisotropic etching that can be used in another step for etching back dielectric layers. (Ex. 1009 at ¶ [0029], FIG. 2(d).) Moreover, *Cronin* explicitly discloses using RIE in a similar step as claim 9, i.e., during formation of a first aperture penetrating through the conformal layer 130 (analogous to interlayer insulating film 23, as explained above). Using RIE as disclosed by *Cronin* as the anisotropic etching technique to form the contact hole CH in *Ono* would have been nothing more than the utilization of a known technique (RIE) to improve a similar device (semiconductor device with contact hole CH in *Ono*) providing the predictable result of the contact hole CH being formed such that the surface of the semiconductor coating layer 22 is exposed in *Ono*. Moreover, the '027 patent does not disclose any advantages or unexpected results achieved by using RIE as the etch process for forming the first aperture.

Id. ¶ 108 (cited at Pet. 39). The above-quoted testimony presents reasoning with rational underpinning as to why one with ordinary skill in the art would have applied Cronin's teaching regarding use of reactive ion etching in *Ono* when forming the contact hole CH in *Ono*'s figure 1(b).

Patent Owner advances no argument for claim 9 separate from those it has advanced for independent claim 1, and we already have addressed and rejected those arguments within the analysis for claim 1. For the foregoing reasons, Petitioner has shown that the combined teachings of *Ono* and *Cronin* disclose "wherein performing an etch process comprises performing a reactive ion etch process." We determine that Petitioner has established, by a preponderance of the evidence, that claim 9 would have been obvious over the combined teachings of *Ono* and *Cronin*.

G. Alleged Unpatentability of Claims
1, 2, 4, 6–8, and 10 as Anticipated by Koyama

1. Koyama

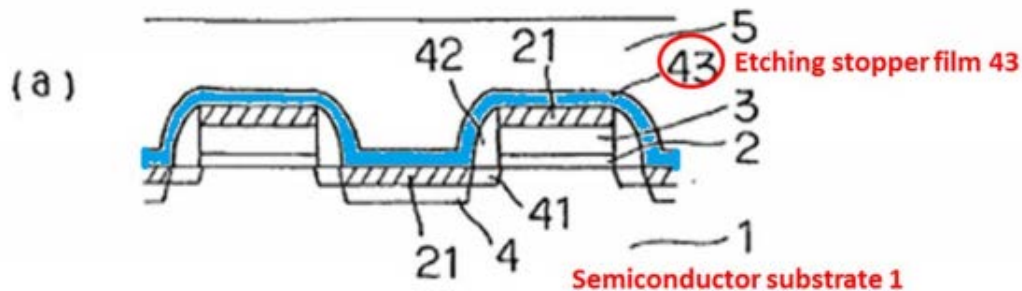
Koyama relates to a method of manufacturing a semiconductor device and, more particularly, to a method of forming a contact structure in the device. Ex. 1005 ¶ 2. Koyama states that its object is to form a contact hole without causing abnormal oxidation of a silicide layer over the substrate or contaminating the apparatus for film deposition. *Id.* ¶ 16. Koyama discloses that no silicide layers are exposed while forming the insulating film to provide sidewalls on the internal lateral faces of a contact hole. *Id.* ¶ 29. Koyama states: “In consequence, a minute contact can be formed well, without shortening the lifetime of carriers in the semiconductor device.” *Id.*

2. Claim 1

Claim 1 recites: “A method of providing a contact via to a surface of a substrate.” Ex. 1001, 4:17–18. Koyama discloses such a method. Ex. 1005 ¶¶ 2, 16, 23–28, 55–61 (cited at Pet. 41). Petitioner’s assertion is supported by the testimony of Dr. Rubloff. Ex. 1002 ¶¶ 109–110 (cited at Pet. 41).

Claim 1 further recites: “forming a first dielectric layer on the surface.” Ex. 1001, 4:19. As we discuss below, Petitioner has shown that Koyama discloses this step. Figure 4(a) of Koyama, as annotated by Petitioner on page 43 of the Petition, is reproduced below.

FIG. 4



The above figure is an annotated version of Figure 4(a) of Koyama, which is a schematic cross-sectional view illustrating the steps of an embodiment of a manufacturing method according to Koyama. Pet. 43; Ex. 1005 ¶ 34.

As indicated above in the discussion of Ono and claim 1, “the surface” in claim 1 refers to the surface of the substrate. Koyama describes:

Next, over the entire surface, an etching stopper film 43 made of a silicon nitride film or such with a thickness of 10 nm to 100 nm or so is formed. This etching stopper film can be grown well, for example, by the plasma CVD, which is characterized by excellent step coverage, at or below 500° C., say, at 250° C. to 450° C.

Id. ¶ 56 (cited at Pet. 42–43). Dr. Rubloff testifies that silicon nitride is a dielectric material. Ex. 1002 ¶ 112 (cited at Pet. 42). Koyama also states that “etching stopper film 43 made of a nitride film is *formed directly over the semiconductor substrate.*” Ex. 1005 ¶ 61 (cited at Pet. 42) (emphasis added). Petitioner identifies etching stopper film 43 as satisfying the claimed first dielectric layer, even though etching stopper film is formed over silicide layer 21. Pet. 43. Petitioner asserts that one with ordinary skill in the art “would have understood that forming the etching stopper film 43 on the surface of [the] silicide layer[] 21 constitutes forming the etching stopper film 43 on ‘a surface of a substrate’ 1, as claimed.” Pet. 43–44.

This assertion is supported by the testimony of Dr. Rubloff, who explains that one with ordinary skill in the art “would have known at the time of the alleged invention of the ’027 patent that the source and drain regions are part of a semiconductor substrate, and that Koyama’s silicide layer 21 is formed by way of silicide formation reaction between a metal film and the silicon of the dopant diffusion layers in the substrate.”¹⁸ Ex. 1002 ¶¶ 114–115 (cited at Pet. 44–45). Indeed, Koyama itself refers to “a silicide formation reaction between the metal film and silicon of the dopant diffusion layers.” Ex. 1005 ¶ 38 (cited at Pet. 44).

Dr. Rubloff further explains,

Therefore, given that the silicide formation reaction produces the silicide layer 21 primarily within the confines of the initial dopant diffusion layer 4, which in turn is part of the substrate 1, *Koyama*’s forming of the etching stopper film 43 on the surface of the silicide layer 21 constitutes “forming a first dielectric layer on the surface [of the substrate]” 1. Indeed, *Koyama* recognizes this point as it discloses that “**the etching stopper film 43 made of a nitride film is formed directly over the semiconductor substrate.**” (*Id.* at ¶ [0061] (emphasis added).) *Koyama* further confirms that the surface of the silicide layer 21 is the surface of the substrate 1 because as can be seen below, the surface of the exposed silicide layer 21 is essentially coplanar with the surface of the semiconductor substrate 1 just like the surface of the exposed source region 6 is flush with the semiconductor substrate 1 in the ’027 patent.

Ex. 1002 ¶ 116 (cited at Pet. 45). We find the above-noted testimony of Dr. Rubloff to be cogent and persuasive, notwithstanding the Patent Owner’s argument discussed below.

¹⁸ Dr. Rubloff explains that Koyama refers to the source and drain regions of the substrate as the dopant diffusion layers. Ex. 1002 ¶ 114 n.15. This characterization is not disputed by Patent Owner.

Patent Owner, on the other hand, argues,

As the silicide is formed directly over the source/drain regions, a person of ordinary skill in the art would understand that the etching stopper film 43, which Samsung contends is the “first dielectric layer,” is not in fact formed on the surface of the semiconductor substrate, but rather it is formed on the silicide. Ex. 2002 at ¶¶ 76–77; Ex. 1005 at ¶ 0056.

PO Resp. 30. It is undisputed, however, that the silicide is not added to and over the source and drain regions of the substrate, but formed by a chemical reaction between a metal film and the silicon within the source and drain regions of the substrate. Also, Dr. Rubloff’s testimony stands unrebutted that the silicide formation reaction produces the silicide layer 21 primarily within the confines of the underlying substrate, and that the surface of the silicide layer essentially is coplanar with the surface of the rest of the substrate. Further, Koyama itself states expressly that etching stopper film 43 is formed “directly over” the semiconductor substrate (Ex. 1005 ¶ 61).

To the extent there is conflicting testimony between Dr. Rubloff and Mr. Maltiel, regarding whether etching stopper film 43 is formed on the semiconductor substrate, we credit the testimony of Dr. Rubloff over that of Mr. Maltiel. For instance, Mr. Maltiel states that silicide is not a semiconductor material but is a conductive metal and therefore should not be considered as a part of the substrate. Ex. 2002 ¶ 43. However, Dr. Rubloff testifies,

I disagree that a silicide is a metal. A silicide is formed by reaction between metal (e.g., Ti) and silicon. The conductivity of a silicide is greater than pure silicon but that does not mean a silicide cannot be part of the substrate. I have reviewed Exhibit 2006 [cited by Mr. Maltiel] and it does not say that a silicide is a metal. In fact, a silicide is no different from the source/drain regions in the ’027 patent in the sense that the conductivity for

both is much greater than a bulk silicon substrate. Clearly, the '027 patent considers the source/drain regions to be part of the substrate (see Ex. 1001 at FIG. 6) and therefore, the mere difference in conductivity between the silicon substrate and the silicide region cannot imply that the silicide is not part of the substrate.

Ex. 1026 ¶ 18 (cited at Pet. 23). For the foregoing reasons, we find that silicide layer 21 in the source and drain region 4 in Koyama is a part of semiconductor substrate 1.

Even assuming that in Koyama the etching stopper film is not formed directly on the surface of the substrate, that would not undermine Petitioner's case, because, as we discussed above, forming a first dielectric layer on the surface of the substrate does not require forming the first dielectric layer "directly on" the surface of the substrate. *See supra* § II.C.1.

For the foregoing reasons, Petitioner sufficiently has shown that Koyama discloses the step of "forming a first dielectric layer on the surface [of the substrate]."

Claim 1 further recites: "forming a second dielectric layer on the first dielectric layer." Ex. 1001, 4:20–21. Koyama discloses this step. Specifically, with reference to Figure 4(a) shown above, Petitioner identifies interlayer insulating film 5 as the second dielectric layer recited in claim 1. Pet. 46–47. Koyama discloses that interlayer insulating film 5 is a silicon oxide film. Ex. 1005 ¶ 39 (cited at Pet. 46). As is shown in Koyama's Figure 4(a) reproduced above, interlayer insulating film 5, i.e., what Petitioner regards as the second dielectric layer, is formed on etching stopper film 43 which Petitioner regards as the first dielectric layer. Dr. Rubloff testifies that silicon oxide is a dielectric material. Ex. 1002 ¶ 119 (cited at

Pet. 46–47). Petitioner has shown that Koyama discloses the step of “forming a second dielectric layer on the first dielectric layer.”

Claim 1 further recites: “providing a first aperture which extends from a surface of the second dielectric layer toward the surface of the substrate for a distance which is less than a combined thickness of the first and second dielectric layers.” Ex. 1001, 4:22–25. Koyama’s Figure 4(b) is reproduced below (cited at Pet. 48):

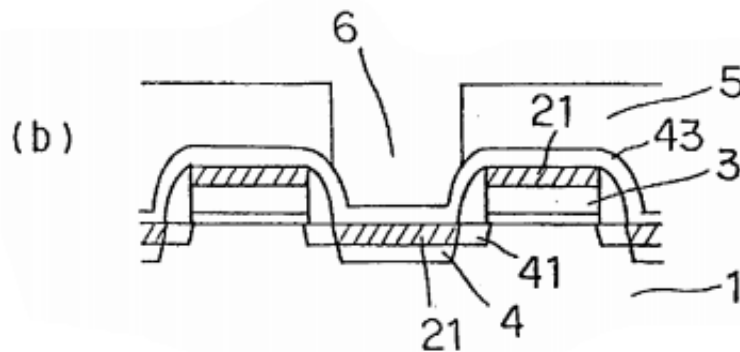


Figure 4(b) is a cross-sectional view illustrating a step of the manufacturing method for the semiconductor device disclosed in Koyama. Ex. 1005 ¶ 34. As shown in Figure 4(b) (cited at Pet. 47), a first aperture has been formed extending from a surface of the second dielectric layer (interlayer insulating film 5) toward the surface of the substrate for a distance that is less than the combined thickness of etching stopper film 43 (first dielectric layer) and interlayer insulating film 5 (second dielectric layer). In that regard, Koyama states: “[I]n the interlayer insulating film 5, an opening 6 is formed to reach the etching stopper film 43 by means of lithography and anisotropic etching.” *Id.* ¶ 57 (cited at Pet. 47). Thus, Petitioner has shown that Koyama discloses “providing a first aperture which extends from a surface of the second dielectric layer toward the surface of the substrate for a

distance which is less than a combined thickness of the first and second dielectric layers.”

Claim 1 further recites: “providing a third dielectric layer covering a surface of the first aperture and an exposed surface of the first dielectric layer.” Ex. 1001, 4:27–29. Figure 4(c) of Koyama is reproduced below (cited at Pet. 49):

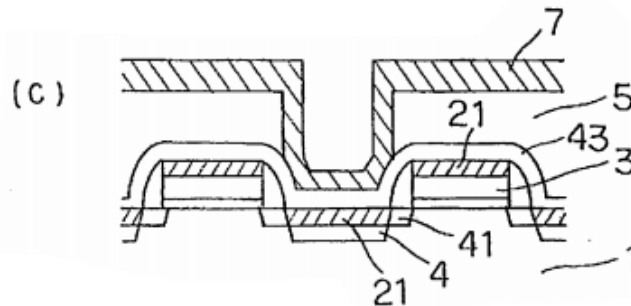


Figure 4(c) is a cross-sectional views illustrating another step of the manufacturing method for the semiconductor device disclosed in Koyama. Ex. 1005 ¶ 34.

Koyama discloses that subsequent to the placement of interlayer insulating film 5, insulating film 7, formed from silicon oxide, is placed over the entire surface of the device. *Id.* ¶ 58 (cited at Pet. 49). Dr. Rubloff testifies that, as is shown in Figure 4(c) of Koyama, insulating film 7 is provided such that it covers a surface of opening 6 and also the exposed surface of etch stopper film 43. Ex. 1002 ¶ 123 (cited at Pet. 49). Dr. Rubloff also testifies that silicon oxide is a dielectric material. *Id.* ¶ 119 (cited at Pet. 46–47). Petitioner identifies etch stopper film 43 as the first dielectric layer and insulating film 7 as the third dielectric layer. Pet. 43, 49. Thus, Petitioner has shown that Koyama discloses “providing a third dielectric layer covering a surface of the first aperture and an exposed surface of the first dielectric layer.”

Claim 1 further recites: “removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.” Ex. 1001, 4:30–32. Figure 4(d) of Koyama is reproduced below (cited at Pet. 50):

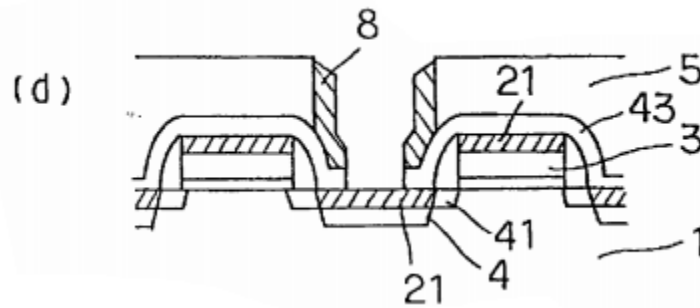


Figure 4(d) is a cross-sectional view illustrating yet another step of the manufacturing method for the semiconductor device disclosed in Koyama. Ex. 1005 ¶ 34.

With respect to Figure 4(b), Koyama describes:

[A]n etch back is performed over the entire surface by anisotropic etching such as the RIE, whereby [the] portion of the insulating film 7 lying in the bottom section of the opening is removed to make sidewalls 8 formed on the internal lateral faces of the opening and then the etching stopper film 43 lying in the bottom section of the opening is removed to expose the silicide layer 21 which is laid on top of the dopant diffusion layer (FIG. 4(d)).

Id. ¶ 59 (cited at Pet. 50). On the basis of that disclosure, Dr. Rubloff testifies that removing the etching stopper layer 43 at the bottom of the opening would expose the portion of the surface of the substrate on which the etching stopper film 43 is formed. Ex. 1002 ¶ 126 (cited at Pet. 50–51). With regard to silicide layer 21, Dr. Rubloff explains that it is primarily within the confines of the initial dopant diffusion layer 4 that is a part of the substrate, and that the surface of silicide layer 21 is essentially coplanar with

the surface of substrate 1. Ex. 1002 ¶ 116 (cited at Pet. 45). Thus, Dr. Rubloff explains that exposing the surface of silicide layer 21 is the same as exposing the surface of substrate 1. *Id.* ¶ 126 (cited at Pet. 51).

Patent Owner advances the same argument it asserted with respect to the step of “forming a first dielectric layer on the surface.” Specifically, Patent Owner contends that in Koyama, the silicide layer is not the surface of the semiconductor substrate. PO Resp. 31. We already discussed and rejected that argument, in the context of the analysis for the step of “forming a first dielectric layer on the surface.” *See supra* § II.C.1. For the same reasons, we reject Patent Owner’s argument.

Thus, Petitioner has shown persuasively that Koyama discloses the step of “removing a portion of the third dielectric layer and a portion of the first dielectric layer to expose a portion of the surface of the substrate.” Having considered the arguments and evidence of record, we determine Petitioner has shown, by a preponderance of the evidence, that claim 1 is anticipated by Koyama.

3. Claims 2, 4, 6–8, and 10

Claim 2 depends from claim 1 and further recites: “wherein forming a first dielectric layer on the surface comprises depositing a layer of silicon nitride on the surface.” Ex. 1001, 4:33–35. Koyama discloses that its etching stopper film 43 is made of silicon nitride film. Ex. 1005 ¶¶ 56, 61 (cited at Pet. 51). Dr. Rubloff also testifies that Koyama discloses the added limitation of claim 2 about depositing a layer of silicon nitride on the surface of the substrate. Ex. 1002 ¶¶ 127–128 (cited at Pet. 51). Thus, we are persuaded that Koyama discloses the limitation “wherein forming a first dielectric layer on the surface comprises depositing a layer of silicon nitride

on the surface.” Having considered the arguments and evidence of record, we determine Petitioner has shown, by a preponderance of the evidence, that claim 2 is anticipated by Koyama.

Claim 4 depends from claim 2 and further recites: “wherein depositing a layer of silicon nitride comprises depositing the layer of silicon nitride using a chemical vapor deposition process.” Ex. 1001, 4:39–41. Koyama discloses that etching stopper film 43 can be grown by “plasma CVD.” Ex. 1005 ¶ 56 (cited at Pet. 52). Koyama also explains that “CVD” means chemical vapor deposition. *Id.* ¶ 7 (cited at Pet. 52). Thus, we are persuaded that Koyama discloses the limitation “wherein depositing a layer of silicon nitride comprises depositing the layer of silicon nitride using a chemical vapor deposition process.” Having considered the arguments and evidence of record, we determine Petitioner has shown, by a preponderance of the evidence, that claim 4 is anticipated by Koyama.

Claim 6 depends from claim 1 and further recites: “wherein removing a portion of the third dielectric layer and the first dielectric layer to expose a portion of the surface of the material comprises performing an anisotropic etch process.” Ex. 1001, 4:47–50. As discussed above, we understand the term “the material” as specifically identifying the surface of the substrate. Koyama describes that insulating film 7 at the bottom of the opening is removed by anisotropic etching such as RIE. Ex. 1005 ¶ 59 (cited at Pet. 53). Dr. Rubloff also testifies that the added limitation of claim 6 is disclosed by Koyama. Ex. 1002 ¶¶ 131–132 (cited at Pet. 53). We are persuaded that Koyama discloses the limitation “wherein removing a portion of the third dielectric layer and the first dielectric layer to expose a portion of the surface of the material comprises performing an anisotropic etch

process.” Having considered the arguments and evidence of record, we determine Petitioner has shown, by a preponderance of the evidence, that claim 6 is anticipated by Koyama.

Claim 7 depends from claim 1 and further recites: “wherein forming a second dielectric layer on the first dielectric layer comprises forming a layer of silicon dioxide on the first dielectric layer.” Ex. 1001, 4:51–53. Koyama discloses that interlayer insulating film 5 comprises silicon oxide or Boron Phosphorous Silicate Glass (BPSG) film. Ex. 1005 ¶ 39 (cited at Pet. 54). Dr. Rubloff testifies that in the field of semiconductor device fabrication techniques, one with ordinary skill in the art would have understood that the term “silicon oxide” is used to refer to “silicon dioxide,” because one with ordinary skill in the art would have understood that silicon oxide is not stoichiometrically balanced. Ex. 1002 ¶ 134 (cited at Pet. 54). Also, Dr. Rubloff testifies that one with ordinary skill in the art would have known that BPSG includes silicon dioxide because BPSG is a material including silicon dioxide doped with boron (B) and phosphorous (P). *Id.* Thus, we are persuaded that Koyama discloses the limitation “wherein forming a second dielectric layer on the first dielectric layer comprises forming a layer of silicon dioxide on the first dielectric layer.” Having considered the arguments and evidence of record, we determine Petitioner has shown, by a preponderance of the evidence, that claim 7 is anticipated by Koyama.

Claim 8 depends from claim 1 and further recites: “wherein providing the first aperture comprises performing an etch process.” Ex. 1001, 4:54–55. Koyama states: “[A]s shown in FIG. 4(b), in the interlayer insulating film 5, an opening is formed to reach the etching stopper film 43 by means of lithography and anisotropic etching.” Ex. 1005 ¶ 57 (cited at Pet. 55).

Dr. Rubloff also testifies that the added limitation of claim 8 is disclosed by Koyama. Ex. 1002 ¶ 135 (cited at Pet. 55). Thus, we are persuaded that Koyama discloses the limitation “wherein providing the first aperture comprises performing an etch process.” Having considered the arguments and evidence of record, we determine Petitioner has shown, by a preponderance of the evidence, that claim 8 is anticipated by Koyama.

Claim 10 depends from claim 1 and further recites: “wherein removing a portion of the third dielectric layer and the first dielectric layer comprises performing a reactive ion etch.” Ex. 1001, 4:59–61. Koyama describes that insulating film 7 at the bottom of the opening is removed by anisotropic etching such as RIE. Ex. 1005 ¶ 59 (cited at Pet. 56). Koyama also identifies “RIE” as reactive ion etching. *Id.* ¶ 10 (cited at Pet. 56). Dr. Rubloff also testifies that the added limitation of claim 10 is disclosed by Koyama. Ex. 1002 ¶ 136 (cited at Pet. 56). Thus, we are persuaded that Koyama discloses the limitation “wherein removing a portion of the third dielectric layer and the first dielectric layer comprises performing a reactive ion etch.” Having considered the arguments and evidence of record, we determine Petitioner has shown, by a preponderance of the evidence, that claim 10 is anticipated by Koyama.

H. Alleged Unpatentability of Claims
3 and 5 as Obvious over Koyama and Ngo

1. Claim 3

Claim 3 depends from claim 1 and further recites: “wherein forming a first dielectric layer on the surface comprises depositing a layer of silicon oxynitride on the surface.” Ex. 1001, 4:36–38. Koyama by itself does not meet this limitation, because in Koyama the first dielectric layer identified

by Petitioner, i.e., etching stopper film 43, is formed of silicon nitride. Ex. 1005 ¶ 56 (cited at Pet. 57). Dr. Rubloff testifies, however, that “[a] person of ordinary skill in the art would have been motivated to modify *Koyama* such that the etching stopper film 43 is a silicon oxynitride film based on the teachings of *Ngo*.” Ex. 1002 ¶ 138 (cited at Pet. 57). *Ngo* describes depositing stop gap layer 22’, “for example silicon oxynitride” on a semiconductor substrate. Ex. 1012, 6:12–15 (cited by Dr. Rubloff at Ex. 1002 ¶ 141 (cited at Pet. 57)).

With regard to that motivation, Dr. Rubloff testifies:

Ngo’s stop layer 22’ is analogous to *Koyama*’s etching stopper film 43, as the stop layer 22’ has a function similar to *Koyama*’s etching stopper film 43, i.e., to minimize “the possibility of etching into substrate 12 . . . [because] [w]ithout stop layer 22, the etching process would likely extend too far into substrate 12 which could damage existing structures therein and/or cause circuit failures.” (*Id.* at 2:7–18.) Although *Ngo* does not specifically disclose the function of its [stop layer 22’], a person of ordinary skill in the art would have readily understood that the function of its stop layer 22’ is similar to the function of the stop layer 22 disclosed in *Ngo* with respect to a prior art embodiment (*e.g.*, compare [Ex. 1012] at FIG. 1 (showing prior-art semiconductor device with stop layer 22) with *id.* at FIG. 2(b) (showing *Ngo*’s semiconductor device with stop layer 22’)).

Ex. 1002 ¶ 139 (cited at Pet. 57). Dr. Rubloff further explains:

One of ordinary skill would have looked to *Ngo* to refine the teachings of *Koyama* because both references relate to semiconductor fabrication and both disclose etch stop layers. Having looked to *Ngo*, a person of ordinary skill in the art would have been motivated to combine *Koyama*’s teachings with *Ngo*’s teachings in this manner [using silicon oxynitride as the etching stopper film 43 instead of silicon nitride] because silicon oxynitride was a well-known alternative to silicon nitride for use as an etch stop film during the formation of contact structures. For example, *Ngo* itself discloses that the stop layer 22 could be

“silicon nitride or silicon oxynitride,” thereby suggesting that silicon nitride or silicon oxynitride could be used interchangeably as the material for forming the stop layer. (*Id.* at 4:57–60.) As discussed earlier, the prior art in the semiconductor fabrication technical fields is replete with similar disclosures of silicon nitride and silicon oxynitride being interchangeable for the purpose of forming etch stop films.

Id. ¶ 142 (cited at Pet. 57–58). Dr. Rubloff then cites to certain other references outside of the asserted grounds to support his opinion that silicon nitride and silicon oxynitride are recognized in the art as interchangeable for purposes of forming an etch stop layer. *Id.* (citing Ex. 1006, 6:7–13, 6:48–58; Ex. 1007, 1:14–19; Ex. 1013, 6:27–33).

Patent Owner argues that Petitioner’s reason for applying Ngo’s teaching in Koyama is too generic to be meaningful. PO Resp. 32. We disagree. Whether the reasoning is too vague depends on what teaching is relied on for the combination. Here, Petitioner is relying on Ngo’s teaching that silicon nitride and silicon oxynitride are interchangeable etch stop layer materials. In that context, Petitioner shows sufficiently that Koyama and Ngo both relate to semiconductor fabrication and disclose use of etch stop layers and that, according to Ngo, silicon nitride and silicon oxynitride are interchangeable as the material for an etch stop layer.

Patent Owner further argues that Koyama and Ngo are aimed at solving different problems and therefore one with ordinary skill in the art would not have thought to use Ngo’s teaching in Koyama.¹⁹ *Id.* The

¹⁹ According to Patent Owner, while Koyama is concerned with forming a contact well while preventing “abnormal oxidation” of the silicide layer on the substrate, Ngo is concerned with reducing outgassing defects during formation of a stop layer and subsequent dielectric layers. PO Resp. 33.

argument is misplaced. A prior art reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect. *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985). The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned, as they are a part of the literature and are relevant for all they contain. *In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) (citing *In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968)). The different focus of Koyama and Ngo, as noted by Patent Owner, does not diminish the applicability of Ngo's disclosure regarding the use of silicon nitride or silicon oxynitride as an etch stop layer.

Patent Owner then argues that one with ordinary skill in the art would not have used silicon oxynitride as the etch stop layer in Koyama because the purpose of Koyama is to prevent "abnormal oxidation" of the silicide layer, and one with ordinary skill in the art would have known that depositing silicon oxynitride on top of the silicide would lead to "abnormal oxidation" of the silicide. PO Resp. 33. Patent Owner further asserts that the oxygen from the silicon oxynitride would be driven into the silicide layer. *Id.* Patent Owner cites to the testimony of its declarant, Mr. Maltiel, but the cited testimony does not adequately support Patent Owner's assertions.

Mr. Maltiel testifies:

Ngo teaches a method of eliminating the defects due to outgassing by depositing CVD at a much higher temperature than typically done. "Prior art deposition processes tend to maintain the deposition temperature at less than 400 C." Ex. 1012 at 4:56–57. Ngo further states that "the present invention, however, it has been determined that higher deposition temperatures have the

benefit of substantially reducing the outgassing defects that the prior art deposition processes tend to suffer from” *Id.* at 4:66–6:2. Thus, combining Ngo’s CVD deposition at a higher temperature with Koyama would exacerbate the problem that Koyama is trying to solve.

Ex. 2002 ¶ 82. As such, Mr. Maltiel explained only that a higher deposition temperature for silicon oxynitride would substantially reduce outgassing defects. Mr. Maltiel did not testify that the oxygen in the silicon oxynitride would be driven into the silicide layer. Nor does his testimony establish why a higher deposition temperature for silicon oxynitride would lead to more oxidation of the silicide and why any such increased oxidation constitutes “abnormal oxidation.”

More importantly, Patent Owner and Mr. Maltiel incorrectly assume that the objective of Ngo to reduce outgassing defects must be preserved in the combined teachings of Koyama and Ngo. But that is not required in the context of obviousness. As we noted above, prior art must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect. *See EWP Corp.*, 755 F.2d at 907. Also, the use of patents as references is not limited to what the patentees describe as their inventions or to the problems with which they are concerned. *In re Heck*, 699 F.2d at 1333. Koyama is not concerned with reducing outgassing defects. Therefore, when depositing silicon oxynitride in Koyama, a higher temperature than that which was typically used is not required.

Dr. Rubloff testifies that a person of ordinary skill in the art would have understood that silicon oxynitride could be formed on the silicide layer in Koyama without triggering abnormal oxidation, and explains as follows:

Ngo discloses that prior art deposition techniques for silicon oxynitride “maintain the deposition temperature at less than 400° C.” (Ex. 1012 at 4:56–57.) Therefore Ngo confirms that a person of ordinary skill in the art at the time of the alleged invention of the ’027 patent would have been able to deposit a silicon oxynitride layer at temperatures below 600° C or even 500° C. Moreover, the specific silicon oxynitride formation technique that Ngo discloses as part of its invention is only 480° C. (*Id.* at 5:3–5.) Because *Koyama* indicates that abnormal oxidation will not occur at temperatures below 600° C, it would have been apparent that even a temperature as high as 480° C for the deposition of silicon oxynitride is low enough to avoid abnormal oxidation of Koyama’s silicide layer. (Ex. 1005 at ¶ [0056].)

Ex. 1026 ¶ 20 (cited at Reply 24). Notably, Koyama describes:

Further, as this etching stopper film is grown on the surface where silicide layers are exposed, the deposition of the film is to be carried out preferably at or below 600° C., and more preferably at or below 500° C, from the viewpoints of preventing abnormal oxidation of the silicide layers and metal contamination of the apparatus for film deposition.

Ex. 1005 ¶ 56 (cited at Ex. 1026 ¶ 20). This disclosure supports

Dr. Rubloff’s testimony that Koyama itself indicates that that abnormal oxidation, in the context of Koyama, will not occur at temperatures below 600° C. Alternatively, and the very least, it indicates that any “abnormal oxidation” that occurs at a deposition temperature below 600° C is acceptable.

Based on the foregoing, we credit the testimony of Dr. Rubloff over the contrary testimony of Mr. Maltiel. Accordingly, Petitioner has presented sufficient motivation for one with ordinary skill in the art to modify Koyama by using silicon oxynitride, instead of silicon nitride, as etching stopper film 43. On the entire trial record, we determine Petitioner has established, by a

preponderance of the evidence, that claim 3 would have been obvious over the combined teachings of Koyama and Ngo.

2. Claim 5

Claim 5 depends from claim 3 and further recites: “wherein depositing a layer of silicon oxynitride comprises depositing the layer of silicon oxynitride using a chemical vapor deposition process.” Ex. 1001, 4:42–45. The combined teachings of Koyama and Ngo discloses this feature.

Koyama discloses that depositing the etching stopper film 43 step includes depositing a silicon nitride layer by using plasma chemical vapor deposition (CVD). Ex. 1005 ¶ 56 (cited at Pet. 60). In the context of claim 3, we have discussed why it would have been obvious to one with ordinary skill in the art, in light of Ngo’s disclosure, to form Koyama’s etching stopper film layer 43 with silicon oxynitride instead of silicon nitride. Here, we note further that Ngo specifically discloses forming its silicon oxynitride layer in a “PECVD system.” Ex. 1012, 6:12–17 (cited at Pet. 61).

We have explained above, in Section II.E.3, when discussing claim 5 in the context of alleged unpatentability over Ono and Ngo, how Ngo discloses using chemical vapor deposition to deposit silicon oxynitride. That is similar to Koyama’s disclosure of using plasma chemical vapor deposition to deposit silicon nitride. Petitioner asserts that it would have been obvious to one with ordinary skill in the art to have used chemical vapor deposition to deposit Koyama’s etching stopper film 43 layer even when silicon oxynitride has been substituted for silicon nitride. Pet. 61. The assertion is

supported by the testimony of Dr. Rubloff that is cited by Petitioner. *See id.* at 61–62 (citing Ex. 1002 ¶¶ 146–147). In that regard, Dr. Rubloff testifies:

[T]he combined *Koyama-Ngo* method would have led to the expected outcome of depositing silicon oxynitride as the etching stopper film 43 in *Koyama*, and therefore would have been predictable. In particular, the combined *Koyama-Ngo* method would merely be a combination of known elements (forming the etching stopper film 43 using silicon oxynitride in the combined *Koyama-Ngo* minute contact structure formation method) using a known technique (PECVD, as disclosed by *Ngo* as well) to achieve the expected result of forming an etching stopper film 43.

Ex. 1002 ¶ 146. In light of Dr. Rubloff’s testimony, and the fact that *Ngo* explicitly describes using chemical vapor deposition to form its layer of oxynitride, we find that Petitioner has articulated reasoning with a rational underpinning why one with ordinary skill would have used chemical vapor deposition to form the oxynitride layer when an oxynitride layer is formed according to the combined teachings of *Koyama* and *Ngo*.

Patent Owner does not advance any argument for claim 5 separate from those it has asserted for claim 3. PO Resp. 34. We have, however, already discussed and rejected Patent Owner’s arguments in the context of claim 3.

For the foregoing reasons, Petitioner has shown that the combined teachings of *Koyama* and *Ngo* discloses “wherein depositing a layer of silicon oxynitride comprises depositing the layer of silicon oxynitride using a chemical vapor deposition process.” Petitioner has established, by a preponderance of the evidence, that claim 5 would have been obvious over *Koyama* and *Ngo*.

I. Alleged Unpatentability of Claim 9
as Obvious over Koyama and Cronin

Claim 9 depends from claim 8 and further recites: “wherein performing an etch process comprises performing a reactive ion etch process.” Ex. 1001, 4:56–58. In the context of claim 8 discussed above, “performing an etch process” refers to the etching that creates the first aperture. Petitioner acknowledges that Koyama does not disclose that the first aperture is created by way of a reactive ion etch process. Pet. 63. Petitioner, however, identifies Cronin as disclosing performing reactive ion etching when forming a first aperture during a contact structure fabrication process for a semiconductor device. *Id.* at 63–64. In that regard, Petitioner refers to Figure 3 of Cronin (*id.* at 64), which is reproduced below:

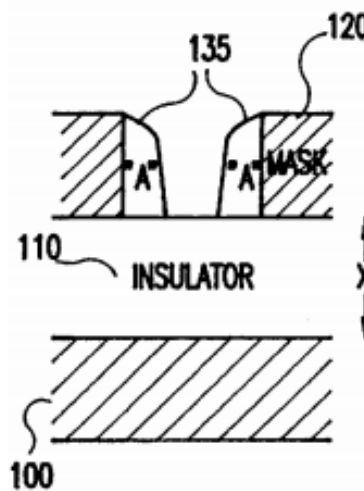


FIG.3

Figure 3 of Cronin illustrates a cross-sectional view of a semiconductor device after it has been etched by reactive ion etching to form sidewall spacers 135. Ex. 1008, 2:27–28, 3:10–12.

Petitioner asserts:

Cronin discloses directionally etching a conformal layer 130, which is a dielectric layer made from silicon oxide or silicon nitride, using a reactive ion etch (RIE) to form sidewall spacers. (Ex. 1008, 1:7–13.) (*Supra*, Section IX.C.1.) The conformal layer 130 penetrated to form the opening in *Cronin* is analogous to the interlayer insulating film 5 (also a dielectric) of *Koyama* which is penetrated to form the opening 6. (*Supra*, Section IX.C.1.) (Ex. 1008, FIG. 3; Ex. 1005, ¶ [0057], FIG. 4(b).)

Pet. 63–64. This assertion is directly supported by the testimony of Dr. Rubloff. Ex. 1002 ¶ 152 (cited at Pet. 64). Dr. Rubloff further explains why one with ordinary skill in the art would have applied Cronin’s teaching to Koyama:

In my opinion, a person having ordinary skill in the art would have looked to *Cronin* to refine the teachings of *Koyama* because both references relate to semiconductor fabrication and disclose the formation of contact holes and vias. Having looked to *Cronin*, a person of ordinary skill in the art would have been motivated to use RIE as the anisotropic etching technique to form the opening 6 in *Koyama*. For example, *Koyama* itself recognizes RIE [reactive ion etch] as a type of anisotropic etching that can be used in another step for etching back dielectric layers. ([Ex. 1005] at ¶ [0059], FIG. 4(d).) Moreover, *Cronin* explicitly discloses using RIE in a similar step as claim 9, i.e., during formation of a first aperture penetrating through the conformal layer 130 (analogous to interlayer insulating film 5, as explained above). Using RIE as disclosed by *Cronin* as the anisotropic etching technique to form the opening 6 in *Koyama* would have been nothing more than the utilization of a known technique (RIE) to improve a similar device (semiconductor device with opening 6 in *Koyama*) providing the predictable result of the opening 6 being formed such that the etching stopper film 43 is exposed in *Koyama*. Moreover, the ’027 patent does not disclose any advantages or unexpected results achieved by using RIE as the etch process for forming the first aperture.

Id. ¶ 153 (cited at Pet. 64).

Patent Owner does not advance, for claim 9, any argument separate from those it asserted in the context of independent claim 1. These arguments, however, already have been discussed and rejected above in our discussion of anticipation of claim 1 by Koyama.

For the foregoing reason, Petitioner has shown that the combined teachings of Koyama and Cronin discloses “wherein performing an etch process comprises performing a reactive ion etch process.” Petitioner has established, by a preponderance of the evidence, that claim 9 would have been obvious over Koyama and Cronin.

III. CONCLUSION

Petitioner has established, by a preponderance of the evidence, that each of claims 1, 2, 4, 6–8, and 10 is anticipated by Ono.

Petitioner has established, by a preponderance of the evidence, that each of claims 3 and 5 would have been obvious over Ono and Ngo.

Petitioner has established, by a preponderance of the evidence, that claim 9 would have been obvious over Ono and Cronin.

Petitioner has established, by a preponderance of the evidence, that each of claims 1, 2, 4, 6–8, and 10 is anticipated by Koyama.

Petitioner has established, by a preponderance of the evidence, that each of claims 3 and 5 would have been obvious over Koyama and Ngo.

Petitioner has established, by a preponderance of the evidence, that claim 9 would have been obvious over Koyama and Cronin.

IV. ORDER

It is

ORDERED that each of claims 1–10 of the ’027 patent is unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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