

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01419
Patent 6,562,714 B1

Before JAMESON LEE, KEVIN F. TURNER, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

TURNER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition for *inter partes* review of claims 1–5, 7–13, and 16 of U.S. Patent No. 6,562,714 B1 (Ex. 1001, “the ’714 Patent”). Paper 1 (“Pet.”). We instituted review of all claims 1–5, 7–13, and 16 on all grounds asserted in the Petition. Paper 7 (“Dec. on Inst.”). ProMOS Technologies, Inc. (“Patent Owner”) filed a Patent Owner Response.¹ Paper 13. In response thereto, Petitioner filed a Reply.^{2, 3} Paper 20. Oral hearing was held on August 16, 2018. A copy of the transcript for the oral hearing has been entered as Paper 32.

We determine that Petitioner has shown by a preponderance of the evidence that each of claims 1–5, 7–13, and 16 is unpatentable.

A. Related Matters

The parties inform us that the challenged patent is the subject of a district court proceeding in the District of Delaware, captioned *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:16-cv-00335-SLR (D. Del.). Pet. 1, Paper 4. In that action, Patent Owner has asserted other patents against Petitioner, and Petitioner has filed *inter partes* review petitions against those other patents in IPR2017-01412, IPR2017-01413, IPR2017-01414, IPR2017-01415, IPR2017-01416, IPR2017-01417, and

¹ Patent Owner also filed a declaration of Mr. Ron Maltiel in support of the Patent Owner Response. Ex. 2003.

² Petitioner also filed a rebuttal declaration of Dr. Stanley Shanfield in support of Petitioner’s Reply. Ex. 1022.

³ Patent Owner filed a Motion for Observations on Cross-Examination. Paper 26. Petitioner filed a Response to Patent Owner’s Motion for Observations on Cross-Examination. Paper 28. We have considered both submissions.

IPR2017-01418. Pet. 1, Paper 4.

Petitioner also identifies these *inter partes* review proceedings, initiated by petitions filed by Petitioner, as involving additional patents asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:15-cv-00898-SLR-SRF (D. Del.): IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. Pet. 1–2.

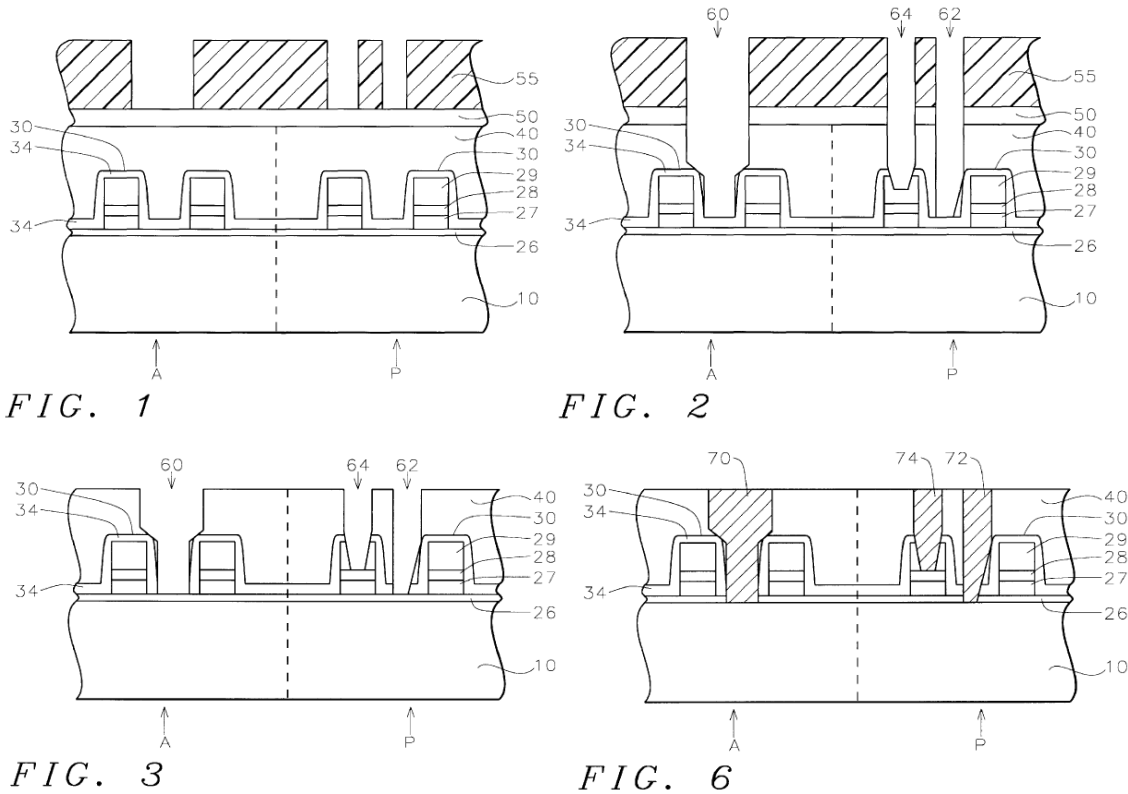
B. The '714 Patent

The '714 Patent is titled “Consolidation method of junction contact etch for below 150 nanometer deep trench-based DRAM devices.” Ex. 1001, [54]. The patent issued on May 13, 2003, from an application filed on November 6, 2001. *Id.* at [45], [22]. The patent is directed to “a method of fabricating deep trench DRAM devices in the fabrication of integrated circuits.” *Id.* at Abstract, 1:5–12.

The '714 Patent discloses that “[t]he consolidation junction contact etch of the present invention makes it possible to consolidate all the junction contact etch steps using one mask.” Ex. 1001, 3:15–17. In conventional techniques, contacts in the array (bit line contacts) and contacts in the periphery (substrate and gate contacts) are formed separately. *Id.* at 1:15–21, 30–37. As dimensions shrink, the risk of shorts between the contacts increases and this can lead to deleterious short channel effects, lowering of the threshold voltage as gate length decreases, junction leakage, and lowering of the effective saturation current. *Id.* at 1:37–50.

To ameliorate the above-discussed effects, the '714 Patent proposes consolidating the formation of contacts in the array (bit line contacts) and

the periphery (substrate and gate contacts) using a single mask with a highly selective self-aligned contact etch scheme in combination with aspect ratio etch rate characteristics. Ex. 1001, 1:65–2:7, 2:35–44, 4:23–28. The following figures from the '714 Patent illustrate these processes:



Id. at Figs. 1–3, 6. Figures 1–3 and 6 are cross-sectional representations of semiconductor devices. *Id.* at 2:30–31.

Figure 1 illustrates a semiconductor device with the gate conductor/interconnection lines 30 formed overlying the semiconductor substrate 10 and gate oxide layer 26, where the gate conductor may be formed from a first layer of polysilicon 27, a second layer of silicide 28, and a third layer of nitride 29. Ex. 1001, 2:45–56. A silicon nitride frame 34 is deposited over the gates 30, and thereafter an oxide inter-layer dielectric layer 40 is deposited and planarized. *Id.* at 2:56–3:5. An anti-reflective coating (ARC) layer 50 may then be deposited, followed by a photoresist

mask 55, with openings for the bit line contact (CB) 60, the substrate contact (CS) 62, and the gate contact (GC) 64, illustrated in Figure 2. *Id.* at 3:6–15, 26–33. The etching of the bit line contact 60 and substrate contact 62 opening stops at the silicon nitride frame 34, but for the gate contact 64 opening, the process etches through the nitride frame and into the capping silicon nitride layer 29 on top of a gate. *Id.* at 3:26–33, Fig. 2.

Figure 3 illustrates the process with the resist mask 55 and ARC layer 50 stripped away, and a highly anisotropic nitride etch is then used to remove the silicon nitride layer 34 at the bottom of the contact holes 60 and 62 and the remaining nitride layer 29 at the bottom of contact hole 64. Ex. 1001, 3:51–56. Subsequently, the remaining gate oxide layer 26 within the contact openings 60 and 62 is removed by either a wet etch or an in-situ dry etch. *Id.* at 4:4–7. The contacts are completed by filling the contact openings 60, 62, and 64 with a metal conductive layer (70, 72, 74), as shown in Figure 6, where the metal may be tungsten, titanium, aluminum, tungsten silicon, or the like. *Id.* at 4:15–19.

C. Illustrative Claim

Petitioner challenges claims 1–5, 7–13, and 16 of the '714 Patent, of which claims 1 and 9 are independent. Pet. 1. Claim 1 is illustrative of the subject matter of the challenged claims and reads as follows:

1. A method of forming contacts in the fabrication of an integrated circuit comprising:

- providing semiconductor device structures in and on a substrate wherein said substrate is divided into an array area and a periphery area;

- covering said semiconductor device structures with an etch stop layer;

- depositing a dielectric layer overlying said etch stop layer;

concurrently first etching through said dielectric layer in said array area to form bit line contact openings and etching through said dielectric layer in said periphery area to form substrate contact openings and through said dielectric layer to form gate contact openings wherein said etching stops at said etch stop layer;

second etching through said etch stop layer using a directional etch selective to said substrate wherein said second etching etches nitride transversely at least three times faster than laterally; and

filling said bit line contact openings, said substrate contact openings, and said gate contact openings with a conducting layer to complete said forming contacts in the fabrication of said integrated circuit device.

Ex. 1001, 4:35–57.

D. Instituted Grounds of Unpatentability

We instituted a trial based on the asserted grounds of unpatentability (“grounds”) set forth in the table below, relying in part on the declaration testimony of Dr. Stanley Shanfield (Ex. 1002). Dec. on Inst. 23.

Reference(s)	Basis	Challenged Claim(s)
Ohkawa, ⁴ Jeng, ⁵ and Matsuoka ⁶	§ 103	1, 2, 4, 5, 7–10, 12, 13, and 16
Ohkawa, Jeng, Matsuoka, and Chakravarti ⁷	§ 103	3 and 11

⁴ U.S. Patent No. 6,091,154, issued July 18, 2000 (Ex. 1005, “Ohkawa”).

⁵ U.S. Patent No. 6,033,962, issued Mar. 7, 2000 (Ex. 1012, “Jeng”).

⁶ U.S. Patent No. 6,130,449, issued Oct. 10, 2000 (Ex. 1011, “Matsuoka”).

⁷ U.S. Patent No. 5,909,044, issued June 1, 1999 (Ex. 1007, “Chakravarti”).

II. ANALYSIS

A. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Consideration of the *Graham* factors “helps inform the ultimate obviousness determination.” *Apple v. Samsung Elecs. Co.*, 839 F.3d 1034, 1048 (Fed. Cir. 2016) (en banc), cert. denied, 138 S. Ct. 420 (2017).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. See *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

Thus, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. We analyze the challenges presented in the Petition in accordance with the above-stated principles.

B. Level of Ordinary Skill

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner proposes that a person of ordinary skill in the art at the time of the alleged invention of the ’714 Patent “would have had a master’s degree or higher in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and three to four years of experience in the design and fabrication of semiconductor devices.” Pet. 4 (citing Ex. 1002 ¶¶ 18–19).

Patent Owner does not address the level of ordinary skill in its Patent Owner Response, but its declarant, Mr. Maltiel, provides:

[A] person having ordinary skill in the relevant art at the time of invention is a person with a Bachelor’s of Science degree in material science, physics, electrical engineering, or chemical engineering and three to four years of practical experience in the development, design, processing, and manufacturing/testing of semiconductor chips and technology. That person would be familiar with the issues such as integrating an interconnecting layer in the structure of a fully processed semiconductor device. An individual with an advanced degree in material science, electrical engineering or chemical engineering, would require less experience in the development, design, processing, and

manufacturing/testing of semiconductor chips and technology (e.g., two to three years).

Ex. 2003 ¶ 39.

Based on the current record, we are concerned that Petitioner’s articulation contains no upper bounds, i.e., “a master’s degree or higher,” such that the level of ordinary skill proposed by Petitioner is not sufficiently specific. As such, we adopt the definition provided by Patent Owner’s declarant, namely: “a person having ordinary skill in the relevant art at the time of invention is a person with a Bachelor’s of Science degree in material science, physics, electrical engineering, or chemical engineering and three to four years of practical experience in the development, design, processing, and manufacturing/testing of semiconductor chips and technology.”

We further find that this definition comports with Dr. Shanfield’s declaration testimony (*see* Ex. 1002 ¶ 18), such that both declarants appear to be addressing the same level of ordinary skill in the art. Additionally, we determine that the level of ordinary skill in the art is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Claim Construction

In this *inter partes* review, we give the claim terms their broadest reasonable interpretation in light of the Specification. 37 C.F.R. § 42.100(b) (2016). Under the broadest reasonable interpretation standard, and absent any special definitions, claim terms are generally given their ordinary and customary meaning, as would be understood by one of ordinary skill in the

art, in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In the Decision on Institution, we acknowledged that Petitioner did not propose an express construction for any claim terms, and Patent Owner contended that “filling” contact openings “to complete said forming contacts” (recited in independent claims 1 and 9) should have a specific meaning. Dec. on Inst. 10 (citing Pet. 8; Prelim. Resp. 12–16). Although we did not provide an explicit construction, we discussed Patent Owner’s contentions later in the context of analyzing the asserted grounds. *Id.* at 18–20.

In its Response, Patent Owner again argues that we should provide an explicit construction for the “filling” steps in independent claims 1 and 9. PO Resp. 10. Patent Owner contends that “filling,” as a verb, “means to make full or to put as much as can be held into.” *Id.* at 11 (citing Ex. 2001, 493). Patent Owner also contends that the use of “and” in the claim limitation, i.e., “and said gate contact openings,” requires that all three contact openings must be filled, and further contends Ohkawa’s use of modifiers “partially” filled or “not completely” filled indicates that, in the absence of such modifiers, “filled” means completely full. *Id.* at 11 & n.7 (citing Ex. 2003 ¶ 43; Ex. 1005, 8:35–38, 18:52–54). Patent Owner also asserts that because the limitation recites “a conductive layer,” the process step requires the openings to be filled with the same layer, i.e., the same material. *Id.* at 11–12 (citing Ex. 1001, 4:15–17). Patent Owner further asserts that the “process of filling the contact openings is also the process step that finishes (‘completes’) forming the contacts in the fabrication process,” implying that no other material can be added to the openings to

form the contacts. *Id.* at 12 (citing Ex. 2003 ¶ 46). Lastly, Patent Owner argues that the contacts are “complete” when they are filled by the conductive layer, as that is how the term “complete” is used in the Specification of the ’714 Patent. *Id.* at 13–14 (citing Ex. 1001, 4:14–16).

In reply, Petitioner asserts that concurrent filling with the same conductive material is not required by independent claims 1 and 9. Pet. Reply 2–3. Petitioner also asserts that the plain meaning of the “filling” step limitations of claims 1 and 9 is that each listed opening is filled, and that Patent Owner could have specified any concurrency of the filling step, such as it did for the “concurrently first etching” steps. *Id.* at 3 (citing Ex. 1022 ¶ 6). Petitioner also argues that the language of claims 1 and 9 does not require each opening to be filled with the same material, only that they be filled with “a conducting layer,” and even taking into account the example from the Specification of the ’714 Patent detailing that the same material is used, it is impermissible to import such limitations into the claims. *Id.* at 4 (citing PO Resp. 12–13; Ex. 1001, 4:15–17, Fig. 6). Petitioner also replies that any construction of “complete” is unnecessary because “[Patent Owner] does not dispute that Petitioner’s prior art discloses completion of contact formation or ‘complete’ gate, bit line, and substrate contacts.” *Id.* at 5.

Petitioner also argues that “filling” does not necessarily mean “completely full.” Pet. Reply 5–9. Petitioner argues that “to construe ‘filling’ as requiring ‘*completely* filling’ should be rejected because it imposes a limitation that is not compelled by the intrinsic evidence or the plain meaning of the term as understood by a [person of ordinary skill in the art].” *Id.* at 5–6. Petitioner continues that a partially filled contact opening can satisfy the “filling” step, and cites to the testimony of Dr. Shanfield and

the deposition of Mr. Maltiel. *Id.* at 6–7 (citing Ex. 1002 ¶¶ 117–118; Ex. 1021, 117:1–119:10). Petitioner concludes that the plain meaning of “filling” would have been understood as “adding sufficient conductive material to the contact opening such that the resulting contact can serve its function of providing an electrical connection.” *Id.* at 8 (citing Ex. 1022 ¶ 3).

Having considered the parties’ arguments, we agree with Patent Owner that an explicit claim construction is warranted for the subject steps of “filling” contact openings to complete the contacts. Notwithstanding, we find persuasive Petitioner’s arguments that Patent Owner’s stipulations would unduly limit the broadest reasonable construction. As such, we construe the step of “filling said bit line contact openings, said substrate contact openings, and said gate contact openings with a conducting layer to complete said forming contacts in the fabrication of said integrated circuit device,” per claim 1, as a step that adds conductive material to three contact openings to make them full, such that it completes formation of a contact in each of the three openings. The similar step in independent claim 9 is similarly construed, with the exception that integrated circuit device is a DRAM integrated circuit device. *See* Ex. 1001, 5:32–35.

In arriving at these constructions, we do not agree that the “filling” steps require concurrent filling, or that the filling occur with the same material. As we discussed at oral hearing, the language of the “filling” steps is broad and does not require that the contact openings be filled at the same time. *See* Tr. 23:5–25:16. The use of “concurrently” in the etching steps of the claims illustrates that Patent Owner could have further limited the “filling” steps, but chose not to provide such limits. Even if the

Specification provides that the contact opening can be filled at the same time, we cannot import such limitations into the claims, where those claims have a broader scope. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1320 (Fed. Cir. 2005). Similarly, the “filling” steps require the contact opening to be filled with “a conducting layer,” but we find nothing in the claims that limits that layer to a single material. As Patent Owner’s counsel acknowledged at oral hearing, “assuming that there is some sort of conducting layer that could be deposited in that way that was some composite or [amalgam] of different materials and it was deposited into all three openings in the same step, I would say that would still meet the claim.” Tr. 22:16–19.

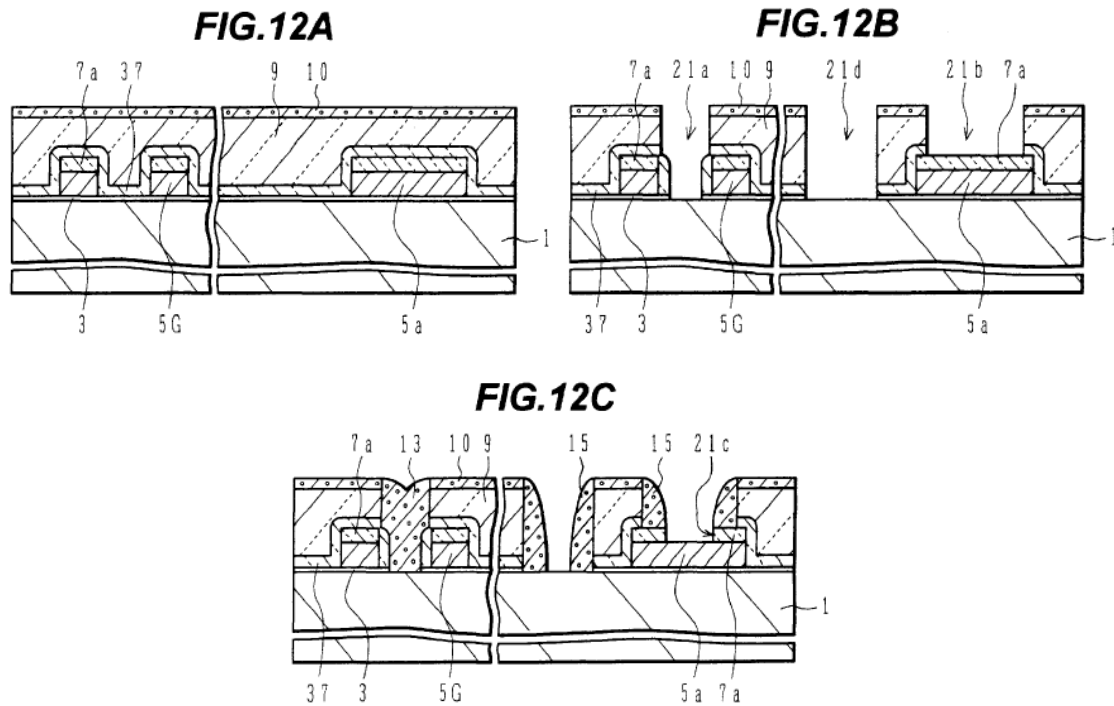
We are further persuaded that the process of the “filling” steps, i.e., “to complete said forming contacts,” addresses that the contacts are completed through the filling process, even though additional steps, such as patterning, may be subsequently needed to complete the overall integrated circuit device. *See* Tr. 18:23–19:11. Lastly, we maintain our determination from the Decision on Institution that “the plain meaning of ‘filling’ is to make full.” Dec. on Inst. 18. Regarding a “degree” of fullness required for any particular contact opening, we determine that sufficient conductive material must be introduced into each opening so that the resulting contact can serve its function of providing an electrical connection. In other words, contact openings are full as long as they provide an electrical connection, and one of ordinary skill in the art would have understood that the degree of fullness was sufficient.

D. Obviousness over Ohkawa, Jeng, and Matsuoka

Petitioner contends that claims 1–5, 7–13, and 16 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ohkawa, Jeng, and Matsuoka. Pet. 3, 9–72. Relying in part on the testimony of Dr. Shanfield and numerous citations to the references, Petitioner explains how the references purportedly would have conveyed the claim limitations and provides purported reasoning for combining the teachings of the references. *Id.* at 9–72. Patent Owner disputes these contentions and raises specific arguments that the references fail to teach or suggest all of the elements of independent claims 1 and 9. PO Resp. 14–57. We first review the cited references, discuss Petitioner’s contentions with respect to the claims, and consider Patent Owner’s counter-arguments.

1. Disclosure of Ohkawa

Ohkawa relates to “a semiconductor device with self-aligned contacts and its manufacture method.” Ex. 1005, Abstract, 1:12–15. Ohkawa discloses that its embodiments are described in detail “by taking DRAM [dynamic random access memory] as an example.” *Id.* at 7:6–8. Ohkawa discloses that in its semiconductor device, the substrate is divided into a memory cell portion MC and a peripheral circuit portion PC. *Id.* at 6:36–38, Figs. 10, 12A–12C. The device formation process, according to one embodiment, is illustrated in Figures 12A through 12C, reproduced below:



Id. at Figs. 12A–12C. Figures 12A–12C are cross sectional views of a semiconductor device in main manufacture processes. *Id.* at 6:42–44.

Ohkawa discloses that gate oxide film 3, gate electrode 5G, and first wiring layer 5a are formed on substrate 1. *Id.* at 18:29–35, Fig. 12A. Thereafter, SiN film 37, BPSG [borophosphosilicate glass] film 9 and a doped silicon layer 10 are formed thereon. *Id.* Contact holes 21a, 21b, and 21d, for a bit line contact BC, bit/gate contact BGC, and substrate contact BSC, respectively, are formed through selective etching. *Id.* at 18:36–39, Fig. 12B. Contact holes 21a, 21b, and 21d are filled or partially filled with a “conducting layer” such as doped silicon layer, W or TiN, to create plug 13 and side walls 15. *Id.* at 18:50–61, Fig. 12C.

2. Disclosure of Jeng

Jeng is directed to methods for forming self-aligned contact openings for a semiconductor device including a two-step, anisotropic reactive ion etching (RIE) procedure. Ex. 1012, Abstract. This includes a first step of

etching a BPSG layer 10 and a second step of etching silicon nitride layer 9c. *Id.* at 4:40–5:7, Figs. 4–6. Jeng discloses an anisotropic RIE of the thin silicon nitride layer 9c that etches silicon nitride layer 9c faster than the exposed silicon in a source/drain region 8 in the semiconductor substrate, using CH_2F_2 and CHF_3 as reactive gases, by a rate between 5 to 20 times faster with respect to the silicon or BPSG materials. *Id.* at 4:59–66. Jeng also discloses that the BPSG layer 10 “is deposited via LPCVD [low pressure chemical vapor deposition] or PECVD [plasma enhanced chemical vapor deposition] procedures.” *Id.* at 4:27–30.

3. *Disclosure of Matsuoka*

Matsuoka is directed to DRAM fabrication techniques. Ex. 1011, 1:5–10, 2:34–40. Matsuoka discloses that “[i]n the sectional view shown in the figure [1], a memory array region, in which memory array cells are formed, is disposed on the left side . . . and a peripheral circuit region, in which a peripheral circuit is formed, is disposed on the right side.” *Id.* at 6:44–49, Fig. 1. Matsuoka also discloses that contact holes are formed for interconnection to semiconductor regions (source and drain) selectively formed on the main surface of the substrate, where those “contact holes [are] for bitlines and storage nodes.” *Id.* at 7:10–15. Matsuoka specifically discloses forming bitline contacts 10 holes in the memory cell array region (*id.* at 9:33–38) and “contacts in the peripheral circuit region” (*id.* at 10:7–12) including “openings above the respective gates of the peripheral circuit” (*id.* at 9:54–56). *See id.* at Figs. 8–9.

4. *Petitioner’s Contentions Regarding Claims 1 and 9*

With respect to independent claims 1 and 9, Petitioner addresses the disclosures of Ohkawa, Jeng, and Matsuoka, as discussed above. Pet. 9–57,

60–71. Petitioner also contends that certain aspects of claims 1 and 9 are obvious over the cited references and proffers motivation to combine the references. *Id.* We discuss each in turn below.

Claim 1 recites, in part, “providing semiconductor device structures in . . . a substrate.” Petitioner acknowledges that Ohkawa’s Figure 12 does not illustrate any semiconductor device structures in substrate 1. *Id.* at 11. Petitioner, however, argues that Ohkawa’s first embodiment confirms the presence of source/drain regions in a DRAM, and that one of ordinary skill in the art would have understood that teachings of Figure 2A of Ohkawa would apply to Figure 12 so that source/drain regions would necessarily be present in the Figure 12 embodiment. *Id.* at 11–13.

Claim 1 also recites, in part, that “said substrate is divided into an array area and a periphery area.” Petitioner asserts that a person of ordinary skill in the art would have understood that the memory cell portion MC of Ohkawa is an array area of the substrate, and that the peripheral circuit portion PC of Ohkawa is a periphery area because the peripheral circuit portion PC is where peripheral circuits such as amplifiers, decoders, etc., are formed that are used to control and drive the memory cells in the array area. *Id.* at 16–19 (citing Ex. 1002 ¶ 65; Ex. 1013, 7:11–18, Figs. 3A–3G). We agree with the correspondence drawn by Petitioner.

Claim 1 further recites the step of “depositing a dielectric layer overlying said etch stop layer.” Petitioner cites Ohkawa as forming its BPSG film 9 “using the method similar to that described in FIGS. 8A and 8B,” and that one of ordinary skill in the art would have understood that to be performed through deposition. *Id.* at 21–23 (citing Ex. 1002 ¶ 72; Ex. 1005, 18:29–35). Petitioner also asserts that Jeng provides a disclosure

of its PBSG film being formed by chemical vapor deposition techniques, and it would have been obvious to form Ohkawa's PBSG film by similar methods in view of Jeng. *Id.* at 23–25 (citing Ex. 1002 ¶ 76; Ex. 1012, 4:27–30). Thus, Petitioner offers multiple rationales, i.e., that it would have been obvious to form Ohkawa's PBSG film through deposition processes disclosed in Ohkawa, or using the processes in Jeng. *Id.* at 25.

Claim 1 also recites concurrent etching steps to create the contact openings. Petitioner argues that Ohkawa discloses the use of a single mask to create the three contact holes (21a, 21b, 21d) and that one of ordinary skill in the art would have understood that the contact holes were concurrently formed. *Id.* at 26–28 (citing Ex. 1002 ¶ 80; Ex. 1005, 18:36–49, Figs. 12A, 12B). Petitioner also argues that it would have been obvious to implement the concurrent formation of the contact holes in view of Ohkawa's disclosure that “[t]here is a great need for reducing the number of processes, for example, by . . . forming contact holes to conductive layers of different levels at the same time in both the [memory cell and peripheral circuit] portions by the same process.” *Id.* at 28 (quoting Ex. 1005, 2:47–53). Thus, Petitioner argues that it would have been obvious to form the contact holes concurrently based on the teachings of Ohkawa alone or in view of Jeng.

Petitioner also argues that although Ohkawa and Jeng disclose the formation of one contact hole of each type, where claim 1 recites “contact openings,” i.e., multiples of each type, it would have been obvious to form plural contact holes in Ohkawa's DRAM integrated circuit because practical DRAM have plural memory cells and peripheral circuits. *Id.* at 32–33 (citing Ex. 1002 ¶ 87). To further this argument, Petitioner also discusses Matsuoka, discussed above, and argues that it would have been obvious to

one of ordinary skill in the art to modify the combination of Ohkawa and Jeng, in view of Matsuoka, to form plural contact holes, per claim 1, for the reasons provided. *Id.* at 33–38 (citing Ex. 1002 ¶ 94).

Claim 1 also recites, in part, “using a directional etch selective to said substrate.” Petitioner acknowledges that Ohkawa does not explicitly disclose the etching through the SiN film to be such a directional and selective etching, but asserts such etching would have been motivated by Jeng. *Id.* at 40 (citing Ex. 1002 ¶¶ 100–108). The etching silicon nitride layer 9c, in Jeng, occurs in a subsequent step and through an anisotropic reactive ion etch (RIE), detailing that it removes the silicon nitride layer 9c at a rate much faster than the rate at which the silicon in the source/drain region 8 is removed. *Id.* at 41–42 (citing Ex. 1012, 4:40–5:7, Figs. 4–6). Petitioner asserts that it would have been obvious to etch SiN film 37, in Ohkawa, using a directional etch selective to the substrate in view of Jeng. *Id.* at 43–44 (citing Ex. 1002 ¶¶ 107–108).

Claim 1 also recites, in part, that the second etching “etches nitride transversely at least three times faster than laterally.” Petitioner acknowledges that the degree of anisotropy of Jeng’s etch is not disclosed, but argues that the degree of anisotropy is a result-effective variable and finding an optimum value of a result effective variable in a known process was obvious. *Id.* at 44–45 (citing *In re Applied Materials, Inc.*, 692 F.3d 1289, 1295 (Fed. Cir. 2012)). Petitioner continues that one of ordinary skill in the art would have understood that it was desirable to obtain a highly anisotropic etch, and that would have provided the benefit of maintaining the silicon nitride sidewalls on the gate electrodes that are necessary for

insulating the gate electrodes from adjacent conductive elements. *Id.* at 45–50 (citing Ex. 1002 ¶¶ 111, 130; Exs. 1008, 1009).

Claim 1 also recites that the contact openings are filled “to complete said forming contacts in the fabrication of said semiconductor device.” Petitioner points out that Ohkawa’s contact hole 21a, in Ohkawa, is filled to form plug 13, and Ohkawa’s contact holes 21b and 21d, are “partially filled.” *Id.* at 50 (citing Ex. 1005, 18:50–65, Fig. 12C). Petitioner asserts that claim 1 does not “specify whether the contact opening must be partially or fully filled,” but also argues that it would have been obvious to one of ordinary skill in the art to completely fill all of the contact holes. *Id.* at 53 (citing Ex. 1002 ¶ 119). Petitioner continues that one of ordinary skill in the art would have understood that while contact hole 21d in the tenth embodiment is not shown as being completely filled by a conductive layer, Ohkawa acknowledges that a contact hole similar to 21d could be filled by a conductive plug (similar to plug 13). *Id.* at 56 (citing Ex. 1002 ¶ 123). We are persuaded that Petitioner’s assertions—that it would have been obvious to completely fill the contact holes based on the teachings of Ohkawa, Jeng, and Matsuoka—are consistent with our claim construction of this element of claims 1 and 9. *See supra* Section II.C.

Independent claim 9 recites many of the same steps recited in claim 1, and Petitioner relies upon its prior discussion of claim 1 in its attempt to show the obviousness of claim 9. *Id.* at 60–71. Petitioner acknowledges that claim 9 further recites “wherein said etch stop layer is etched into to a lesser extent through said substrate contact openings and said bit line contact openings than through said gate contact openings.” *Id.* at 62. Petitioner asserts that such a feature would have been inherent in Ohkawa, arguing that

the etching of BPSG film 9 is selective to the underlying SiN film 37, which implies that the oxide is etched at a much faster rate than nitride. *Id.* at 63 (citing Ex. 1002 ¶ 140). Petitioner continues that a person of ordinary skill in the art “would have understood that the SiN film 37 is etched into to a lesser extent through the substrate contact holes 21d and the bit line contact holes 21a than through the gate contact holes 21b, as claimed.” *Id.* at 66–67 (citing Ex. 1002 ¶ 144). Petitioner also asserts that the limitation in claim 9 would have been obvious over the etching processes disclosed in Jeng. *Id.* at 67–70 (citing Ex. 1002 ¶¶ 146–151).

5. Patent Owner’s Arguments Regarding Independent Claims 1 and 9

a. The “filling” steps of independent claims 1 and 9

Patent Owner argues that Ohkawa does not disclose the “filling” steps of independent claims 1 and 9 because Ohkawa is alleged to “specifically teach[] the use of separate and different process steps to form the bit line and gate contacts.” PO Resp. 18. Patent Owner describes Ohkawa’s process as providing a deposition process that “fills the bit line contact opening 21a to complete the bit line contact (plug 13), [and although it] adds material to holes 21b and 21c, it only forms side walls 15, [and] not completed contacts.” *Id.* at 22 (citing Ex. 1005, 5:21–24, 18:50–58, Fig. 12c). Patent Owner points out that Ohkawa provides a subsequent deposition process to complete the gate contact. *Id.* at 24 (citing Ex. 1005, 18:66–67). Patent Owner concludes that “[b]ecause Ohkawa uses different process steps to form the bit line contact and gate contacts, it doesn’t have a step for ‘filling’ all three contact openings,” and cannot disclose a filling step to complete the formation of the three contacts. *Id.*

Petitioner replies that Patent Owner’s argument is premised on a “faulty claim construction,” that requires the contact openings to be filled concurrently with the same conductive material and be made completely full. Pet. Reply 10. Petitioner points out that “one of ordinary skill in the art would have found it obvious to form a plug (similar to metal plug 13) in contact hole 21d such that contact hole 21d is completely filled.” *Id.* at 12 (citing Pet. 53–57; Dec. on Inst. 16–17, 19–20). Petitioner further argues that all of Patent Owner’s arguments rest on its proposed claim construction, which is erroneous. *Id.* at 13–15.

We agree with Petitioner that one of ordinary skill in the art would have found it obvious to perform the “filling” steps of claims 1 and 9 in view of Ohkawa. As discussed in Section II.C above, we are not persuaded that the contact openings must necessarily be filled concurrently, nor with the exact same material. We also point out that the “comprising” language found in both of independent claims 1 and 9 makes clear that sub-steps may be employed to perform the claimed process. *See, e.g., Mars Inc. v. H.J. Heinz Co.*, 377 F.3d 1369, 1376 (Fed. Cir. 2004); Tr. 19:22–20:23. We remain persuaded that Petitioner has demonstrated that filling all of the contact openings would have been an obvious variation, especially in view of the other “completed” plugs in the contact opening in Ohkawa. Contrary to Patent Owner’s arguments, we do not find Petitioner’s contentions with respect to the “filling” step of claims 1 and 9 to be deficient in the ground of unpatentability of over Ohkawa, Jeng, and Matsuoka.

b. Etching the nitride transversely at least three times faster than laterally, as recited in independent claims 1 and 9

Patent Owner points out that Petitioner has acknowledged that Ohkawa does not teach the “claimed transverse etching limitation,” and

attempts to cure the deficiency by relying on the combination of Ohkawa with Jeng. PO Resp. 31–32 (citing Pet. 40–41). Patent Owner argues that a person of ordinary skill in the art would not have been motivated to combine Ohkawa with Jeng, and even if they were combined, they would not teach or suggest the transverse etching limitation. *Id.* at 32 (citing Ex. 2003 ¶¶ 84–85).

Patent Owner argues that although Petitioner has pointed out some similarities between Ohkawa and Jeng, this is not sufficient motivation for the combination. PO Resp. 35 (citing *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1379 (Fed. Cir. 2016)). Patent Owner also argues that the etch used in Jeng could cause problems with the processes applied in Ohkawa because Ohkawa provides a nitride layer on a thin oxide layer, and not directly on the substrate, per Jeng. *Id.* at 35–36 (citing Ex. 2003 ¶¶ 95–96; Ex. 1005, 14:52–60, Figs. 8A, 12A, 12B).

Patent Owner also argues that Jeng’s nitride etch is focused on achieving a high degree of selectivity, i.e., with the etch rate varying between different materials, such that its etch process would be typically inversely related to directionality. PO Resp. 37–38 (citing Ex. 2003 ¶¶ 98–99; Ex. 1006, 162, Fig. 10-19; Ex. 2009, 178:8–15, 179:15–180:9). Patent Owner also argues that the combination of Ohkawa and Jeng would produce an etch that would be highly selective but would have poor directionality characteristics, and thus would not suggest the transverse etching limitation. *Id.* at 39–40 (citing Ex. 2003 ¶¶ 100–102; Ex. 1012, 2:48–53, 3:1–6, 4:7–14, 4:62–66). Patent Owner also argues that “a person of ordinary skill in the art would not modify the Ohkawa-Jeng combination in order to achieve higher

anisotropy because this modification is at odds with Jeng’s express focus on selectivity.” *Id.* at 41–43.

Petitioner replies that Ohkawa does not say that its nitride etch must remove both the nitride etch stop layer 37 and the oxide layer 3 in the same etching step, and that a person of ordinary skill in the art would have understood that an additional etch could have been used to remove the remaining silicon oxide layer after the nitride etch, just like in the ’714 Patent. Pet. Reply 15–16 (citing Ex. 1022 ¶ 11; Ex. 1001, 4:4–7). Based on this, Petitioner asserts that the differences raised by Patent Owner would not dissuade ordinarily skilled artisans from combining Ohkawa and Jeng. *Id.*

Petitioner also argues that the degree of etching anisotropy is a result-effective variable that could be optimized, and that Petitioner has supplied sufficient evidence of the benefits of increasing the etching anisotropy of the nitride etch in the combination of Ohkawa, Matsuoka, and Jeng. Pet. Reply 17–18 (citing Ex. 1022 ¶¶ 110–112). Petitioner also points out that Jeng refers to its nitride etch as being “anisotropic,” that the etch chemistry applied in the ’714 Patent and Jeng is the same, and that Jeng neither discourages one from using a directional etch nor increases the anisotropy of the etch. *Id.* at 18–20 (citing Pet. 40, 42; Ex. 1001, 3:51–56, FIG. 3; Ex. 1002 ¶ 106; Ex. 1012, 4:59–66; Ex. 1022 ¶¶ 12, 15; Ex. 2003 ¶ 103).

We agree with Petitioner that Ohkawa does not specify that its nitride etch must be accomplished through a single etching step, so that the fact that Ohkawa has a nitride layer on a thin oxide layer, and not directly on the substrate, per Jeng, would not necessarily be problematic to the combination. We find Dr. Shanfield’s testimony to be more persuasive than Mr. Maltiel’s

testimony on this point. *Compare* Ex. 1022 ¶ 11, *with* Ex. 2003 ¶¶ 95–96. We agree with Dr. Shanfield that one of ordinary skill in the art would have understood that Jeng’s etch could have left behind an oxide film, but such a film would have been etched away in a subsequent etching step, as also disclosed by the ’714 Patent. Ex. 1022 ¶ 11 (citing Ex. 1001, 4:4–7). We concur that such a subsequent step would have been within the understanding of ordinarily skilled artisans, and would not have dissuaded such artisans from combining Ohkawa and Jeng.

With respect to the anisotropy of the etching process, we note that Exhibit 2006, Silicon VLSI Technology, relied upon by Patent Owner, includes the following: “the selectivity in both HDP and RIE reactive ion etch systems can be very good while still achieving anisotropy by choosing the right etch chemistries and utilizing ion-enhanced etching.” Ex. 1006, 30. As such, the anisotropy and the selectivity of a given etching process need not be at odds. As Petitioner has shown, the etch chemistry applied in the ’714 Patent and Jeng is the same. Pet. Reply 19 (citing Pet. 40, 42; Ex. 1001, 3:51–56, FIG. 3; Ex. 1002 ¶ 106; Ex. 2003 ¶ 103).

Although Patent Owner has argued that the same etchants can be used under different conditions to achieve different etch characteristics (PO Resp. 40 n.15 (citing Ex. 2003 ¶ 103)), we find Dr. Shanfield’s testimony to be persuasive, in that the matching etch chemistries in the ’714 Patent and Jeng demonstrate that Jeng would have been capable of supporting the level of anisotropy claimed. *See* Ex. 1022 ¶ 14. Further, Dr. Shanfield testifies that “a person of ordinary skill in the art would have easily been able to determine and set the etching conditions for an anisotropic etching profile for Jeng’s etch.” *Id.* As well, Dr. Shanfield testifies Jeng discourages

neither from using a directional etch nor increasing the anisotropy of the nitride etch. *Id.* ¶ 15. Thus, contrary to Patent Owner’s arguments, a person of ordinary skill in the art would have been motivated to combine Ohkawa with Jeng.

c. The differential etching of the etch stop layer recited in independent claim 9

Independent claim 9 recites, in part, that “wherein said etch stop layer is etched into to a lesser extent through said substrate contact openings and said bit line contact openings than through said gate contact openings.” Patent Owner argues that both Ohkawa and Jeng disclose etches that will not materially etch the nitride layer underlying the oxide dielectric, and their etch rate could be even slower at the gate contact opening than the other contact openings. PO Resp. 44–45 (citing Ex. 2003 ¶ 110). Patent Owner also argues that the cited limitation in claim 9 is a “specific consequence of an etching process where selectivity is a function of aspect ratio, with selectivity increasing with increasing aspect ratio.” *Id.* at 45 (citing Ex. 2003 ¶ 112). Patent Owner further argues that Ohkawa fails to teach such an aspect ratio dependent etch, and that such a feature is not inherent to the processes of Ohkawa. *Id.* at 46–51 (citing Ex. 2003 ¶¶ 114–118, 120–121). Patent Owner additionally argues that Petitioner has presented no evidence that Jeng’s etch process, which etches oxide 10–20 times faster than nitride, would necessarily remove more nitride over the gate than at the bottom of the contact opening, as alleged. *Id.* at 52–56 (citing Ex. 2003 ¶¶ 103, 122, 124–127).

Petitioner responds that the etching process in Ohkawa would reach the SiN film 37 in hole 21b before it would reach the SiN film 37 covering the substrate in contact holes 21a and 21d, so the SiN film in the gate contact

opening would be etched more compared to the same film in the bit line and substrate contact openings because it is exposed to the etch for a longer time. Pet. Reply 21–22 (citing Ex. 1002 ¶¶ 141–144). Petitioner also points out that the subject limitation of claim 9 does not require a special etching process where selectivity is a function of aspect ratio, but only requires differential etching through different openings. *Id.* at 22–23. Petitioner also emphasizes that the combination of Ohkawa and Jeng would utilize the same etchant, selectivity, and aspect ratio dependency as those disclosed in the ’714 Patent, such that it would be expected to achieve the same results. *Id.* at 26 (citing Ex. 1022 ¶¶ 21, 30; Ex. 1021, 107:18–108:21).

We agree with Petitioner that the subject limitation of claim 9 does not require an etching processes where selectivity is a function of the aspect ratio of openings or other features. Claim 9 requires that the etch stop layer is etched into to a lesser extent through the substrate contact openings than through the other recited openings; although this could be accomplished through an aspect ratio dependent etch, such an etch is not required. Even if, as Patent Owner argues, the Specification of the ’714 Patent provides for such an aspect ratio dependent etch, such a condition should not be imported into claim 9. *See Phillips*, 415 F.3d at 1320.

In contrast, Petitioner is asserting a “time based” view of the process, wherein the etch process would reach certain portions before others, so that the former would be etched more than the latter. Pet. Reply 21–22. Although Patent Owner indicates that the claim limitation is dependent on an aspect ratio (PO Resp. 45), we conclude that claim 9 does not require such a limitation. As such, we are persuaded that Petitioner has demonstrated that

the combination of Ohkawa, Jeng, and Matsuoka teaches differential etching of the etch stop layer as recited in independent claim 9.

6. Conclusions Regarding Independent Claims 1 and 9

We have reviewed Petitioner’s explanations and supporting evidence as to how the proffered combinations teach the limitations of independent claims 1 and 9, as well as its explanations as to how one of ordinary skill in the art would have combined the relevant teachings of the references. *See* Pet. 3, 72–76. We have also reviewed Patent Owner’s arguments regarding this ground and the independent claims. We agree with Petitioner’s analysis and we do not agree with Patent Owner’s arguments. *In particular, we are persuaded* that one of ordinary skill in the art would have found it obvious to perform the “filling” steps of claims 1 and 9 in view of Ohkawa, that the differences raised by Patent Owner would not dissuade ordinarily skilled artisans from combining Ohkawa and Jeng, and that the differential etching of the etch stop layer of claim 9 does not require an etching processes where selectivity is a function of the aspect ratio of openings or other features. *See* Pet. Reply 10–16, 21–22. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the subject matter of independent claims 1 and 9 would have been obvious over the combined teachings of Ohkawa, Jeng, and Matsuoka.

7. Dependent Claims 2, 4, 5, 7, 8, 10, 12, 13, and 16

With respect to claims 2, 4, 10, and 12, Petitioner asserts that Ohkawa discloses that the semiconductor device structure includes two gate electrodes 5G and source/drain regions, and that Ohkawa discloses its film 37 is formed from SiN. Pet. 57–58, 71. With respect to claims 5 and 13, Petitioner asserts that Ohkawa discloses that “an SiN film 37 is formed

30 to 70 nm thick over the substrate,” which is equivalent to between 300 to 700 Angstroms, and it would have been obvious to use such a SiN film as the etch stop. *Id.* at 58–59, 72 (citing Ex. 1005, 13:34–36; Ex. 1002 ¶ 130). With respect to claim 7, Petitioner asserts one of ordinary skill in the art would have understood that the first etch of the BPSG film 9, in Ohkawa, is selective to BPSG with respect to SiN film 37 because the etch etches BPSG but stops at the SiN film 37, demonstrating a selective oxide with respect to nitride etch. *Id.* at 59–60 (citing Ex. 1002 ¶ 132). With respect to claims 8 and 16, Petitioner asserts that Jeng discloses using CH₂F₂ and CHF₃ as reactive gases. *Id.* at 60, 72. We are persuaded by Petitioner’s showing.

In its Patent Owner Response, Patent Owner does not address separately whether the combined teachings of the references account for the limitations recited in dependent claims 2, 4, 5, 7, 8, 10, 12, 13, and 16. *See generally* PO Resp. 14–57. Patent Owner reiterates its arguments regarding the “fundamental deficiencies in Ohkawa in combination with Matsuoka and Jeng as discussed above,” and argues that these deficiencies affect Petitioner’s analysis of the dependent claims. *Id.* at 56. As discussed above, we do not agree with Patent Owner’s arguments and we determine that they do not undermine Petitioner’s showing with respect to the dependent claims.

We have reviewed Petitioner’s explanations and supporting evidence as to how the proffered combinations teach these limitations, as well as its explanations as to how one of ordinary skill in the art would have combined the relevant teachings of the references, and we agree with Petitioner’s analysis. *See* Pet. 57–60, 71–72. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the subject matter of dependent claims

2, 4, 5, 7, 8, 10, 12, 13, and 16 would have been obvious over the combined teachings of Ohkawa, Jeng, and Matsuoka.

E. Obviousness over Ohkawa, Jeng, Matsuoka, and Chakravarti

Petitioner contends that claims 3 and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ohkawa, Jeng, Matsuoka, and Chakravarti. Pet. 3, 72–76. Petitioner, relying on citations to the references and declaration testimony of Dr. Shanfield, sets forth how the references would have conveyed the claim limitations and provides reasoning for combining the teachings of the references. *Id.* at 72–76.

Claims 3 and 11 recite the further step of “forming deep trench DRAM devices in said substrate.” Petitioner acknowledges that the combined Ohkawa-Jeng-Matsuoka method does not disclose forming deep trench DRAM devices in the substrate. *Id.* at 72–73. Petitioner cites to Chakravarti, which discloses that its method “is particularly useful for producing a DRAM device having a dense array region with self-aligned deep trench storage capacitors connected by buried straps.” *Id.* at 73 (citing Ex. 1007, Abstract).

Petitioner asserts that it would have been obvious to modify the combined Ohkawa-Jeng-Matsuoka method to form deep trench DRAM devices in the substrate because Ohkawa and Chakravarti are directed to the same technical field of fabricating DRAM devices, and the combination would have amounted to nothing more than combining known elements (Ohkawa’s process for forming a DRAM semiconductor device with Chakravarti’s process for forming deep trench storage capacitors as the DRAM device) according to known methods (first forming the deep trench storage capacitors followed by forming the transistor, as disclosed by

Chakravarti) to produce the expected result of forming a functional DRAM device with deep trench storage capacitors. *Id.* at 74–76 (citing Ex. 1002 ¶ 166; *KSR*, 550 U.S. at 416). We are persuaded by Petitioner’s showing.

In its Response, Patent Owner does not address separately whether the combined teachings of the references account for the limitations recited in dependent claims 3 and 11. *See generally* PO Resp. 14–57. Patent Owner reiterates its arguments regarding the “fundamental deficiencies in Ohkawa in combination with Matsuoka and Jeng as discussed above,” and argues that Chakravarti does not cure those deficiencies. *Id.* at 56–57. As discussed above, we do not agree with Patent Owner’s arguments and we determine that they do not undermine Petitioner’s showing with respect to the dependent claims.

We have reviewed Petitioner’s explanations and supporting evidence as to how the proffered combinations teach these limitations, as well as its explanations as to how one of ordinary skill in the art would have combined the relevant teachings of the references, and we agree with Petitioner’s analysis. *See* Pet. 3, 72–76. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the subject matter of dependent claims 3 and 11 would have been obvious over the combined teachings of Ohkawa, Jeng, Matsuoka, and Chakravarti.

III. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence that (1) claims 1, 2, 4, 5, 7–10, 12, 13, and 16 under 35 U.S.C. § 103 as unpatentable over Ohkawa, Jeng, and Matsuoka; and (2) claims 3 and 11 are

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unpatentable under 35 U.S.C. § 103 over Ohkawa, Jeng, Matsuoka, and Chakravarti.

IV. ORDER

It is

ORDERED that each of claims 1–5, 7–13, and 16 of U.S. Patent No. 6,562,714 B1 is unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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