

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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POWER INTEGRATIONS, INC,  
Petitioner,

v.

SEMICONDUCTOR COMPONENTS INDUSTRIES LLC,  
Patent Owner.

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Case IPR2017-01453  
Patent 8,854,841 B2

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Before BRIAN J. McNAMARA, JOHN F. HORVATH, and  
KAMRAN JIVANI, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*35 U.S.C. § 318(a) and*  
*37C.F.R. § 42.73*

## BACKGROUND

On November 22, 2017 we instituted an *inter partes* review of claims 5–7 (all challenged claims) of U. S. Patent No. 8,854,841 B2 (“the ’841 patent”). Paper 7 (“Dec. to Inst.”). Patent Owner filed a Patent Owner Response (Paper 12, “PO Resp.”), Petitioner filed a Petitioner Reply (Paper 13, “Pet. Reply”). Patent Owner also filed a Motion to Exclude the testimony of Petitioner’s expert, Mr. William Bohannon, including the Declaration of Mr. William Bohannon (Ex. 1004, “Bohannon Decl.”) and the Second Declaration of Mr. William Bohannon (Ex. 1009, “Bohannon Reply Decl.”). Paper 19, Mot. To Exclude. Patent Owner relies upon the testimony of Dr. Douglas Holberg (Declaration of Dr. Douglas Holberg, Ex. 2001 “Holberg Decl.”) and Declaration of Dr. Douglas Holberg In Support of Patent Owner Response (Ex 2004 “Holberg Resp. Decl.”). Petitioner filed an Opposition to Patent Owner’s Motion to Exclude, Paper 22 (“Opp. To Mot. To Exclude”), and Patent Owner filed a Reply to Petitioner’s Opposition to the Motion to Exclude, Paper 22 (“Reply to Opp. To Mot. To Exclude”). Patent Owner also filed a Motion for Observations on the Cross Examination of Mr. Bohannon (Paper 18) and Petitioner filed a Response (Paper 23). A transcript of an oral hearing held on July 19, 2018 (Paper 29, “Hrg. Tr.”) has been entered into the record.

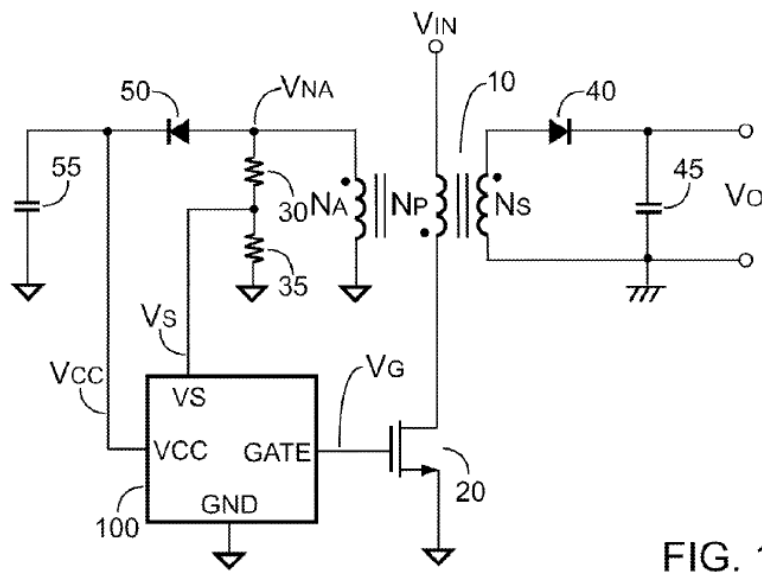
We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. §318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

Having reviewed the arguments of the parties and the supporting evidence, we conclude that Petitioner has demonstrated by a preponderance of the evidence that challenged claim 5 is unpatentable. We also conclude

that Petitioner has not demonstrated that challenged claims 6 and 7 are unpatentable.

THE '841 PATENT (EXHIBIT 1001)

The '841 patent concerns a controller for a power converter. Ex. 1001, Abstract. The power converter is shown in Figure 1 of the '841 patent reproduced below.



### Figure 1 of the '841 Patent

In the primary side controlled power converter of Figure 1, switching signal  $V_G$  output from controller 100 controls power transistor 20 to switch primary winding  $N_P$  of transformer 10. *Id.* at 1:31–33. When switching signal  $V_G$  goes low, turning transistor 20 off, reflected signal  $V_{NA}$  charges capacitor 55 via rectifier 50 to provide supply voltage  $V_{CC}$  to controller 100. *Id.* at 1:37–40, Fig. 4A. A resistive divider (resistors 30 and 35) attenuates  $V_{NA}$  to provide detection signal  $V_S$  at terminal VS of controller 100. *Id.* at 1:20–31.

Figure 4A of the '841 patent illustrates that when  $V_G$  goes low undesirable oscillating transients occur at the leading edge of reflected signal  $V_{NA}$  for a period  $T_{S1}$ , so that for some time period detection signal  $V_S$  does not accurately represent the current switched through transformer 10. *Id.* at 1:47–56. This transient oscillation, which is the result of leakage inductance of transformer 10 and parasitic capacitance of transistor switch 20, slows down power regulation, especially in the case of a high frequency switching transformer. *Id.* The '841 patent describes discharge circuits that seek to reduce the period of this oscillating transient. *Id.* at Fig. 2, Fig. 6.

In the embodiment of Figure 2 shown below, pulse generator 200 generates a logic-high pulse  $S_B$  for a period  $T_D$  when  $V_G$  at terminal VIN of pulse generator 200 drops from logic-high to logic-low, indicating that transistor 20 has been turned off and  $V_{NA}$  is rising. *Id.* at 4:27–32.

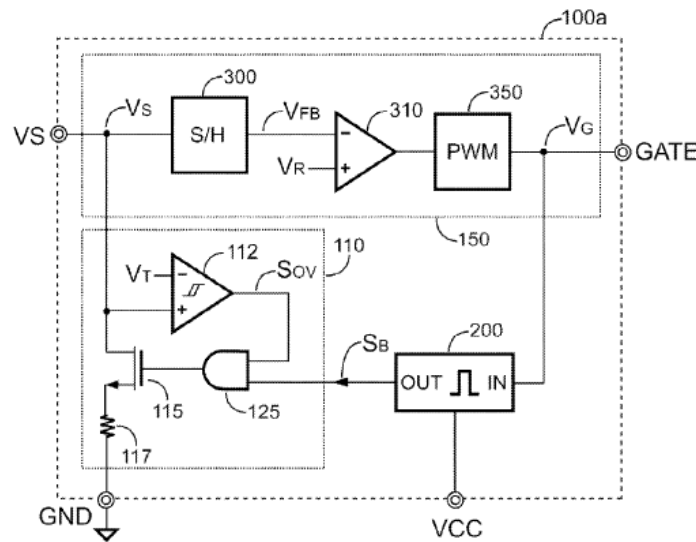


FIG. 2

Figure 2 of the '841 patent

Attenuated signal  $V_{NA}$ , i.e., detection signal  $V_S$ , is compared against a threshold  $V_T$  to generate a logic-high signal  $S_{OV}$  when  $V_S$  exceeds  $V_T$ .  $S_{OV}$

and  $S_B$  are applied to AND gate 125 turning transistor 115 on during period  $T_D$  causing transistor 115 to clamp  $V_S$  to be less than  $V_T$ . *Id.* at 4:33–41. As a result of clamping  $V_S$ , the oscillating energy of  $V_{NA}$  is discharged in a relatively short period  $T_{S2}$ . *Id.*

In the embodiment of Figure 6 shown below, pulse generator 200 generates a logic-high pulse  $S_B$  for a period  $T_D$  when  $V_G$  at terminal VIN of pulse generator 200 drops from logic-high to logic-low, indicating that transistor 20 has been turned off and  $V_{NA}$  is rising.

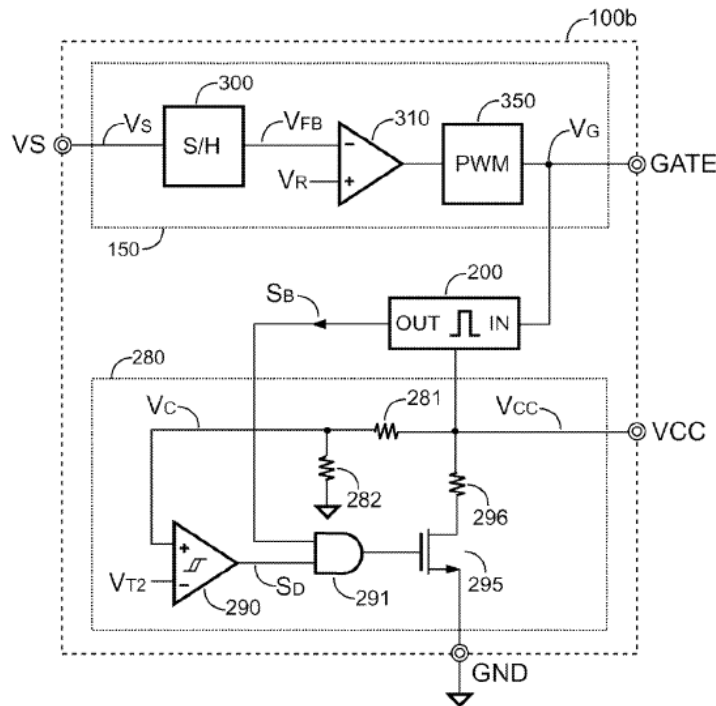


Figure 6 of the '841 patent

The embodiment in Figure 6 discharges a current sourced from supply terminal  $V_{CC}$  by the reflected signal  $V_{NA}$  during an off period  $T_{OFF}$  of switching signal  $V_G$ . *Id.* at 4:55–58. Supply voltage  $V_{CC}$ , which is derived from  $V_{NA}$ , is connected through resistor 296 to transistor 295 and to a resistive divider (resistors 281 and 282), which provides attenuated signal

$V_C$  to comparator 290. Attenuated signal  $V_C$  is compared to threshold  $V_{T2}$  to form discharging signal  $S_D$ . When  $V_C$  exceeds  $V_{T2}$  during delay time  $T_D$ , AND gate 291 provides a signal to turn transistor 295 on, drawing current from supply terminal VCC, thereby discharging the oscillating energy of reflected signal  $V_{NA}$  and reducing the oscillating period at the leading edge of  $V_{NA}$  when switching signal  $V_G$  is disabled. *Id.* at 5:1–13.

#### ILLUSTRATIVE CLAIM

Claim 5 reproduced below is illustrative:

5. A controller for a power converter, the power converter comprising a power transistor, and the controller comprising:
  - a switching circuit, generating a switching signal in response to a detection signal from said transformer, wherein said power transistor is coupled to said switching circuit and driven by said switching signal to switch said transformer for regulating said power converter; and
  - a discharging circuit, coupled to a supply terminal of said controller, wherein said controller is powered by a reflected signal of said transformer via said supply terminal of said controller, said discharging circuit is coupled to discharge a current sourced from said supply terminal of said controller during a delay time starting from a falling edge of said switching signal.

#### GROUND OF INSTITUTION

In our Decision to Institute, we instituted trial on the sole asserted ground that challenged claims 5–7 of the '841 patent are anticipated by U.S. Patent No. 5,305,192 (Ex. 1002 “Bonte”).

#### CLAIM CONSTRUCTION

Neither Petitioner nor Patent Owner contends that any claim terms require construction. We agree that there is no need to construe any claim

terms. As in the Decision to Institute, in this Decision we apply the ordinary and customary meaning to all the terms of the challenged claims.

## ANALYSIS OF PRIOR ART CHALLENGES

### *Anticipation of Claim 5*

#### *The Bonte Reference*

Citing Figure 4A of Bonte, Petitioner argues that Bonte anticipates the challenged claims. Pet. 13. Bonte discloses a magnetic flux sensing primary side control flyback converter having an auxiliary winding that provides a predetermined, substantially constant output voltage on the secondary side of a transformer from an unregulated input voltage. Pet. 12–14 (citing Ex. 1002, 1:11–19, 1:65–2:12; Fig. 4A; Ex. 1004, Bohannon Decl. ¶ 39). Referencing Figure 1, Bonte explains that in a conventional flyback converter a feedback signal derived from voltage VBIAS (on bias winding 120) is used to control the on and off duty cycle of switch 104, e.g., a power transistor. Ex. 1002, 5:12–15. When switch 104 is on (i.e., conducting), primary winding 110 sees VDC and secondary and bias windings, 130 and 120, respectively, go to negative voltages, such that current builds in the primary winding 110 as transformer 101 stores energy. Ex. 1002, 5:33–37. When switch 104 turns off, voltage across the switch “flies back” to a large voltage until the energy in the primary leakage inductor 112 associated with primary winding 110 dissipates. *Id.* at 5:38–42. During the “switch off” time, energy in transformer 101 transfers to secondary winding 130 and bias winding 120. *Id.* at 5:55–57.

Figure 3 of Bonte illustrates a typical prior art magnetic flux sensing feedback circuit that turns the switch on and off. Ex. 1002, 7:1—3—. In Figure 3, the peak detector formed by diode 310 and capacitor 330

establishes the largest value of the bias winding voltage on capacitor 330 before bias diode 310 reverse biases and provides a supply voltage for the regulator. *Id.* at 7:19–22. That voltage is attenuated through a resistive divider 340 to provide a feedback signal (FB) at terminal 352 of error amplifier 350, which compares FB to reference voltage 351 to generate switch control signal 360. *Id.* at 7:5–11. The feedback circuitry also peak detects a primary leakage induced spike superimposed on the bias winding flyback voltage, artificially enlarging feedback signal FB at terminal 352 of error amplifier 350, and causing the output voltage to sag. *Id.* at 7:25–33.

As Petitioner notes, the power supply control circuit in Bonte prevents primary leakage current inductance spike effects from propagating through the error amplifier by employing a “leakage inductance spike blanking circuit” that suppresses the error signal at the input of the error amplifier for a fixed period after the “switch off” time until the leakage inductance spike has died away. Pet. 15 (citing Ex. 1002, 11:7–17, Fig. 7).

Figure 4A of Bonte is shown below.

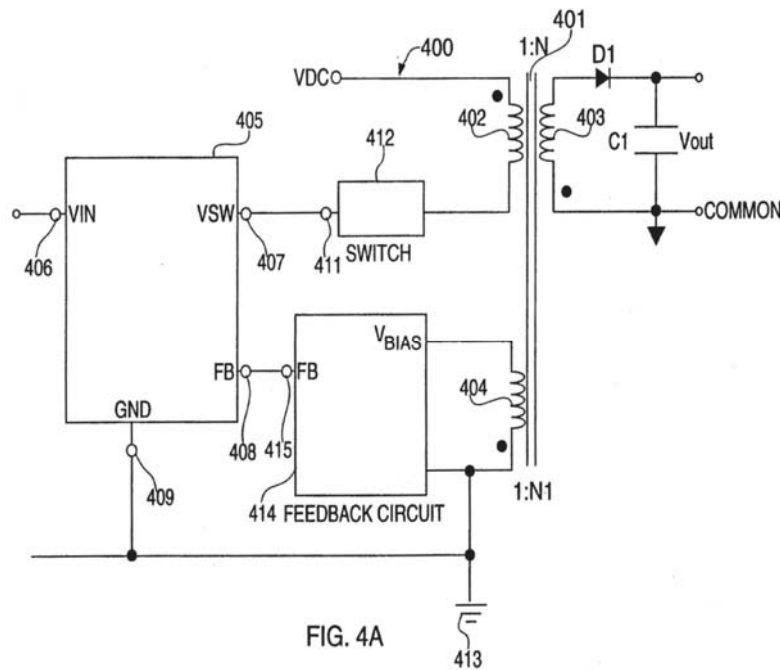


Figure 4A is a block diagram of an illustrative application circuit in which Bonte's invention can be used in a flyback converter switching configuration. Ex. 1002, 3:46–48. Petitioner cites Figure 4A of Bonte as disclosing a controller for a power converter with switch 412 in the form of a power transistor coupled to a switching circuit that is driven by switching signal VSW to switch the transformer to regulate the power converter. Pet. 17–19. Petitioner notes that Bonte discloses switching regulator control circuit 405 outputs switching signal VSW to the control terminal 411 of switch 412 to control the on and off duty cycle of the switch. *Id.* at 18. Petitioner further cites Bonte as disclosing that switch 412 may comprise a FET connected as described in connection with Figures 10 and 12. *Id.* at 22 (citing Ex. 1001, 8:23–26).

Figures 6A–6D of Bonte show simplified block diagrams of alternative embodiments of switching regulator control circuit 405 of

Figures 4A and 4B. Ex. 1002, 3:54–57. Figure 7 of Bonte is a block diagram of an embodiment of sampling error amplifier 610 of Figures 6A–6D. *Id.* at 3:57–58. Amplifier 705 in Figure 7 of Bonte corresponds to amplifier 1125 in Figure 11B. *Id.* at 15:18–19. Amplifier 705 is connected to the leakage inductance blanking circuit in block 710 of Figure 7, which corresponds to block 1126 in Figure 11B. *Id.* at 15:21–22. Bonte discloses:

The output of amplifier 1125 is connected to leakage inductance blanking circuit 1126. PNP transistor Q53 is a constant current source which feeds current to node 1126a connecting capacitor DC1 and transistor Q54. Transistor Q54 is switched between on and off states by logic signal FFQ<sup>[1]</sup> which is generated in logic block 1104 of Figure 11A. It is this signal which triggers the leakage inductance blanking. The length of time that the leakage inductance blanking circuit remains on is set by capacitor DC1, which in the present embodiment gives rise to a 1.5 micro-second pulse width.

*Id.* at 15:21–32.

Figure 11A of Bonte is a block level diagram of voltage regulator control circuit 405 shown in Figure 10. *Id.* at 4:1–4, 14:46–48. Logic block 1104, shown in more detail in Figure 11J, illustrates flip-flop 1141 whose Q output is taken from terminal FFQ so that the output of the driver circuit, i.e., the VSW output of stage one block 1113 and output of stage two block 1112, is turned on and off. *Id.* at 19:5–9. When FFQ is high, the driver circuit is turned on, when FFQ is pulled low by the output of the current limiter comparator, flip-flop 1141 is reset and the driver circuit is turned off. *Id.* at 19:10–12. Signal FFQ controls the state of the switch in the

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<sup>1</sup> The Specification of Bonte refers to signal FFQ. In the Figures of Bonte the same signal is labeled FFO. The parties have used both designations. In this Decision, we use the designation FFQ as used in the Specification of Bonte.

implementations of Figures 10 and 12, as the modifications made to Figure 11 that differentiate the embodiments shown in Figures 10 and 12, do not affect FFQ. *Id.* at 20:24–32.

### *Petitioner's Arguments*

The preamble of claim 5 recites a controller for a power converter. The Petition divides the claimed controller into a switching circuit (claim element 5(a)) and a discharging circuit (claim element 5(b)). Pet. 16–29. Claim element 5(b) also states that the controller is powered by a reflected signal of the transformer via a supply terminal.

The switching circuit (claim element 5 (a)) generates a switching signal in response to a detection signal from the transformer. That switching signal drives a power transistor coupled to the switching circuit to switch the transformer to regulate the power converter. Discussing the implementation of Figures 4A and 6A, the Petition identifies voltage regulator control circuit 405 of Bonte (as illustrated in Figure 6A) as the providing a control signal, i.e., switching signal VSW, to control terminal 411 of switching circuit 412. Pet. 18–19 (discussing annotated version of Ex. 1002, Fig. 4A, citing Ex. 1004, Bohannon Decl., ¶¶ 45–46), 20 (discussing annotated version of Ex. 1002, Fig. 6A, citing Ex. 1002 6:46–53).

The discharging circuit (claim element 5 (b)) discharges a current sourced from a supply terminal of the controller during a delay time starting from a falling edge of the switching signal. The Petition notes that in Bonte the falling edge of signal FFQ shown in Figs. 11A and 11B creates a pulse delay time by charging capacitor DC1, which enables transistor Q49 to discharge the current from the feedback signal FB. *Id.* at 27. As a result, the time that the leakage inductance blanking circuit remains on is set by

capacitor DC1. *Id.* Petitioner states, “the FFQ signal is used as the switching signal and thus the delay period of the discharge is timed off of the falling edge of the switching signal.” *Id.* at 27 (citing Ex. 1002 19:5–12).

As discussed below, Patent Owner acknowledges that the discharge begins on the falling edge of FFQ. PO Resp. 15–16.

*Patent Owner’s Response*

Patent Owner argues that when discussing claim element 5(a) the Petition identifies VSW as the switching signal that drives the power transistor, but when discussing claim element 5(b), the Petition argues that discharge begins at the falling edge of a different signal, i.e., FFQ. PO Resp. 1 (citing Pet. 19–20, 25–27). Specifically, Patent Owner argues, “the only evidence in the record demonstrates that FFQ and VSW are different signals and that the falling edge of FFQ coincides with the rising edge of VSW.” PO Resp. 15.

Noting that during his deposition Petitioner’s expert, William Bohannon, testified that signal VSW is the drive signal, Patent Owner contends that Petitioner has not demonstrated Bonte satisfies this temporal limitation because in Bonte, the alleged discharge begins at the rising edge of the signal Petitioner alleges drives the power transistor, i.e., VSW. PO Resp. 8–9, 12 (citing Ex. 2003, 115:12, 29:10–20). Patent Owner acknowledges that the alleged discharge begins at the falling edge of FFQ, but argues that because VSW is the only signal Petitioner identifies as a switching signal that drives the power transistor, Petitioner has not demonstrated that Bonte anticipates claim 5. PO Resp. 15–16 (arguing that

“Bonte teaches the alleged ‘delay time’ begins on the falling edge of FFQ, but on the **rising** edge of the alleged switching signal VSW.”)

*Petitioner’s Reply*

Noting Patent Owner’s emphasis on the difference in phase between FFQ and VSW, Petitioner replies that Bonte discloses two embodiments, as referenced in discussion of Figure 4A in the ’841 patent and in the Petition. Pet. Reply. 6–7 (citing Ex. 1002, Fig. 10 (first embodiment) and Fig. 12(second embodiment)). Petitioner acknowledges that in the embodiment of Figure 10, FFQ and VSW are out of phase, but argues that in the embodiment of Figure 12, FFQ and VSW are in phase. *Id.* at 7. Petitioner emphasizes that the Petition does not rely upon the embodiment in Figure 10, arguing that the Petition cites the description of Figure 4A at column 8, lines 28–36, which states that the switching circuit may comprise an FET connected as described in connection with Figures 10 and 12. Pet. Reply 2 (citing Pet. 19, 22).

*Analysis*

Citing Petitioner’s identification of signal VSW as the switching signal Patent Owner argues Petitioner’s citation of the embodiment in Figure 12 is an improper new argument first raised in the Petitioner Reply. Hrg. Tr. 30–33. We now consider this argument.

The Petition includes an annotated version of Figure 6A (Pet. 20) in which VSW is labelled as the switching signal, but the Petition does not identify explicitly VSW as the switching signal in its claim charts, referencing instead Figure 4A, Figure 5, Figure 7, and Figure 11. Pet. 17–28. In its claim charts, Petitioner specifically cites Bonte’s disclosure that

FFQ is the signal that triggers the leak inductance blanking. *Id.* at 28 (citing Ex. 1001, 15:8–32)

Although Patent Owner's expert performed an extensive analysis of the circuit in Figure 10 (PO Resp. 12–13), Petitioner notes that Patent Owner's expert did not testify about the embodiment in Figure 12. Pet. Reply 7. In Figure 10 the FET gate is driven by VSW, which is out of phase with FFQ, such that the delay time is from the rising edge of VSW and falling edge of FFQ. In Figure 12, however, the regulator circuit includes a totem pole output of the type shown in Figure 6C, in which VSW applied to the switching transistor and FFQ are in phase. Patent Owner contends that the Petition's reference to Figure 6A, which concerns an open collector output stage is specific to the embodiment shown in Figure 10. Hrg. Tr. 31.

Although the Petition does not mention Figure 6C specifically, signal VSW in Figure 6C is also shown in the embodiment in Figure 6A (the switching regulator control circuit 405) annotated by Petitioner. Ex. 1002, 13:10–15. Bonte distinguished the implementations in Figures 6A and 6B from the implementations in Figures 6C and 6D. In Figures 6A and 6B, gate bias detector circuit 640 monitors the voltage on VSW terminal 407, but in Figures 6C and 6D, gate bias detector circuit 640 monitors the voltage on terminal 641, which is regulated by regulator block 680, and is connected to the driver stages of logic/driver circuit 630. Ex. 1002, 10:49–62. As discussed above, however, in all embodiments, the switch acts to start the delay on the falling edge of FFQ.

Bonte describes Figures 6A–6D as embodiments of switching regulator control circuit 405, with Figure 10 being a first embodiment and Figure 12 being a second embodiment. Ex. 1002, 3:54–57, 3:64–68, 4:29–

34. Patent Owner argues that Petitioner failed to argue Bonte relative to the embodiment of Figure 12, but Patent Owner does not contend that claim 5 covers only the embodiment of Figure 12.

The Petition identifies a passage of Bonte that points to the embodiment of Figures 10 and 12, and signal VSW is used to control the status of the switch in each embodiment. Therefore, we do not disregard the embodiment of Figure 12 in our analysis of claim 5.

As discussed below Petitioner contends that both the embodiment in Bonte's Figure 12 and the embodiment in Bonte's Figure 10 anticipate claim 5. Pet. Reply 8–15 (arguing that claim 5 is anticipated by the embodiment in Figure 10 and 11K). We now address both embodiments.

*The Embodiment of Figure 12 of Bonte*

The circuit that generates FFQ in Bonte is described with reference to Figure 11J. Ex. 1002, 4:21–22. Figure 11A is a top level diagram of a preferred integrated circuit embodiment of the switching voltage regulator 405 shown in Figure 10 and is discussed extensively following the discussion of Figure 10. *Id.* at 4:1–4. Bonte states both the first embodiment of the switching regulator control circuit in Figure 10 and the second embodiment of the switching regulator control circuit in Figure 12 largely use the same circuitry described in Figures 11A-11M, and use the same logic block 1104 shown in Figure 11J to generate FFQ. See Ex. 1002, 4:21–22, 20:14–32 (disclosing the only modifications between the embodiments of Figures 10 and 12 are to the output stage one block 1113, output stage two block 1112, gate bias detect block 1105, and current sense amplifier block 1111). Neither party asserts any material differences exist in the circuits of Figure 11 that generate FFQ in the embodiments of Figures 10

and 12. Patent Owner acknowledges that in all embodiments the switch acts in response to the falling edge of FFQ. PO Resp. 15–16. Thus, we agree with Petitioner that to the extent claim 5 is interpreted to limit the switching signal to Bonte’s signal VSW, the Figure 12 embodiment of Bonte anticipates the limitation that the discharge circuit “discharge a current sourced from said supply terminal of said controller during a delay time starting from a falling edge of said switching signal” because signals FFQ and VSW are in phase in Bonte’s Figure 12 embodiment.

*The Embodiment of Figure 10 of Bonte*

In our Decision to Institute, we noted that claim element 5(b) is not drawn to the switching signal itself, but recites a temporal limitation stating the discharge circuit discharges a current “during a delay time starting from a falling edge of said switching signal. To the extent that FFQ triggers a discharge that starts at the falling edge of the switching signal, the limitation is satisfied by Bonte.” Dec. to Inst. 12. Noting that during his deposition Petitioner’s expert, William Bohannon, testified that signal VSW is the drive signal, Patent Owner contends that Petitioner has not demonstrated Bonte satisfies this temporal limitation because in Bonte’s Figure 10 embodiment, the alleged discharge begins at the rising edge of the signal Petitioner alleges drives the power transistor, i.e., VSW. PO Resp. 8–9, 12 (citing Ex. 2003, 115:12, 29:10–20). As discussed above, Patent Owner acknowledges that the alleged discharge begins at the falling edge of FFQ, but argues that because VSW is the only signal Petitioner identifies as a switching signal that drives the power transistor, the Petition is limited to the embodiment in Figure 10 of Bonte and Petitioner has not demonstrated that this embodiment of Bonte anticipates claim 5. PO Resp. 15–16 (arguing that “Bonte teaches

the alleged ‘delay time’ begins on the falling edge of FFQ, but on the *rising* edge of the alleged switching signal VSW.”)

Petitioner argues the embodiment of Figure 10 of Bonte also anticipates claim 5. Pet. Reply 8–15. According to Petitioner, Patent Owner’s reading of the Petition is overly narrow and unjustified. *Id.* at 14. Petitioner argues that the Petition bases its anticipation analysis on signal FFQ that controls VSW, i.e., a single signal (FFQ) controls switching and is therefore a switching signal that triggers the leakage inductance delay circuit on its falling edge. Pet. Reply 11–12. Petitioner emphasizes that “both Bonte and the Petition make clear that it is the FF[Q] signal that ultimately controls when the switch driver is turned ON and OFF (by driving VSW).” Pet. Reply 12.

Petitioner maintains that “whether the ‘switching signal’ is VSW itself or FF[Q], which directly generates VSW in the driver block, is purely a semantic difference related to how VSW is coupled to the switch and does not avoid anticipation.” *Id.* at 9. Petitioner emphasizes that in every embodiment, FFQ and VSW represent the same internal state because one signal controls the other and the switch’s ON/OFF state time matches the logic state of FFQ, such that the “falling edge” element is met. Pet. Reply 2.

Petitioner’s analysis focuses on the timing relationships in the circuit, rather than the identity of the signal, noting that the delay period of the discharge is timed off the falling edge of FFQ. *Id.* at 2. That the specific signal (VSW) supplied to the switching transistor has a falling edge in the Figure 12 embodiment and a rising edge in the Figure 10 embodiment, does not change the undisputed fact that the falling edge of FFQ triggers the delay time claimed in either embodiment.

Claim 5 recites a “switching circuit generating a switching signal in response to a detection signal from said transformer.” Claim 5 further recites “a power transistor is coupled to said switching circuit and driven by said switching signal.” The power transistor switches the transformer to regulate the power converter. Claim 5 also recites that “during a delay time starting from a falling edge of said switching signal” a discharge circuit is coupled to discharge current sourced from the supply terminal of the claimed controller. The claimed delay time starts on a specific edge of the switching signal, i.e., the falling edge of the switching signal. Claim 5 does not recite a specific structure by which the power transistor “is coupled to said switching circuit” or “driven by said switching signal,” and does not require the transistor to be directly coupled to the switching circuit. In particular, claim 5 recites only a timing relationship, i.e., the start of the delay, and does not require that the power transistor be driven by the switching signal in any specific way. Thus, translating the signal FFQ to another phase, such as the phase of VSW, does not alter the fact that the power transistor ultimately is driven by FFQ as a switching signal, and that the delay time of the discharge circuit starts at the falling edge of that switching signal. This is true in both the embodiment of Figure 12, where FFQ is in phase with VSW, and in the embodiment of Figure 10, where FFQ is out of phase with VSW. Thus, we are persuaded that Petitioner has demonstrated that Bonte discloses all the elements of claim 5 and anticipates claim 5.

*Anticipation of Claims 6 and 7*

*Claim 6*

Claim 6 depends from claim 5 and recites two additional elements. Petitioner designates as claim element 6(a) the limitation reciting “a

comparison circuit, coupled to compare a voltage level correlated to a voltage level at said supply terminal with a threshold voltage for generating a discharging signal.” Pet. 29. Citing Figures 5, 7, and 11B of Bonte, Petitioner notes that feedback signal voltage FB is correlated to the voltage VBIAS at the supply terminal and is compared to a reference voltage VREF, e.g., 4.5 volts at terminal PIN in Figure 11B to generate the discharge signal. Pet. 29–33.

Petitioner designates as claim element 6(b) the limitation reciting “a transistor, coupled to said comparison circuit for discharging said current sourced from said supply terminal of said controller in response to said discharging signal.” Pet. 34. Noting that in Bonte amplifier 1125 connected to leakage inductance blanking circuit 1126 in Figure 11B corresponds to amplifier 705 in Figure 7, Petitioner identifies transistor Q49 in Figure 11B as a transistor coupled to comparison circuit 1125 used to discharge current sourced from VBIAS in response to the discharging signal provided by capacitor DC1. *Id.* (citing Ex. 1002, 19:5–12<sup>2</sup>). Capacitor DC1 is connected to transistor Q54 that is turned on and off by FFQ, and sets the period of the blanking interval. Ex. 1002, 15:25–28, Fig. 11B. Patent Owner does not dispute Petitioner’s contentions concerning claim element 6(b) except as discussed below.

Patent Owner contends that in Bonte the comparison circuit and transistor are coupled in a manner different from that recited in claim 6 and that “there is no discharge signal that is both generated by the comparison circuit and determines when the transistor discharges.” PO Resp. 18. Patent

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<sup>2</sup> The text cited by Petitioner is found at Ex. 1002, 15:28–31.

Owner cites the embodiment in Figure 6 of the '841 patent in which comparison circuit 290 compares attenuated supply voltage  $V_C$  to threshold  $V_{T2}$  to provide signal  $S_D$  (the discharge signal);  $S_D$  is applied to AND gate 291 that drives the gate of transistor 295 ON (when pulse signal  $S_B$  is enabled) thereby causing transistor 295 to discharge current sourced from supply terminal VCC during a period  $T_{OFF}$ . *Id.* at 17. Patent Owner contrasts this embodiment with Bonte, arguing that Bonte's comparison circuit 1125 generates an error signal, but a signal internal to the leakage inductance blanking circuit provided by DC1 to Q49 is the discharging signal. *Id.* at 19–20. Thus, according to Patent Owner, the discharging signal in Bonte is not generated by the comparison circuit as required by claim 6. *Id.* at 20.

Patent Owner's analysis is predicated on its re-stating the limitations of claim 6 arguing, "[i]n other words, the transistor and comparison circuit of claim 6 are coupled such that the transistor switches in response to the signal generated by the comparison circuit (i.e., "the discharging signal")." PO Resp. 16. Petitioner argues that Patent Owner's restatement of claim 6 imports limitations that are not in the claim. Pet. Reply 16. Petitioner argues that claim 6 does not require that the transistor switch on and off in response to the signal generated by the comparison circuit, or that the discharge signal control the switching of the transistor, as argued in Patent Owner's discussion of supplying a "discharging signal" to the gate of a MOSFET through an AND gate in the embodiment of Figure 6. Pet. Reply 17–18. Instead, claim 6 requires only that the transistor be coupled to the comparison circuit that generates the discharging signal and that the discharge be in response to the generated discharging signal. *Id.*

The discharge signal in claim 6 is generated by the comparison circuit. Petitioner argues that in Bonte, transistor Q49, through which the discharge (of supply terminal VBIAS) is accomplished, is connected to the output of comparison circuit 1125. Pet. 34, Pet. Reply 18. However, the presence of the discharging signal at the collector of transistor Q49 in Bonte does not mean that Bonte discloses that the transistor acts in response to the discharging signal output from the comparison circuit. Petitioner acknowledges that the discharge timing is controlled at the base terminal of transistor Q49 that is coupled to capacitor DC1. *Id.* at 18–19, Pet. 34. In Bonte, transistor Q49 acts in response to the signal on its base (i.e., to the voltage on capacitor DC1) to discharge current through its collector, but Q49 does not act in response to the output of the comparison circuit, which generates the discharging signal that discharges the current sourced from the supply terminal. Thus, we are not persuaded by Petitioner’s arguments that Bonte anticipates claim 6. See also Fig. 7.

*Claim 7*

Claim 7 depends from claim 6 and recites the additional limitation “a pulse generation circuit, generating a pulse signal having said delay time in response to a falling edge of said switching signal, wherein said pulse signal is further coupled to control said transistor for discharging said current sourced from said supply terminal of said controller.”

As we have determined that Petitioner has not demonstrated by a preponderance of the evidence that claim 6 is anticipated by Bonte, we conclude that Petitioner has not carried its burden with respect to claim 7.

### MOTION TO EXCLUDE

Patent Owner moves to exclude the entire testimony of Petitioner's expert, including his declarations (Exhibits 1004 and 1009), arguing that William Bohannon "lacks at least the requisite educational background and further because he also lacks the requisite work experience, he cannot qualify as a POSITA, much less an expert." Reply to Opp. To Mot. To Exclude 1. Patent Owner notes that Mr. Bohannon defined a person of ordinary skill as one with a degree, or its equivalent, in electrical engineering or physics and two years of practical experience working with switching regulators and analog/mixed signal circuit design, or an equivalent combination of academic study and work experience. *Id.* at 1–2 (citing Ex. 1004 ¶ 34; Pet. 4). According to Patent Owner, Mr. Bohannon does not meet his self-identified criteria because he did not earn a B.S. degree, or its equivalent, in electrical engineering or physics (and has not undertaken an equivalent course of study, particularly for purposes of complicated mixed signal circuits at issue in this proceeding), and does not have the requisite work experience in designing analog/mixed signal circuits. *Id.* at 2–3.

Petitioner opposes Patent Owner's Motion to Exclude, noting the denial of a similar motion to exclude Mr. Bohannon's testimony filed by Patent Owner in a proceeding concerning similar switch mode power converter technology. Opp. To Mot. To Exclude 2–3 (citing *ON Semiconductor Corp. v. Power Integrations, Inc.*, Case IPR2016-00809 (PTAB Sept. 22, 2017) (Final Written Decision, Paper 67 at 62)). Although Patent Owner argues that the record concerning Mr. Bohannon's background

has evolved in this proceeding<sup>3</sup> (Reply to Opp. To Mot. To Exclude 1), Petitioner argues that Patent Owner's current Motion to Exclude repeats Patent Owner's prior contentions concerning Mr. Bohannon's degree in mathematics with additional physics coursework and his experience. Opp. To Mot. To Exclude 2–3. Petitioner also contends that Patent Owner's Motion to Exclude is improper because Patent Owner's general objections to Mr. Bohannon's qualifications at deposition raised none of the specific issues articulated in the Motion to Exclude. *Id.* at 3–4.

Petitioner emphasizes that there is no requirement for expert knowledge to be obtained in school rather than from industry experience and that in his role as Chief Scientist at Computer Accessories, Mr. Bohannon worked on “buck and boost” converters, that at Manx Research Mr. Bohannon studied all available power supply architectures, and that at Edge Semiconductors, Planet ATE, and ATE Engines, Mr. Bohannon was responsible for the development of power supplies and power supply control ICs used in testing devices. *Id.* at 6–8, see Ex. 1009 Bohannon Reply Decl. ¶¶ 8–12.

Noting that Petitioner does not dispute Mr. Bohannon's academic record fails to comport with his definition of a person of ordinary skill, Patent Owner argues that, although Mr. Bohannon “worked for companies that developed power supplies during the course of his career,” he “never designed a switch mode power supply” and has “never published on the

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<sup>3</sup> Mr. Bohannon testified that, although he has worked as an expert on switching power supplies in other cases, his deposition in this proceeding was his first deposition on the subject. Ex. 2007, Transcript of Deposition of William Bohannon, (“Bohannon Dep. Tr.”) 6:14–20.

design of switching regulators.” Mot. To Exclude 4–5; Reply to Opp. To Mot. To Exclude 1, 3. In particular, Patent Owner contends that Mr. Bohannon’s work experience on design reviews for power supplies, and building switching regulators on design boards using parts he selected, is insufficient to qualify him as an expert under FRE 702. Reply to Opp. To Mot. To Exclude 3.

Patent Owner’s arguments do not persuade us that we should exclude Mr. Bohannon’s testimony. There need not be a perfect match between the expert’s qualifications and the patent at issue. *See SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1373 (Fed. Cir. 2010). It is not necessary for Mr. Bohannon to demonstrate that he spent the bulk of his career designing power supplies. Indeed, to testify as an expert under FRE 702, a person need not be one of ordinary skill, but may be ““qualified in the pertinent art.”” *See B/E Aerospace, Inc. v. MAG Aerospace Indus. LLC*, Case IPR2014-01513 (PTAB March 18, 2016) slip op. at 13–14 (Final Written Decision) (sustaining consideration of testimony of expert witness that lacked hands-on experience with the claimed subject matter). We agree with Petitioner that Mr. Bohannon’s experience over 25 years, including his work on “buck and boost” converters and flyback power supplies provides him sufficient experience and knowledge of the claimed subject matter for his opinion to remain of record. Indeed, although the academic background of Patent Owner’s expert, Dr. Holberg, is extensive, his CV and declaration state only that he has “experience with the technology described in the ’764 Patent” including various electrical components and circuits involved (resistors, transformers, switching circuit). Ex. 2001 ¶ 8. Patent Owner’s expert, Dr. Holberg, states that he has designed high frequency synthesizers

for hard-disk read-channel applications and started a company where he designed A/D converters, and other circuits, but does not state explicitly that he designed power supplies. *Id.* ¶ 11.

We further note that neither expert's testimony has been a significant factor in determining the outcome of this proceeding. Our citations to Mr. Bohannon's testimony mostly concern Patent Owner's criticism of Mr. Bohannon's testimony in the Patent Owner Response. Policy considerations for excluding expert testimony, such as those implemented by the gatekeeping framework established by the Supreme Court in *Daubert v. Merrell Dow Pharms., Inc.*, 509 U.S. 579 (1993), are less compelling in bench proceedings such as *inter partes* reviews than in jury trials. *See, e.g., Volk v. United States*, 57 F. Supp. 2d 888, 896 n.5 (N.D. Cal. 1999); *In re Bay Area Material Handling, Inc.*, No. C 95-1163 VRW, 1995 WL 729300, at \*6 (N.D. Cal. Dec. 4, 1995). In the context of this proceeding, we can assess adequately each expert's testimony and assign it appropriate weight.

Having weighed the evidence and arguments presented, we deny Patent Owner's Motion to Exclude the testimony of Petitioner's expert.

## CONCLUSION

Having reviewed all the evidence presented and the arguments of the parties, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claim 5 is unpatentable as anticipated by Bonte, but has not demonstrated by a preponderance of the evidence that claims 6 and 7 are anticipated by Bonte.

ORDER

In consideration of the above, it is  
ORDERED that claim 5 of the '841 patent is unpatentable;  
FURTHER ORDERED that Patent Owner's Motion to Exclude is  
DENIED; and  
FURTHER ORDERED, that because this is a final written decision,  
parties to the proceeding seeking judicial review of the decision must  
comply with the notice and service requirements of 37 C.F.R. § 90.2.

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