

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01560
Patent 5,912,188

Before GRACE KARAFFA OBERMANN, KRISTINA M. KALAN, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Micron Technology, Inc. (“Petitioner”) challenges the patentability of claims 1–5, 7–13, 15–23, and 25–29 of U.S. Patent No. 5,912,188. Ex. 1001 (“the ’188 patent”), assigned to Lone Star Silicon Innovations, LLC (“Patent Owner”).¹ Claims 1, 2, 4, 5, and 7–10 have been disclaimed. Ex. 2013.

We have jurisdiction under 35 U.S.C. § 6. This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 3, 11–13, 15, and 18–20 of the ’188 patent are unpatentable. We determine that Petitioner has not shown by a preponderance of the evidence that claims 16, 17, 21–23, and 25–29 of the ’188 patent are unpatentable.

I. BACKGROUND

A. *Procedural History*

Petitioner filed a Petition seeking *inter partes* review of claims 1–5, 7–13, 15–23, and 25–29 of the ’188 patent. Paper 1 (“Pet.”). Patent Owner filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). We instituted *inter partes* review of claims 1–5, 8–13, 15, and 18–20 and denied institution as to claims 7, 16, 17, 21–23, and 25–29. Paper 10 (“Institution Decision” or “Dec.”).

¹ Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 38, 1.

Patent Owner filed a Response. Paper 15 (“PO Resp.”).² Concurrent with the Response, Patent Owner filed a disclaimer of claims 1, 2, 4, 5, and 7–10 of the ’188 patent. Ex. 2013.

Following the Supreme Court’s decision in *SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348 (2018), we modified our Institution Decision to include review of all challenged claims on all grounds presented in the Petition. Paper 17. With the Board’s prior authorization, Patent Owner filed a supplemental response regarding the newly-instituted grounds. Paper 22 (“PO Supp. Resp.”)

Petitioner filed a Reply. Paper 27 (“Pet. Reply”). With the Board’s prior authorization (Ex. 2024), Patent Owner filed a Sur-Reply addressing limited issues. Paper 31 (“PO Sur-Reply”).

With the Petition, Petitioner filed a declaration of Richard Fair, Ph.D. Ex. 1003. Patent Owner cross-examined Dr. Fair and filed a transcript of his deposition testimony as Exhibit 2007. With the Reply, Petitioner filed a second declaration of Dr. Fair. Ex. 1022.

With the Preliminary Response, Patent Owner filed a declaration of Wilmer R. Bottoms, Ph.D. Ex. 2001. With the Patent Owner Response, Patent Owner filed a second declaration of Dr. Bottoms. Ex. 2012. With its Supplemental Response, Patent Owner filed a third declaration of Dr. Bottoms. Ex. 2020. With its Sur-Reply, Patent Owner filed a fourth declaration of Dr. Bottoms. Ex. 2025. Petitioner cross-examined

² Two exhibits accompanying Patent Owner’s Response were filed less than one hour past the deadline. Good cause having been shown, Patent Owner’s unopposed motion to excuse the late filing of these exhibits (Paper 16) is granted.

Dr. Bottoms twice and filed transcripts of his deposition testimony as Exhibits 1024 and 1030.

Pursuant to the parties' requests, oral argument in Case IPR2017-01560 and Case IPR2017-01561 was consolidated into a single argument, which was held September 18, 2018. A transcript of the oral argument was entered in the record. Paper 40 ("Tr.").

B. Related Matters

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner states that the '188 patent has been asserted in the following pending appellate and district court proceedings: *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, Appeal No. 2018-1578 (Fed. Cir., filed Feb. 15, 2018) and *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (N.D. Cal., filed Mar. 16, 2018). Paper 38, 2–3.

Pursuant to 37 C.F.R § 42.8(b)(2), the parties identify the following *inter partes* review proceeding involving the '188 patent: *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01561. Pet. 3; Paper 38, 1.

C. The '188 Patent (Ex. 1001)

The '188 patent, titled "Method of forming a contact hole in an interlevel dielectric layer using dual etch stops," was issued June 15, 1999 from Application No. 08/905,686, filed August 4, 1997. Ex. 1001, [21], [22], [45], [54].

The '188 patent relates to integrated circuit manufacturing, and more specifically, to a method of forming a contact hole in an interlevel dielectric layer using dual etch stops. *Id.* at [54], [57], 1:7–10.

The '188 patent addresses the problem of overetching and gouging of underlying materials when forming contact holes. *Id.* at 2:29–50, 2:65–67, 3:2–4. According to the '188 patent, one known solution is an interlevel dielectric layer with a thick silicon dioxide layer on a thin silicon nitride layer and a two-step etching process, whereby the first etch is highly selective of silicon dioxide with respect to silicon nitride. *Id.* at 2:51–56. The '188 patent states that this approach has a drawback in that the second etch is highly selective of both silicon nitride and silicon and may cause substantial damage to an underlying silicon surface. *Id.* at 2:58–63.

The solution proposed by the '188 patent is an interlevel dielectric with first, second, and third dielectric layers and a three-step etching process, whereby the first dielectric layer is etched using the second dielectric layer as an etch stop, and the second dielectric layer is etched using the third dielectric layer as an etch stop. *Id.* at 3:4–10.

Figures 1A–1J of the '188 patent illustrate process steps for forming a contact hole in an interlevel dielectric. *Id.* at 4:17–20. Figures 1D through 1G are reproduced below:

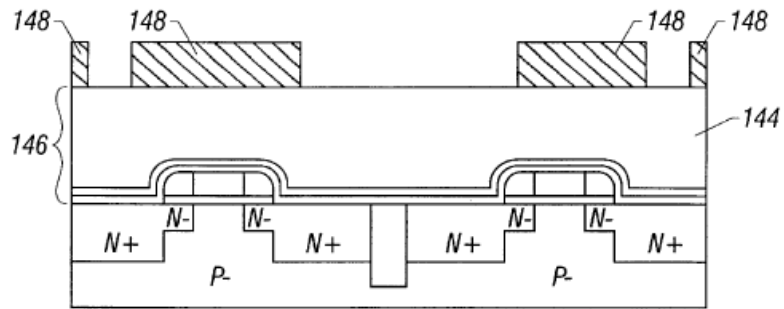


FIG. 1D

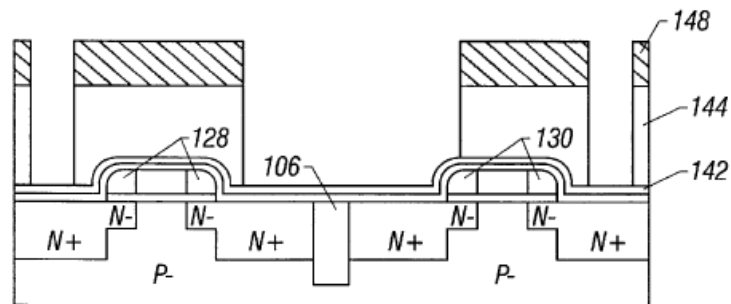


FIG. 1E

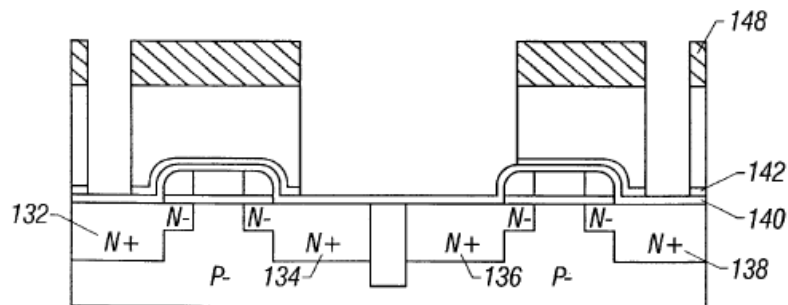


FIG. 1F

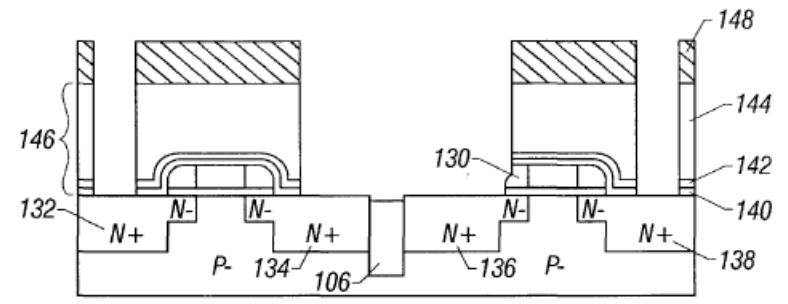


FIG. 1G

Figures 1D through 1G of the '188 patent illustrate process steps for forming a contact hole in an interlevel dielectric. Ex. 1001, 4:17–20. Figure 1D

shows interlevel dielectric layer 146, including silicon oxide layer 140, silicon nitride layer 142, and silicon oxide layer 144. *Id.* at 5:31–54. The interlevel dielectric layer is formed on a silicon substrate having active regions separated by trench oxide 106. *Id.* at 4:29–38, 5:31–54. Each active region includes a gate oxide layer and a gate, which are formed on the substrate, and source and drain regions, which are formed in the substrate. *Id.* at 4:44–5:30. Patterned photoresist layer 148 is formed on silicon oxide layer 144 to define contact holes. *Id.* at 5:59–67.

Figure 1E shows the result of a first etching step. According to the '188 patent, “a long anisotropic reactive ion etch is applied that is highly selective of silicon dioxide with respect to silicon nitride using photoresist layer 148 as an etch mask and using nitride layer 142 as an etch stop” to form holes in oxide layer 144 that extend to nitride layer 142. *Id.* at 6:1–5.

Figure 1F shows the result of a second etching step. According to the '188 patent, “the etch chemistry is changed and a brief anisotropic reactive ion etch is applied that is highly selective of silicon nitride with respect to silicon dioxide using photoresist layer 148 as an etch mask and using oxide layer 140 as an etch stop” to form holes in nitride layer 142 that extend to oxide layer 140. *Id.* at 6:14–19.

Figure 1G shows the result of a third etching step. According to the '188 patent, “the etch chemistry is changed again and a brief anisotropic reactive ion etch is applied that is highly selective of silicon dioxide with respect to silicon nitride using photoresist layer 148 as an etch mask.” *Id.* at 6:25–28.

After completion of the etching steps, the photoresist layer is stripped, conductive plugs are formed in the contact holes, and a metal-1 pattern is formed in contact with the conductive plugs. *Id.* at 6:48–7:19, Figs. 1H–1J.

D. Illustrative Claim

The Petition challenges claims 1–5, 7–13, 15–23, and 25–29 of the '188 patent, of which claims 1, 11, and 21 are independent. Ex. 1001, 8:57–12:35. Claim 1, which has been disclaimed, is nevertheless illustrative of the challenged claims and is reproduced below:

1. A method of forming a contact hole in an interlevel dielectric layer using dual etch stops, comprising:
 - providing a semiconductor substrate;
 - forming a gate over the substrate,
 - forming a source/drain region in the substrate;
 - providing a source/drain contact electrically coupled to the source/drain region;
 - forming an interlevel dielectric layer that includes first, second and third dielectric layers over the source/drain contact;
 - forming an etch mask over the interlevel dielectric layer;
 - applying a first etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the etch mask using the second dielectric layer as an etch stop, thereby forming a first hole in the first dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer;
 - applying a second etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the etch mask using the third dielectric layer as an etch stop, thereby forming a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact; and
 - applying a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the etch mask, thereby forming a third hole in the third dielectric layer that extends to the source/drain contact,

wherein the first, second and third holes in combination provide a contact hole in the interlevel dielectric layer.

Ex. 1001, 8:58–9:22.

E. Asserted Grounds of Unpatentability

The Petition challenges claims 1–5, 7–13, 15–23, and 25–29 of the '188 patent under 35 U.S.C. § 103(a). Claims 1, 2, 4, 5, and 7–10 have been disclaimed. Ex. 2013. Taking into account the disclaimer, the asserted grounds of unpatentability that remain in this decision are as follows:

Reference(s)	Claim(s)
Hashimoto ³	3, 8, 11–13, 15, 18, and 19
Hashimoto and Sung ⁴	20
Hashimoto and Kawai ⁵	16, 17, 21–23, and 25–27
Hashimoto, Sung, and Kawai	28 and 29

Pet. 4.

II. ANALYSIS

A. Claim Construction

The '188 patent expired on August 4, 2017. PO Resp. 16 n.1. For expired patents, we apply the claim construction standard set forth in

³ JP H9-64297, published March 7, 1997, including original Japanese application and certified English translation, Ex. 1005 (“Hashimoto”).

⁴ US 5,550,078, filed June 28, 1995 and issued August 27, 1996, Ex. 1006 (“Sung”).

⁵ JP H8-46173, published February 16, 1996, including original Japanese application and certified English translation, Ex. 1007 (“Kawai”).

Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (“the Board’s review of the claims of an expired patent is similar to that of a district court’s review”); see also *Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed. App’x 1019, 1024 (Fed. Cir. 2016) (holding that in an *inter partes* review, “[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]”).

Under the *Phillips* standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

In the Institution Decision, we construed “anisotropic etch” as “an etch that is directional such that horizontal surfaces are etched at a higher rate than vertical surfaces and straight, nearly vertical, sidewalls without undercutting of the etch mask are produced.” Dec. 13. The parties propose two modifications of our preliminary construction, one of which is agreed upon, and the other of which is disputed. The parties agree that the construction for “anisotropic etch” should not include a requirement for straight, nearly vertical, sidewalls without undercutting of the etch mask. PO Resp. 20, 23–29; Pet. Reply 3. The parties disagree as to whether an “anisotropic etch” requires a vertical etch rate that is *substantially* higher than the lateral etch rate, as proposed by Patent Owner. PO Resp. 19–20, 29 (emphasis added); Pet. Reply 3–5.

Each party concedes, however, that the construction of “anisotropic etch” is not critical to its position. Tr. 4:4–9 (Petitioner); *id.* at 24:22–25:3 (Patent Owner). In view of the parties’ concessions and the record as a whole, we determine it is not necessary to construe the term “anisotropic etch” for purposes of resolving the controversy. Although we provided a preliminary construction for “anisotropic etch” in the Institution Decision, we do not reach a final determination on the construction of that phrase, given that resolving the construction is not necessary to this final decision. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Principles of Law

Regarding the challenged claims of the ’188 patent that have not been disclaimed by Patent Owner, Petitioner bears the burden of proving unpatentability, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish the facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is

resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In this case, neither party relies on objective evidence of nonobviousness, i.e., secondary considerations.

C. Level of Ordinary Skill in the Art

Petitioner’s declarant, Dr. Fair, testifies that a person of ordinary skill in the art (“POSA”) would have had at least a Bachelor of Science degree in electrical engineering, chemical engineering, chemistry, physics, materials science, or a closely related field, along with at least five years of experience in semiconductor fabrication. Ex. 1003 ¶ 18. Dr. Fair further testifies that an individual with an advanced degree in one of these fields would require less experience in semiconductor fabrication. *Id.* Patent Owner’s declarant, Dr. Bottoms, testifies that a POSA would have held a master’s degree in physics, electrical engineering or a related field and at least three years of experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. Ex. 2012 ¶ 30.

In our view, there is little difference between the declarants’ descriptions of a POSA, and our patentability determinations would be the same regardless of which description we adopt. For purposes of our Institution Decision, we accepted the description provided by Dr. Bottoms. Dec. 14 (citing Ex. 2001 ¶ 30). Dr. Fair testifies that Dr. Bottoms’ description of the level of ordinary skill in the art is consistent with the level

proposed in his original declaration (Ex. 1003 ¶ 18), and the Board's adoption of that description does not change his opinions. Ex. 1022 ¶ 5.

Therefore, consistent with our Institution Decision, we adopt Dr. Bottoms' description of a POSA. Ex. 2012 ¶ 30. We also rely on the cited prior art references as reflecting the level of ordinary skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

After reviewing the qualifications of Dr. Fair and Dr. Bottoms, as set forth in each witness's declaration and curriculum vitae ("CV"), we find that each of these declarants is qualified to testify from the perspective of a POSA. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2012 ¶¶ 6–19.

Regarding Dr. Fair, we find particularly relevant his experience as an acting president, vice president, and director at the Microelectronics Center of North Carolina ("MCNC") from 1981 to 1994, where he directed research on semiconductor processing, including photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD of thin films, metallization, and anisotropic etch processes, and conducted research on multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, and selective tungsten deposition for via filling. Ex. 1003 ¶ 9, Ex. 1004, 3. Regarding Dr. Bottoms, we find particularly relevant his experience at Varian Associates from 1976 to 1985, including his experience as Manager of Research and Development, where he was involved in developing tools used to fabricate semiconductor devices including lithography, sputtering, ion implantation, etching, and evaporation processes. Ex. 2012 ¶¶ 9–11; Ex. 2002, 1.

Petitioner argues that we should credit Dr. Fair's testimony and reject Dr. Bottoms' testimony because "Dr. Bottoms' expertise in the field pales in comparison to Dr. Fair's." Pet. Reply 25–26. Petitioner bases its argument on Dr. Bottoms' response to deposition questions regarding "Miller capacitance" and "the Miller effect" and a comparison of the number of papers and conference presentations for the period 1984 to 2004, as listed on each declarant's CV. *Id.* (citing Ex. 1004, 3–16; Ex. 1024, 69:4–10 [*sic*, 69:14–21]; Ex. 2002, 6–7). Petitioner's argument does not persuade us to reject Dr. Bottoms' testimony. Dr. Bottoms' inability to recall a name (Miller) associated with a particular scientific principle does not in our view conclusively prove a lack of expertise. Furthermore, the number of papers and conference presentations listed on Dr. Bottoms' CV is not the sole or necessarily the best measure of his level of expertise. The number of such items may depend on the institutional setting in which he worked, e.g., in industry rather than academia. On this record, we find that both Dr. Fair and Dr. Bottoms are sufficiently qualified to opine from the perspective of a POSA at the time of the invention. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2012 ¶¶ 6–19.

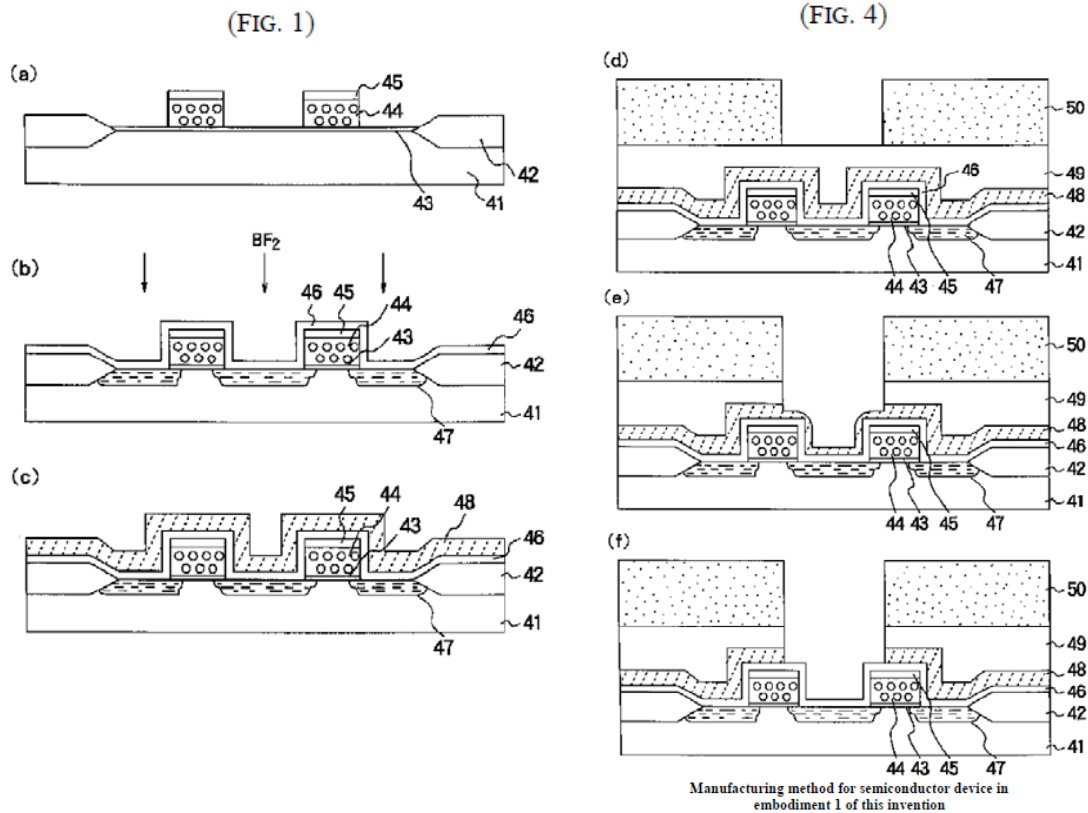
D. Prior Art References

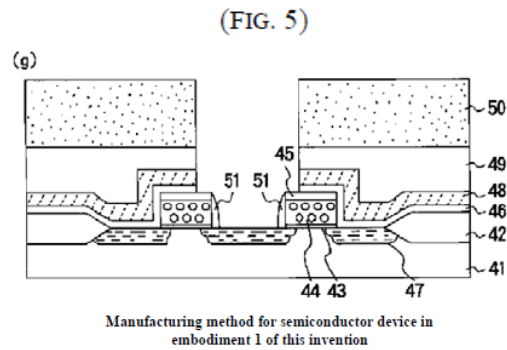
1. Hashimoto (Ex. 1005)

Hashimoto discloses a method for manufacturing a semiconductor device and, more specifically, a method for opening a contact hole in a wiring pattern. Ex. 1005, p. 2 (claim 1), ¶ 1. Hashimoto discloses forming three layers on a silicon substrate: a first silicon oxide-based insulating film, a silicon nitride film, and a second silicon oxide-based interlayer insulating film. *Id.* at p. 2 (claim 1), ¶ 6. Hashimoto discloses a three-step process for

opening a contact hole: (1) selectively dry etching the second interlayer insulating film with the silicon nitride film as an etching stopper; (2) selectively dry etching the silicon nitride film with the silicon oxide-based film as an etching stopper; and (3) selectively dry etching the first silicon oxide-based film while preventing penetration of the silicon substrate. *Id.* at p. 2 (claims 1 and 3), ¶ 6.

Petitioner relies on Hashimoto's Embodiment 1, which is described in paragraphs 7–10 and illustrated in Figures 1(a)–(c), 4(d)–(f), and 5(g), which are reproduced below:





Hashimoto Figures 1(a)–(c), 4(d)–(f), and 5(g) illustrate a semiconductor manufacturing method. Ex. 1005 ¶ 7. Figure 1(a) shows silicon substrate 41, field oxide film 42, gate oxide film 43, phosphorus-doped polycrystalline silicon conductive layer 44, and Non-doped Silicate Glass (“NSG”) insulating layer 45. *Id.* Hashimoto discloses that conductive layer 44 and NSG layer 45 are patterned to form a word line (gate) wiring pattern. *Id.* Figure 1(b) shows NSG film 46 and ion-implanted source/drain 47. *Id.* ¶ 8. Figure 1(c) shows silicon nitride film 48. *Id.* Figure 4(d) shows Boron Phospho Silicate Glass (“BPSG”) interlayer insulation film 49 and photoresist/contact hole pattern 50. Figures 4(e), 4(f), and 5(g) show the results of first, second, and third etching steps, respectively. *Id.* ¶¶ 8, 9.

Hashimoto discloses that, in the first etching step, BPSG 49 is removed using resist pattern 5 as an etching mask and silicon nitride film 48 as an etch stopper. *Id.* ¶ 8. In the second etching step, silicon nitride film 48 is removed without NSG film 46 being etched. *Id.* ¶ 9. In the third etching step, NSG film 46 is etched and source/drain 47 is not etched. *Id.* After the third etching step, resist pattern 50 is removed, bit contacts are formed, and other components are formed to complete the manufacture of a dynamic random access memory (“DRAM”) cell. *Id.*

2. *Sung (Ex. 1006)*

Sung discloses a process for fabricating DRAM devices on a semiconductor substrate using a complementary metal oxide (CMOS) field effect transistor approach. Ex. 1006, 1:7–9, 2:15–17, 3:65–4:1. Sung’s process includes forming a first interlevel dielectric, forming contact hole openings to source and drain regions, contact metallization, and forming a first metal structure. *Id.* at 3:25–29. With reference to Figure 18, Sung discloses depositing a first interlevel dielectric (“ILD-1”) 34 of BPSG. *Id.* at 7:16–19, Fig. 18. Sung discloses forming contact hole 35 in ILD-1 and filling the contact hole with TiN-tungsten to form contact stud 36. *Id.* at 7:26–32, Fig. 18. Sung discloses depositing and patterning a layer of Al-Cu to create metal-1 (“M1”) structure 37. *Id.* at 7:32–36, Fig. 18.

3. *Kawai (Ex. 1007)*

Kawai discloses a method of producing a semiconductor device, such as a DRAM. Ex. 1007 ¶¶ 1, 2. Petitioner relies on Kawai’s Example 1, which is described in paragraphs 54–80 and illustrated in Figures 1–13. *See, e.g.,* Pet. 26–28, 69–70. Petitioner directs us to Kawai Figure 13 (Pet. 28), which is reproduced below:

(FIG. 13)

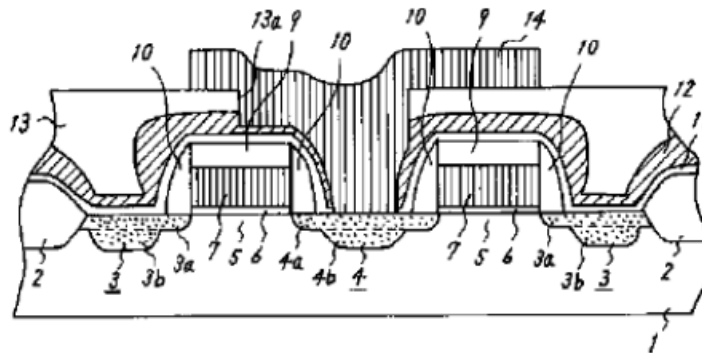


Figure 13 shows a cross-section of a semiconductor device, including semiconductor substrate 1, source/drain regions 3 and 4, gate electrode 7, gate insulating overlay silicon oxide film 9, sidewall silicon oxide film 10, first insulating layer 11 made of silicon oxide film, etching stopper layer (second insulating layer) 12 made of silicon nitride film, interlaminar insulating layer 13 made of silicon oxide film, contact hole 13a, and wiring layer 14. Ex. 1007 ¶¶ 54–59. Kawai discloses process steps for forming insulating layers 11, 12, and 13 and a contact hole resist mask. *Id.* ¶¶ 64–69, Figs. 5–9. Kawai discloses three etching steps for forming a contact hole. *Id.* ¶¶ 70–76. In the first etching step, dry etching that is highly selective of silicon oxide relative to silicon nitride is performed using a resist mask to form contact hole 13a in interlaminar insulating layer 13. *Id.* ¶ 70, Fig. 10. In the second etching step, anisotropic etching that is highly selective of silicon nitride relative to silicon oxide is performed to form an opening 12a in the etching stopper layer 12. *Id.* ¶ 74, Fig. 11. In the third etching step, dry etching that is highly selective of silicon oxide relative to silicon nitride is performed to form an opening 11a in insulating layer 11. *Id.* ¶ 76, Fig. 12.

E. Hashimoto-Based Grounds

Petitioner contends that claims 1–5, 8–13, 15, 18, and 19 are unpatentable as obvious in view of Hashimoto and that claim 20 is unpatentable as obvious in view of Hashimoto alone or in combination with Sung. Pet. 28–64. Claims 1, 2, 4, 5, and 7–10 have been disclaimed. Ex. 2013. We address the remaining claims below.

1. Claim 3

Claim 3 depends from claim 1 and recites “the first, second and third etches are anisotropic etches and the contact hole has straight sidewalls.”

Ex. 1001, 9:26–28. Petitioner directs us to substantial evidence that the limitations of claim 1 are disclosed or suggested by Hashimoto. Pet. 29–43. Patent Owner does not contest that evidence. See PO Resp. i–ii.

Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that Hashimoto discloses or suggests the limitations of claim 3 that are incorporated from claim 1. The remainder of our analysis focuses on the disputed limitations of claim 3, i.e., anisotropic etches and straight sidewalls.

a. Anisotropic etches

Petitioner contends that the etching conditions disclosed in Hashimoto produce an anisotropic etch and that Hashimoto Figures 4(e), 4(f), and 5(g) show anisotropic etches. Pet. 48 (first etch), 51–52 (second etch), 53 (third etch), 55 (claim 3). In the alternative, Petitioner contends that it would have been obvious to a POSA to use anisotropic etches for Hashimoto’s first, second, and third etches. *Id.* at 49–50, 52, 54–55.

Patent Owner argues that Hashimoto does not disclose or suggest anisotropic etches. PO Resp. 43–55. Patent Owner additionally argues that a POSA would not have been motivated to use anisotropic etch steps. *Id.* at 44, 56–58.

In the Institution Decision, we stated: “Even if Hashimoto’s disclosed etch conditions are not ‘necessarily’ anisotropic, unpatentability may be shown, if the evidence demonstrates that it would have been obvious to use an anisotropic etch.” Dec. 19–20 (citing *Southwire Co. v. Cerro Wire LLC*, 870 F.3d 1306, 1311–12 (Fed. Cir. 2017)). For the reasons discussed below, and based on the record developed during trial, we find that a POSA would have recognized that either anisotropic etches or isotropic etches are suitable

for Hashimoto's etch steps and that Petitioner has shown by a preponderance of the evidence that a POSA would have had a reason or motivation to use anisotropic etches for each of those steps.

Hashimoto discloses that the first, second, and third etches are carried out using dry etching, which the '188 patent discloses may be used to produce an anisotropic etch. Ex. 1005, claim 3, ¶¶ 8, 9; Ex. 1001, 1:64–2:2. It is undisputed that isotropic dry etching and anisotropic dry etching were both well known in the art. *See, e.g.*, Ex. 2012 ¶ 91 (“Plasma etch processes, including reactive ion etch, were well known in the art to be either isotropic or anisotropic.”); Ex. 3001, 11:35–42; Tr. 37:8–9 (Patent Owner: “It was known in the art that plasma processes could be either isotropic or anisotropic in nature.”). It is also undisputed that a POSA would have known how to control the etching conditions so as to produce an anisotropic etch. Ex. 2012 ¶¶ 59–61, 91 (discussing parameters that can be varied to control the isotropic versus anisotropic characteristics of an etch); *see also* Ex. 1010,⁶ 1 (“A wide range of conditions have been employed to achieve anisotropic etching.”). The '188 patent is silent regarding etching conditions, such as equipment, pressure, power, gas composition, and flow rate. The '188 patent thus presumes that the conditions necessary to produce an anisotropic etch were known in the art.

⁶ V.M. Donnelly et al., *Anisotropic Etching of SiO₂ in Low-Frequency CF₄/O₂ and NF₃/Ar Plasmas*, 55(1) J. Appl. Phys. 242–252 (Jan. 1984), Ex. 1010 (“Donnelly”). We cite Donnelly (Ex. 1010) using the page numbers added by Petitioner.

Petitioner has established, by a preponderance of the evidence, three rationales for why a POSA would have been motivated to use anisotropic etches for Hashimoto's first, second, and third etches.

First, Petitioner has shown that a POSA would have been motivated to use anisotropic etches in order to produce an integrated circuit with high-resolution patterning and features that are submicron in size. Pet. 50 (citing Ex. 1003 ¶ 148); Pet. Reply 27. Our finding is supported by Dr. Fair's testimony that a POSA "would have known that anisotropic etching 'is important for high-resolution patterning of silicon integrated circuits,' like those taught in Hashimoto." Ex. 1003 ¶ 148 (quoting Ex. 1010, 1 (Donnelly)). Our finding is further supported by Donnelly, which teaches that anisotropic etching "is important for high-resolution patterning of silicon integrated circuits" and "is often desirable for contact windows in silicon integrated circuits." Ex. 1010, 1. We find that Donnelly's teachings are applicable to Hashimoto, which discloses a method of forming contact holes and addresses problems associated with "increasingly fine patterns" in semiconductor devices. Ex. 1005 ¶¶ 1, 3.

Our finding is further supported by the submicron size of Hashimoto's contact holes. Pet. Reply 27; Ex. 1005 ¶ 8 (disclosing a contact hole pattern with a diameter of 0.7 μm). The experts agree that a POSA understood at the time of the invention that an isotropic etch is undesirable for submicron features. Ex. 1022 ¶ 11; Ex. 2012 ¶ 54 (citing Ex. 2006,⁷ 80).

Second, Petitioner has shown that a POSA would have been motivated to use anisotropic etches for Hashimoto's etches in order to form

⁷ Jerzy Ruzyllo, *Semiconductor Glossary* (1st ed. 2004), Ex. 2006 (excerpts).

contact holes with straight sidewalls. Pet. 50, 52 (citing Ex. 1003 ¶¶ 148, 155); Pet. Reply 27. As Patent Owner concedes, “straight sidewalls are typically formed using highly anisotropic etch steps.” PO Resp. 53. Our finding is supported by Dr. Fair’s testimony that a POSA would have been motivated to use anisotropic etches for Hashimoto’s first, second, and third etches in order to produce a contact hole having straight sidewalls. Ex. 1003 ¶¶ 147, 148, 153, 155, 160, 162. Our finding is further supported by Dr. Fair’s undisputed testimony that straight sidewalls would have been understood by a POSA to be a benefit. Ex. 2007, 77:15–22.

Third, Petitioner has shown that a POSA would have been motivated to form Hashimoto’s contact holes using anisotropic etches, rather than isotropic etches, in order to avoid increasing the contact area over the gates causing undesirable parasitic capacitance known as Miller capacitance. Pet. Reply 14–15, 27–28 (citing Ex. 2007, 86:25–87:25; Ex. 1022 ¶¶ 18–20).⁸ Our finding is supported by Dr. Fair’s deposition testimony, as follows:

If you used an isotropic etch for [Hashimoto’s layer] 48, you would balloon the contact hole open on top of the gates, such that when you filled your bit line contact, you would have significantly higher parasitic capacitance; so when you swing your bit line up and down, you would be having to charge and discharge that parasitic capacitance over the gate.

Ex. 2007, 87:4–10. According to Dr. Fair, the desire not to balloon open the contact over the gates so as to increase parasitic capacitance “would have been known and obvious to one of ordinary skill in the art.” *Id.* at 87:11–25.

⁸ Patent Owner requested and received authorization to file a Sur-Reply to respond to Petitioner’s reply arguments regarding Miller capacitance. Ex. 2024, 2–3; PO Sur-Reply 1–5. We address Patent Owner’s Sur-Reply arguments below.

Our finding is further supported by Dr. Fair’s reply testimony that isotropic etching in Hashimoto would increase the contact area over the gates, which a POSA would recognize as causing an increase in undesirable parasitic capacitance known as Miller capacitance. Ex. 1022 ¶¶ 18–20. Dr. Bottoms agrees with Dr. Fair’s testimony that “Miller capacitance” is “a component of ‘the amount of drain-gate capacitance, C_{gd} , which in turn depends on the amount of overlap between the gate and the drain contact.’” Ex. 2025 ¶ 5 (quoting Ex. 1022 ¶ 19); see PO Sur-Reply 2. Dr. Bottoms refers to capacitance between the gate electrode and the drain of a transistor as “gate-drain capacitance” and agrees that it is undesirable parasitic capacitance. Ex. 2025 ¶¶ 5, 6.

We now turn to Patent Owner’s arguments regarding motivation to use anisotropic etches for Hashimoto’s etch steps. PO Resp. 56–58.

Patent Owner argues that a POSA would have been motivated to use an isotropic etch to remove vertical portions of silicon nitride layer 48 in Hashimoto’s first and second etch steps. *Id.* at 51, 56–57. Patent Owner relies on Dr. Bottoms’ testimony that an isotropic etch would be more efficient and simpler than an anisotropic etch for removing the vertical portions of layer 48. *Id.* at 51, 57; Ex. 2012 ¶ 99.

The experts agree that Hashimoto Figure 4(f) shows vertical portions of the silicon nitride layer are removed by the second etch. Ex. 2012 ¶ 98; Ex. 1022 ¶ 28. But the experts disagree as to whether removal of vertical portions would have motivated the use of an isotropic etch. Ex. 1022 ¶¶ 28, 35; Ex. 2007, 85:19–87:10; Ex. 2012 ¶ 99. On this point, we are persuaded by Petitioner’s argument (Pet. Reply 20) and the cited testimony of Dr. Fair (Ex. 1022 ¶ 28) that an anisotropic etch would remove vertical portions of

Hashimoto's silicon nitride layer and, further, that the benefits of an anisotropic etch outweigh any time-saving advantage of an isotropic etch identified by Dr. Bottoms. More specifically, we credit the following testimony of Dr. Fair:

Even assuming there would be an increase in time [to remove the vertical portions of silicon nitride layer 48], the benefit of producing straight sidewalls with no undercutting of the etch mask using an anisotropic etch *would outweigh* the alleged time advantage of an isotropic etch, because the isotropic etch would undercut the etch mask and impair the operation of the device due to an increase in Miller capacitance. Moreover, there is no reason to believe the time would be excessive and a person of ordinary skill in the art would have understood that longer times provide a better ability for quality control. Indeed, it is common in anisotropic etching to extend the etching time by up to 100% just to be sure that all undesired material is removed during over etching and a quality etching step is achieved. Thus, a person of ordinary skill in the art would, *on balance*, prefer using an anisotropic etch to protect the performance of the device and the process yield over the time saved, if any, with an isotropic etch.

Ex. 1022 ¶ 28 (emphasis added); *see also* Ex. 2007, 86:25–87:10 (an isotropic etch would “balloon the contact hole open on top of the gates” resulting in “significantly higher parasitic capacitance”).

Patent Owner and its expert do not dispute that the vertical portions of Hashimoto's silicon nitride layer would be removable with an anisotropic etch. Indeed, Dr. Bottoms testifies that “every plasma etch includes some degree of both isotropic and anisotropic characteristics.” Ex. 2012 ¶ 40; PO Resp. 7; Ex. 1024, 60:2–5; 78:21–79:2; *see also* Tr. 54:14–15 (Patent Owner: “the experts have both agreed that lateral etching can be a component of an anisotropic etch”).

Dr. Bottoms testifies that isotropic etching would be more efficient and simpler than anisotropic etching for removing vertical portions of the silicon nitride layer. Ex. 2012 ¶ 99. In contrast to the above-quoted testimony of Dr. Fair, however, Dr. Bottoms does not weigh any advantage of an isotropic etch, such as time saving, against the benefits of an anisotropic etch, including the desire for straight sidewalls and the desire to avoid Miller capacitance. Ex. 1022 ¶ 28. Nor does Dr. Bottoms explain why removal of the vertical portions of the silicon nitride layer would have been important to a POSA in the context of Hashimoto’s disclosed device and process. Accordingly, we give greater weight to the above-quoted testimony of Dr. Fair (Ex. 1022 ¶ 28) relied upon by Petitioner than to the testimony of Dr. Bottoms (Ex. 2012 ¶ 99) cited by Patent Owner.

Next, Patent Owner argues that a POSA generally understood “it was difficult to achieve both high selectivity and anisotropy” and “would not undertake the ‘difficult’ project of doing both when Hashimoto’s disclosed and not anisotropic etch would suffice.” PO Resp. 57–58 (citing Ex. 2012 ¶ 100; Ex. 2008,⁹ 357; Ex. 1012, 1).

Dr. Bottoms testifies that “a person having ordinary skill in the art understood that it was difficult to achieve both high selectivity and a high degree of anisotropy.” Ex. 2012 ¶ 100. As Patent Owner recognizes, however, the claims of the ’188 patent merely require an anisotropic etch, not a “high degree of anisotropy.” See PO Resp. 25–26 (contrasting “a mere anisotropic etch” with “a **highly** anisotropic etch”) (emphasis in original).

⁹ C.Y. Yang and S.M. Sze, *ULSI Technology* (1996), Ex. 2008 (excerpts) (“Yang”). Yang is relied upon by Patent Owner to counter Petitioner’s contentions regarding anisotropic etches. PO Resp. 47, 57.

Although Patent Owner and Dr. Bottoms rely on Yang (Ex. 2008) and Siozawa (Ex. 1012), the cited evidence does not support Patent Owner's argument. Patent Owner quotes Yang as stating, "[a]chieving high selectivity and etch anisotropy at the same time is difficult for most ion-enhanced etching processes." PO Resp. 57 (quoting Ex. 2008, 357). As Petitioner argues and Dr. Fair testifies, however, the passage quoted from Yang relates to etching polysilicon or metal silicide, not silicon oxide or silicon nitride—the materials being etched in Hashimoto's contact hole-forming process. Pet. Reply 28; Ex. 2008, 357 (Yang); Ex. 1005 ¶¶ 8, 9 (Hashimoto); Ex. 1022 ¶ 36. Indeed, the passage quoted by Patent Owner appears under the heading, "7.5.2. Polysilicon and Polycide Gate Etching." Ex. 2008, 357. Etching of silicon oxide and silicon nitride are addressed in a separate, subsequent section headed, "7.5.3. Oxide and Nitride Etching." *Id.* In that relevant section, Yang explains that silicon nitride can be etched anisotropically with a high degree of selectivity to both silicon and silicon oxide. *Id.* at 358. Thus, at least with respect to silicon nitride, we agree with Petitioner (Pet. Reply 29) that Yang itself contradicts Patent Owner's argument that it was generally understood that it was difficult to achieve both high selectivity and anisotropy.

Patent Owner quotes Siozawa as stating "it is difficult to achieve both high selectivity and anisotropy." PO Resp. 57 (quoting Ex. 1012, 1). As Petitioner argues and Dr. Fair testifies, however, the quoted statement describes an etch that uses a C₄F₈ plasma. Pet. Reply 29; Ex. 1012, 1; Ex. 1022 ¶ 37. Siozawa goes on to state that, with the addition of oxygen to the C₄F₈ plasma, "[h]igh selectivity of SiO₂ to Si or photoresist and high anisotropy could be achieved." Ex. 1012, 1 (quoted at Pet. Reply 29;

Ex. 1022 ¶ 37). Siozawa, thus, does not support Patent Owner’s argument that high selectivity and anisotropy would be difficult to achieve. As Dr. Bottoms concedes, a POSA knew how to control parameters, including chamber pressure, flow rate, plasma power, etchant gas, and etchant gas concentration, to obtain the desired isotropic or anisotropic etch characteristics. Ex. 2012 ¶¶ 59–61, 91. Moreover, Siozawa discusses the desirability of anisotropic etching for fabricating high-density integrated circuits (Ex. 1012, 1), thus contradicting Patent Owner’s argument that a POSA would not have been motivated to use anisotropic etches to form Hashimoto’s contact holes.

Next, Patent Owner argues that Hashimoto’s third etch “would not necessarily require an anisotropic etch” because the depth of the etch is only 50 nm, and the width of the contact hole is 700 nm. PO Resp. 58 (citing Ex. 1005 ¶ 8; Ex. 2012 ¶ 103). Patent Owner’s argument is persuasively rebutted by Petitioner’s argument that non-directional etching would have undercut the mask. Pet. Reply 9, 16, 21 (citing Ex. 1022 ¶ 21). We credit the cited testimony of Dr. Fair, as follows:

For a single etch, hole size relative to etch layer thickness is a general rule of thumb. However, when you have three layers and the etch undercut for each etch can expand the etch area for the next layer, then a person of ordinary skill in the art would have understood that the rule of thumb no longer applies. In other words, what LSSI is referring to is general guidance that is intended for a single etch step. Hashimoto’s contact hole requires three sequential etches. Isotropic (e.g., non-directional) etches etch in all directions at the same rate and result in undercutting of the etch mask. Thus, each isotropic etch step would balloon open the hole that will define the edge of the masking layer that defines the size of the subsequently etched hole. So instead of relying on a defined mask pattern and vertical

sidewalls to etch a hole, isotropic etching would increase process variability and reduce hole dimensional control.

Ex. 1022 ¶ 21. Dr. Fair’s testimony persuasively explains why anisotropic etching is preferred over isotropic etching in the context of Hashimoto’s contact holes. *Id.* Patent Owner and Dr. Bottoms, on the other hand, rely on the thickness of a single layer—Hashimoto’s 50 nm layer 46—and a general rule of thumb regarding aspect ratio (Ex. 2012 ¶ 103), which, as Dr. Fair explains, does not apply to multi-layer structures and multi-step etch processes like Hashimoto’s (Ex. 1022 ¶ 21).

Patent Owner’s argument also is persuasively rebutted by Petitioner’s argument regarding Hashimoto’s sidewall gate spacers. Pet. Reply 21–22, 30 (citing Ex. 1022 ¶ 32). We credit the following testimony of Dr. Fair relied upon by Petitioner:

In addition, the only way to form sidewall gate spacers 51 from NSG layer 46, as depicted in [Hashimoto] Figure 5(g), would be with an anisotropic etch. Isotropic etching would laterally etch away the vertical sidewall spacers (51) at the same rate that it removes the NSG at the bottom of the hole. This would create a short circuit by exposing the polysilicon gate to the metal contact.

Ex. 1022 ¶ 32. Dr. Fair’s testimony is consistent with Hashimoto, which discloses that, “[i]n the third etching step, NSG film is etched . . . forming side wall NSG 51.” Ex. 1005 ¶ 9. As Dr. Fair persuasively explains, an anisotropic etch is required in order to remove the NSG at the bottom of the contact hole without etching away the vertical sidewall spacers 51. Ex. 1022 ¶ 32. Patent Owner’s argument regarding the depth of the etch does not take into account Hashimoto’s teaching regarding sidewall spacers 51.

Next, Patent Owner advances a number of arguments regarding Miller capacitance. PO Sur-Reply 1–5. Patent Owner argues that increased

parasitic capacitance would have been accepted in exchange for the benefits of Hashimoto's "self-aligned" contact holes, that the contribution of the source/drain electrode is small in comparison to other sources of parasitic capacitance, that a POSA knew how to control parasitic capacitance by increasing the thickness of the dielectric layer on top of the gate, and that the Miller effect is not as significant for DRAMs as for other devices. PO Sur-Reply 2–5 (citing Ex. 2025 ¶¶ 4–14). Although Patent Owner and its expert seek to diminish the significance of Miller capacitance as a motivating factor, they do not dispute that a desire to avoid parasitic capacitance would have been a reason for a POSA to favor anisotropic etches over isotropic etches for Hashimoto's etch steps. More specifically, Patent Owner and its expert do not dispute that isotropic etching would have resulted in increased contact hole size, which would have in turn caused increased overlap between the gate electrode and the source/drain contact and an increase in undesirable parasitic capacitance known as Miller capacitance. PO Sur-Reply 3, 4; Pet. Reply 14–15, 27–28; Ex. 2007, 87:4–25; Ex. 1022 ¶¶ 18, 19.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that it would have been obvious to a POSA to use anisotropic etches for Hashimoto's first, second, and third etch steps.

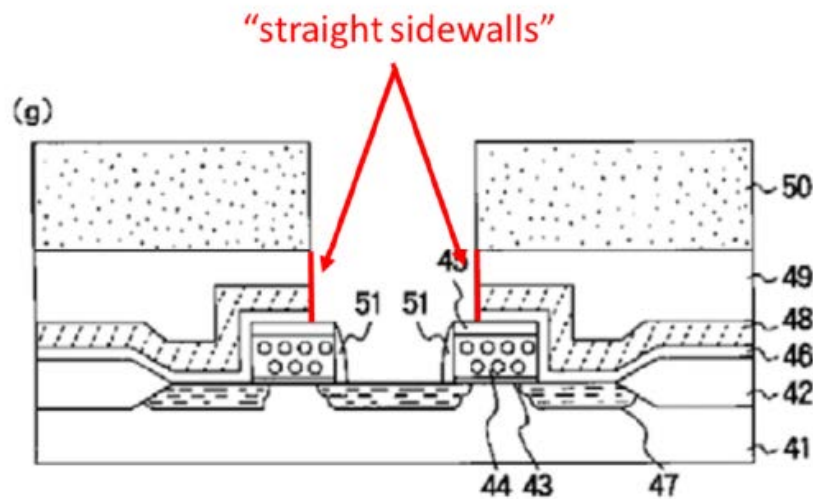
b. Straight sidewalls

Petitioner contends that Hashimoto discloses a contact hole with straight sidewalls. Pet. 48, 51, 53, 55. Petitioner further contends that a POSA "would have known that an anisotropic etch would produce straight sidewalls for the contact hole" and would have been motivated to use

anisotropic etches for Hashimoto's first, second, and third etches in order to form contact holes with straight sidewalls. *Id.* at 49–50, 52.

Patent Owner argues that Hashimoto neither discloses nor suggests contact holes having straight sidewalls. PO Resp. 58–60. Patent Owner additionally argues that a POSA would not have been motivated to replace the stepped sidewalls of Hashimoto with straight sidewalls. *Id.* at 60.

We find that Petitioner’s contention is supported by Hashimoto Figure Figure 5(g), which is reproduced below with Petitioner’s annotations:



Hashimoto Figure 5(g) shows a semiconductor device and a contact hole, which Petitioner and Dr. Fair have annotated to identify straight sidewalls. Pet. Reply 30; Ex. 1022 ¶ 40. Petitioner's reliance on Hashimoto Figure 5(g) to show a contact hole with straight sidewalls can be compared with Patent Owner's reliance on Figure 1E of the '188 patent to show the same feature. Patent Owner's annotation of Figure 1E is reproduced below:

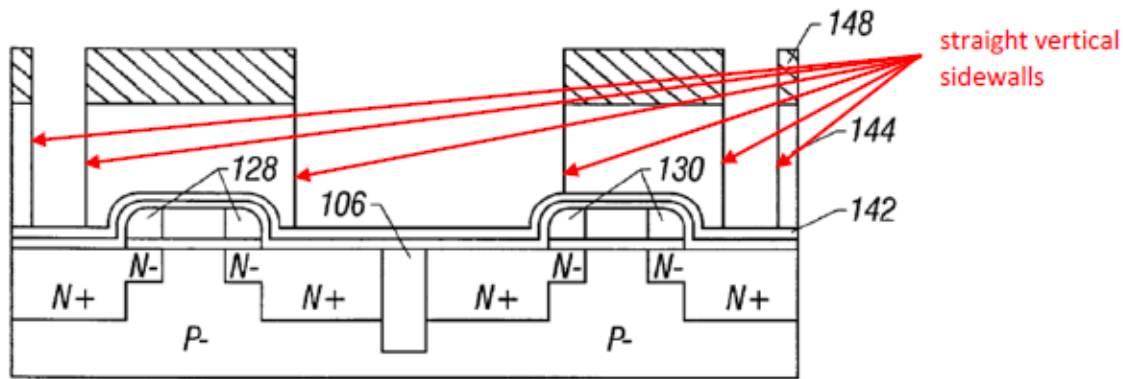


FIG. 1E

Figure 1E of the '188 patent shows contact holes. Patent Owner and Dr. Bottoms have annotated Figure 1E to identify contact holes with straight, vertical sidewalls. PO Resp. 7; Ex. 2012 ¶ 57.

We find that Hashimoto Figure 5(g) shows a contact hole with straight sidewalls in the same manner as Patent Owner contends the '188 patent shows contact holes with straight sidewalls. In both cases, the figures show a contact hole with straight vertical sidewalls, at least where the contact hole is bounded by the interlevel dielectric layers, as opposed to the insulating layers around the gate.

Citing *Nystrom v. Trex Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005), Patent Owner argues that “Hashimoto’s drawing figures cannot be assumed to be proportional or to include all features of the device.” PO Resp. 48. Patent Owner concedes that Hashimoto Figures 4(e) and 4(f) do not show undercutting of the etch mask, but argues that “Hashimoto was not concerned with the overall width of the top of the hole—and consequently did not accurately illustrate the etch effects in the upper layers.” *Id.* at 48, 51 (citing *Nystrom*). Petitioner responds that it is not relying on Hashimoto’s figures to show precise proportions or particular sizes, but

instead to show that no undercutting was present. Pet. Reply 11–12 (citing *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972)).

We determine that Petitioner’s reliance on Hashimoto’s drawings to show straight sidewalls is not inconsistent with *Nystrom*. There, the Federal Circuit reversed a judgment of invalidity that was based on a computer-generated model of structures illustrated in a prior art patent figure and computations performed on that model to determine a ratio for comparison with a numerical limitation of the claim. *Nystrom*, 424 F.3d at 1148. The Court admonished that “patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Id.*, 424 F.3d at 1149 (quoting *Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000)). The *Nystrom* Court explained: “[a]bsent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value.” *Id.* (quoting *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977)).

In *Hockerson-Halberstadt*, the Court found “unavailing” the patentee’s argument against prosecution history disavowal, where the argument “hinge[d] on an inference drawn from certain [patent] figures about the quantitative relationship between the respective widths” of two structures shown in the figures. *Id.*, 222 F.3d at 956. In *Wright*, the Court was unpersuaded by the USPTO’s argument that comparison of the relative dimensions of appellant’s and a prior art patent’s drawings showed that the prior art had a length “of roughly 1/2 to 1 inch.” *Wright*, 569 F.2d at 1127.

In contrast to *Nystrom*, *Hockerson-Halberstadt*, and *Wright*, Petitioner’s “straight sidewalls” argument does not rely on Hashimoto’s

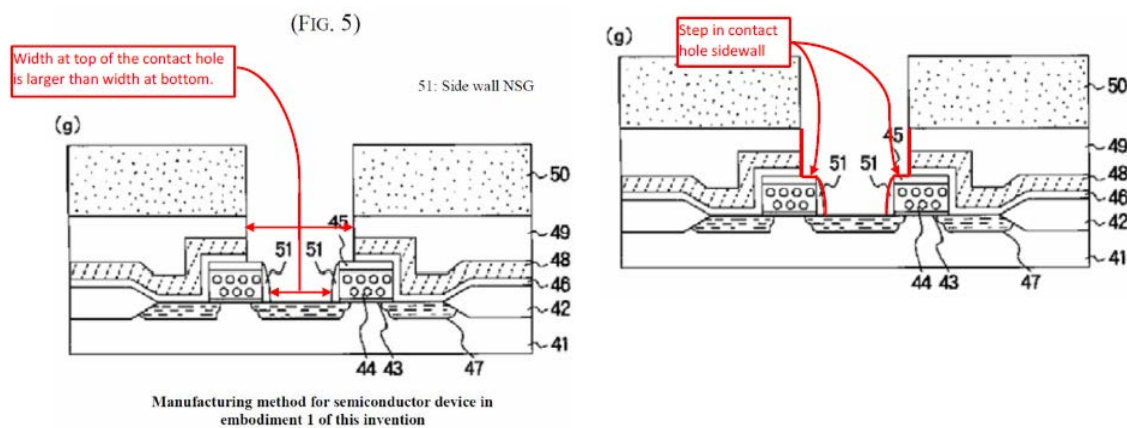
drawings to show precise proportions, particular sizes, quantitative values, a quantitative relationship, or relative dimensions of the contact hole. Instead, Petitioner relies on Hashimoto's drawings to show a contact hole with straight sidewalls.

We find the *Mraz* decision cited by Petitioner (Pet. Reply 12) to be more on point than any of *Nystrom*, *Hockerson-Halberstadt*, or *Wright*. In *Mraz*, the claim recited, among other things, edge rolls having a groove angle "not exceeding 15°." *Mraz*, 435 F.2d at 1070. The Court held it was not improper to rely on a prior art patent figure to show edge rolls having a groove angle within the claimed range. *Id.* at 1072–73. The Court explained that, although patent drawings are not working drawings, "things patent drawings show clearly are not to be *disregarded*." *Id.* at 1072. The Court cited precedent in which "the teachings of patent drawings, even as to features unexplained by the specification, proved dispositive." *Id.* (citing *In re Bager*, 47 F.2d 951, 952–953 (CCPA 1931)).

We find that Petitioner's reliance on Hashimoto's figures to show a contact hole with straight sidewalls is proper under the holding of *Mraz*. Like the patent figures relied upon in *Mraz*, Hashimoto's figures show the contact holes "with great particularity." *Id.* at 1072. Hashimoto Figures 4(d) through 4(f) and 5(g) show a step-by-step process for forming a contact hole, illustrating in detail which layers and parts of layers are removed during each step. Hashimoto Figure 4(e), for example, shows the result of a first etch. The lines are drawn to show that layer 49 and a portion of layer 48 are removed during a first etch. Notably, both parties' experts rely on Hashimoto's figures to show features, such as etching of vertical surfaces of the silicon nitride film, that are not expressly disclosed in the text of

Hashimoto. *See, e.g.*, Ex. 1003 ¶ 145; Ex. 2012 ¶ 93 (both presenting annotations of Hashimoto Fig. 4(e)). Taken together, these circumstances support our view that a POSA would have understood Hashimoto’s figures as disclosing a contact hole with straight sidewalls, notwithstanding that straight sidewalls are not discussed in the text of Hashimoto. If anything, this case favors reliance on the patent drawings more strongly than *Mraz* because the claim limitation “straight sidewalls” is qualitative, not quantitative, whereas the claim at issue in *Mraz* recited a numerical limit on the size of an angle. *See Mraz*, 435 F.2d at 1070 (“not exceeding 15°”).

Patent Owner argues that Hashimoto neither discloses nor suggests a contact hole having straight sidewalls because the width of the top of the contact hole is larger than the width at the bottom of the contact hole and because there is a “step” in the contact hole sidewall. PO Resp. 59–60. Patent Owner illustrates its argument with the following annotations of Hashimoto Figure 5(g):



Id. Hashimoto Figure 5(g) illustrates a step in a process for forming a contact hole. Ex. 1005 ¶ 9. We find Patent Owner’s arguments regarding Hashimoto Figure 5(g) are inconsistent with its arguments regarding Figure 1E of the ’188 patent. More specifically, Patent Owner argues that

Figure 1E of the '188 patent shows contact holes with straight, vertical sidewalls, illustrating its argument with the following annotation of Figure 1E:

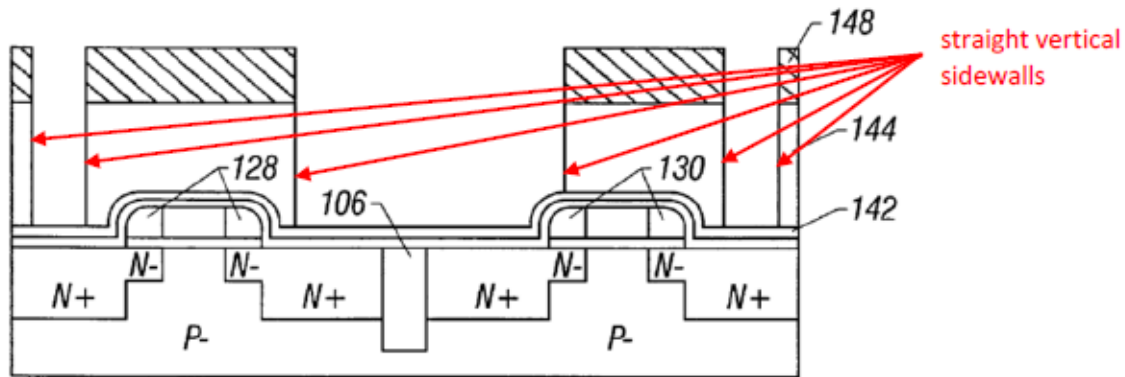


FIG. 1E

Figure 1E illustrates a step in a process for forming a contact hole. Ex. 1001, 4:17–20. Patent Owner contends that each of the contact holes shown in Figure 1E of the '188 patent has “straight vertical sidewalls,” notwithstanding that the contact hole in the middle of the figure has a configuration similar to that shown in Hashimoto Figure 1(g), with a “step” at the bottom of the contact hole and a width at the top of the contact hole that is larger than a width at the bottom of the contact hole. In view of this similarity, we find that Hashimoto Figure 1(g) shows a contact hole with straight sidewalls in the same way that Patent Owner asserts Figure 1E of the '188 patent shows a contact hole with straight sidewalls.

Our finding is reinforced by the claim language, as argued by Petitioner. Pet. Reply 30–31. When the limitations of claims 1 and 3 are read as a whole, the contact hole that is required to have “straight sidewalls” is a contact hole “in the interlevel dielectric layer.” Ex. 1001, 9:20–22, 9:26–28; *see also id.* at 11:32–34 (claim 21: “the first, second and third

holes in combination provide a contact hole with straight sidewalls in the interlevel dielectric layer”). As argued by Petitioner, we find that Hashimoto Figure 5(g) shows a contact hole in the interlevel dielectric layer (layers 46, 48 and 49) having straight sidewalls. Pet. Reply 30–31; Ex. 1022 ¶ 40; *see also* Ex. 1003 ¶ 79 (the interlevel dielectric in Hashimoto consists of layers 46, 48, and 49). The “straight sidewalls” limitation of the claims is met, even if Hashimoto discloses an additional contact hole portion that extends below the interlevel dielectric layer and does not have straight sidewalls.

Moreover, even if the “straight sidewalls” limitation is not expressly disclosed by Hashimoto, Petitioner has established that it would have been obvious in view of Hashimoto to fabricate a contact hole with straight sidewalls. It is undisputed that a contact hole with straight sidewalls is typically produced with highly anisotropic etch steps. Pet. 74 (“A POSA would have known that anisotropic etches will produce a contact hole with straight sidewalls.”); PO Resp. 53 (“straight sidewalls are typically formed using highly anisotropic etch steps”). For the reasons discussed in section II.E.1.a. above, Petitioner has shown by preponderance of the evidence that a POSA would have been motivated to use anisotropic etches for each of Hashimoto’s etch steps. This same evidence establishes that a POSA would have been motivated to use highly anisotropic etches to produce a contact hole with straight sidewalls.

Accordingly, after considering the parties’ arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claim 3 of the ’188 patent is unpatentable as obvious in view of Hashimoto.

2. *Claim 11*

Claim 11 is similar to claim 1, except that claim 11 recites additional limitations relating to a gate insulator, steps for forming the first, second, and third dielectric layers, and gate thickness. Ex. 1001, 9:55, 9:63–67. Claim 11 also recites that each of the first, second, and third etches is “anisotropic.” *Id.* at 10:2, 10:9, 10:16.

For the “anisotropic etch” limitations, both parties rely on the same arguments for claim 11 as are presented for claim 3. Pet. 47–55; PO Resp. 61. For the reasons discussed in section II.E.1.a. above, we determine Petitioner has shown by a preponderance of the evidence that a POSA would have been motivated to use anisotropic etches for each of Hashimoto’s etch steps.

Petitioner directs us to substantial evidence that the remaining limitations of claim 11 are disclosed by Hashimoto. Pet. 29–47. Patent Owner does not contest that evidence. PO Resp. 61. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that these limitations of claim 11 are disclosed by Hashimoto.

Accordingly, after considering the parties’ arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claim 11 of the ’188 patent is unpatentable as obvious in view of Hashimoto.

3. *Claim 15*

Claim 15 depends from claim 11 and recites “the interlevel dielectric layer consists of the first, second and third dielectric layers.” Ex. 1001, 10:30–32.

Relying on Hashimoto Figure 4(d), Petitioner contends that Hashimoto discloses an interlevel dielectric layer consisting of oxide layer 46, silicon nitride layer 48, and oxide layer 49. Pet. 35, 59.

Patent Owner argues that the “consisting of” language of claim 15 is not met because Hashimoto discloses an interlevel dielectric layer having four separate layers, including gate oxide film 43. PO Resp. 62–63.

In the Institution Decision, we made the following preliminary findings (Dec. 23): According to the ’188 patent, an interlevel dielectric layer is between the polysilicon gates of a transistor and a metal-1 pattern. Ex. 1001, 5:50–53, 7:20–22, 8:37–42, Fig. 1D (showing interlevel dielectric layer 146 between polysilicon gates 114 and 116 and a metal-1 pattern to be subsequently formed). In contrast, Hashimoto’s gate oxide film 43 is beneath polysilicon gate 44, not between the gate and a metal-1 pattern. Ex. 1005 ¶ 7, Fig. 1(a). As Petitioner argues (Pet. Reply 32), these unchallenged findings from the Institution Decision support that Hashimoto’s gate oxide film 43 is not part of an interlevel dielectric layer.

Patent Owner’s argument relies on Dr. Bottoms’ testimony. PO Resp. 63 (citing Ex. 2012 ¶ 82). Tellingly, however, Dr. Bottoms does not testify that Hashimoto’s gate oxide film 43 is part of an interlevel dielectric layer. Instead, Dr. Bottoms testifies that a POSA “would understand that, in the regions between the word lines, the layer 46 illustrated in FIG. 1(b) includes both the gate oxide film 43 and the NSG.” Ex. 2012 ¶ 82. We agree with Petitioner that Patent Owner’s argument is inconsistent with Hashimoto Figures 1(b), 1(c), 4(d), 4(e), and 4(f), all of which depict NSG layer 46 as a separate structure from oxide layer 43 beneath the gate. Ex. 1005; Pet. Reply 32 (citing Ex. 1022 ¶ 42). Dr. Bottoms’ testimony is

persuasively contradicted by the cited testimony of Dr. Fair that a POSA “would have understood that thermal oxide layer 43 is not part of NSG layer 46.” Ex. 1022 ¶ 42. Dr. Fair explains that “[t]o maintain process control, any remaining oxide 43 between the gates is removed prior to the deposition of layer 46, so that a controlled thickness of NSG exists during the third etch in Figure 5(g).” *Id.* In contrast to Dr. Fair’s testimony, Dr. Bottoms provides no technical explanation for his opinion that layer 46 includes both gate oxide film 43 and NSG. Ex. 2012 ¶ 82. In view of Dr. Fair’s credible technical explanation (Ex. 1022 ¶ 42), we give more weight to Dr. Fair’s testimony than Dr. Bottoms’ testimony (Ex. 2012 ¶ 82) regarding the composition of Hashimoto’s interlevel dielectric layer.

Accordingly, after considering the parties’ arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claim 15 of the ’188 patent is unpatentable as obvious in view of Hashimoto.

4. *Claims 12, 13, 18, and 19*

Claims 12, 13, 18, and 19 each depend from claim 11. Claim 12 recites “the second anisotropic etch is highly selective of the source/drain contact with respect to the third dielectric layer.” Ex. 1001, 10:23–25. Claim 13 recites “the source/drain contact is the source/drain region.” *Id.* at 10:26–27. Claim 18 recites “the gate is polysilicon and the etch mask is photoresist.” *Id.* at 10:42–43. Claim 19 recites “forming a conductive plug in the contact hole that contacts the source/drain contact.” *Id.* at 10:44–46.

Petitioner directs us to substantial evidence that Hashimoto discloses the features recited in dependent claims 12, 13, 18, and 19. Pet. 55–57, 59–60. Patent Owner does not contest that evidence and presents no argument

regarding dependent claims 12, 13, 18, and 19 separate from its arguments regarding independent claim 11. *See* PO Resp. 61. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that the limitations of claims 12, 13, 18, and 19 are disclosed by Hashimoto.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claims 12, 13, 18, and 19 of the '188 patent are unpatentable as obvious in view of Hashimoto.

5. *Claim 20*

Claim 20 depends indirectly from claim 11 and recites "forming a metal-1 pattern on the first dielectric layer that contacts the conductive plug." Ex. 1001, 10:47–49.

Petitioner directs us to substantial evidence that the subject matter of claim 20 would have been obvious in view of Hashimoto. Pet. 60–61. In the alternative, Petitioner directs us to substantial evidence that the subject matter of claim 20 is disclosed by Sung and would have been obvious in view of Hashimoto and Sung. *Id.* at 61–64. Regarding a motivation to combine Hashimoto and Sung, Petitioner directs us to substantial evidence that a POSA would have known that the formation of higher-level interconnects, as taught by Sung, was necessary to complete a DRAM device, as disclosed by Hashimoto. Pet. 63–64.

Patent Owner does not contest that evidence and presents no argument regarding dependent claim 20 separate from its arguments regarding independent claim 11. *See* PO Resp. 64.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a

preponderance of the evidence that claim 20 of the '188 patent is unpatentable as obvious in view of Hashimoto or, alternatively, in view of Hashimoto and Sung.

F. Kawai-Based Grounds

Petitioner contends that claims 7, 16, 17, 21–23, and 25–27 are unpatentable as obvious in view of Hashimoto and Kawai and that claims 28 and 29 are unpatentable as obvious in view of Hashimoto, Kawai, and Sung. Pet. 65–82. Claim 7 has been disclaimed. Ex. 2013. We address the remaining claims below.

1. Claims 16, 21, and 25

Independent claim 21 and dependent claims 16 and 25 each recite that “the first and third dielectric layers are the same material.” Ex. 1001, 10:33–34, 11:2–3, 12:5–6.

Petitioner contends that Hashimoto teaches or suggests all limitations of claim 21, except for “the first and third dielectric layers are the same material.” Pet. 65–74. Petitioner contends that this limitation would have been obvious in view of Hashimoto, asserting that a “POSA would have known that the use of the same material (e.g., NSG) for the first and third dielectric layers was a simple design choice and would simplify the manufacturing process by using the same etch conditions for etching the first and third dielectric layers.” *Id.* at 68–69 (citing Ex. 1003 ¶ 245). In addition, Petitioner contends that Kawai teaches the same material and the same etch conditions for the first and third dielectric layers. *Id.* at 69–70 (citing Ex. 1007 ¶¶ 64, 67, 68, 70, 76). Petitioner asserts that a “POSA would have been motivated to follow the semiconductor manufacturing process of Hashimoto but use Kawai’s teaching of forming first and third

dielectric layers of the same material” in order “to simplify the manufacturing process of Hashimoto and reduce the number of different deposition and etching conditions.” *Id.* at 71 (citing Ex. 1003 ¶¶ 250, 251). For claims 16 and 25, Petitioner relies on its analysis of claim 21. *Id.* at 74–75.

Patent Owner argues that Petitioner fails to establish obviousness of claims 16, 21, and 25 based on either Hashimoto alone or Hashimoto in view of Kawai. PO Supp. Resp. 9–15. According to Patent Owner, Hashimoto’s BPSG material has advantages, and replacing it with NSG, as proposed by Petitioner, would not simplify the manufacturing process. *Id.* at 10–12. Patent Owner contends that Kawai does not teach forming the first and third layers of the same material and does not disclose using the same etch conditions for these layers. *Id.* at 13–15.

We are not persuaded that Petitioner’s proposed modification of Hashimoto would simplify Hashimoto’s manufacturing process, for at least two reasons.

First, Patent Owner presents uncontroverted testimony that a POSA would have recognized that, even if the first and third dielectric layers are the same material, the etch conditions for etching these layers would not necessarily be the same. PO Supp. Resp. 12 (citing Ex. 2020 ¶ 26). As Dr. Bottoms explains, the etch conditions depend not only on the material being etched, but also on the surrounding material that is not supposed to be etched. Ex. 2020 ¶ 26. For example, as Hashimoto teaches, the first etch needs to be selective of the first dielectric layer (silicon oxide-based film) relative to the second dielectric layer (silicon nitride etch stopper), and the

third etch needs to be selective of the third dielectric layer (another silicon-oxide based film) relative to the silicon substrate. Ex. 1005 ¶ 6.

Although Petitioner contends that Kawai teaches “the same etch conditions” for the first and third dielectric layers (Pet. 69), Patent Owner shows that Kawai actually discloses the same *ranges* of conditions for these etch steps. PO Supp. Resp. 14 (citing Ex. 1007 ¶¶ 70, 76). Patent Owner presents uncontroverted testimony that a POSA would recognize that changes of conditions within Kawai’s disclosed ranges “would result in significant changes in both etch rates and selectivity.” Ex. 2020 ¶ 30. Petitioner does not address the possibility of selecting different conditions within Kawai’s disclosed ranges. Patent Owner shows that selectivity considerations would have been a reason not to use the same etch conditions for the first and third etch steps. PO Supp. Resp. 12 (citing Ex. 1001, 6:1–4, 6:25–28, 6:35–38; Ex. 2020 ¶ 26). Like the ’188 patent, Hashimoto discloses different selectivity for the first and third etches. Ex. 1005 ¶ 6.

Second, we agree with Patent Owner (PO Supp. Resp. 10–15) Petitioner has not shown persuasively that its proposed modification of Hashimoto would have been a simplification of the manufacturing process, when planarization steps are taken into account. It is undisputed that planarization is an essential step in forming an interlevel dielectric layer. Pet. 78; Ex. 1002,¹⁰ 98; Ex. 1003 ¶ 297; Ex. 1008, 6; Ex. 2020 ¶ 25. Hashimoto teaches a first dielectric layer made of boron-doped silicate glass (BPSG), but Petitioner proposes substituting non-doped silicate glass (NSG) for BPSG. Pet. 68. Patent Owner shows that one advantage of using doped

¹⁰ Stanley Wolf, *Silicon Processing for the VLSI Era, Vol. 2: Process Integration* (1990), Ex. 1002, 77–128 (excerpts) (“Wolf”).

silicon oxide, such as BPSG, as an interlevel dielectric material is that it has a lower glass transition temperature as compared with undoped silicon oxide, such as NSG. The lower glass transition temperature allows BPSG to be reflowed at a relatively low temperature, which assists in planarization. PO Supp. Resp. 10 (citing Ex. 2005,¹¹ 3; Ex. 2020 ¶ 23). Dr. Fair testifies that reflowing alone is not sufficient to planarize BPSG. Ex. 1022 ¶ 45. But neither Petitioner nor Dr. Fair explains how planarization would be conducted, if NSG were substituted for BPSG in Hashimoto's process.

Patent Owner, on the other hand, presents undisputed testimony that when a reflowable material, such as BPSG, is not used as the upper layer, it is necessary to use additional planarizing steps, such as those disclosed in Kawai. Ex. 2020 ¶¶ 22, 29. As Dr. Bottoms explains, Kawai's planarizing technique includes first applying a TEOS film 13A, then applying a layer of liquid SOG 13B that flows to form a flat surface, and lastly etching the layers to remove the SOG layer 13B and the discontinuities in the TEOS film 13A. *Id.*; Ex. 1007 ¶¶ 67, 68, Figs. 7, 8. Although Petitioner relies on Kawai as evidence that Hashimoto's manufacturing process would be simplified by substituting NSG for BPSG (Pet. 71), neither Petitioner nor Dr. Fair compares Kawai's planarization steps with the steps needed to planarize BPSG.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are not persuaded Petitioner has established by

¹¹ *Handbook of Multilevel Metallization For Integrated Circuits: Materials, Technology, and Applications* (Syd R. Wilson et al. eds., 1993), Ex. 2005 (excerpts) ("Wilson"). We cite to Wilson (Ex. 2005) using the page numbers added by Patent Owner.

a preponderance of the evidence that claims 16, 21, and 25 of the '188 patent are unpatentable as obvious in view of Hashimoto alone or in view of Hashimoto and Kawai.

2. *Claims 17, 22, 23, 26, and 27*

Petitioner contends that claims 17, 22, 23, 27, and 27 are unpatentable as obvious in view of Hashimoto and Kawai. Pet. 75–77. Claim 17 depends from claim 16. Claims 22 and 23 depend from claim 21. Claims 26 and 27 depend, directly or indirectly, from claim 25.

The deficiencies in Petitioner's arguments and evidence regarding claims 16, 21, and 25, as discussed above, are not remedied by Petitioner's evidence and arguments regarding claims dependent 17, 22, 23, 26, and 27. *See* Pet. 75–77.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are not persuaded Petitioner has established by a preponderance of the evidence that claims 17, 22, 23, 26, and 27 of the '188 patent are unpatentable as obvious in view of Hashimoto alone or in view of Hashimoto and Kawai.

3. *Claims 28 and 29*

Petitioner contends that claims 28 and 29 are unpatentable as obvious in view of Hashimoto, Kawai, and Sung. Pet. 77–82. Claims 28 and 29 each depend from claim 21.

The deficiencies in Petitioner's arguments and evidence regarding claim 21, as discussed above, are not remedied by Petitioner's arguments and evidence regarding dependent claims 28 and 29 and Sung. *See* Pet. 77–82.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are not persuaded Petitioner has established by a preponderance of the evidence that claims 28 and 29 of the '188 patent are unpatentable as obvious in view of Hashimoto, Kawai, and Sung.

G. Section 325(d)

Patent Owner contends that we should vacate the Institution Decision and terminate the review pursuant to 35 U.S.C. § 325(d), arguing that Hashimoto is similar to Ogawa, a prior art reference that was cited during prosecution. PO Resp. 42–43. Petitioner disagrees. Pet. Reply 6–7.

Under section 325(d), we have discretion to deny a petition that presents the same or substantially the same prior art or arguments as previously presented to the Office. 35 U.S.C. § 325(d). After considering the parties' arguments, we are persuaded there are substantial differences between Ogawa and Patent Owner's arguments regarding Ogawa during prosecution, on the one hand, and Hashimoto and Patent Owner's arguments regarding Hashimoto during this review, on the other hand.

Patent Owner concedes that, in contrast to Hashimoto, Ogawa requires isotropic etching. PO Resp. 12, 43. As Patent Owner explains: "Ogawa discloses a series of embodiments, each of which requires the use of 'isotropic dry etching.'" *Id.* at 12 (citing Ex. 3001, 8:67–9:3, 12:11–26, 12:34–44, 13:56–68). Patent Owner further concedes that, during prosecution, Applicants distinguished Ogawa based on the requirement for isotropic etching. *Id.* at 15. As Patent Owner explains, "applicants emphasized that 'at least one step in each embodiment requires an isotropic etch to undercut an overlying layer.'" *Id.* (quoting Ex. 1002, 61).

Patent Owner also concedes that, in contrast to Ogawa, “Hashimoto fails to use the word ‘isotropic’ in describing its etching steps.” *Id.* at 43. Patent Owner distinguishes Hashimoto by arguing that its etching steps would not necessarily be understood as anisotropic. *Id.* at 36. That argument is substantially different from the argument presented during prosecution, where Applicants distinguished Ogawa by arguing that at least one of its etching steps was required to be isotropic. *Id.* at 15; Ex. 1002, 61.

Accordingly, we decline to exercise our discretion to deny review under section 325(d).

III. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 3, 11–13, 15, and 18–20 of the ’188 patent are unpatentable. Petitioner has not shown by a preponderance of the evidence that claims 16, 17, 21–23, and 25–29 of the ’188 patent are unpatentable.

IV. ORDER

Accordingly, in consideration of the foregoing, it is hereby:

ORDERED that, based on a preponderance of the evidence, claims 3, 11–13, 15, and 18–20 of the ’188 patent are unpatentable;

FURTHER ORDERED that, based on a preponderance of the evidence, claims 16, 17, 21–23, and 25–29 of the ’188 patent are not shown to be unpatentable; and

FURTHER ORDERED that Patent Owner’s unopposed motion to excuse the late filing of Exhibits 2012 and 2013 is *granted*; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01560
Patent 5,912,188

PETITIONER:

Jeremy Jason Lang
Robert Stephen Magee
WEIL, GOTSHAL & MANGES LLP
jason.lang@weil.com
robert.magee@weil.com

PATENT OWNER:

Timothy P. Maloney
Nicholas T. Peters
David Gosse
FITCH, EVEN, TABIN & FLANNERY LLP
tim@fitcheven.com
ntpete@fitcheven.com
dgosse@fitcheven.com