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Paper No. 34
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01561
Patent 5,912,188

Before GRACE KARAFFA OBERMANN, KRISTINA M. KALAN, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Micron Technology, Inc. ("Petitioner") challenges the patentability of claims 1–5, 7–13, 15–23, and 25–29 of U.S. Patent No. 5,912,188. Ex. 1001 ("the '188 patent"), assigned to Lone Star Silicon Innovations, LLC ("Patent Owner").[1] Claims 1, 2, 4, 5, and 7–10 have been disclaimed. Ex. 2011.

We have jurisdiction under 35 U.S.C. § 6. This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 3, 11–13, 15–23, and 25–29 of the '188 patent are unpatentable.

I. BACKGROUND

A. Procedural History

Petitioner filed a Petition seeking *inter partes* review of claims 1–5, 7–13, 15–23, and 25–29 (the "challenged claims") of the '188 patent. Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 6 ("Prelim. Resp."). We instituted *inter partes* review of all challenged claims. Paper 8 ("Institution Decision" or "Dec.").

Patent Owner filed a Response. Paper 13 ("PO Resp.").[2] Concurrent with the Response, Patent Owner filed a disclaimer of claims 1, 2, 4, 5, and 7–10 of the '188 patent. Ex. 2011.

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[1] Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 31, 1.

[2] Patent Owner's Response and exhibits accompanying the response were filed less than one hour past the deadline. Good cause having been shown, Patent Owner's unopposed motion to excuse the late filing of Patent Owner's Response and exhibits (Paper 14) is granted.

Petitioner filed a Reply. Paper 20 ("Pet. Reply"). With the Board's prior authorization (Ex. 2016), Patent Owner filed a Sur-Reply addressing limited issues. Paper 24 ("PO Sur-Reply").

With the Petition, Petitioner filed a declaration of Richard Fair, Ph.D. Ex. 1003. Patent Owner cross-examined Dr. Fair and filed a transcript of his deposition testimony as Exhibit 2005. With the Reply, Petitioner filed a second declaration of Dr. Fair. Ex. 1018.

With the Preliminary Response, Patent Owner filed a declaration of Wilmer R. Bottoms, Ph.D. Ex. 2001. With the Patent Owner Response, Patent Owner filed a second declaration of Dr. Bottoms. Ex. 2010. With its Sur-Reply, Patent Owner filed a third declaration of Dr. Bottoms. Ex. 2017. Petitioner cross-examined Dr. Bottoms twice and filed transcripts of his deposition testimony as Exhibits 1020 and 1022.

Pursuant to the parties' requests, oral argument in Case IPR2017-01560 and Case IPR2017-01561 was consolidated into a single argument, which was held September 18, 2018. A transcript of the oral argument was entered in the record. Paper 33 ("Tr.").

B. Related Matters

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner states that the '188 patent has been asserted in the following pending appellate and district court proceedings: *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, Appeal No. 2018-1578 (Fed. Cir., filed Feb. 15, 2018) and *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (N.D. Cal., filed Mar. 16, 2018). Paper 31, 2–3.

Pursuant to 37 C.F.R § 42.8(b)(2), the parties identify the following *inter partes* review proceeding involving the '188 patent: *Micron*

Technology, Inc. v. Lone Star Silicon Innovations, LLC, Case IPR2017-01560. Pet. 3; Paper 31, 1.

C. The '188 Patent (Ex. 1001)

The '188 patent, titled "Method of forming a contact hole in an interlevel dielectric layer using dual etch stops," was issued June 15, 1999 from Application No. 08/905,686, filed August 4, 1997. Ex. 1001, [21], [22], [45], [54].

The '188 patent relates to integrated circuit manufacturing, and more specifically, to a method of forming a contact hole in an interlevel dielectric layer using dual etch stops. *Id.* at [54], [57], 1:7–10.

The '188 patent addresses the problem of overetching and gouging of underlying materials when forming contact holes. *Id.* at 2:29–50, 2:65–67, 3:2–4. According to the '188 patent, one known solution is an interlevel dielectric layer with a thick silicon dioxide layer on a thin silicon nitride layer and a two-step etching process, whereby the first etch is highly selective of silicon dioxide with respect to silicon nitride. *Id.* at 2:51–56. The '188 patent states that this approach has a drawback in that the second etch is highly selective of both silicon nitride and silicon and may cause substantial damage to an underlying silicon surface. *Id.* at 2:58–63.

The solution proposed by the '188 patent is an interlevel dielectric with first, second, and third dielectric layers and a three-step etching process, whereby the first dielectric layer is etched using the second dielectric layer as an etch stop, and the second dielectric layer is etched using the third dielectric layer as an etch stop. *Id.* at 3:4–10.

Figures 1A–1J of the ’188 patent illustrate process steps for forming a contact hole in an interlevel dielectric. *Id*. at 4:17–20. Figures 1D through 1G are reproduced below:

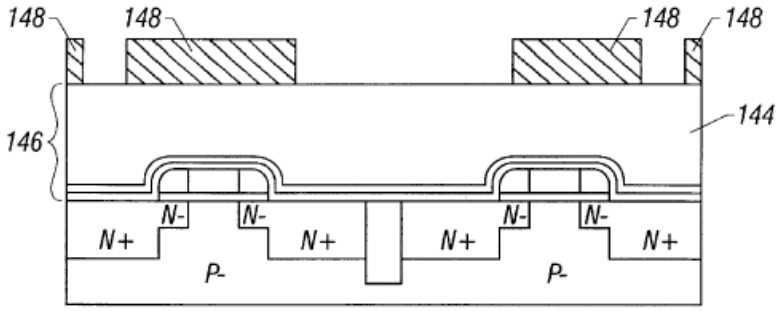


FIG. 1D

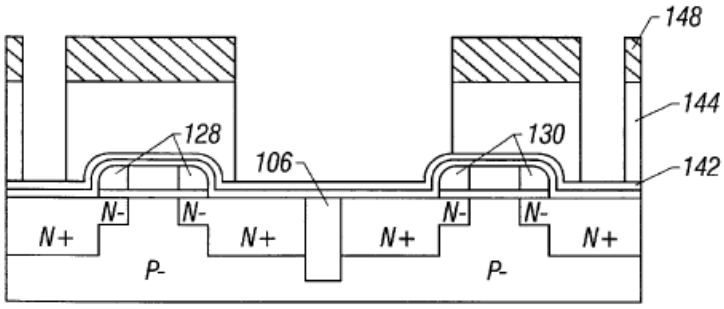


FIG. 1E

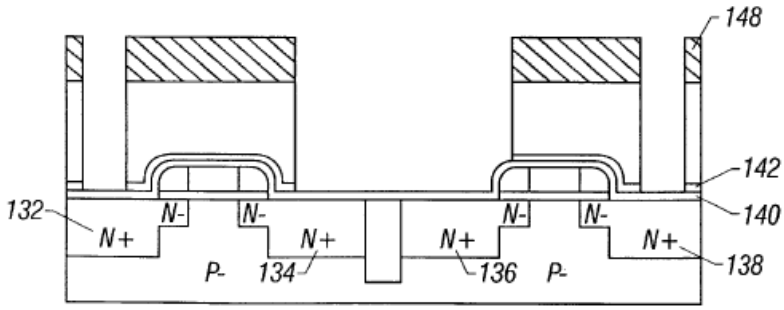


FIG. 1F

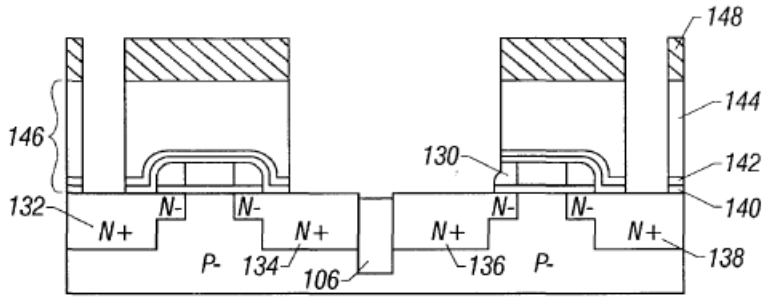


FIG. 1G

Figures 1D through 1G of the ’188 patent illustrate process steps for forming a contact hole in an interlevel dielectric. Ex. 1001, 4:17–20. Figure 1D shows interlevel dielectric layer 146, including silicon oxide layer 140, silicon nitride layer 142, and silicon oxide layer 144. *Id.* at 5:31–54. The interlevel dielectric layer is formed on a silicon substrate having active regions separated by trench oxide 106. *Id.* at 4:29–38, 5:31–54. Each active region includes a gate oxide layer and a gate, which are formed on the substrate, and source and drain regions, which are formed in the substrate. *Id.* at 4:44–5:30. Patterned photoresist layer 148 is formed on silicon oxide layer 144 to define contact holes. *Id.* at 5:59–67.

Figure 1E shows the result of a first etching step. According to the ’188 patent, “a long anisotropic reactive ion etch is applied that is highly selective of silicon dioxide with respect to silicon nitride using photoresist layer 148 as an etch mask and using nitride layer 142 as an etch stop” to form holes in oxide layer 144 that extend to nitride layer 142. *Id.* at 6:1–5.

Figure 1F shows the result of a second etching step. According to the ’188 patent, “the etch chemistry is changed and a brief anisotropic reactive ion etch is applied that is highly selective of silicon nitride with respect to silicon dioxide using photoresist layer 148 as an etch mask and

using oxide layer 140 as an etch stop" to form holes in nitride layer 142 that extend to oxide layer 140. *Id.* at 6:14–19.

Figure 1G shows the result of a third etching step. According to the '188 patent, "the etch chemistry is changed again and a brief anisotropic reactive ion etch is applied that is highly selective of silicon dioxide with respect to silicon nitride using photoresist layer 148 as an etch mask." *Id.* at 6:25–28.

After completion of the etching steps, the photoresist layer is stripped, conductive plugs are formed in the contact holes, and a metal-1 pattern is formed in contact with the conductive plugs. *Id.* at 6:48–7:19, Figs. 1H–1J.

D. Illustrative Claim

The Petition challenges claims 1–5, 7–13, 15–23, and 25–29 of the '188 patent, of which claims 1, 11, and 21 are independent. Ex. 1001, 8:57–12:35. Claim 1, which has been disclaimed, is nevertheless illustrative of the challenged claims and is reproduced below:

> 1. A method of forming a contact hole in an interlevel dielectric layer using dual etch stops, comprising:
>
> providing a semiconductor substrate;
>
> forming a gate over the substrate,
>
> forming a source/drain region in the substrate;
>
> providing a source/drain contact electrically coupled to the source/drain region;
>
> forming an interlevel dielectric layer that includes first, second and third dielectric layers over the source/drain contact;
>
> forming an etch mask over the interlevel dielectric layer;
>
> applying a first etch which is highly selective of the first dielectric layer with respect to the second dielectric layer through an opening in the etch mask using the second dielectric layer as an etch stop, thereby forming a first hole in the first dielectric layer that extends to the second dielectric layer without extending to the third dielectric layer;

> applying a second etch which is highly selective of the second dielectric layer with respect to the third dielectric layer through the opening in the etch mask using the third dielectric layer as an etch stop, thereby forming a second hole in the second dielectric layer that extends to the third dielectric layer without extending to the source/drain contact; and
>
> applying a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact through the opening in the etch mask, thereby forming a third hole in the third dielectric layer that extends to the source/drain contact, wherein the first, second and third holes in combination provide a contact hole in the interlevel dielectric layer.

Ex. 1001, 8:58–9:22.

E. Asserted Grounds of Unpatentability

The Petition challenges claims 1–5, 7–13, 15–23, and 25–29 of the '188 patent under 35 U.S.C. § 103(a). Claims 1, 2, 4, 5, and 7–10 have been disclaimed. Ex. 2011. Taking into account the disclaimer, the asserted grounds of unpatentability that remain in this decision are as follows:

Reference(s)	Claim(s)
Kawai[3]	3, 8, 11–13, 15–19, 21–23, and 25–27
Kawai and Sung[4]	20, 28, and 29

Pet. 4.

[3] JP H8-46173, published February 16, 1996, including original Janapese application and certified English translation, Ex. 1005 ("Kawai").

[4] US 5,550,078, filed June 28, 1995 and issued August 27, 1996, Ex. 1006 ("Sung").

II. ANALYSIS

A. Claim Construction

The ’188 patent expired on August 4, 2017. PO Resp. 17 n.1. For expired patents, we apply the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (“the Board’s review of the claims of an expired patent is similar to that of a district court’s review”); *see also Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed. App’x 1019, 1024 (Fed. Cir. 2016) (holding that in an *inter partes* review, “[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]”).

Under the *Phillips* standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

In the Institution Decision, we provided express constructions for the terms, “highly selective” and “anisotropic etch.” Dec. 9–15. We construed “highly selective” to mean “highly selective of X with respect to Y,” to mean “having an etch rate of X far greater than the etch rate of Y.” Dec. 11. We construed “anisotropic etch” as “an etch that is directional such that horizontal surfaces are etched at a higher rate than vertical surfaces and straight, nearly vertical, sidewalls without undercutting of the etch mask are produced.” Dec. 15.

At this stage, the parties agree that the term "highly selective" does not need to be construed. PO Resp. 20; Pet. Reply 2. Regarding the term "anisotropic etch," the parties propose two modifications of our preliminary construction, one of which is agreed upon and the other of which is disputed. The parties agree that the construction for "anisotropic etch" should not include a requirement for straight, nearly vertical, sidewalls without undercutting of the etch mask. PO Resp. 25–26, 29–34; Pet. Reply 5. The parties disagree as to whether an "anisotropic etch" requires a vertical etch rate that is *substantially* higher than the lateral etch rate, as proposed by Patent Owner. PO Resp. 26–29, 34 (emphasis added); Pet. Reply 5–7.

Each party concedes, however, that the construction of "anisotropic etch" is not critical to its position. Tr. 4:4–9 (Petitioner); *id.* at 24:22–25:3 (Patent Owner). In view of the parties' concessions and the record as a whole, we determine it is not necessary to construe the terms "highly selective" and "anisotropic etch" for purposes of resolving the controversy. Although we provided preliminary constructions for "highly selective" and "anisotropic etch" in the Institution Decision, we do not reach a final determination on the constructions of these phrases, given that resolving the constructions is not necessary to this final decision. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Principles of Law

Regarding the challenged claims of the '188 patent that have not been disclaimed by Patent Owner, Petitioner bears the burden of proving

unpatentability, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish the facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In this case, neither party relies on objective evidence of nonobviousness, i.e., secondary considerations.

C. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Fair, testifies that a person of ordinary skill in the art ("POSA") would have had at least a Bachelor of Science degree in electrical engineering, chemical engineering, chemistry, physics, materials science, or a closely related field, along with at least five years of experience in semiconductor fabrication. Ex. 1003 ¶ 18. Dr. Fair further testifies that an individual with an advanced degree in one of these fields would require less experience in semiconductor fabrication. *Id.* Patent Owner's declarant, Dr. Bottoms, testifies that a POSA would have held a master's degree in

physics, electrical engineering or a related field and at least three years of experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. Ex. 2010 ¶ 30.

In our view, there is little difference between the declarants' descriptions of a POSA, and our patentability determinations would be the same regardless of which description we adopt. For purposes of our Institution Decision, we accepted the description provided by Dr. Bottoms. Dec. 15–16 (citing Ex. 2001 ¶ 30). Dr. Fair testifies that Dr. Bottoms' description of the level of ordinary skill in the art is consistent with the level proposed in his original declaration (Ex. 1003 ¶ 18), and the Board's adoption of that description does not change his opinions. Ex. 1018 ¶ 5.

Therefore, consistent with our Institution Decision, we adopt Dr. Bottoms' description of a POSA. Ex. 2010 ¶ 30. We also rely on the cited prior art references as reflecting the level of ordinary skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

After reviewing the qualifications of Dr. Fair and Dr. Bottoms, as set forth in each witness's declaration and curriculum vitae ("CV"), we find that each of these declarants is qualified to testify from the perspective of a POSA. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2010 ¶¶ 6–19. Regarding Dr. Fair, we find particularly relevant his experience as an acting president, vice president, and director at the Microelectronics Center of North Carolina ("MCNC") from 1981 to 1994, where he directed research on semiconductor processing, including photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD of thin films, metallization, and anisotropic etch processes, and conducted research on

multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, and selective tungsten deposition for via filling. Ex. 1003 ¶ 9, Ex. 1004, 3. Regarding Dr. Bottoms, we find particularly relevant his experience at Varian Associates from 1976 to 1985, including his experience as Manager of Research and Development, where he was involved in developing tools used to fabricate semiconductor devices including lithography, sputtering, ion implantation, etching, and evaporation processes. Ex. 2010 ¶¶ 9–11; Ex. 2002, 1.

Petitioner argues that we should credit Dr. Fair's testimony and reject Dr. Bottoms' testimony because "Dr. Bottoms' expertise in the field pales in comparison to Dr. Fair's." Pet. Reply 19. Petitioner bases its argument on Dr. Bottoms' response to deposition questions regarding "Miller capacitance" and "the Miller effect" and a comparison of the number of papers and conference presentations for the period 1984 to 2004, as listed on each declarant's CV. *Id.* at 19–20 (citing Ex. 1004, 3–16; Ex. 1020, 69:14–21; Ex. 2002, 6–7). Petitioner's argument does not persuade us to reject Dr. Bottoms' testimony. Dr. Bottoms' inability to recall a name (Miller) associated with a particular scientific principle does not in our view conclusively prove a lack of expertise. Furthermore, the number of papers and conference presentations listed on Dr. Bottoms' CV is not the sole or best measure of his level of expertise. The number of such items may depend on the institutional setting in which he worked, e.g., in industry rather than academia. Dr. Bottoms explains that his CV lists selected presentations and publications and omits some data for the relevant time period. Ex. 2017 ¶¶ 2–4. On this record, we find that both Dr. Fair and Dr.

Bottoms are sufficiently qualified to opine from the perspective of a POSA at the time of the invention. Ex. 1003 ¶¶ 5–12; Ex. 1004; Ex. 2002; Ex. 2012 ¶¶ 6–19.

D. Prior Art References

1. Kawai (Ex. 1005)

Kawai discloses a method of producing a semiconductor device, such as a DRAM. Ex. 1005 ¶¶ 1, 2. Petitioner relies on Kawai's Example 1, which is described in paragraphs 54–80 and illustrated in Figures 1–13. *See, e.g.*, Pet. 19–26, 28–41. Petitioner directs us to Kawai Figure 13 (Pet. 26), which is reproduced below:

(FIG. 13)

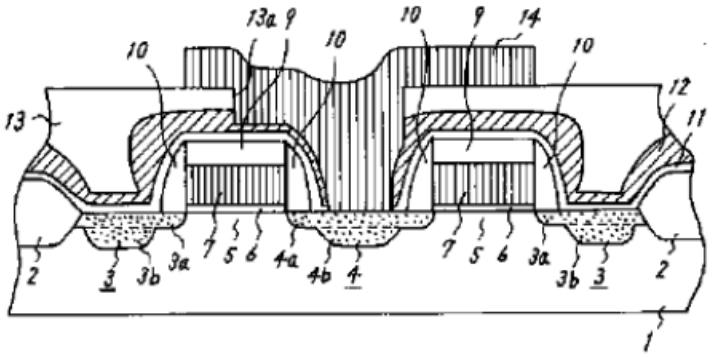


Figure 13 shows a cross-section of a semiconductor device, including semiconductor substrate 1, source/drain regions 3 and 4, gate electrode 7, gate insulating overlay silicon oxide film 9, sidewall silicon oxide film 10, first insulating layer 11 made of silicon oxide film, etching stopper layer (second insulating layer) 12 made of silicon nitride film, interlaminar insulating layer 13 made of silicon oxide film, contact hole 13a, and wiring layer 14. Ex. 1005 ¶¶ 54–59. Kawai discloses process steps for forming insulating layers 11, 12, and 13 and a contact hole resist mask. *Id.* ¶¶ 64–69,

Figs. 5–9. Kawai discloses three etching steps for forming a contact hole. *Id.* ¶¶ 70–76. In the first etching step, dry etching that is highly selective of silicon oxide relative to silicon nitride is performed using a resist mask to form contact hole 13a in interlaminar insulating layer 13. *Id.* ¶ 70, Fig. 10. In the second etching step, anisotropic etching that is highly selective of silicon nitride relative to silicon oxide is performed to form an opening 12a in the etching stopper layer 12. *Id.* ¶ 74, Fig. 11. In the third etching step, dry etching that is highly selective of silicon oxide relative to silicon nitride is performed to form an opening 11a in insulating layer 11. *Id.* ¶ 76, Fig. 12.

2. Sung (Ex. 1006)

Sung discloses a process for fabricating DRAM devices on a semiconductor substrate using a complementary metal oxide (CMOS) field effect transistor approach. Ex. 1006, 1:7–9, 2:15–17, 3:65–4:1. Sung's process includes forming a first interlevel dielectric, forming contact hole openings to source and drain regions, contact metallization, and forming a first metal structure. *Id.* at 3:25–29. With reference to Figure 18, Sung discloses depositing a first interlevel dielectric ("ILD-1") 34 of boro-phospho-silicate glass ("BPSG"). *Id.* at 7:16–19, Fig. 18. Sung discloses forming contact hole 35 in ILD-1 and filling the contact hole with TiN-tungsten to form contact stud 36. *Id.* at 7:26–32, Fig. 18. Sung discloses depositing and patterning a layer of Al-Cu to create metal-1 ("M1") structure 37. *Id.* at 7:32–36, Fig. 18.

E. Petitioner's Obviousness Grounds

Petitioner contends that claims 1–5, 7–13, 15–19, 21–23, and 25–27 are unpatentable as obvious in view of Kawai and that claims 20, 28, and 29 are unpatentable as obvious in view of Kawai in combination with Sung. Pet. 27–73. Claims 1, 2, 4, 5, and 7–10 have been disclaimed. Ex. 2011. We address the remaining claims below.

1. Claim 3

Claim 3 depends from claim 1 and recites "the first, second and third etches are anisotropic etches and the contact hole has straight sidewalls." Ex. 1001, 9:26–28. Claim 1 recites, among other limitations, "applying a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact." *Id.* at 9:16–17.

Petitioner directs us to substantial evidence that the limitations of claim 1 are disclosed or suggested by Kawai. Pet. 28–42. Patent Owner does not contest that evidence, except to argue that Kawai does not disclose or suggest the "highly selective" third etch limitation. PO Resp. 46–47, 50–52. For the remaining limitations of claim 3 that are incorporated from claim 1, we determine Petitioner has shown by a preponderance of the evidence that Kawai discloses or suggests these limitations. The remainder of our analysis focuses on the disputed limitations of claim 3, i.e., a highly selective third etch, anisotropic etches, and straight sidewalls.

a. Highly selective third etch

Regarding the third etch, Petitioner contends that an etch performed under conditions disclosed in Kawai is highly selective for silicon oxide with

respect to the silicon substrate. Pet. 40 (citing Ex. 1003 ¶ 112; Ex. 1008,[5] 1). Petitioner contends that Kawai Figure 12 shows that the third etch does not materially etch source/drain region. *Id.* at 40–41. In addition, Petitioner contends that it would have been obvious to a POSA to conduct Kawai's third etch under conditions that are highly selective for the third dielectric layer with respect to the source/drain region. *Id.* at 41–42. Petitioner asserts two motivations: (1) so that the third etch "does not materially etch the source/drain region of the substrate," and (2) "in order to open contact holes with decreasing tolerances between the MOS transistors . . . ." *Id.* (citing Ex. 1003 ¶ 116; Ex. 1008, 1).

Patent Owner argues that Kawai emphasizes protecting etching stopping layer 12 and is silent as to whether the third etch would be highly selective of first insulating layer 11 relative to the underlying source/drain region 4. PO Resp. 46–47, 50. Patent Owner argues that Petitioner's obviousness analysis is insufficient. *Id.* at 51–52.

Patent Owner has disclaimed claim 1 of the '188 patent, which recites: "a third etch which is highly selective of the third dielectric layer with respect to the source/drain contact." Ex. 1001, 9:16–17; Ex. 2011. Patent Owner refused to agree that its disclaimer of claim 1 moots the "highly selective" issue with respect to claim 3, but Patent Owner's reasoning pertains solely to motivation, not to whether the claim limitation was known in the art. Tr. 47:19–48:4. Patent Owner does not dispute Petitioner's contention that "it was "well known" to perform the claimed highly selective

[5] Siozawa et al., *SiO_2 etching in C_4F_8/O_2 Electron Cyclotron Resonance Plasma*, 35 Jpn. J. Appl. Phys. 2483–2487 (April 1996), Ex. 1008 ("Siozawa").

etch step." PO Resp. 50. We find Petitioner has established that an etch that is highly selective of a silicon oxide layer relative to an underlying silicon substrate (source/drain region) was known in the art. Pet. 40 (citing Ex. 1008, 1). Our finding is supported by Siozawa, which discloses that, in a previously reported study, "[h]igh selectivity of SiO_2 to Si or photoresist and high anisotropy could be achieved with O_2 addition to C_4F_8 plasma." Ex. 1008, 1.

Petitioner has also established, by a preponderance of the evidence, two rationales for why a POSA would have been motivated to use a third etch that is highly selective of the third dielectric layer with respect to the source/drain contact in Kawai's process.

First, relying on the undisputed testimony of Dr. Fair, Petitioner has shown that a POSA would have been motivated to use a highly selective etch for Kawai's third etch to protect the underlying source/drain region. Pet. 41 (citing Ex. 1003 ¶ 116); Pet. Reply 11–12 (citing Ex. 1018 ¶ 13). We credit Dr. Fair's testimony that a POSA would have been motivated to use a third etch that is highly selective relative to the substrate in order to prevent damage or etching of the source/drain region of the substrate. Ex. 1003 ¶ 116. We also credit the cited reply testimony, where Dr. Fair persuasively explains that a POSA "knew at the time that etching into the source/drain by even a few hundred angstroms was undesirable and would degrade the performance of the device because good metal Ohmic contact to the source/drain regions requires the metal contact to be adjacent to the highest doping regions of the source/drain, which typically occur near the

silicon surface." Ex. 1018 ¶ 13 (citing Ex. 1021,[6] 3–11). Dr. Bottoms does not dispute that a desire to protect the underlying source/drain region is a reason to use a highly selective etch.

Second, relying on Dr. Fair's testimony, Petitioner shows that a POSA would have been motivated to use a highly selective etch for Kawai's third etch in order to open contact holes with small tolerances between the MOS transistors. Pet. 42 (citing Ex. 1003 ¶ 116; Ex. 1008, 1); Pet. Reply 11–12 (citing Ex. 1018 ¶ 14). We credit Dr. Fair's testimony (Ex. 1003 ¶ 116), which is supported by Siozawa's teaching: "For SiO_2 etching, higher selectivity to the photoresist and underlying layers and anisotropy are required for obtaining high-aspect-ratio features." Ex.1008, 1. We find that Siozawa's teaching is applicable to Kawai, which discloses fine geometry features, including MOS transistors with spacing of 0.36 μm or less between adjacent gates. Ex. 1005 ¶¶ 3, 56 (Example 1). Our finding is supported by the cited testimony of Dr. Fair that "[g]iven the high density and narrow features in Kawai's device, Siozawa's teaching to use a high selectivity oxide etch would have motivated a person of ordinary skill in the art to use a highly selective third etch." Ex. 1018 ¶ 14.

We now turn to Patent Owner's arguments. According to Patent Owner, Petitioner's obviousness analysis is insufficient because Petitioner does not evaluate the effect of any change in etch chemistry on selectivity relative to Kawai's etching stopper layer 12. PO Resp. 51 (citing Ex. 2010 ¶ 109). Dr. Bottoms testifies that "any change in etch chemistry affecting

[6] W.R. Runyan and K.E. Bean, *Semiconductor Integrated Circuit Processing Technology* (1990), Ex. 1021 (excerpts) ("Runyan"). We cite Runyan (Ex. 1021) using the page numbers added by Petitioner.

the selectivity of any etch step with respect to the etching stopper layer would require careful analysis to determine whether the etch rate of the silicon nitride in the etching stopper layer 12 would be affected." Ex. 2010 ¶ 110.

Tellingly, Dr. Bottoms does not testify that a change in etch chemistry would have been necessary to make Kawai's third etch highly selective of the third dielectric layer with respect to the source/drain contact. No such change in etch chemistry is proposed by Petitioner. Pet. 42 ("a POSA would have been motivated to use the known method of performing the C_4F_8/O_2 etch disclosed in Kawai under conditions that are highly selective for the third dielectric layer with respect to the source/drain region," citing Ex. 1003 ¶ 116). Dr. Bottoms does not dispute Dr. Fair's testimony relied upon by Petitioner that a POSA would have known how to adjust the etch conditions in Kawai to produce an etch that is highly selective for the third dielectric layer with respect to the source/drain region. Ex. 1003 ¶ 116; *see* Pet. 42.

Although Dr. Bottoms testifies a "careful analysis" would be required to determine the effect of any change in etch chemistry on the etching stopper layer (Ex. 2010 ¶ 110), there is no persuasive evidence in the record that such an analysis would have required more than an ordinary level of skill in the art. The absence of such evidence is consistent with the '188 patent, which is silent regarding etch chemistry and presumes that a POSA knew how to control the etch chemistry and etch conditions to produce a third etch that is highly selective of the third dielectric layer with respect to the source/drain contact. For these reasons, we are persuaded there is no insufficiency in Petitioner's analysis regarding etch chemistry.

Next, Patent Owner argues that Petitioner and Dr. Fair do not explain how decreasing tolerances between the MOS transistors would relate to the need for a third etch with high selectivity for silicon dioxide with respect to silicon. PO Resp. 52. We disagree. Petitioner and Dr. Fair rely on Siozawa's teaching that "[f]or SiO_2 etching, higher selectivity to the photoresist and underlying layers and anisotropy are required for obtaining high-aspect-ratio features." Pet. 42; Pet Reply 12; Ex. 1003 ¶ 116; Ex. 1008, 1; Ex. 1018 ¶ 14. As Dr. Fair explains (Ex. 1018 ¶ 14), Siozawa's teaching regarding high-aspect ratio features is applicable to Kawai, which requires forming contact holes between narrowly-spaced gates. Ex. 1005 ¶¶ 3, 56 (Example 1). We are persuaded by Petitioner's argument (Pet Reply 12) and find that Dr. Fair's testimony regarding Siozawa's teaching and its applicability to Kawai establish a motivation to use a third etch with high selectivity for silicon dioxide with respect to silicon.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that it would have been obvious to POSA to use a third etch that is highly selective of the third dielectric layer with respect to the source/drain contact in Kawai's process.

b. Anisotropic etches

Petitioner contends that the etching conditions disclosed in Kawai produce an anisotropic etch. Pet. 46 (first etch), 50 (third etch). Petitioner relies on Dr. Fair's testimony, as well as Siozawa's discussion of anisotropic etching. *Id.* at 46 (citing Ex. 1003 ¶ 141; Ex. 1008, 1). Petitioner contends that Kawai Figures 10–12 show an anisotropic etch. *Id.* at 46–48. Petitioner further contends that it would have been obvious to a POSA to use

anisotropic etches for Kawai's first and third etches. *Id.* at 49 (citing Ex. 1003 ¶ 145; Ex. 1008, 1).

Patent Owner argues that Kawai's first and third etch steps are not anisotropic. PO Resp. 53–57. Patent Owner additionally argues that a POSA would not have been motivated to use anisotropic etches and that Siozawa teaches away from an anisotropic etch. *Id.* at 49, 58–60.

In the Institution Decision, we stated: "even if Kawai's first and third etches are not required to be anisotropic, unpatentability may be shown, if the evidence demonstrates that it would have been obvious to use an anisotropic etch." Dec. 23 (citing *Southwire Co. v. Cerro Wire LLC*, 870 F.3d 1306, 1311–12 (Fed. Cir. 2017)). For the reasons discussed below, and based on the record developed during trial, we find that a POSA would have recognized that either anisotropic etches or isotropic etches are suitable for Kawai's first and third etch steps and that Petitioner has shown by a preponderance of the evidence that a POSA would have had a reason or motivation to use anisotropic etches.

Kawai discloses that the first and third etches are carried out using dry etching, which the '188 patent discloses may be used to produce an anisotropic etch. Ex. 1005, ¶¶ 70, 76; Ex. 1001, 1:64–2:2. It is undisputed that isotropic dry etching and anisotropic dry etching were both well known in the art. *See, e.g.*, Ex. 2010 ¶ 108 ("It was well-known in the art that plasma etch processes, including reactive ion etch, could be either isotropic or anisotropic."); Ex. 3001, 11:35–42; Tr. 37:8–9 (Patent Owner: "It was known in the art that plasma processes could be either isotropic or anisotropic in nature."). It is also undisputed that a POSA would have known how to control the etching conditions so as to produce an anisotropic

etch. Ex. 2010 ¶¶ 86–88 (discussing parameters that can be varied to control the isotropic versus anisotropic characteristics of an etch). The '188 patent is silent regarding etching conditions, such as equipment, pressure, power, gas composition, and flow rate. The '188 patent thus presumes that the conditions necessary to produce an anisotropic etch were known in the art.

Petitioner has established, by a preponderance of the evidence, three rationales for why a POSA would have been motivated to use anisotropic etches for Kawai's first and third etches.

First, Petitioner has shown that a POSA would have been motivated to use anisotropic etches in order to produce high aspect ratio contact holes that are submicron in size with decreasing tolerances between the MOS transistors. Pet. 49 (citing Ex. 1003 ¶ 145); Pet. Reply 23. Our finding is supported by Dr. Fair's testimony that a POSA "would . . . have known that in order to open contact holes with small tolerances between the MOS transistors, which is the subject matter of Kawai, 'SiO2 etching [with] higher . . . anisotropy [is] required.'" Ex. 1003 ¶ 145 (quoting Ex. 1008, 1). Our finding is further supported by Siozawa, which teaches that "[f]or SiO_2 etching, higher selectivity to the photoresist and underlying layers and anisotropy are required for obtaining high-aspect-ratio features." Ex. 1008, 1. We find that Siozawa's teachings are applicable to Kawai's first and third etches, both of which are silicon oxide etches. Ex. 1005 ¶¶ 57, 58, 70, 76. Our finding is further supported by Dr. Fair's testimony that a POSA "would have been motivated to use the known method of performing the C_4F_8/O_2 etch disclosed in Kawai under conditions that are highly anisotropic for all of the etches to produce . . . a contact hole with a high-aspect ratio as illustrated in Kawai." Ex. 1003 ¶ 145. There is no dispute that Kawai's

contact hole has a high aspect ratio. *Id.*; Ex. 1005 ¶ 58 (contact hole 13a has depth of 4000 Å (0.40 μm) and diameter of 0.30 to 0.35 μm at upper surface and 0.20 μm at bottom of hole).

Our finding is further supported by the submicron size of Kawai's contact holes. Pet. Reply 23–24; Ex. 1005 ¶ 69 (disclosing resist mask for opening contact hole with a diameter from 0.30 to 0.35 μm). The experts agree that a POSA understood at the time of the invention that an isotropic etch is undesirable for submicron features. Ex. 1018 ¶ 19; Ex. 2010 ¶ 81 (citing Ex. 2004,[7] 80). We credit the undisputed testimony of Dr. Fair that "Kawai's hole size dictates that the etch should be anisotropic." Ex. 1018 ¶ 21.

Second, Petitioner has shown that a POSA would have been motivated to use anisotropic etches for Kawai's etches in order to form contact holes with straight sidewalls. Pet. 49–50 (citing Ex. 1003 ¶ 145); Pet. Reply 23. As Patent Owner and Dr. Bottoms concede, "straight sidewalls are typically formed using highly anisotropic etch steps." PO Resp. 57; Ex. 2010 ¶ 113. Our finding is supported by the cited testimony of Dr. Fair that a POSA would have been motivated to use anisotropic etches for all of Kawai's etches in order to produce a contact hole having straight sidewalls. Ex. 1003 ¶ 145. Our finding is further supported by Dr. Fair's undisputed testimony that straight sidewalls would have been understood by a POSA to be a benefit. Ex. 2005, 77:15–22.

[7] Jerzy Ruzyllo, *Semiconductor Glossary* (1st ed. 2004), Ex. 2004 (excerpts). Patent Owner mistakenly uses the exhibit number (2006) from the related IPR2017-01560.

Third, Petitioner has shown that a POSA would have been motivated to form Kawai's contact holes using anisotropic etches, rather than isotropic etches, in order to avoid increasing the contact area over the gates causing undesirable parasitic capacitance known as Miller capacitance. Pet. Reply 1–2, 18–19, 23 (citing Ex. 1018 ¶¶ 21–23).[8] Our finding is supported by Dr. Fair's deposition testimony, as follows:

> If you used an isotropic etch . . . you would balloon the contact hole open on top of the gates, such that when you filled your bit line contact, you would have significantly higher parasitic capacitance; so when you swing your bit line up and down, you would be having to charge and discharge that parasitic capacitance over the gate.

Ex. 2005, 87:4–10. Although Dr. Fair's testimony responds to a question regarding Hashimoto,[9] his discussion of ballooning the contact hole applies equally to Kawai. *See* Pet. Reply 19 (arguing that an isotropic etch in Kawai would have ballooned out the contact area, degrading performance due to the Miller effect). According to Dr. Fair, the desire not to balloon open the contact over the gates so as to increase parasitic capacitance "would have been known and obvious to one of ordinary skill in the art." *Id.* at 87:11–25. Our finding is further supported by Dr. Fair's reply testimony that isotropic etching in Kawai would increase the contact area over the gates, which a POSA would recognize as causing an increase in undesirable parasitic

[8] Patent Owner requested and received authorization to file a Sur-Reply to respond to Petitioner's reply arguments regarding Miller capacitance. Ex. 2016, 2–3; PO Sur-Reply 1–5. We address Patent Owner's Sur-Reply arguments below.

[9] JP H9-64297, published March 7, 1997 ("Hashimoto") is asserted as prior art to the '188 patent in related IPR2017-01560. Dr. Fair's deposition testimony (Ex. 2005) pertains to both IPR2017-01560 and IPR2017-01561.

capacitance known as Miller capacitance. Ex. 1018 ¶¶ 21–23. Dr. Bottoms agrees with Dr. Fair's testimony that "Miller capacitance" is "a component of 'the amount of drain-gate capacitance, C_{gd}, which in turn depends on the amount of overlap between the gate and the drain contact.'" Ex. 2017 ¶ 8 (quoting Ex. 1018 ¶ 22) *see* PO Sur-Reply 2. Dr. Bottoms refers to capacitance between the gate electrode and the drain of a transistor as "gate-drain capacitance" and agrees that it is undesirable parasitic capacitance. Ex. 2017 ¶¶ 8, 9.

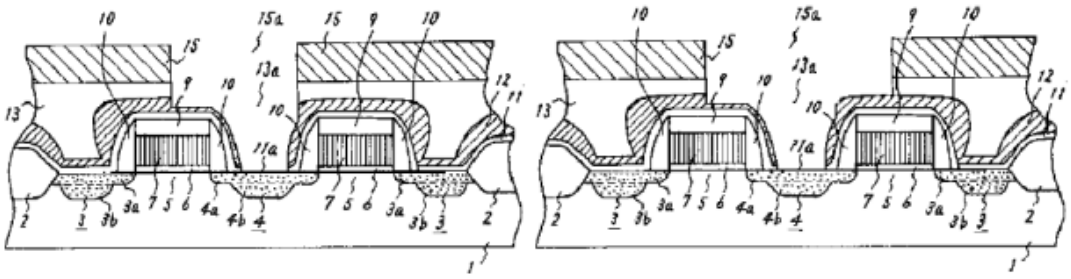
We now turn to Patent Owner's arguments regarding motivation to use anisotropic etches for Kawai's etch steps. PO Resp. 57–61.

Patent Owner argues that a POSA would recognize that "Kawai's design eliminates the need for anisotropic etching because the diameter of the contact hole (and any undercut caused by an isotropic etch) need not be strictly controlled." PO Resp. 58 (citing Ex. 2010 ¶ 110). According to Patent Owner, "the anisotropic nature of the etch . . . is of little importance to Kawai" because etching stopper layer 12 allows the contact holes to self-align and corrects for misaligned and oversized contact holes. *Id*. at 58–59 (citing Ex. 2010 ¶¶ 58, 109, 110; Ex. 1005 ¶¶ 73, 80).

Patent Owner relies on Dr. Bottoms' testimony, which we find to be not as credible as Dr. Fair's testimony. Dr. Bottoms agrees that Kawai discloses an electron cyclotron resonance device, which is typically used for reactive ion etching, and that a reactive ion etch could be either isotropic or anisotropic. Ex. 2010 ¶¶ 107, 108. Dr. Bottoms further agrees that an isotropic etch was understood to be undesirable for submicron features. *Id.* ¶ 81. That testimony contradicts Dr. Bottoms' opinion that there is no need

for anisotropic etching in Kawai, which has submicron contact holes. *Id.* ¶ 109; Ex. 1005 ¶ 58 (0.30 to 0.35 µm contact holes).

Although Dr. Bottoms testifies that Kawai's process "allows . . . for oversized contact holes" (Ex. 2010 ¶ 109), he does not identify any contact hole in Kawai larger than one micron. *See* Pet. Reply 24 ("Kawai discloses a submicron contact hole" and a "POSA . . . would have understood Kawai to be concerned with the size of the contact hole"). Instead, Dr. Bottoms relies on a modified figure that is not part of Kawai's disclosure. *Id*. More specifically, Dr. Bottoms illustrates his testimony (*id.*) with the following images:



The above images show contact holes, and the left image is Kawai Figure 12. According to Dr. Bottoms, the contact hole on the right "is nearly twice the size" as the contact hole on the left, and "[i]n both examples," a contact hole is opened to the source/drain region. Ex. 2010 ¶ 109. Although Dr. Bottoms characterizes both images as "examples," the image on the right with the oversized contact hole is not part of Kawai's disclosure and appears to have been modified by Patent Owner. We find that Dr. Bottoms' testimony lacks credibility to the extent that it relies upon, but does not acknowledge, Patent Owner's modification of Kawai's figure.

Based on the above comparison of Kawai Figure 12 and a modification of that figure, Dr. Bottoms testifies that a POSA "would

recognize that anisotropic etching is not strictly required because the diameter of the hole 15a (and any undercut caused by an isotropic etch) need not be strictly controlled." Ex. 2010 ¶ 109; *see* PO Resp. 58–59 (relying on Dr. Bottoms' testimony). We do not give significant weight to this testimony because it fails to take into account undesired parasitic capacitance known as Miller capacitance, which Dr. Bottoms agrees results from overlap between the gate and the drain contact. Ex. 1018 ¶¶ 21, 22; Ex. 2017 ¶ 8. We give greater weight to Dr. Fair's testimony, which accounts for both Kawai's self-aligned contact hole design and the desire to avoid Miller capacitance. Ex. 1018 ¶ 23 ("the geometry of Kawai's contact hole and the fact that the first etch was "self-aligning" would suggest using an anisotropic etch because an isotropic etch would have ballooned out the contact area to create excessive drain contact over the gates, seriously degrading performance due to the Miller effect").

Next, Patent Owner argues that a POSA generally understood "it was difficult to achieve both high selectivity and anisotropy" and "a POSA would not go through the extra effort that Siozawa says will be needed to configure the first etch to be both highly selective (as required by Kawai) and anisotropic." PO Resp. 59–60 (citing Ex. 2010 ¶¶ 58, 100; Ex. 1005 ¶¶ 70–73, 76, 77; Ex. 1008, 1). Although Patent Owner cites paragraphs 58 and 100 of Dr. Bottoms' testimony (*id.*), neither paragraph discusses selectivity nor supports that it would be difficult to achieve both high selectivity and anisotropy in Kawai.

Patent Owner quotes Siozawa as stating "it is difficult to achieve both high selectivity and anisotropy." PO Resp. 60 (quoting Ex. 1008, 1). As Petitioner argues and Dr. Fair testifies, however, the quoted statement

describes an etch that uses a C_4F_8 plasma. Pet. Reply 25; Ex. 1008, 1; Ex. 1018 ¶ 28. Siozawa goes on to state that with the addition of oxygen to the C_4F_8 plasma, "[h]igh selectivity of SiO_2 to Si or photoresist and high anisotropy could be achieved." Ex. 1008, 1; Ex. 1018 ¶ 28. Siozawa thus does not support Patent Owner's argument that "extra effort" would be required to achieve both high selectivity and anisotropy. PO Resp. 60. As Dr. Bottoms concedes, a POSA knew how to control parameters, including chamber pressure, flow rate, plasma power, etchant gas, and etchant gas concentration, to obtain the desired isotropic or anisotropic etch characteristics. Ex. 2010 ¶¶ 86–88. Moreover, Siozawa discusses the desirability of anisotropic etching for fabricating high-density integrated circuits (Ex. 1008, 1), thus contradicting Patent Owner's argument that a POSA would not have been motivated to use anisotropic etches to form Kawai's contact holes.

Next, Patent Owner advances a number of arguments regarding Miller capacitance. PO Sur-Reply 1–5. Patent Owner argues that increased parasitic capacitance would have been accepted in exchange for the benefits of Kawai's "self-aligned" contact holes, that the contribution of the source/drain electrode is small in comparison to other sources of parasitic capacitance, that a POSA knew how to control parasitic capacitance by increasing the thickness of the dielectric layer on top of the gate, and that the Miller effect is not as significant for DRAMs as for other devices. PO Sur-Reply 2–5 (citing Ex. 2017 ¶¶ 7–17). Although Patent Owner and its expert seek to diminish the significance of Miller capacitance as a motivating factor, they do not dispute that a desire to avoid parasitic capacitance would have been a reason for a POSA to favor anisotropic etches over isotropic

etches for Kawai's etch steps. More specifically, Patent Owner and its expert do not dispute that isotropic etching would have resulted in increased contact hole size, which would have in turn caused increased overlap between the gate electrode and the source/drain contact and an increase in undesirable parasitic capacitance known as Miller capacitance. PO Sur-Reply 3, 4; Pet. Reply 1–2, 18–19, 23; Ex. 2005, 87:4–25; Ex. 1018 ¶¶ 21, 22.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that it would have been obvious to a POSA to use anisotropic etches for Kawai's first and third etch steps.

c. Straight sidewalls

Petitioner contends that Kawai discloses a contact hole with straight sidewalls. Pet. 55, 57 (citing Ex. 1005, Fig. 12). Petitioner further contends that a "POSA would have known that anisotropic etches will produce a contact hole with straight sidewalls" and would have been motivated to use anisotropic etches for Kawai's first and third etches in order to form contact holes with straight sidewalls. *Id.* at 49, 56.

We find that Petitioner's contention is supported by Kawai Figure 12, which is reproduced below:

(FIG. 12)

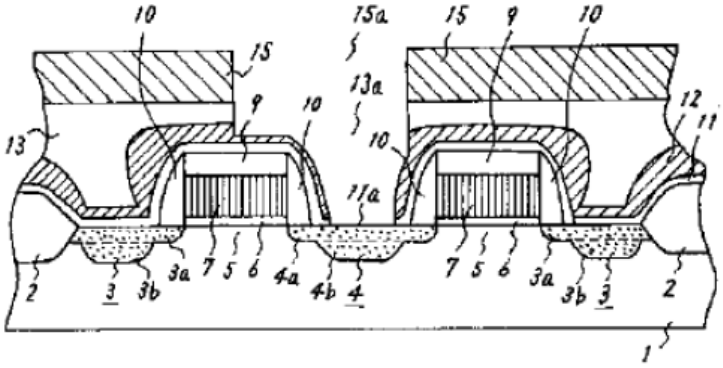


Figure 12 shows a cross-section of a semiconductor device, including contact hole 13a. Ex. 1005 ¶ 76. Petitioner's reliance on Kawai Figure 12 to show a contact hole with straight sidewalls can be compared with Patent Owner's reliance on Figure 1E of the '188 patent to show the same feature. Patent Owner's annotation of Figure 1E is reproduced below:

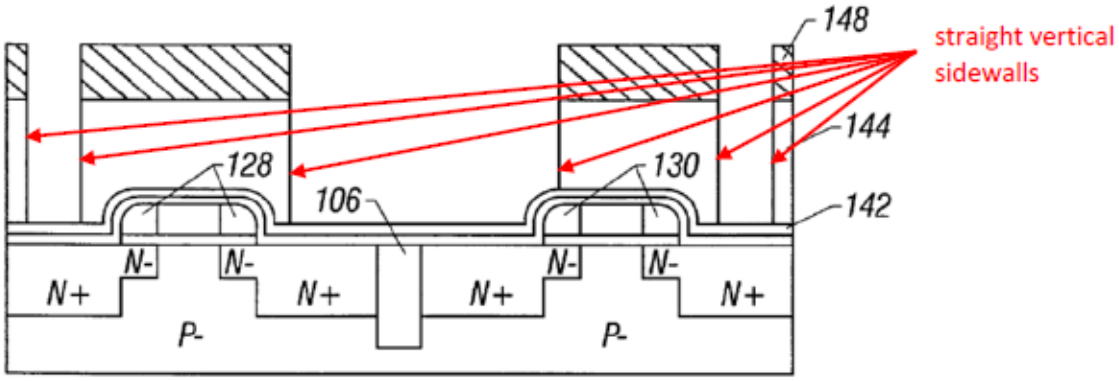


FIG. 1E

Figure 1E of the '188 patent shows contact holes. Patent Owner and Dr. Bottoms have annotated Figure 1E to identify contact holes with straight, vertical sidewalls. PO Resp. 7; Ex. 2010 ¶ 84.

We find that Kawai Figure 12 shows a contact hole with straight sidewalls in the same manner as Patent Owner contends the '188 patent shows contact holes with straight sidewalls. In both cases, the figures show

a contact hole with straight vertical sidewalls, at least where the contact hole is bounded by the interlevel dielectric layers, as opposed to the insulating layers around the gate.

Patent Owner argues that Kawai neither discloses nor suggests contact holes having straight sidewalls (PO Resp. 49, 62), but does not meaningfully develop that argument, which, therefore, is unpersuasive. In the alterative, we determine that Patent Owner's undeveloped argument is waived. *Cf. Fresenius USA, Inc. v. Baxter Int'l, Inc.*, 582 F.3d 1288, 1296 (Fed. Cir. 2009) (a party cannot preserve an argument if it presents "only a skeletal or undeveloped argument to the trial court").

We have considered paragraph 116 of Dr. Bottoms' testimony, even though it is not cited or explained in the Patent Owner Response. There, Dr. Bottoms opines that "Kawai does not suggest or disclose that its contact holes have straight sidewalls." Ex. 2010 ¶ 116. Although Dr. Bottoms discusses Kawai's self-aligned contact holes and the size of the mask opening relative to the width of the contact hole in the region between the gates (*id.*), he does not explain why these features support his conclusion regarding straight sidewalls. Accordingly, we do not give substantial weight to paragraph 116 of Dr. Bottoms' testimony.

Patent Owner presents an argument concerning the "anisotropic etch" limitation that we consider in the context of the "straight sidewalls" limitation. Citing *Nystrom v. Trex Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005), Patent Owner argues that "Kawai's drawing figures cannot be assumed to be proportional or to include all features of the device." PO Resp. 55. Patent Owner concedes that Kawai's drawing figures illustrate straight sidewalls with no undercutting of the etch mask, but argues that

"Kawai was not concerned with the overall width of the top of the hole—and consequently did not accurately illustrate the etch effects in the upper layers." *Id.* at 54–55 (citing *Nystrom*). Petitioner responds that it is not relying on Kawai's figures to show precise proportions or particular sizes, but instead to show that no undercutting was present. Pet. Reply 16.

We determine that Petitioner's reliance on Kawai's drawings to show straight sidewalls is not inconsistent with *Nystrom*. There, the Federal Circuit reversed a judgment of invalidity that was based on a computer-generated model of structures illustrated in a prior art patent figure and computations performed on that model to determine a ratio for comparison with a numerical limitation of the claim. *Nystrom*, 424 F.3d at 1148. The Court admonished that "patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." *Id.*, 424 F.3d at 1149 (quoting *Hockerson-Halberstadt, Inc. v. Avia Group Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000)). The *Nystrom* Court explained: "[a]bsent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value." *Id.* (quoting *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977)).

In *Hockerson-Halberstadt*, the Court found "unavailing" the patentee's argument against prosecution history disavowal, where the argument "hinge[d] on an inference drawn from certain [patent] figures about the quantitative relationship between the respective widths" of two structures shown in the figures. *Id.*, 222 F.3d at 956. In *Wright*, the Court was unpersuaded by the USPTO's argument that comparison of the relative

dimensions of appellant's and a prior art patent's drawings showed that the prior art had a length "of roughly 1/2 to 1 inch." *Wright*, 569 F.2d at 1127.

In contrast to *Nystrom*, *Hockerson-Halberstadt*, and *Wright*, Petitioner's "straight sidewalls" argument does not rely on Kawai's drawings to show precise proportions, particular sizes, quantitative values, a quantitative relationship, or relative dimensions of the contact hole. Instead, Petitioner relies on Kawai's drawings to show a contact hole with straight sidewalls.

We find the *Mraz* decision cited by Petitioner (Pet. Reply 11) to be more on point than any of *Nystrom*, *Hockerson-Halberstadt*, or *Wright*. In *Mraz*, the claim recited, among other things, edge rolls having a groove angle "not exceeding 15°." *Mraz*, 435 F.2d at 1070. The Court held it was not improper to rely on a prior art patent figure to show edge rolls having a groove angle within the claimed range. *Id.* at 1072–73. The Court explained that, although patent drawings are not working drawings, "things patent drawings show clearly are not to be *disregarded*." *Id.* at 1072. The Court cited precedent in which "the teachings of patent drawings, even as to features unexplained by the specification, proved dispositive." *Id.* (citing *In re Bager*, 47 F.2d 951, 952–953 (CCPA 1931)).

We find that Petitioner's reliance on Kawai's figures to show a contact hole with straight sidewalls is proper under the holding of *Mraz*. Like the patent figures relied upon in *Mraz*, Kawai's figures show the contact holes "with great particularity." *Id.* at 1072. Kawai Figures 9–12 show a step-by-step process for forming a contact hole, illustrating in detail which layers and parts of layers are removed during each step. Kawai Figure 10, for example, shows the result of a first etch. The lines are drawn

to show that layer 13 and a portion of layer 12 are removed during a first etch. Notably, both parties' experts rely on Kawai's figures to show features, such as lateral etching, that are not expressly disclosed in the text of Kawai. *See, e.g.*, Ex. 1003 ¶ 142; Ex. 2010 ¶ 114 (both presenting annotations of Kawai Figure 10). Taken together, these circumstances support our view that a POSA would have understood Kawai's figures as disclosing a contact hole with straight sidewalls, notwithstanding that straight sidewalls are not discussed in the text of Kawai. If anything, this case favors reliance on the patent drawings more strongly than *Mraz* because the claim limitation "straight sidewalls" is qualitative, not quantitative, whereas the claim at issue in *Mraz* recited a numerical limit on the size of an angle. *See Mraz*, 435 F.2d at 1070 ("not exceeding 15°").

Moreover, even if the "straight sidewalls" limitation is not expressly disclosed by Kawai, Petitioner has established that it would have been obvious in view of Kawai to fabricate a contact hole with straight sidewalls. It is undisputed that a contact hole with straight sidewalls is typically produced with highly anisotropic etch steps. Pet. 56 ("A POSA would have known that anisotropic etches will produce a contact hole with straight sidewalls."); PO Resp. 57 ("straight sidewalls are typically formed using highly anisotropic etch steps"). For the reasons discussed in section II.E.1.b. above, Petitioner has shown by a preponderance of the evidence that a POSA would have been motivated to use anisotropic etches for Kawai's first and third etch steps. This same evidence establishes that a POSA would have been motivated to use highly anisotropic etches to produce a contact hole with straight sidewalls.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claim 3 of the '188 patent is unpatentable as obvious in view of Kawai.

2. Claim 11

Claim 11 is similar to claim 1, except that claim 11 recites additional limitations relating to a gate insulator, steps for forming the first, second, and third dielectric layers, and gate thickness. Ex. 1001, 9:55, 9:63–67. Claim 11 also recites that each of the first, second, and third etches is "anisotropic." *Id.* at 10:2, 10:9, 10:16.

For the "anisotropic etch" limitations, both parties rely on the same arguments for claim 11 as are presented for claim 3. Pet. 46–50, 57; PO Resp. 61–62. For the reasons discussed in Section II.E.1.b. above, we determine Petitioner has shown by a preponderance of the evidence that a POSA would have been motivated to use anisotropic etches for Kawai's first and third etch steps.

Petitioner directs us to substantial evidence that the remaining limitations of claim 11 are disclosed by Kawai. Pet. 28–46. Patent Owner does not contest that evidence. PO Resp. 61–62. Accordingly, we determine Petitioner has shown by a preponderance of the evidence that these limitations of claim 11 are disclosed by Kawai.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claim 11 of the '188 patent is unpatentable as obvious in view of Kawai.

3. Claim 21

Claim 21 is similar to claim 11, except that claim 21 recites a "gate oxide" instead of a "gate insulator," a "polysilicon gate" instead of a "gate," a "photoresist layer" instead of an "etch mask," "consists of" instead of "includes," and "through the third dielectric layer" instead of "in the third dielectric layer." *Compare* Ex. 1001, 9:55–56, 9:61, 10:1, 11:19 (claim 11), *with id.* at 10:55–56, 10:63, 11:7–8, 11:30–31 (claim 21). Claim 21 recites additional limitations not found in claim 11 relating to the source/drain contact, interlevel dielectric layer, and etches. *Id.* at 10:59–62, 10:67–11:3, 11:5–6, 11:11–12, 11:19–20, 11:28–29. Different from claim 11, claim 21 recites a contact hole with "straight sidewalls." *Id.* at 11:33.

For the "highly selective" third etch limitation, both parties rely on the same arguments for claim 21 as are presented for claim 3. Pet. 55; PO Resp. 62. For the reasons discussed in Section II.E.1.a. above, we determine Petitioner has shown by a preponderance of the evidence that it would have been obvious to POSA to use a third etch that is highly selective of the third dielectric layer with respect to the source/drain contact in Kawai's process.

For the "anisotropic etch" limitations, both parties rely on the same arguments for claim 21 as are presented for claims 3 and 11. Pet. 54–56; PO Resp. 62–63. For the reasons discussed in Section II.E.1.b. above, we determine Petitioner has shown by a preponderance of the evidence that a POSA would have been motivated to use anisotropic etches for Kawai's first and third etch steps.

Petitioner directs us to substantial evidence that the remaining limitations of claim 21 are disclosed by Kawai. Pet. 50–56. Patent Owner does not contest that evidence. PO Resp. 62–63. Accordingly, we

determine Petitioner has shown by a preponderance of the evidence that these limitations of claim 21 are disclosed by Kawai.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claim 21 of the '188 patent is unpatentable as obvious in view of Kawai.

4. Claims 12, 13, 15–19, 22, 23, and 25–27

Claims 12, 13, and 15–19 each depend directly or indirectly from claim 11. Claims 22, 23, and 25–27 each depend directly or indirectly from claim 21. Claims 12 and 22 each recite "the second anisotropic etch is highly selective of the source/drain contact with respect to the third dielectric layer." Ex. 1001, 10:23–25, 11:35–37. Claims 13 and 23 each recite "the source/drain contact is the source/drain region." *Id.* at 10:26–27, 12:1–2. Claim 15 recites "the interlevel dielectric layer consists of the first, second and third dielectric layers." *Id.* at 10:30–32. Claims 16 and 25 each recite: "the first and third dielectric layers are the same material." *Id.* at 10:33–34, 12:5–6. Claims 17, 26, and 27 each recite materials for the dielectric layers, including silicon dioxide for the first and third layers and silicon nitride for the second layer. *Id.* at 10:35–41, 12:7–14. Claim 18 recites "the gate is polysilicon and the etch mask is photoresist." *Id.* at 10:42–43. Claim 19 recites "forming a conductive plug in the contact hole that contacts the source/drain contact." *Id.* at 10:44–46.

Petitioner directs us to substantial evidence that Kawai discloses the features recited in dependent claims 12, 13, 15–19, 22, 23, and 25–27. Pet. 58–60, 62–65. Patent Owner does not contest that evidence. Patent Owner presents no argument regarding dependent claims 16 and 17. Patent Owner

presents no argument regarding dependent claims 12, 13, 15, 18, and 19 separate from its arguments regarding independent claim 11. *See* PO Resp. 62. Patent Owner presents no argument regarding dependent claims 22, 23, and 25–27 separate from its arguments regarding independent claim 21. *See id.* at 63. Accordingly, we determine Petitioner has shown by a preponderance of the evidence that the limitations of claims 12, 13, 15–19, 22, 23, and 25–27 are disclosed by Kawai.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claims 12, 13, 15–19, 22, 23, and 25–27 of the '188 patent are unpatentable as obvious in view of Kawai.

5. Claims 20, 28, and 29

Claim 20 depends from claim 19, which depends from claim 11. Claim 20 recites "forming a metal-1 pattern on the first dielectric layer that contacts the conductive plug." Ex. 1001, 10:47–49. Claim 28 depends from claim 21 and recites: "planarizing the interlevel dielectric by applying chemical-mechanical polishing before forming the photoresist layer." *Id.* at 12:15–17. Claim 29 depends from claim 21 and recites the following sequence of steps: "stripping the photoresist layer after forming the contact hole; forming a conductive plug in the contact hole that contacts the source/drain contact; and forming a metal-1 pattern on the first dielectric layer that contacts the conductive plug." *Id.* at 12:18–26.

Petitioner directs us to substantial evidence that the subject matter of claim 20 would have been obvious in view of Kawai alone. Pet. 65–66. In the alternative, Petitioner directs us to substantial evidence that the subject matter of claim 20 is disclosed by Sung and would have been obvious in

view of Kawai and Sung. *Id.* at 66–69. Regarding a motivation to combine Kawai and Sung, Petitioner directs us to substantial evidence that a POSA would have known that the formation of higher-level interconnects, as taught by Sung, was necessary to complete a DRAM device, as disclosed by Kawai. Pet. 68–69.

Patent Owner does not contest that evidence. Patent Owner presents no argument regarding dependent claim 20 separate from its arguments regarding independent claim 11. *See* PO Resp. 63–64. Patent Owner presents no argument regarding dependent claims 28 and 29 separate from its arguments regarding independent claim 21. *See id.* at 64.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claim 20 of the '188 patent is unpatentable as obvious in view of Kawai or alternatively in view of Kawai and Sung and that claims 28 and 29 are unpatentable in view of Kawai and Sung.

III. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 3, 11–13, 15–23, and 25–29 of the '188 patent are unpatentable.

IV. ORDER

Accordingly, in consideration of the foregoing, it is hereby:

ORDERED that, based on a preponderance of the evidence, claims 3, 11–13, 15–23, and 25–29 of the '188 patent are unpatentable;

FURTHER ORDERED that Patent Owner's unopposed motion to excuse the late filing of the Patent Owner Response and accompanying exhibits is *granted*; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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