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Paper No. 30
Entered: December 13, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS LLC,
Patent Owner.

Case IPR2017-01562
Patent 6,097,061

Before GRACE KARAFFA OBERMANN, KRISTINA M. KALAN, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Determining That Claims 1, 3–6, 11,
And 13–16 Are Proven Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

This is an *inter partes* review of claims 1, 3–6, 11, and 13–16 ("the challenged claims") of U.S. Patent No. 6,097,061 (Ex. 1001, "the '061 patent") based on grounds set forth in the Petition (Paper 1, "Pet.") filed by Micron Technology, Inc. ("Petitioner"). Paper 8 ("Dec."). Petitioner bears the burden of proving unpatentability by a preponderance of the evidence, a burden that never shifts to Patent Owner. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc*., 800 F.3d 1375, 1378 (Fed. Cir. 2015). We have jurisdiction under 35 U.S.C. § 6. We issue this decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

The Petition is supported by a Declaration of Richard Fair, Ph.D. (Ex. 1003). Lone Star Silicon Innovations LLC[1] ("Patent Owner") filed a Response to the Petition (Paper 13, "Resp.") supported by two Declarations of W. R. Bottoms, Ph.D. Exs. 2001, 2007. Petitioner filed a Reply (Paper 15, "Reply") supported by a second Declaration of Dr. Fair. Ex. 1020. With Board pre-authorization (Ex. 2009), Patent Owner filed a Sur-Reply (Paper 16, "Sur-Reply") supported by a third Declaration of Dr. Bottoms. Ex. 2011. In forming our final determinations, we take account also of the parties' Motions for Observations Regarding Cross-Examination (Papers 21, 25) and Responses thereto (Papers 24, 26).

As an initial matter, based on the experience and qualifications asserted in their curricula vitae, we find both Dr. Fair and Dr. Bottoms qualified to opine from the perspective of a person of ordinary skill in the art

[1] Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 4, 1.

at the time of the invention of the '061 patent. *See* Ex. 1004 (Dr. Fair's resume); Ex. 2002 (Dr. Bottoms's resume).

A. Related Proceedings

We directed the parties to file updated mandatory notices identifying related proceedings. Dec. 3 n.2. Petitioner filed an updated notice that does not address the matter of related proceedings. Paper 14.

Patent Owner filed two updated notices that identify a single administrative proceeding relating to the '061 patent (Case IPR2018-00063, which we refer to herein as "the Nanya IPR" or "IPR063," brought by a different petitioner) and several "concurrent" administrative proceedings (two of which were terminated pursuant to Patent Owner's request for adverse judgment), involving patents allegedly "unrelated" to the '061 patent "except by their common assignment to [Patent Owner] and by having been asserted in lawsuits involving [Patent Owner]." Paper 11, 1–2; Paper 27, 1–2. The "concurrent" administrative proceedings identified by Patent Owner include three cases (specifically, IPR2017-01560, involving U.S. Patent No. 5,912,188 ("the '188 patent), IPR2017-01561, also involving the '188 patent, and IPR2017-01563, involving U.S. Patent No. 6,103,611), which were heard together with the instant matter in a combined final oral hearing conducted on September 18, 2018. The record includes a transcript of the hearing. Paper 29.

Patent Owner, in its updated mandatory notices, also identifies seven "actions" involving the '061 patent: (1) *Lone Star Silicon Innovations, LLC v. STMicroelectronics, Inc.*, No. 3:17-cv-07206 (Dec. 19, 2017, N.D. Cal.) (dismissed without prejudice); (2) *Lone Star Silicon Innovations, LLC v. Toshiba Corp.*, No. 3:17- cv-03980 (Oct. 14, 2016, N.D. Cal.) (dismissed

without prejudice); (3) *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:17-cv-05458 (Oct. 7, 2016, N.D. Cal.) (dismissed without prejudice); (4) *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, Appeal No. 2018-1578 (Feb. 15, 2018, Fed. Cir.); (5) *Lone Star Silicon Innovations, LLC v. Nanya Technology Corp.*, No. 3:17-cv-04032 (Oct. 7, 2016, N.D. Cal.) (dismissed without prejudice); (6) *Lone Star Silicon Innovations, LLC v. Nanya Technology Corp.*, Appeal No. 2018-1581 (Feb. 15, 2018, Fed. Cir.); and (7) *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (Mar. 16, 2018, N.D. Cal.). Paper 11, 3; Paper 27, 2–3.

B. The '061 patent (Ex. 1001)

The '061 patent, titled "Trenched Gate Metal Oxide Semiconductor Device and Method," was filed March 30, 1998, and issued August 1, 2000. Ex. 1001, at [21], [22], [45], [54]. The '061 patent relates to metal oxide semiconductor ("MOS") devices having a trenched gate. *Id.* at [57].

Figure 2B of the '061 patent is reproduced below.

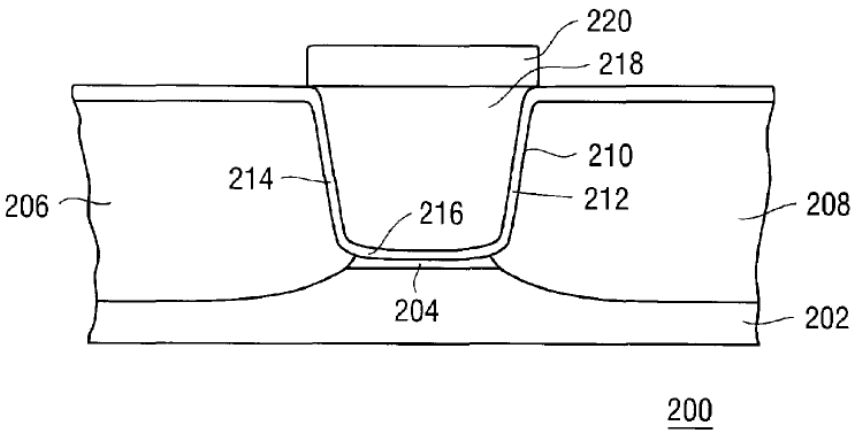


FIG. 2B

Figure 2B, above, is a cross-sectional view of a MOS device fabricated according to the principles described in the '061 patent. *Id.* at 2:65–67.

As seen in Figure 2B, semiconductor structure 200 includes substrate 202, channel region 204, source region 206, drain region 208, trench 210, trench-to-gate insulating layer 212, and trenched gate electrode 218. *Id.* at 3:2–8. "Trench-to-gate insulating layer 212 preferably comprises a trench dielectric spacer 214 formed on the vertical surfaces inside trench 210 and a trench gate dielectric 216 formed on the bottom surface inside trench 210." *Id.* at 3:30–33. Tungsten silicide layer 220 may be formed on a top surface of trenched gate electrode 218. *Id.* at 3:60–61.

"Source region 206 and drain region 208 are diffusion regions of semiconductor material that are doped with impurities that have a conductivity opposite to the conductivity of substrate 202" and "have a depth substantially equal to or greater than the depth of trench 210 and partially extend laterally underneath the bottom of trench 210 to form source and drain junctions disposed along portions of the sidewalls and bottom surface of trench 210." *Id.* at 3:5–8, 3:15–20. In a description of the preferred embodiment of the invention, the specification further refers to "[c]hannel region 204" as "an implanted region formed beneath the bottom surface of trench 210 and is immediately contiguous source region 206 and drain region 208." *Id.* at 3:20–22.

According to the '061 patent, a "trenched polysilicon gate structure improves the overall topography of the structure for better process control and improved manufacturability," "improves the device packing density and scaleability [sic] by reducing the lateral diffusion of the source and drain regions under the trenched polysilicon gate," and "minimizes the process

variations of overlaps between the trenched polysilicon gate and the source and drain regions." *Id.* at 1:49–57; *see id.* at 4:30–52; *see also id.* at 1:24–42 (discussing limitations on packing density and performance of conventional transistors formed on top surface of substrate).

B. Illustrative Claim

Of the challenged claims, claims 1 and 11 are independent. Claims 3–6 depend, directly or indirectly, from claim 1, and claims 13–16 depend, directly or indirectly, from claim 11. Independent claim 1 of the '061 patent is reproduced below, and is illustrative of the challenged claims.

> 1. A semiconductor transistor comprising:
>
> a semiconductor substrate of a first conductivity type;
>
> a source region of a second conductivity type in the semiconductor substrate;
>
> a drain region of the second conductivity type spaced from the source region in the semiconductor substrate;
>
> a trench having substantially upright vertical surfaces and a bottom surface formed in the semiconductor substrate intermediate the source and drain regions;
>
> ***a channel region formed in the semiconductor substrate***, the channel region forming a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions;
>
> a trench-to-gate insulating layer formed on the substantially upright vertical surfaces and the bottom surface inside the trench, the trench-to-gate insulating layer forming a contiguous layer inside the trench; and
>
> a trenched gate electrode having a top surface and formed on the trench-to-gate insulating layer inside the trench.

Ex. 1001, 7:50–8:2 (emphasis added).

C. The Applied References

Petitioner relies on the following references in the asserted grounds.

Reference	**Issue Date**	**Exhibit**
U.S. Patent No. 5,408,116 ("Tanaka")	Apr. 18, 1995	Ex. 1005
U.S. Patent No. 5,283,449 ("Ooka")	Feb. 1, 1994	Ex. 1006
U.S. Patent No. 5,300,447 ("Anderson")	Apr. 5, 1994	Ex. 1007

Pet. 4–5.

D. The Asserted Grounds

We instituted review of the '061 patent based on the following challenges to claims 1, 3–6, 11, and 13–16 set forth in the Petition.

Reference(s)	**Basis**	**Claims Challenged**
Tanaka	§ 103	1, 3–5, 11, 13–15
Tanaka and Ooka	§ 103	6, 16
Anderson	§ 103	1, 3, 4, 11, 13, 14

Pet. 4–5, 32–90; Dec. 23.

II. ANALYSIS

In our reproduction of claim 1 above, we emphasize a limitation that requires, in a semiconductor transistor, "a channel region formed in the semiconductor substrate." Ex. 1001, claim 1. That same phrase appears in the only other independent challenged claim. *Id.* at claim 11. In the next section, we resolve the construction of that disputed claim phrase. To the extent that the meaning of any other claim term requires discussion, we provide it in our analysis of the patentability challenges.

A. Claim Construction

The '061 patent has expired. Resp. 13; Ex. 1001, [22] (filing date of March 30, 1998). Accordingly, we apply a district court-type claim construction approach. *In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) ("[T]he Board's review of the claims of an expired patent is similar to that of a district court's review."); *see Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed. App'x 1019, 1024 (Fed. Cir. 2016) (in an *inter partes* review, "[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc)").

Under the *Phillips* standard, we assign claim terms their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). Neither party directs us to the prosecution history of the '061 patent; therefore, we focus our analysis on the language of the claims and the disclosure of the specification.

The challenged claims require, in a semiconductor transistor, "a channel region formed in the semiconductor substrate." Ex. 1001, claims 1 and 11 (the independent challenged claims). Patent Owner contends this phrase should be construed as "a channel region defined by the presence of dopants that are separate or additional relative to the semiconductor substrate of a first conductivity type." Resp. 15. Petitioner opposes that construction, asserting that no express construction of the channel region limitation is necessary. Reply 5–14.

Our analysis begins with the language of the claims, which nowhere mentions a channel region defined by the presence of dopants. Ex. 1001, claims 1 and 11. The '061 patent specification, however, discusses a "preferred embodiment" in which the channel region "is formed using an implant of boron," i.e., a dopant. Ex. 1001, 5:36–45.

Petitioner argues, and Patent Owner does not dispute, that at the time of the invention, the plain and ordinary meaning of the phrase "a channel region formed in the semiconductor substrate" in this particular field of endeavor denoted the region circumscribed by the gate, gate oxide, source, and drain in a transistor; that is, the place in the transistor where a channel forms during normal operation or use, regardless of whether the channel is doped differently than the substrate. Reply 7–9; Ex. 1019 ("Sedra")[2], 6; Ex. 1022 ("Weste")[3], 5–6; Ex. 1007, Abstract, 2:34–36 (the Anderson patent, identified in the patentability challenges); *see* Sur-Reply 3–4 (declining to contest that "the 'most well-understood way' and the 'textbook way' of forming a channel region required forming the surrounding structures" (quoting Reply 5–6, 10)).

On that critical point, regarding the plain and ordinary meaning of the disputed claim phrase, Patent Owner's own witness, Dr. Bottoms, testified that "textbooks" published at the relevant time reflect "a standard use of the term 'channel region' in the art" that "encompass[es] a portion of the

[2] Sedra and Smith, *Microelectric Circuits,* Saunders College Publishing (3rd ed. 1991).
[3] Weste and Eshraghian, *Principles of CMOS VLSI Design, A Systems Perspective,* Addison-Wesley (2nd ed. 1993).

substrate where an induced channel will be formed during operation of the device." Ex. 1031, 33:17–35:2; *see* Paper 25, 1 (Observation No. 2).

The *Thorner* decision is especially applicable to the facts of this case. There, our reviewing court considered a district court's decision that narrowed the plain and ordinary meaning of claim terms to comport with the manner in which those terms were "consistently use[d]" in "the embodiments in the specification." *Thorner*, 669 F.3d at 1365. The Federal Circuit stated, "[T]he district court improperly limited" the claim terms in view of embodiments described in the specification. *Id*. at 1369. Given that the specification included no "clear and explicit statement by the patentee" that rose to the level of "lexicography or disavowal," the district court erred by selecting constructions that were narrower than the plain and ordinary meaning of claim terms as understood by an ordinarily skilled artisan at the time of the invention. *Id*. at 1367–68; *see GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) (identifying patentee "lexicography and disavowal" as the only two circumstances that warrant narrowing the plain and ordinary meaning of a claim term).

The principles set forth in *Thorner* guide our construction of the claim phrase "a channel region formed in the semiconductor substrate." *Id*. The specification of the '061 patent identifies "[c]hannel region 204" as "an implanted region formed beneath the bottom surface of trench 210" in "one embodiment" of the invention. *Id*. at 2:65; 3:20–23. But the specification does not establish that the patentee, with sufficient clarity or deliberateness, "act[ed] as its own lexicographer" to narrow the plain and ordinary meaning

of the disputed claim phrase to require a channel region formed by channel doping. Reply 10 (citation omitted).[4]

On the contrary, where the specification describes the channel region as implanted with a dopant, the specification cabins that description to "one embodiment" or a "preferred embodiment" of the invention. Ex. 1001, 1:58, 62–64 ("[i]n one embodiment of the present invention," a channel region "is implanted in the substrate beneath the bottom surface of the trench"); 2:40–41, 3:20–23 ("[p]referred [e]mbodiment" includes a "[c]hannel region" that is "an implanted region formed beneath the bottom surface of [the] trench"); 4:55; 4:65–66; 5:36–45 ("one embodiment" or "a preferred embodiment of the present invention" includes a channel region formed using a boron implant); 7:29–28, 40–41 (in "one embodiment" "the substrate is ion implanted to form 414 the channel region for the device.").

Patent Owner responds, "[E]ven if ion implantation is not explicitly required by the claims, 'formed in the semiconductor substrate'" implies "a channel region that is a ***structural feature*** defined by the presence of dopants separate or additional relative to the semiconductor substrate of a first conductivity type." Resp. 15 (emphasis Patent Owner's). Nothing adduced at trial, however, persuades us that the "first conductivity type," to

[4] Patent Owner submits that Petitioner, in arguing against importation of limitations from the specification into the claims, cites cases that apply "the 'broadest reasonable interpretation' standard—not the *Phillips* standard that applies here." Sur-Reply 4 (citations omitted). But Petitioner also identifies Federal Circuit precedent informing, in the context of a district-court type construction, that "[t]he standards for finding lexicography and disavowal are exacting" and it may be "improper to import limitations even from [a] sole embodiment." Reply 10 (quoting *GE Lighting*, 750 F.3d at 1309); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004).

which Patent Owner refers (*id*.), distinguishes the channel region from the semiconductor substrate on the basis of its conductivity type. Those words are used in the claim to distinguish the semiconductor substrate from the "source region" and "drain region" of a "second conductivity type." Ex. 1001, claims 1 and 11. Moreover, as further discussed below, Petitioner's evidence persuades us that an ordinarily skilled artisan would not have understood the words "formed in" as requiring the presence of channel dopants.

Petitioner directs us to persuasive evidence that an ordinarily skilled artisan would have recognized "that creating the source/drain, gate oxide, and gate structures forms the channel region" as a structural feature of the transistor. Reply 8–9 (citing Ex. 1019, 6; Ex. 1022, 5–6; Ex. 1007, Abstract, 2:34–35); Paper 25, 1 (Observation No. 2) (citing Ex. 1031, 14:21–15:3). The Sedra textbook establishes the plain and ordinary meaning of "a channel region formed in a semiconductor substrate" as the region where a channel forms, whether or not that region is doped differently than the substrate. Ex. 1001, claims 1 and 11.

Specifically, Petitioner directs us to Figure 5.1 of the Sedra textbook, which illustrates a "[c]hannel region" in a semiconductor "substrate" before a voltage is applied, in a transistor that is manufactured without implanted channel dopants. Ex. 1019, 5–8; Reply 6 (reproducing Ex. 1019, 6 (Fig. 5.1)). We reproduce Figure 5.1 of the Sedra textbook below.

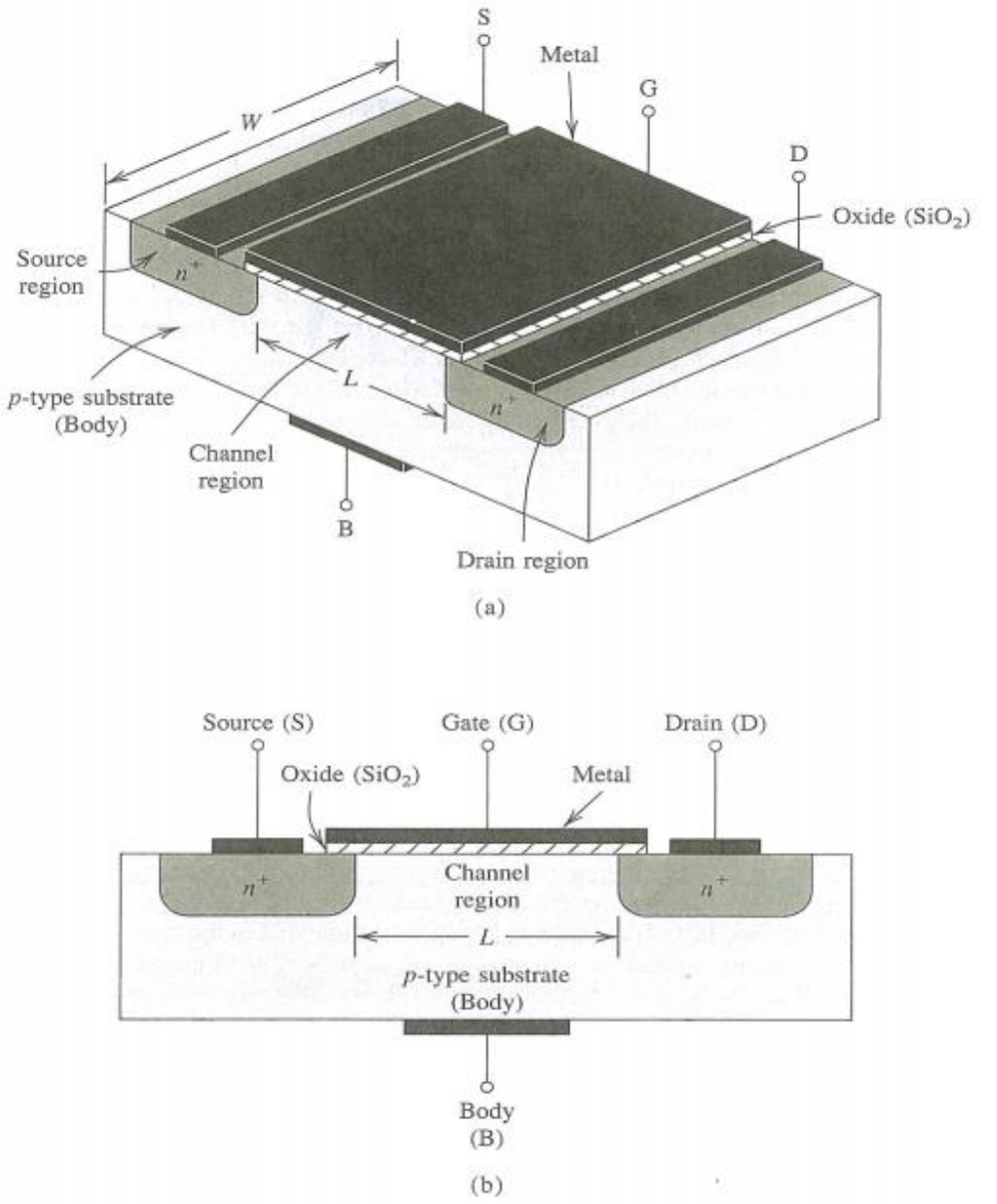


Fig. 5.1 Physical structure of enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically L = 1 to 10 μm, W = 2 to 500 μm, and the thickness of the oxide layer is of the order of 0.1 μm.

Reply 6 (reproducing Ex. 1019, 6 (Fig. 5.1)). Figure 5.1 includes perspective and cross sectional views of the physical structure of an *n*-type metal oxide semiconductor ("NMOS") transistor, and depicts a channel region in relation to the other transistor structures, including the gate, gate oxide, source, drain, and substrate body of the semiconductor device.

Figure 5.1 of the Sedra textbook identifies "the physical structure" of a transistor that "is fabricated on a p-type substrate" without mentioning ion implantation or channel doping. Ex. 1019, 5–8. As Dr. Fair explains, an ordinarily skilled artisan would have understood that the structure, identified and illustrated as the "[c]hannel region" in Figure 5.1 of the Sedra textbook, is not defined by channel dopants. Ex. 1020 ¶¶ 5–10; Reply 10. Significantly, Figure 5.1 identifies a "[c]hannel region" by the arrangement of surrounding structures, including the gate, gate oxide, source, drain, and substrate body. Reply 7; Ex. 1019, 6 (Fig. 5.1).

Referring to Figure 5.1 in the Sedra textbook, Patent Owner's witness, Dr. Bottoms, testified, "It's not just this textbook" that defines a channel region in this manner. Ex. 1031, 13:20. Dr. Bottoms explained, "[W]here the channel is induced" during normal operation or use of a transistor is "commonly referred to as a channel region." *Id*. at 13:18–20. Dr. Bottoms repeatedly stated that the "channel will be induced below the gate oxide" during normal operation or use of a transistor. Reply 8 (identifying, by three bullet points, relevant portions of Dr. Bottoms's deposition testimony) (quoting Ex. 1021, 69:16–71:2, 72:21–74:12). Further, Dr. Bottoms admitted that "textbooks," which provide background information bearing on how an ordinarily skilled artisan would have used terms in this field, demonstrate "a standard use of the term 'channel region' in the art" that would broadly "encompass a portion of the substrate where an induced channel will be formed during operation of the device." Ex. 1031, 33:17–35:2; *see* Paper 25 (Observation No. 1).

Other evidence of record supports a conclusion that the plain and ordinary meaning of "a channel region formed in the semiconductor

substrate" refers to the area delineated by the substrate, gate, source, and drain; that is, the area in a fully functional transistor where the channel forms, regardless of whether the channel is doped differently than the substrate. Petitioner's witness, Dr. Fair, explains that the Anderson patent, asserted in the grounds of unpatentability, "refers to the step of bounding the substrate region, under gate oxide/gate, with the source/drain regions as 'forming the transistor channel' because at this point, a region has been created in which an induced channel will form." Ex. 1020 ¶ 9; *see* Ex. 1020 ¶ 10 (citing Ex. 1022, 5–6 (background reference, describing the formation of a "channel" in the "region immediately under the gate," *i.e.*, the "channel region")); *see also* Reply 6 (directing us to these paragraphs of Dr. Fair's declaration). In addition, Petitioner directs us to the Weste treatise, which describes "forming a 'channel' in 'the region immediately under the gate'" of a semiconductor transistor—without any requirement of channel doping. Reply 6 (quoting Ex. 1022, 5–6).

Accordingly, we find that the Sedra textbook, the Anderson patent, the Weste treatise, and the opinion testimony of both parties' witnesses consistently affirm this key point: By the 1990's, a well-known way to "form[] a channel region in the semiconductor substrate" was "to surround a substrate region of one dopant type with (1) a source and drain of a second dopant type, (2) a gate oxide, and (3) a gate." Reply 10 (citing Ex. 1019, 5). A channel region formed in that manner generally would have been recognized as a structural element distinguishable from the substrate body at the point of manufacture, as illustrated in Figure 5.1 of the Sedra textbook. Reply 7; *see* Ex. 1019, 5–8, Fig. 5.1 (identifying a "[c]hannel region" and a "substrate ([b]ody)" as separate elements of a transistor, without use of

channel dopants, and before a voltage is applied). Patent Owner was afforded a full and fair opportunity to contest Petitioner's proposed plain and ordinary meaning of the disputed claim term, but did not do so effectively. *See generally* Sur-Reply.

Patent Owner argues that Petitioner's own witness, Dr. Fair, agrees that the specified channel region "is a structural feature formed by doping separate from that of the substrate." Resp. 39 (citing Ex. 2008 107:5–18). Dr. Fair's testimony, however, leaves no doubt that the witness was merely describing (correctly) one embodiment of the invention set forth in the specification as including an implanted channel region (identified as "channel region 204"). Reply 5–6 n.3 (quoting Ex. 2008, 107:5–18). Similarly, we find unpersuasive Patent Owner's further view that an ordinarily "skilled artisan would recognize that dopants within the channel region are ***the only potential means*** for distinguishing the channel region relative to the pre-existing semiconductor substrate." Sur-Reply 5 (citing Ex. 2011 ¶ 10) (emphasis added). On that point, Petitioner persuasively establishes that Patent Owner's proposed construction excludes "the most well understood way of forming a channel region" known at the time of the invention—a way that did not require channel doping or ion implantation, but rather, involved forming a channel by the placement of a source, drain, gate, and gate oxide in a transistor. Reply 5.

Petitioner presents persuasive evidence that the channel region of a semiconductor transistor would have been identifiable even before the transistor is "turned 'on.'" Reply 11. As Petitioner's evidence shows, one of ordinary skill in the art would have distinguished the "[c]hannel region" (that is, the region where a channel will be induced during normal operation)

from the "substrate ([b]ody)" of a transistor, even when the transistor is idle. Ex. 1019, 6 (Fig. 5.1) (illustrating a "[c]hannel region" and a "substrate ([b]ody)" as separate structural elements in an idle transistor); Reply 7. Indeed, Patent Owner's own witness confirmed that the channel "will be induced below the gate oxide" and "will always be in the substrate material with some spa[t]ial relationship to the source and drain." Reply 8 (quoting Ex. 1021, 69:16–71:2, 72:21–74:12 (Dr. Bottoms's testimony)).

Further, Petitioner shows that an induced channel, formed when a voltage is applied to the transistor, would have been understood to be "opposite in conductivity type (n-type) compared to the semiconductor substrate (p-type)." *Id*. at 12 (reproducing Ex. 1019, 8 (Fig. 5.2)); *see* Ex. 1019, 8 (textual description in Figure 5.2, explaining, "An *n* channel is induced at the top of the substrate beneath the gate."); Ex. 1020 ¶¶ 17–18 (Dr. Fair's testimony). Patent Owner does not meaningfully dispute that, when a MOS transistor is "turned 'on'" (Reply 11), an inversion layer is created characterized by a conductivity type that is opposite to that of the substrate body (*id*. at 6 n.4, 11 n.5, 12 (and evidence cited therein)). *See* Sur-Reply 1–7 (nowhere disputing that fact). Figure 5.2 of the Sedra textbook, reproduced below, illustrates the induced channel that forms when a voltage is applied to a semiconductor transistor in use. Reply 12 (reproducing Ex. 1019, 8 (Fig. 5.2)).

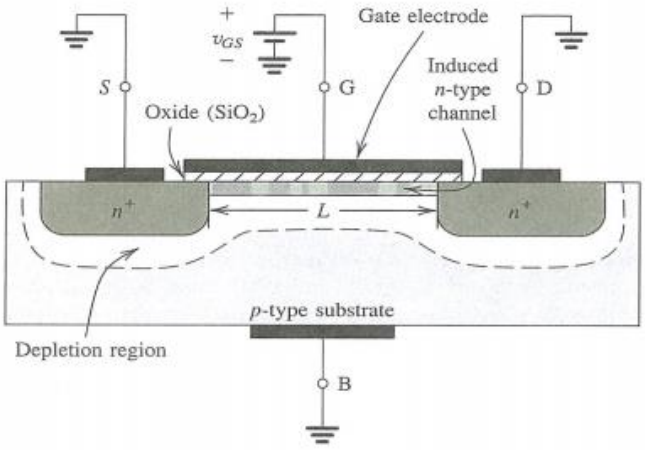


Fig. 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

Figure 5.2 is an illustration of an enhancement type NMOS transistor with a positive voltage applied to the gate. Figure 5.2 identifies an "[i]nduced n-type-channel" as a shaded area under the gate and gate oxide, and extending between the source and drain. Figure 5.2 further explains, "An *n* channel is induced at the top of the substrate beneath the gate."

Figure 5.2 leaves no doubt that an induced channel, even without channel doping, would have been readily distinguishable from the substrate based on a difference in conductivity. Reply 11; *see* Ex. 1019, 6 (Fig. 5.2, depicting an "*n*-type channel" and a "*p*-type substrate"); Ex. 1020 ¶¶ 17–18 (Dr. Fair's testimony). And an ordinarily skilled artisan would have recognized the area where an induced channel forms as a "[c]hannel region" even before a voltage is applied to the transistor. Ex. 1019, 6 (Fig. 5.1) (illustrating a "[c]hannel region" in an idle transistor before a voltage is applied and without the presence of channel dopants).

We have considered Patent Owner's position that "the ordinarily skilled artisan would recognize that separate channel doping is part of the novelty of the invention, in view of the claims and the description in the specification." Sur-Reply 4 (citing Ex. 2011 ¶ 8). We are aware that "there

is sometimes a fine line between reading a claim in light of the specification, and reading a limitation into the claim from the specification." *Phillips*, 415 F.3d at 1323 (quoting *Comark Communications, Inc. v. Harris Corp*., 156 F.3d 1182, 1186–87 (Fed. Cir. 1998)). Here, however, the patentee did not, through "lexicography or disavowal" (*Thorner*, 669 F.3d at 1367–68), narrow the plain and ordinary meaning of the phrase "a channel region formed in the semiconductor substrate" to require formation by channel doping or exclude a channel region that, during normal operation, accommodates an induced channel. Ex. 1001, claims 1 and 11.

On that point, Petitioner directs us to Dr. Fair's discussion of disclosures in the specification that identify a channel region without any mention of channel doping. Reply 9–10; Ex. 1020 ¶ 16 (citing Ex. 1001, Abstract, 1:24–35). Patent Owner observes that those disclosures "do not preclude a channel region with additional doping"—an observation that misses the mark. Sur-Reply 5. The relevant inquiry is whether the specification, with sufficient clarity and deliberateness, reflects "lexicography or disavowal" that warrants a narrowing of the plain and ordinary meaning of the disputed claim phrase to require channel dopants. *GE Lighting*, 750 F.2d at 1308–09 (only "lexicography and disavowal" will "compel departure from the plain meaning" of claim terms). Based on our review of the specification, we are compelled to answer that question in the negative. The specification consistently describes an implanted channel region as part of "one embodiment" or a "preferred embodiment" of the claimed semiconductor transistor. Ex. 1001, 1:58, 62–64; 2:40–41, 3:20–23; 4:55; 4:65–66; 5:36–45; 7:29–28, 40–41 ().

Patent Owner also argues that the words "formed in" are used consistently in the claims to denote features created "during manufacture of the claimed semiconductor transistor"—such as the "trench" of claim 1, the "trench spacer dielectric layer" of claim 4, and the "layer of tungsten silicide" of claim 6. Resp. 17–18. That argument is unpersuasive, in light of our finding that a channel region is formed in the semiconductor substrate during manufacture "by creating the source/drain, a gate oxide, and a gate." Reply 15 (citing Pet. 46–47); *see id*. at 9–14 (and evidence cited therein). Simply stated, the "[c]hannel region," labelled and identified as a separate structural feature in the idle transistor depicted in Figure 5.1 of the Sedra textbook (Ex. 1019, 6), would have been universally recognized as a "channel region," with or without the presence of channel dopants, the moment the source, drain, gate, and gate oxide are created to form a fully functional transistor. *See* Reply 17 (reproducing Ex. 1019, 6 (Fig. 5.1)).

Patent Owner further argues that the specification would have informed an ordinarily skilled artisan that the channel region must "exist ***regardless of whether the transistor is in use***." Resp. 16 (emphasis Patent Owner's). As illustrated in Sedra's Figure 5.1 (illustrating an idle transistor) and Figure 5.2 (illustrating a transistor in use), a channel region would have been understood to exist without regard to whether the transistor is idle or in use. Ex. 1019, 5–8. Patent Owner's observation that "the word 'formed' is recited in past tense" (Resp. 18) is of no import. Even before a transistor is turned on to induce a channel, a region formed to accommodate that channel is identifiable by the placement of the source, drain, gate, and gate oxide. At the point of manufacture, that region would have been recognized as "a channel region formed in the semiconductor substrate" without regard to

whether the region is defined by the presence of channel dopants. Ex. 1001, claims 1 and 11; *see* Ex. 1019, 6 (Fig. 5.1) (illustrating a "[c]hannel region" that exists as a separate structural element, relative to the "substrate ([b]ody)," without channel doping and before a voltage is applied to the transistor).

Because "[t]he claims themselves set forth the limits of the patent grant" (*Phillips*, 415 F.3d at 1323), we come back again to the broad language used in the claims, which specify a semiconductor transistor having "a channel region formed in the semiconductor substrate" without any mention of channel doping or ion implantation (Ex. 1001, claims 1 and 11). As Petitioner observes, "Nothing from the specification redefines the plain and ordinary meaning of" the disputed claim phrase to exclude a channel region that would have been universally recognized as the area formed to accommodate a channel, as delineated by the source, drain, gate, and gate oxide in a transistor. Reply 10 (quoting *GE Lighting*, 750 F.3d at 1309 (citation omitted); *Liebel-Flarsheim Co.*, 358 F.3d at 906. Patent Owner's counterview that "the channel induced during operation could either be larger or smaller than [an] additionally doped region of the substrate" is without merit. Sur-Reply 5 (citing Ex. 2011 ¶ 11). The claims do not specify, and our construction does not require, a channel region that is coextensive with the induced channel. Ex. 1001, claims 1 and 11.

We agree with Patent Owner that the specification describes a channel region formed by implanting channel dopants—and it follows that a channel region defined by implanted dopants may fall within the scope of the claims. But we cannot ignore that the specification repeatedly describes an implanted channel region as merely "one embodiment" or a "preferred

embodiment" of the invention. Ex. 1001, 1:58, 61–64 (describing "one embodiment of the present invention" in which "[t]he device structure further includes a source region, a drain region and a channel region which is implanted in the substrate beneath the bottom surface of the trench."), 3:20–23 ("Channel region 204 is an implanted region formed beneath the bottom surface of trench 210 and is immediately contiguous source region 206 and drain region 208."), 5:40–42 (describing "a preferred embodiment of the present invention" in which "channel region 312 is formed using an implant of boron"), 7:28–29, 40–41 (in "one embodiment" of the invention, "the substrate is ion implanted to form 414 the channel region for the device."). Those disclosures in the specification, combined with the breadth of the claim language itself, persuades us that the patentee included a preferred embodiment that is "exemplary in nature," but did not convey, with sufficient clarity or deliberateness, an intent to "define the outer limits of the claim term." *Phillips*, 415 F.3d at 1323.[5]

[5] Our reluctance to read a limitation from the preferred embodiment into the claims is not inconsistent with the Federal Circuit's decision in *Cross Med. Prods., Inc. v. Medtronic Sofamor Danek*, 424 F.3d 1293, 1311–12 (Fed. Cir. 2005), which is discussed in the briefs but has little practical relevance to the issue at hand. *See* Resp. 18–19; Reply 12–13; Sur-Reply 3. There, the Federal Circuit considered whether a surgical device "capable of operative joinder to [a] bone segment" met a claim limitation that required a device "operatively joined" to "bone." *Cross Med. Prods.*, 424 F.3d at 1303, 1310–11. Unsurprisingly, the Federal Circuit indicated the apparatus claim could be infringed during use, for example, when a surgeon connects the device to bone. *Id*. The dispute in *Cross* centered on whether a device manufacturer was liable for inducing the surgeon's infringing activity. *Id*. The Cross decision confirms the familiar tenet that an apparatus claim may be met by a device in use. *See id*.; *see also* Reply 13 (citing *Broadcom Corp. v. Emulex Corp*., 732 F.3d 1325, 1333 (Fed. Cir. 2013)).

We recognize that, in the Nanya IPR, we preliminarily determined that the claims of the '061 patent "require something 'more than a channel region that is merely a place within the semiconductor substrate.'" IPR063, Paper 9, 10 (quoting IPR063, Paper 5, 25)). We made that finding on a preliminary record that did not include the Sedra textbook, the Anderson patent, the Weste treatise, or the consistency in the opinions of both parties' witnesses bearing on the plain and ordinary meaning of the disputed claim phrase. On the complete record now before us, and in this particular field of endeavor, we determine that an ordinarily skilled artisan readily would have recognized the area where the channel forms—as delineated by the placement of the source, drain, gate, and gate oxide in a semiconductor transistor—as "a channel region formed in a semiconductor substrate," with or without the presence of channel dopants. Ex. 1001, claims 1 and 11; *see* Ex. 1019, 6 (Fig. 1) (the Sedra textbook, illustrating such a "[c]hannel region" in an idle transistor without channel doping); Reply 3–15 (and evidence cited therein). That finding aligns with our observation in the Nanya IPR, "If the patentee intended the claims to require dopants defining the channel region, the claims could have been drafted to recite such dopants. Nothing about the word 'formed' in the claims necessarily requires that the channel region be defined by the presence of dopants that are 'separate or additional relative to the semiconductor substrate of a first conductivity type.'" IPR063, Paper 9, 11; *see* Sur-Reply 4 (citing Ex. 1021 ¶ 8) (quoting Patent Owner's Preliminary Response (Paper 6)).

We assign the words "a channel region formed in the semiconductor substrate" (Ex. 1001, claims 1 and 11) their plain and ordinary meaning in the art, which, at the time of the invention, was broad enough to embrace the

area—delineated by the "spa[t]ial arrangement" of the source, drain, gate, and gate oxide—created to accommodate a channel. Reply 8 (quoting Ex. 1021, 69:16–71:2, 72:21–74:12 (testimony of Patent Owner's witness, Dr. Bottoms)); Ex. 1019, 6, 8 (Figs. 5.1, 5.2) (illustrating a "[c]hannel region" before, and an "[i]nduced" channel after, a voltage is applied to transistor).

B. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.[6] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

An obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). A prima facie case of obviousness is established when the prior art, itself, would appear to have

[6] Neither party directs our attention to any objective evidence of non-obviousness. *See generally, e.g.*, Resp.

suggested the claimed subject matter to a person of ordinary skill in the art. *See In re Rinehart*, 531 F.2d 1048, 1051 (CCPA 1976).

We analyze the asserted grounds of unpatentability in accordance with those principles to discern whether Petitioner meets its burden of proving by a preponderance of the evidence that the challenged claims are unpatentable.

C. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art "would be a person with at least a Bachelor's degree in electrical engineering, material science, physics, or a closely related field and at least five years of industry experience in the fabrication of semiconductor devices." Pet. 18 (citing Ex. 1003 ¶¶ 19–20). Petitioner continues, "[a]n individual with an advanced degree in a relevant field would require less experience in semiconductor fabrication." *Id.* (citing Ex. 1003 ¶ 20). Patent Owner agrees with Petitioner's proposed definition. Resp. 10–11. We adopt that agreed-upon definition, which is supported by the specification and consistent with the disclosures of the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

D. The Asserted Prior Art

Tanaka (Ex. 1005)

Tanaka relates to a "grooved gate transistor" having particular shape characteristics such that the threshold voltage does not decrease and/or such that the threshold voltage can be adjusted by shape. Ex. 1005, at [57].

Figures 1A and 7A of Tanaka are reproduced below.

FIG. 1A

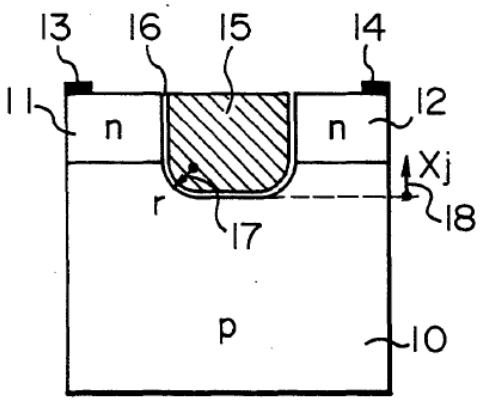
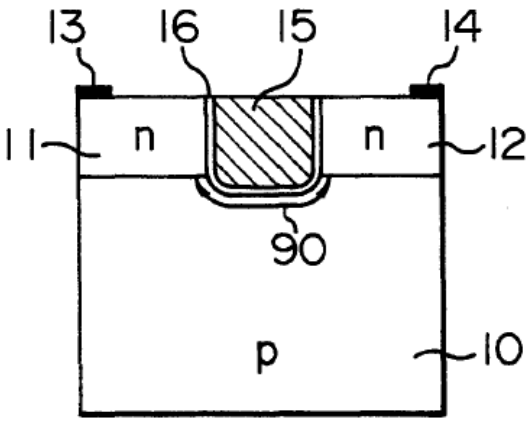


FIG. 7A



Figures 1A and 7A, above, are sectional views of a semiconductor device according to Tanaka. *Id.* at 3:8–19, 3:27–30. As seen in each of Figures 1A and 7A, the semiconductor device includes p type-silicon substrate 10, n type-diffused layers 11, 12, source electrode 13, drain electrode 14, gate electrode 15, and oxide 16. *Id.* at 3:50–58. Figure 1A further illustrates a junction depth X_j 18 of diffused layers 11, 12 and a radius of curvature r 17 of gate electrode 15, each of which is related to the particular shape of gate electrode 15 according to the embodiments of Tanaka. *Id.* at 3:59–68. Channel length 90 is illustrated in Figure 7A. *See id.* at 1:46–47, 3:27–30.

Ooka (Ex. 1006)

Ooka relates to a semiconductor integrated circuit device having MOSFETs (that is, metal-oxide-semiconductor field-effect transistors). Ex. 1006, at [57]. In relevant part, Ooka teaches a gate electrode formed of an N^+-type polycrystalline silicon film with a tungsten silicide film thereon. *Id.* at 4:67–5:11, Fig. 1B.

Anderson (Ex. 1007)

Anderson relates to an "extremely small minimum scaled Metal-Oxide-Semiconductor, MOS, transistor." Ex. 1007, at [57]. Figures 1a and 1b of Anderson are reproduced below.

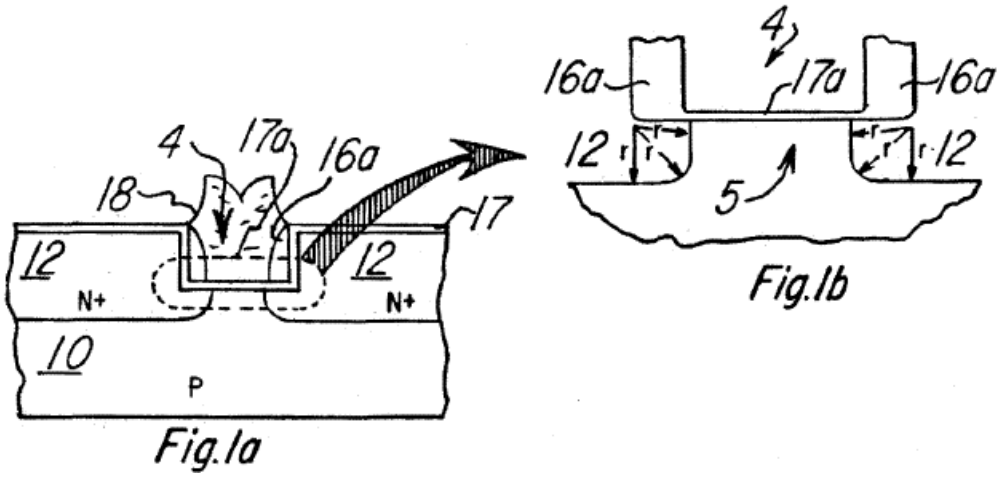


Figure 1a, above, is a sectional view of a semiconductor device according to Anderson, and Figure 1b, also above, is an enlarged view of the channel area of the semiconductor device of Figure 1a. *Id.* at 2:46–50. As seen in the figures, the semiconductor device includes P type substrate 10, gate conductor 18 formed in trench 4, doped regions 12 (source and drain), channel 5, and insulators 16a, 17a. *Id.* at 2:58–3:43.

E. Asserted Obviousness Based, at Least in Part, on Tanaka

Petitioner asserts that claims 1, 3–5, 11, and 13–15 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Tanaka, and that claims 6 and 16 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Tanaka and Ooka. Pet. 4, 32–67. Patent Owner argues that Tanaka does not teach "a channel region formed in the semiconductor substrate that is also immediately contiguous the source and drain regions" as required by independent claims 1 and 11 (Resp. 39–46), and that an ordinarily skilled

artisan would not combine Tanaka and Ooka in the manner asserted by Petitioner (*id.* at 48–52). Based on our review of the arguments and evidence presented by the parties, and for the reasons explained below, we determine that Petitioner shows by a preponderance of the evidence that the challenged claims are unpatentable.

1. Asserted Obviousness in View of Tanaka

Independent Claim 1

Petitioner advances color-coded figures that "correspond the claim limitations of claim 1 to Figures 1A and 7A of Tanaka." Pet. 21–22. Petitioner also provides "a side-by-side comparison of Fig. 2B of the ['061 patent and Figure 7A of Tanaka." *Id*. at 23. The following table provides a summary of Petitioner's mapping of Tanaka to structural elements of claim 1.

Claim 1	**Tanaka**
semiconductor transistor	"A finely structured grooved gate transistor . . . " Ex. 1005, at [57].
semiconductor substrate	p type-silicon substrate 10
source region	n type-diffused layer 11
drain region	n type-diffused layer 12
trench	groove in which gate electrode 15 is formed
trench-to-gate insulating layer	gate oxide 16
trenched gate electrode	gate electrode 15

See Pet. 35–45, 49–53 (citing Ex. 1005, at [57], 3:44–58, 4:3–11, 4:13–15, 4:25–33, 4:37–5:3, 5:31–38, Figs. 1A, 2, 7A, 7B, 8; Ex. 1003 ¶¶ 92, 94, 95, 97–99, 101–106, 115). Patent Owner does not meaningfully dispute that the claim elements identified in the above table are met by the semiconductor transistor disclosed in Tanaka. *See generally* Resp.

Claim 1 further recites "a channel region formed in the semiconductor substrate, the channel region forming a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions" ("the channel region limitation"). Regarding that claim limitation, Petitioner asserts that, although "Tanaka does not expressly refer to a 'channel region,' Tanaka describes this area with reference to a 'channel length,' confirming that the area underneath the gate would have been understood by a [person of ordinary skill in the art] . . . to be the channel region, i.e., the 'channel length' is the length of the channel region." Pet. 48 (citing Ex. 1003 ¶¶ 110–112). Petitioner also points to Tanaka's disclosure that "Boron (B) . . . is injected . . . to form a *p* type-impurity region as channel doping." *Id.* (quoting Ex. 1005, 4:30–33) (emphasis omitted). Petitioner asserts, although "Tanaka does not expressly state that the channel is 'immediately contiguous to the source and drain regions,' it would have been understood by a [person of ordinary skill in the art] as such in light of Tanaka disclosures, and at least obvious." *Id.* at 46 (citing Ex. 1003 ¶¶ 107–112). Petitioner points to channel length 90 in Figure 7A, which, according to Petitioner, is "immediately contiguous to the source and drain regions 11, 12, and is below the trench." *Id.* (citing Ex. 1005, 1:46–47).

Tanaka illustrates that channel length 90 "forms a contiguous region beneath the bottom surface of the trench." *Id.* at 46–47 (citing Ex. 1005,

Fig. 7A). Citing Dr. Fair's testimony, Petitioner argues, and we agree, that a channel region is formed between the source and drain regions in Tanaka, because it is this region "in which a voltage on the gate induces a channel to make the transistor conduct (in simple terms, to turn on the transistor)" and, necessarily, "there must be a channel region contiguous between the source and drain for the transistor to actually operate properly, and as is conventional." *Id.* at 49 (citing Ex. 1003 ¶¶ 110–112).

Patent Owner argues that Tanaka's channel length 90 is not a channel region as specified in claim 1. *See* Resp. 39–46. Specifically, Patent Owner argues that Tanaka's "doping of the channel region is not altered by a separate step of doping" and, on that basis, submits that Tanaka's channel length 90 "becomes structurally distinguishable from the substrate" "***only in operation***." *Id*. at 33 (emphasis Patent Owner's). For the reasons stated above in our claim construction analysis, we disagree. The objective evidence on point supports that a person of ordinary skill in the art would have understood that a channel region is the area where the channel is formed, whether or not that area is separately doped relative to the semiconductor substrate. *See supra* section II.A.

Patent Owner further argues that Tanaka does not disclose source and drain regions that are "immediately contiguous to an implanted channel region." Resp. 43. Here again, however, claim 1 does not require "an implanted channel region." *Id*. We determine that Figure 7A of Tanaka illustrates that channel length 90 touches (and, therefore, "is immediately contiguous to") the source and drain regions (13, 14). Pet. 47 (annotated reproduction of Figure 7A of Tanaka). Similar to the '061 patent, moreover, Tanaka describes the implantation of boron to form a channel. *Id.*; *compare*

Ex. 1005, 4:20–46, *with* Ex. 1001, 5:36–45. On this record, although "Tanaka does not expressly refer to a 'channel region,' Tanaka describes this area with reference to a 'channel length,' confirming that the area underneath the gate would have been" recognized by an ordinarily skilled artisan as a channel region; that is, in Tanaka "the 'channel length' is the length of the channel region." Pet. 48 (citing Ex. 1003 ¶¶110–112).

Patent Owner attempts to distinguish Tananka's boron-based channel doping from the boron-based channel doping described in the '061 patent. Resp. 29–35. Patent Owner also advances technical reasons why Tanaka's channel length 90 is not "immediately contiguous to the source and drain regions" (Ex. 1001, claim 1). Resp. 35–38. Those arguments are unpersuasive because they do not take account of the disclosure of Tanaka, including Figure 7A, which depicts a channel length that extends from the source to the drain and, thereby, demonstrates the "immediately contiguous" relationship specified in claim 1. Ex. 1005, Fig. 7A. We find that Tanaka's Figure 7A illustrates a channel region (identified by Tanaka as "channel length 90") that "extends between and contacts the source and drain regions." Reply 16. The claim 1 phrase, "immediately contiguous," requires no more. Ex. 1001, claim 1; *see id*. at Fig. 3D; 5:40 (element 312).

In the alternative, we find that Tanaka discloses or suggests a channel region that exists as an inversion layer that contiguously extends from the source to the drain when the transistor is turned on. Ex. 1005, Fig. 7A; *see* Ex. 1019, 7–8 and Fig. 5.2 (the Sedra textbook, showing that, in operation, a transistor includes an inversion layer that contiguously extends from source to drain). As Sedra explains, when "a positive voltage" is applied "to the

gate" of a transistor, the resulting inversion layer contiguously extends from source to drain:

> [T]he positive gate voltage attracts electrons from the *n*+ source and drain regions (where they are in abundance) in the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an *n* region is in effect created, connecting the source and drain regions, as indicated in Fig. 5.2. Now if a voltage is applied between drain and source, current flows through this induced *n* region, carried by the mobile electrons. The induced *n* region thus forms a **channel** for current flow from drain to source and is aptly called so. . . . The channel is created by inverting the substrate surface from p type to *n* type. Hence the induced channel is called an **inversion layer**.

Ex. 1019, 7–8 (emphasis in original); *see id*. at Fig. 5.2; *see also* Reply 18 (citing Ex. 1019, 7–8 and reproducing Fig. 5.2). Although the inversion layer forms only when a voltage is applied to the transistor in normal use, Tanaka's transistor is no less a "semiconductor transistor" when in use than when idle. Ex. 1001, claims 1 and 11.

The Sedra textbook, therefore, confirms Petitioner's view that an ordinarily skilled artisan would have recognized that, when Tanaka's transistor is turned on (Ex. 1005, Fig. 7A; Reply 11; Ex. 1003 ¶ 110), a channel region forms as an inversion layer that has an opposite conductivity type compared to the substrate body and, further, the inversion layer contiguously extends from source to drain (Ex. 1019, 7–8 and Fig. 5.2). *See supra* section II.A; Pet. 48–49 (and evidence cited therein); *see also* Reply 16–17 (asserting that Tanaka forms an induced channel during normal operation that is "a channel formed in the substrate").

Patent Owner, for its part, does not dispute that Tanaka discloses or suggests an induced channel region as an inversion layer that contiguously

extends from source to drain. *See generally* Sur-Reply. Patent Owner focuses on its own proposed (but incorrect) claim construction, arguing that Tanaka fails to "disclose channel doping that" forms a channel region "defined by the presence of additional dopant atoms" that contiguously extend from source to drain. Sur-Reply 6; *see supra* section II.A (for correct claim construction). Patent Owner concedes Tanaka forms an induced channel region "***in operation***." Resp. 33 (emphasis Patent Owner's).

For the above reasons, we find that a preponderance of the evidence supports Petitioner's view that Tanaka suggests a channel region formed "immediately contiguous to the source and drain regions." Ex. 1001, claim 1; Ex. 1005, Fig. 7A; Ex. 1019, 7–8 and Fig. 5.2. Accordingly, we find that Petitioner has demonstrated by a preponderance of the evidence that Tanaka renders obvious claim 1.

Claims 3–5, 11, and 13–15

Petitioner directs us to substantial evidence that Tanaka discloses or suggests each limitation of claims 3–15 (which depend from claim 1), independent claim 11, and claims 13–15 (which depend from claim 11). Pet. 53–65. Patent Owner does not contest that evidence, except to argue that Tanaka fails to disclose "a separately doped region" immediately contiguous to the source and drain regions (Resp. 46); *see generally id*. 29–46 (variations of the same argument). Patent Owner's arguments are unpersuasive because they are tethered to an incorrect construction of the claim phrase "a channel region formed in the semiconductor substrate." Ex. 1001, claims 1 and 11; *see supra* section II.A. Accordingly, we find that Petitioner has demonstrated by a preponderance of the evidence that Tanaka renders obvious claims 3–5, 11, and 13–15.

2. Asserted Obviousness in View of Tanaka and Ooka

Claims 6 and 16 depend from claims 1 and 11, respectively, and each recites "a layer of tungsten silicide formed on the top surface of the trenched gate electrode." Petitioner relies on Ooka as disclosing this claim feature. Pet. 32–35, 65–67. Ooka is concerned with providing "an improved semiconductor integrated circuit device adapted for increasing the operating speed." Ex. 1006, 2:19–21. According to Petitioner, "Ooka discloses a gate electrode that includes a layer of tungsten silicide formed on the top surface of the gate electrode." Pet. 65 (citing Ex. 1006, 4:65–5:11). Specifically, Ooka indicates that employing "a gate electrode having a structure of laminating a metal silicide film on a polycrystalline silicon film . . . or a gate electrode only made of a metal silicide film" was known to increase resistance to lower the operating speed of the circuit. Pet. 30 (quoting Ex. 1006, 1:34–44); *see* Ex. 1003 ¶¶ 73, 76 (Dr. Fair, explaining the disclosure of Ooka).

Petitioner argues that an ordinarily skilled artisan would have been led to include the tungsten silicide layer of Ooka on the gate electrode of Tanaka in order to "increase the device speed of the Tanaka transistor." *Id.* at 32–35, 66 (citing Ex. 1003 ¶¶ 75–86). Relying on testimony of Dr. Fair, Petitioner argues that it was "well known that lowering the resistance of the gate electrode would increase the speed of the device" and, further, that it was "also well known that including a layer of silicide, e.g., tungsten silicide, as the top portion of the polysilicon gate electrode would reduce the gate electrode resistance and increase device speed." *Id.* at 32–33 (citing Ex. 1003 ¶¶ 76–81; Ex. 1006, 1:34–44, 4:65–5:11); *see id.* at 33–34 (citing Ex. 1003 ¶¶ 77–81; Ex. 1005, 1:10–20, 1:34–44, 3:68–4:2) (observing that

disclosure in Tanaka would indicate to a person of ordinary skill in the art that Tanaka's gate would have high gate resistance, thus providing a desire to reduce the resistance); *see also* Reply 27 (citing Ex. 1003 ¶¶ 74–85).

Petitioner persuasively argues that a person of ordinary skill in the art would have had a high expectation of success because "such silicide layers were conventional in the art by at least mid-1980 and obtainable by conventional and compatible methods such as CVD."[7] Pet. 34 (citing Ex. 1003 ¶¶ 82–83; Ex. 1009). Dr. Fair states that the application of the tungsten silicide layer of Ooka on the polysilicon gate of Tanaka "is merely combining prior art elements (Tanaka's gate electrode and Ooka's tungsten silicide layer) according to known methods (*e.g.*, CVD, as Ooka describes) to yield predictable results (a gate with a tungsten silicide layer on top was a conventional device . . .)" (Ex. 1003 ¶ 83), "is merely the use of known technique" that "improves similar devices . . . in the same way" (*id.* ¶ 84), and "is merely applying a known technique . . . to a known device . . . ready for improvement . . . to yield predictable results" (*id.* ¶ 85). *See* Pet. 34–35.

Patent Owner does not meaningfully address the showing made by Petitioner, but instead directs our attention to Ooka's disclosure of an alternative use of the silicide to increase resistance against electrostatic discharge ("ESD"). Resp. 46–49; *see* Ex. 1006, 1:62–2:25 (Ooka's disclosure that ESD decreases by lowering the gate electrode resistance). As Petitioner points out, however, "the Petition relies on the portions of Ooka's disclosure in which the silicide layer decreases resistance." Reply 28 (citing Pet. 33 n.7); Pet. 33 n.7 (addressing Ooka's alternative use of silicide

[7] In this particular field of endeavor, "CVD" refers to chemical vapor deposition. *See, e.g.*, Resp. 51–52 (bridging sentence).

pertaining to ESD); Reply 28 (same). Dr. Fair expressly addressed Ooka's additional technique, explaining that, although "lowering the overall gate electrode resistance may also lower the ESD resistance (which for some applications is preferably high), other solutions exist to increase the ESD resistance if a particular application calls for a higher ESD resistance." Ex. 1003 ¶ 73 n.7; *see* Pet. 33 n.7 (same). Patent Owner's argument relating to formation of "silicides in a manner that increases ESD resistance" does not undercut Petitioner's showing that the application of Ooka's tungsten silicide layer on Tanaka's polysilicon gate of Tanaka would be understood to decrease ESD resistance and increase processing speed. Resp. 47. Evaluating Ooka for all that it teaches, we conclude that one skilled in the art would have recognized that the tungsten silicide layer would increase Tanaka's processing speed. Pet. 30 (quoting Ex. 1006, 1:34–44); *see* Ex. 1003 ¶¶ 73, 76 (Dr. Fair, explaining the disclosure of Ooka).

Patent Owner also (1) attacks the asserted references individually instead of addressing what they fairly disclose in combination; (2) relies on bare attorney argument that Ooka's silicide structures are "incompatible" with Tanaka's transistors; and (3) asserts that Dr. Fair formed his opinion by relying on evidence from "recent years." Resp. 48–50; *see* Reply 28 (for persuasive counterarguments). "One cannot show non-obviousness by attacking references individually where, as here," an assertion of unpatentability is "based on combinations of references." *In re Keller*, 642 F.2d 413, 426 (C.C.P.A. 1981). Conclusory attorney argument cannot take the place of evidence lacking in the record. *See, e.g., In re Geisler*, 116 F.3d 1465, 1470 (Fed. Cir. 1997); *In re De Blauwe*, 736 F.2d 699, 705 (Fed.

Cir. 1984). And Dr. Fair referred to "recent years" when quoting from Ooka's 1991 patent filing. Ex. 1003 ¶¶ 72, 78 (citing 1006, 1:34–44).

We credit Dr. Fair's testimony, discussed above, that a person of ordinary skill in the art would have been motivated to include the tungsten silicide layer of Ooka on the gate electrode of Tanaka. We are persuaded that Petitioner proves by a preponderance of the evidence that an ordinarily skilled artisan would have recognized the benefit of applying the tungsten silicide layer disclosed in Ooka to the gate electrode of Tanaka to improve processing speed. Accordingly, we determine that Petitioner carries its burden of showing by a preponderance of the evidence that the combined disclosures of Ooka and Tanaka renders obvious claims 6 and 16. On that basis, we find that claims 6 and 16 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Tanaka and Ooka.

F. Asserted Obviousness Based on Anderson

Petitioner asserts that claims 1, 3, 4, 11, 13, and 14 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Anderson. Pet. 5, 67–90. Patent Owner argues that Anderson does not teach "a doped channel region" and, therefore, "cannot establish that the claimed channel region is formed in the semiconductor substrate" as required by claims 1 and 11. Resp. 59. As explained above in our claim construction analysis, however, the challenged claims do not require a channel region that is formed by channel doping. *See supra* section II.A. That circumstance guides our analysis, set forth below, regarding the application of the prior art to the properly construed patent claims.

Independent Claim 1

As discussed in the Petition in more detail, the following table provides a summary of Petitioner's mapping of Anderson to the structural elements of claim 1.

Claim 1	**Anderson**
semiconductor transistor	"An extremely small minimum scaled Metal-Oxide-Semiconductor, MOS, transistor." Ex. 1007, at [57].
semiconductor substrate	semiconductor substrate 10 (p-type)
source region	doped region 12 (n-type) [on the left side of trench 4 in Figs. 1a and 1b]
drain region	doped region 12 (n-type) [on the right side of trench 4 in Figs. 1a and 1b]
trench	trench 4
trench-to-gate insulating layer	gate oxide layer 15 and gate oxide layer 17a
Trench gate electrode	gate electrode 18

See Pet. 67–73, 77–81 (citing Ex. 1007, at [57], 2:58–3:25, 4:2–15, 4:34–56, 5:10–25, Figs. 1a, 1b, 2, 4; Ex. 1003 ¶¶ 164, 167, 172, 180; Ex. 1001, 3:30–50). Patent Owner does not meaningfully dispute that the claim elements identified in the above table are met by the semiconductor transistor disclosed in Anderson. *See generally* Resp.

As discussed above with respect to the grounds based on Tanaka, claim 1 also includes a channel region limitation. Regarding that claim feature, Petitioner relies on "channel 5" disclosed in Anderson. Pet. 74–77; Ex. 1003 ¶¶ 174–177. For example, Petitioner points to disclosures in

Anderson that "[t]he channel is formed under the recess" (in which gate electrode 18 is later formed) (Pet. 75–76 (citing Ex. 1007, 2:27–41)) and "[t]he bottom of the N+ source/drain regions 12 next to channel 5 extend below the trench 4 on either side" (*id.* at 76 (citing Ex. 1007, 3:8–15)).

Patent Owner argues that Anderson's channel 5 is not a "doped channel region" within the meaning of the claims. Resp. 59. That argument, however, depends entirely on Patent Owner's erroneous view that claims 1 and 11 require a channel region defined by the presence of dopants. *See id.* at 56–60. For example, Patent Owner argues that "one of ordinary skill in the art would understand that the channel region 5 is nothing more than the p-doped substrate with the annealed source and drain on either side as opposed a separate and additional doped channel region relative to the semiconductor substrate as required by claims 1 and 11." *Id.* at 59 (citing Ex. 2007 ¶ 75). Similarly, Patent Owner states, "The Petition provides no other discussion or evidence to show that Anderson's channel region 5 is a doped channel region separately identifiable relative to the semiconductor substrate and, therefore, cannot establish that the claimed channel region is formed in the semiconductor substrate." *Id.* at 59 (citing Ex. 2007 ¶ 86). Because we are not persuaded by Patent Owner's arguments with respect to Patent Owner's proposed construction of the channel region limitation (*see supra* section II.A.), we also are not persuaded by arguments attempting to distinguish the claimed subject matter from Anderson's transistor based on that incorrect construction.

Based on our review of the arguments and evidence presented by the parties, we are persuaded that Petitioner has shown by a preponderance of the evidence that Anderson renders obvious claim 1.

Claims 3, 4, 11, 13, and 14

Petitioner directs us to substantial evidence that claims 3, 4, 11, 13, and 14 are obvious over Anderson. Pet. 81–90. Patent Owner does not meaningfully contest that evidence, except to argue that Anderson lacks a doped channel region that falls within the scope of the claims. Resp. 53–60. Here again, Patent Owner's counterarguments are unpersuasive because they are keyed to an incorrect claim construction. *See supra* section II.A. Accordingly, we determine that Petitioner has demonstrated by a preponderance of the evidence that Anderson renders obvious claims 3, 4, 11, 13, and 14. Pet. 81–90.

II. CONCLUSION

Petitioner has established by a preponderance of the evidence that: (1) claims 1, 3–5, 11, and 13–15 are unpatentable as obvious over Tanaka; (2) claims 6 and 16 are unpatentable as obvious over Tanaka and Ooka; and (3) claims 1, 3, 4, 11, 13, and 14 are unpatentable over Anderson.

III. ORDER

It is

ORDERED that each of claims 1, 3–6, 11, and 13–16 of the '061 patent is unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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