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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01563
Patent 6,103,611

Before GRACE KARAFFA OBERMANN, KRISTINA M. KALAN, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge.*

FINAL WRITTEN DECISION

Finding Claims 1–5, 8–12, and 15 Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–5, 8–12, and 15 of U.S. Patent No. 6,103,611 (Ex. 1001, "the '611 patent"). Paper 1 ("Pet."). Lone Star Silicon Innovations, LLC[1] ("Patent Owner") filed a Preliminary Response. Paper 6. We instituted an *inter partes* review of claims 1–5, 8–12, and 15 on all grounds of unpatentability alleged in the Petition. Paper 8 ("Institution Decision" or "Inst. Dec.").

After institution of trial, Patent Owner filed a Patent Owner Response. Paper 11 ("PO Resp."). Petitioner filed a Reply. Paper 14 ("Reply"). Patent Owner, with Board authorization, filed a Sur-Reply (Paper 16, "Sur-Reply"), to which Petitioner replied (Paper 22, "Reply to Sur-Reply"). An oral hearing was held on September 18, 2018. A transcript of the hearing is included in the record. Paper 28 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has established by a preponderance of the evidence that claims 1–5, 8–12, and 15 of the '611 patent are unpatentable.

A. Related Proceedings

The parties identify a number of proceedings as related, including: *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:17-cv-05458 (N.D. Cal. Oct. 7, 2016) (dismissed without prejudice) and *Lone*

[1] Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 4, 1.

Star Silicon Innovations, LLC v. Micron Technology, Inc., Appeal No. 2018-1578 (Fed. Cir. Feb. 15, 2018). Pet. 3, Paper 26, 2.

B. The '611 Patent

The '611 patent, titled "Methods and Arrangements for Improved Spacer Formation Within a Semiconductor Device," was filed December 18, 1997, and issued August 15, 2000. Ex. 1001, at [22], [45], [54]. The '611 patent relates to increasing the process control during the formation of spacers within a semiconductor device. *Id.* at [57].

As described in the '611 patent, a problem existed in the prior art in which uneven spacing between gate conductors could lead to spacers formed adjacent thereto having inconsistent widths, which "can have a deleterious effect on the semiconductor device being fabricated." *Id.* at 5:22–62.

Figure 2b of the '611 patent is reproduced below.

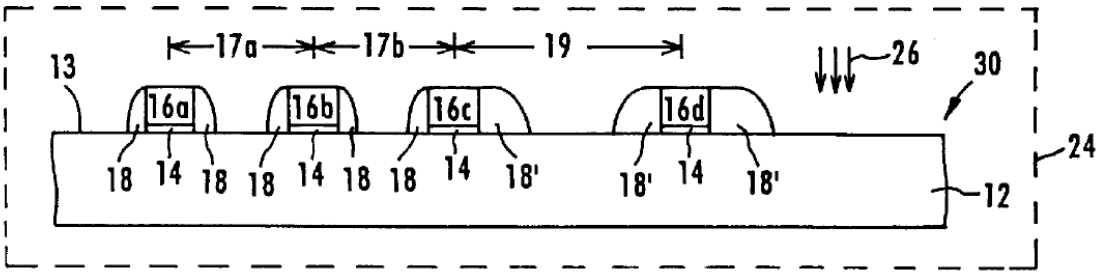


Fig. 2b (PRIOR ART)

Figure 2b, above, shows a portion of a prior-art semiconductor device following formation of spacers 18, 18'. *Id.* at 3:63–65. In the device of Figure 2b, gate conductors 16a, 16b, 16c, 16d are formed on substrate 12. *Id.* at 5:23–26. The center points of gate conductors 16a and 16b are separated by space 17a; the center points of gate conductors 16b and 16c are separated by space 17b; the center points of gate conductors 16c and 16d are

separated by space 19. *Id.* at 5:26–33. As seen in Figure 2b, space 19 is larger than spaces 17a and 17b. *Id.* at 5:31. As a result, "the spacers 18' formed within second space 19 are differently shaped and have a wider width at their base than the spacers 18 formed, for example, in first spaces 17a and 17b." *Id.* at 5:51–54.

In order to solve this problem, the '611 patent teaches using non-operational transistor gate arrangements to divide the larger space into more equal smaller spaces, "to provide more uniformity in the spaces/aspect ratios between gate conductors." *Id.* at 6:9–25.

Figures 4a and 4b of the '611 patent are reproduced below.

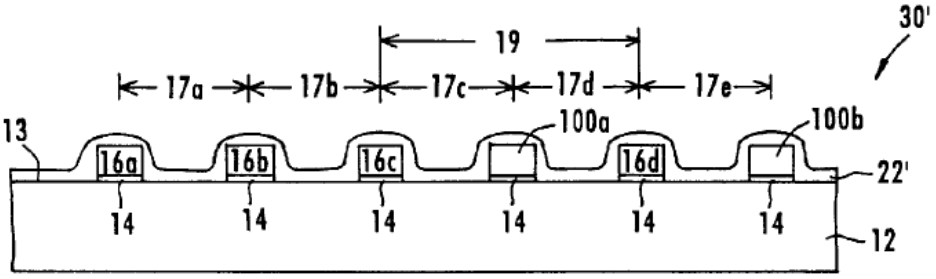


Fig. 4a

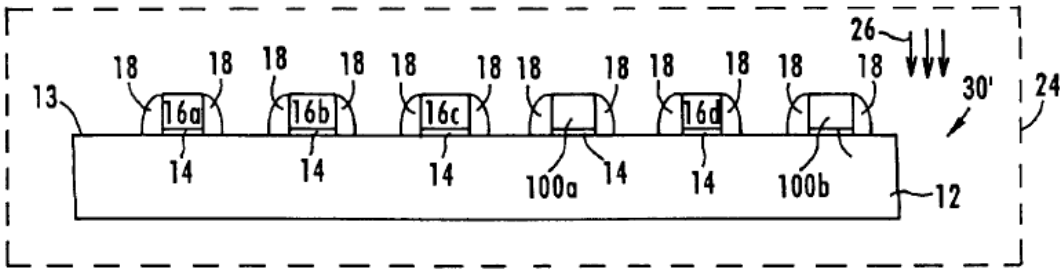


Fig. 4b

Figures 4a and 4b, above, show steps in a process for forming "substantially uniformly sized spacers" in a semiconductor device, in accordance with embodiments of the '611 patent. *Id.* at 4:3–13. In the device of Figure 4a, gate conductors 100a, 100b are formed on substrate 12, in addition to gate

conductors 16a, 16b, 16c, 16d previously described with respect to the prior art device of Figure 2b. *Id.* at 6:9–14. The addition of gate conductor 100a, for example, "effectively divide[s] second space 19 into two first spaces 17c and 17d, which are each substantially equivalent to first spaces 17a and 17b." *Id.* at 6:15–17. As described in the '611 patent, "[t]he result of adding these additional non-operational transistor gate arrangements is that the topology . . . has been altered to provide more uniformity in the spaces/aspect ratios between gate conductors." *Id.* at 6:21–25.

Shown in Figure 4a, dielectric layer 22' is deposited over substrate 12 and gate conductors 16a, 16b, 16c, 16d, 100a, 100b, using conventional processes. *Id.* at 6:26–30. Shown in Figure 4b, dielectric layer 22' is subjected to anisotropic etching plasma 26, resulting in the formation of spacers 18. *Id.* at 6:34–40. Due to the uniformity in the spaces/aspect ratios between gate conductors in this embodiment, spacers 18 "have substantially uniformly sized widths." *Id.* at 6:47–49. In turn, "the source and drain regions 20a and 20b [of the semiconductor device] (not shown in FIG. 4b) will be more uniformly shaped and sized." *Id.* at 6:49–51. Non-operational gate conductors 100a, 100b may be removed (*id.* at 6:52–63, Fig. 5a), or may remain in the complete semiconductor device (*id.* at 6:64–7:2).

C. Illustrative Claim

Of the challenged claims, claims 1, 8, and 15 are independent. Claims 2–5 depend, directly or indirectly, from claim 1, and claims 9–12

depend directly from claim 8. Independent claim 1 of the '611 patent is reproduced below, and is illustrative of the challenged claims.

> 1. A method for forming substantially uniformly sized spacers on transistor gate arrangements within semiconductor devices on a common substrate, the method comprising:
>
> forming a plurality of gate arrangements on a top surface of the substrate, wherein two of the plurality of gate arrangements are positioned parallel to one another and separated by a defined space;
>
> forming a dielectric layer over at least a portion of the two gate arrangements and at least a portion of the defined space;
>
> removing portions of the dielectric layer to form a plurality of spacers, wherein each of the plurality of spacers physically contacts one of the two gate arrangements and the substrate, and wherein the spacers located within the defined space each have a base width that is approximately the same;
>
> configuring one of the two gate arrangements to control an electrical current between a source region and a drain region formed in the substrate; and
>
> configuring the remaining one of the two transistor gate arrangements to be non-operational.

Ex. 1001, 7:65–8:18.

D. Instituted Grounds of Unpatentability

Petitioner relies on the following references. Pet. 4–5.

Reference	**Publication Date/ Issue Date**	**Exhibit**
JP Pub. No. H2-37725 ("Yonemaru")	Feb. 7, 1990	Ex. 1005
U.S. Patent No. 5,019,527 ("Ohshima")	May 28, 1991	Ex. 1006
U.S. Patent No. 5,410,161 ("Narita")	Apr. 25, 1995	Ex. 1007

Petitioner also relies on the Declarations of Sanjay Banerjee, Ph.D. (Ex. 1003, Ex. 1031) to support its positions. Patent Owner relies on the Declarations of W. R. Bottoms, Ph.D. (Ex. 2001; Ex. 2008) to support its positions.

We instituted an *inter partes* review of claims 1–5, 8–12, and 15 of the '611 patent on ground of whether claims 1–5, 8–12, and 15 would have been obvious under 35 U.S.C. § 103(a) in view of Yonemaru, Ohshima, and Narita. Inst. Dec. 23.

II. ANALYSIS

A. Claim Construction

The parties agree that the '611 patent expired during this proceeding, and that the claim construction principles outlined in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) apply. Pet. 16; PO Resp. 6; *see also* Inst. Dec. 8–9 (calculating expiration date of December 18, 2017). Because the parties agree that the '611 patent has expired and, thus, the claim construction standard set forth in *Phillips* should apply, we adopt a district court-type claim construction approach for purpose of this Decision. 37 C.F.R. § 42.100 (2016); *cf. In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) ("[T]he Board's review of the claims of an expired patent is similar to that of a district court's review."); *see also Black & Decker, Inc. v. Positec USA, Inc.*, 646 F. App'x 1019, 1024 (Fed. Cir. 2016) (holding that in an *inter partes* review, "[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]").

Under the *Phillips* standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary

skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

Petitioner indicates that "[a]ll claim terms have been accorded their plain and ordinary meaning as understood by a [person of ordinary skill in the art] and consistent with the intrinsic record." Pet. 16. Patent Owner "agrees with Petitioner[] that all claim terms should be accorded their plain and ordinary meaning as understood by a person having ordinary skill in the art and as consistent with the intrinsic record." PO Resp. 6. We do not construe any claim terms for purposes of this Decision. *See, e.g.*, *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("[C]laim terms need only be construed 'to the extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999)).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art "would be a person with at least a Bachelor of Science degree in electrical engineering or physics, or a closely related field, with at least 5 years of experience in semiconductor fabrication." Pet. 17 (citing Ex. 1003 ¶¶ 18–19). Petitioner also proposes that "[a]n individual with an advanced degree in a relevant field would require less experience in semiconductor fabrication." *Id.* (citing Ex. 1003 ¶¶ 18–19).

Patent Owner asserts that a person of ordinary skill in the art "would have held a master's degree in physics, electrical engineering or a related field and three years or more experience working with the technologies

implemented in semiconductor devices and the fabrication of semiconductor devices." PO Resp. 5 (citing Ex. 2001 ¶ 29).

In our Institution Decision, we noted the parties' proposals differed only in the specific number of years of experience in semiconductor fabrication, and that neither party argues this distinction makes a difference in analyzing the asserted ground. Inst. Dec. 10–11. For the purposes of our Institution Decision, we accepted Petitioner's contentions regarding the level of ordinary skill in the art. *Id.*

Patent Owner, in its Response, emphasizes that its proposal differs from Petitioner's proposal in that it indicates a master's degree requirement, in the specific number of years of experience in semiconductor fabrication, and in that experience in technologies implemented in semiconductor devices is required. PO Resp. 5–6 (citing Inst. Dec. 11).

Petitioner replies that the Board "acknowledged, however, that [Petitioner's] proposal states that a POSITA may have an advanced degree but less experience than a POSITA with an undergraduate degree," and that the parties "actually agree" about "whether a POSITA would have had design experience to understand 'technologies implemented in semiconductor devices.'" Reply 24–25.

We agree with Petitioner that the parties' respective positions are not substantially different. In light of the evidence before us, we adopt Petitioner's definition of one of ordinary skill in the art. The record reflects no reason to require that one of ordinary skill in the art have a master's degree when a Ph.D. degree with fewer years of work experience or a Bachelor's degree with more years of work experience would suffice. We also find that Petitioner's proposed level of skill in the art is reflected by the

references themselves. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) ("[T]he absence of specific findings on the level of skill in the art does not give rise to reversible error 'where the prior art itself reflects an appropriate level and a need for testimony is not shown.'"); *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (finding that the Board of Patent Appeals and Interferences did not err in concluding that the level of ordinary skill in the art was best determined by the references of record). In any event, neither party argues that the outcome of this case would differ based on our adoption of one party's definition over the other. PO Resp. 5–6; Reply 24–25.

C. Overview of the Asserted References

1. Yonemaru (Ex. 1005)

Yonemaru relates to a manufacturing method for a semiconductor device. Ex. 1005, 1. In particular, Yonemaru describes forming a plurality of transistors, each having the same characteristics, by forming side walls (or, in other words, spacers) having the same shape at the sides of each gate electrode. *Id.* at 2. Yonemaru accomplishes this by using dummy gate electrodes between the gate electrodes. *Id.*

The manufacturing process of Yonemaru is discussed in more detail with respect to Figures 1(A)–1(E). Figure 1(A) is reproduced below.

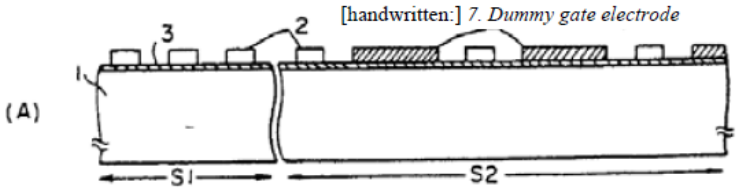


Figure 1(A), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* Gate electrodes 2 and dummy gate electrodes 7 are formed over gate oxide film 3

on semiconductor substrate 1. *Id.* As described in Yonemaru, the spacing between gate electrodes 2 may be 0.9 μm in closely spaced portion S1 and 4.5 μm in widely spaced portion S2. *Id.* "[D]ummy gate electrode 7 is positioned in such a way as to intervene between gate electrodes 2 at widely spaced portion S2, and furthermore is positioned such that its distance from gate electrodes 2 is 0.9μm, or the distance between gate electrodes 2 at closely positioned portion S1." *Id.* Yonemaru notes that "dummy gate electrode 7 . . . serves no purpose in the semiconductor integrated circuit, and is not used as wiring." *Id.* at 3.

After formation of source/drain zone 5 (*see id.* at Fig. 1(B)), a PSG (Phospho Silicate Glass) film, for example, is deposited over the entire surface (*id.* at 2–3), as seen in Figure 1(C), reproduced below.

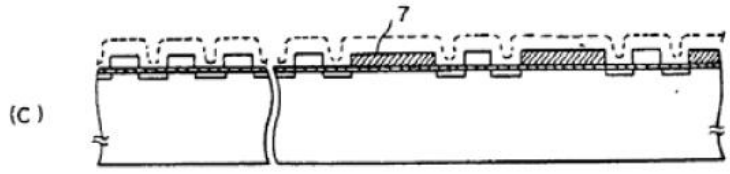


Figure 1(C), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* at 2. As seen in Figure 1(C), the "placement of a dummy gate electrode 7 causes PSG film to be deposited in the same shape at closely spaced portion S1 and widely spaced portion S2." *Id.* at 3.

Figure 1(D) is reproduced below.

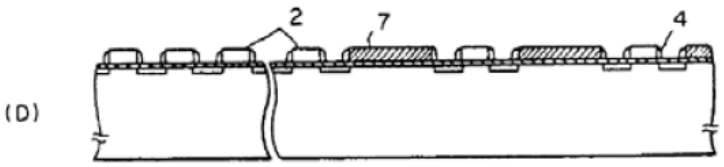


Figure 1(D), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* at 2. As shown in Figure 1(D), side walls 4 are formed at the sides of gate electrodes 2 and dummy gate electrodes 7, by anisotropically etching the PSG film. *Id.* at 3. "Because PSG film has already been deposited in the same shape at both the closely and widely spaced portions S1 and S2 during the above-described process, side wall 4 is also formed to the same shape." *Id.* Source/drain zone 6 (*see id.* at Figure 1(E)) is subsequently formed. *Id.*

2. Ohshima (Ex. 1006)

Ohshima relates to a method of forming semiconductor memories. Ex. 1006, at [57]. In relevant part, Ohshima teaches removing portions of oxide film 2 between gate structures, such that corresponding portions of substrate 1 are exposed. *See id.* at 5:43–50, Figs. 3D, 4C, 5C. Ohshima forms its sidewalls by depositing silicon dioxide via CVD and etching via reactive ion etching. *Id.* at 5:63–6:14.

3. Narita (Ex. 1007)

Narita relates to a semiconductor device having dummy transistors and regular transistors. Ex. 1007, at [57]. In relevant part, Narita discloses a semiconductor device including gate electrode 4, dummy gate electrodes 5, contact holes 8, diffused layers 6 serving as source/drain regions, and aluminum interconnection layers 9 connected with gate electrode 4 and diffused layers 6.[2] *Id.* at 2:36–44, Figs. 2A, 2B. Whereas Narita Figure 2A shows contact hole 8 for providing a connection to gate electrode 4, no such contact holes are shown for dummy gate electrodes 5. *See id.* at Fig. 2A.

[2] Narita's use of reference numeral 8 to refer to the diffused layers appears to be a typographical error. Ex. 1007, 2:44.

Dr. Banerjee explains that the connection to aluminum interconnection layers 9 is "what allow[s] the gate electrode to receive power and control signals." Ex. 1003 ¶ 58; Pet. 24 (citing Ex. 1003 ¶ 58).

D. Analysis

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We note that, during this proceeding, the parties did not direct our attention to any objective evidence of non-obviousness.

In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). A prima facie case of obviousness is established when the prior art, itself, would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. *See In re Rinehart*, 531 F.2d 1048, 1051 (CCPA 1976).

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent

Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Petitioner must demonstrate obviousness by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). A party that petitions the Board for a determination of obviousness must show that "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so." *Procter & Gamble Co. v. Teva Pharm. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (quoting *Pfizer, Inc. v. Apotex, Inc.*, 408 F.3d 1348, 1361 (Fed. Cir. 2007)). We analyze both parties' arguments, below, in accordance with the above-stated principles.

1. Petitioner's Arguments for Independent Claims 1, 8, and 15

Petitioner challenges each of claims 1–5, 8–12, and 15 as being unpatentable under 35 U.S.C. § 103 as obvious in view of Yonemaru, Ohshima, and Narita. Pet. 4–5, 25–66.

Claim 1 recites a "method for forming substantially uniformly sized spacers on transistor gate arrangements within semiconductor devices on a common substrate." Petitioner contends that Yonemaru teaches forming side walls 4 (i.e., spacers) in a manner such that "'side walls with the same shape,' *i.e.*, of the same size and width, 'can be formed at the side wall portion of all gate electrodes when subsequently performing anisotropic etching.'" Pet. 26–27 (quoting Ex. 1005, 3); *see id.* at 25–27 (citing Ex. 1005, 2–3, Figs. 1(A), (D); Ex. 1003 ¶¶ 62–64).

Claim 1 further recites "forming a plurality of gate arrangements on a top surface of the substrate, wherein two of the plurality of gate arrangements are positioned parallel to one another and separated by a defined space." For this claim step, Petitioner points to gate electrodes 2 and dummy gate electrodes 7 of Yonemaru. *Id.* at 27 (citing Ex. 1005, 2; Ex. 1003 ¶ 67). Petitioner further points to Figure 1(A) of Yonemaru, in which, according to Petitioner, "the gate electrodes 2 and dummy gate electrodes 7 are arranged in parallel to one another and consistently separated by the same distance, which in one embodiment is 0.9μm." *Id.* at 28 (citing Ex. 1005, 2; Ex. 1003 ¶¶ 68–70).

The method of claim 1 further includes "forming a dielectric layer over at least a portion of the two gate arrangements and at least a portion of the defined space." For this claim step, Petitioner points to Figure 1(C) of Yonemaru, and Yonemaru's disclosure of depositing PSG film over the entire surface. *Id.* at 29 (citing Ex. 1005, 3; Ex. 1003 ¶ 73). Petitioner contends that PSG is a dielectric. *Id.* at 30 (citing Ex. 1003 ¶ 74; Ex. 1019, 4).

Claim 1 next recites "removing portions of the dielectric layer to form a plurality of spacers, wherein each of the plurality of spacers physically contacts one of the two gate arrangements and the substrate, and wherein the spacers located within the defined space each have a base width that is approximately the same." For this step, Petitioner points to Yonemaru's disclosure of anisotropically etching away portions of the PSG film to form side walls 4. *Id.* at 31 (citing Ex. 1005, 3). Petitioner notes that both side walls 4 physically contact the electrodes and extend into the spaces between the electrodes, because side walls 4 are formed on the side wall portions of

electrodes 2, 7. *Id.* (citing Ex. 1005, 3; Ex. 1003 ¶¶ 77–80). As noted above, Yonemaru teaches side walls 4 are formed "to the same shape," or in other words, have the same width, as claimed. *Id.* (citing Ex. 1003 ¶¶ 84–85).

Petitioner admits that side walls 4 of Yonemaru are separated from the substrate by gate oxide film 3, but argues that "it would have been obvious to a [person of ordinary skill] . . . to apply Ohshima's teaching to Yonemaru to remove the excess gate oxide film 3 in Yonemaru." *Id.* at 32 (citing Ex. 1003 ¶¶ 81–83). Petitioner continues, "[t]he side walls 4 formed in subsequent steps would then directly contact the semiconductor substrate 1." *Id.* (citing Ex. 1003 ¶¶ 81–83).

Petitioner provides reasons that a person of ordinary skill in the art "would have been motivated to apply Ohshima's teaching to Yonemaru to remove the exposed portions of gate oxide film 3 during the gate formation step." Pet. 60. First, according to Petitioner, "a [person of ordinary skill in the art] would have recognized that etching away the exposed gate oxide presents an additional benefit, in that the gate oxide would not interfere with the ion implantation steps used to form source and drain regions." *Id.*; *see id.* at 60–61 (citing Ex. 1003 ¶ 191; Ex. 1011, 6; Ex. 1012, 8; Ex. 1013, 4; Ex. 1015, 6–7) (providing additional details on this point). Second, Petitioner contends that a person of ordinary skill "would have been choosing from a finite number of identified, predictable means for forming transistor gate electrodes and associated source/drain regions, with a reasonable expectation of success." *Id.* at 61. In particular, Petitioner identifies what it contends are two identified and well-known methods of forming gate electrodes—namely, leaving the gate oxide intact when etching

the polysilicon into gates, or etching both the polysilicon and the gate oxide during gate formation. *Id.* at 61–62 (citing Ex. 1003 ¶¶ 192–194; Ex. 1005, 2; Ex. 1006, 5:43–50, Figs. 4A, 4B; Ex. 1007, 3:19–25; Ex. 1008 ¶ 2, Fig. 1; Ex. 1009, 6; Ex. 1018, 26; Ex. 1001, 5:3–16, Fig. 2b).

Finally the method of claim 1 requires "configuring one of the two gate arrangements to control an electrical current between a source region and a drain region formed in the substrate" and "configuring the remaining one of the two transistor gate arrangements to be non-operational." For the operational gates, Petitioner points to Yonemaru's teaching of source/drain zones 5, 6 (Ex. 1005, 3, Fig. 1(E)), noting that the formation of these zones "suggests that the gate electrodes 2 are provided to control the flow of current between these zones." Pet. 34–35 (citing Ex. 1003 ¶ 89). Petitioner relies on Narita as providing express disclosure of connecting gate electrodes to a voltage source, thus, configuring gate electrodes to control the electrical current between source and drain regions. *Id.* at 35–37 (citing Ex. 1007, 2:36–44, Figs. 2A, 2B; Ex. 1003 ¶¶ 89–92; Ex. 1016, 6; Ex. 1017, 6). For the non-operational gates, Petitioner notes that Yonemaru expressly discloses that dummy gate electrodes 7 "serve[] no purpose in the semiconductor integrated circuit, and [are] not used as wiring." Ex. 1005, 3; Pet. 38 (citing Ex. 1003 ¶ 95). Petitioner contends that Narita teaches making the dummy gate electrodes non-operational by not connecting them to interconnection layers. Pet. 38–39 (citing Ex. 1007, 2:36–44, Fig. 2A; Ex. 1003 ¶¶ 96–98). Thus, according to Petitioner, the proposed combination of Yonemaru, Ohshima, and Narita teaches non-operational dummy gates. *Id.* at 39–40 (citing Ex. 1003 ¶ 99).

Petitioner provides reasons that a person of ordinary skill in the art "would have been motivated to apply Narita's teachings to Yonemaru to connect the gate electrodes 2, but not the dummy gate electrodes 7, of Yonemaru to aluminum interconnection layers as taught in Narita." *Id.* at 62. First, Yonemaru teaches that gate electrodes 2 are for forming MOS transistors (Ex. 1005, 1–3), and Petitioner contends that a person of ordinary skill in the art "would have understood that a MOS transistor gate controls current flow between drain and source regions based on the voltage applied to the gate." Pet. 63 (citing Ex. 1003 ¶ 196; Ex. 1018, 7). According to Petitioner, a person of ordinary skill in the art would have had a reasonable expectation of success in using the conventional metal interconnection layers of Narita in Yonemaru. *Id.* (citing Ex. 1003 ¶ 196; Ex. 1016, 6; Ex. 1017, 6). Similarly, Yonemaru teaches that dummy electrode 7 "serves no purpose in the semiconductor integrated circuit, and is not used as wiring" (Ex. 1005, 3), and Petitioner contends that a person of ordinary skill in the art "would have . . . ensure[d] that the dummy gate electrodes 7 were disabled from functioning." Pet. 63–64 (citing Ex. 1003 ¶ 196). According to Petitioner, a person of ordinary skill in the art would have had a reasonable expectation of success in not connecting Yonemaru's dummy electrodes to the metal interconnection layers, as taught in Narita. *Id.* at 64 (citing Ex. 1003 ¶ 196).

Petitioner further contends that its proposed "combination [of Narita with Yonemaru] combines prior art elements according to known methods to yield predictable results." *Id.* (citing Ex. 1003 ¶ 197); *see id.* at 64–65 (citing Ex. 1003 ¶ 197; Ex. 1005, 2; Ex. 1007, 3:10–49; Ex. 1009, 6–16; Ex. 1016, 6; Ex. 1017, 6; Ex. 1018, 5–8) (providing additional details on this point). Petitioner also asserts that its proposed "combination [of Narita with

Yonemaru] applies a known technique to a known device [(Yonemaru's semiconductor device)] ready to be completed, as taught in Narita, to yield predictable results" of "connecting Yonemaru's gate electrodes to a power supply through Narita's metal interconnection layers." *Id.* at 65–66 (citing Ex. 1003 ¶ 198; Ex. 1005, 2–3; Ex. 1007, 2:36–44, 3:10–49; Ex. 1016, 6; Ex. 1017, 6).

Regarding independent claims 8 and 15, Petitioner relies on similar arguments and evidence as presented with respect to claim 1. *See* Pet. 45–51, 53–60; Ex. 1003 ¶¶ 91, 115–117, 120–129, 131–143, 152–154, 156, 157, 160–163, 168–170, 173–177, 179–189, 195–200.

2. Patent Owner's Arguments for Independent Claims 1, 8, and 15

Patent Owner's Response, in addressing claim 1, presents two primary arguments against Petitioner's asserted grounds—that Petitioner's proposed modification of Yonemaru renders Yonemaru unsatisfactory for its intended purpose (PO Resp. 14–27), and that the combination does not result in the claimed invention (*id.* at 27–29). Patent Owner also argues that claims 8 and 15 "are not obvious for the same reasons as claim 1." *Id.* at 29.

Patent Owner argues that Petitioner's proposed modification, i.e., removing the gate oxide layer between the side walls and the substrate, would render Yonemaru unsatisfactory for its intended purpose such that one of ordinary skill in the art would not have a reasonable expectation of success. PO Resp. 15. First, Patent Owner argues that one of ordinary skill in the art would recognize that the gate oxide layer between the side walls and the substrate in Yonemaru serves a crucial function. PO Resp. 16. More particularly, Patent Owner argues that "Yonemaru discloses only two materials for forming side walls: PSG and phosphorus-doped

polycrystalline silicon." *Id.* When these phosphorous-doped materials "are in physical contact with silicon substrate," Patent Owner argues, "the phosphorus impurity is known to migrate into the substrate through diffusion." *Id.* Moreover, argues Patent Owner, the oxide layer functionally serves as a phosphorus barrier layer and, in the absence of the oxide layer acting as a phosphorous barrier, "uncontrolled rapid phosphorus diffusion would occur" while forming Yonemaru's source and drain by ion implantation and thermal diffusion of arsenic. *Id.* at 17.

Next, Patent Owner argues that removing the exposed gate oxide layer in Yonemaru would render Yonemaru unsuitable for its intended purpose, namely, "to form a MOS-type semiconductor with lightly doped drain (LDD) structures that 'prevent the short channel effect and punch through phenomenon, as well as to reduce parasitic capacitance by minimizing overlap of the source/drain zone and gate electrodes.'" PO Resp. 18, 21 (citing Ex. 1005, 1). According to Patent Owner, if the barrier oxide layer were to be removed from Yonemaru under the sidewalls, "Petitioner's proposed modification of Yonemaru's disclosed process would lead to uncontrolled diffusion of phosphorus, change the dopant concentration of the substrate, and negatively affect the functionality and reliability of the resulting transistor." *Id.* at 22–23 (citing Ex. 2001 ¶ 48).

Regarding whether the proposed modification of Yonemaru would result in the claimed invention, Patent Owner takes issue with Petitioner's contention that "[t]o the extent that Yonemaru does not disclose that the side walls 4 physically contact the substrate because they are separated from the substrate by the gate oxide film 3," it would have been obvious to one of ordinary skill in the art, "to apply Ohshima's teaching to Yonemaru to

remove the excess gate oxide film 3 in Yonemaru by the same anisotropic etching that is used to form the **side walls 4**." PO Resp. 27 (quoting Pet. 32) (modifications by Patent Owner). Patent Owner contends that Petitioner's proposed modification would require "several extra steps . . . to add a second set of sidewalls after removing the first set of sidewalls." *Id.* at 28.

3. Petitioner's Reply Arguments

Petitioner replies that Patent Owner's unsatisfactory-for-its-intended-purpose argument fails because it is based on the false premise that the Yonemaru combination requires phosphorus sidewalls. Reply 5. First, Petitioner argues, Yonemaru would have been understood to disclose non-phosphorus sidewall materials, because "(1) Yonemaru focuses on the function and shape of the sidewall (i.e., to serve as a mask for ion implantation), not on the specific type of material that is used to form it; (2) Yonemaru discloses no process steps for which phosphorus or any other dopant in the sidewall is necessary"; and "(3) Yonemaru provides non-limiting examples of sidewall materials." *Id.* at 6. Regarding the first argument, Petitioner elaborates, Yonemaru's "sidewall material . . . is irrelevant so long as it performs the masking function." *Id.* Regarding the second argument, Petitioner argues that Yonemaru does not disclose that use of PSG as a material for the side walls is important to the process disclosed therein. *Id.* at 7. Regarding the third argument, Petitioner maintains that Yonemaru's references to phosphorus-sidewall materials such as PSG are "merely exemplary, not essential." *Id.* at 8. Next, Petitioner argues that Ohshima expressly discloses silicon dioxide as the sidewall material, and one of ordinary skill in the art would have had a reasonable expectation of success using this sidewall in place of Yonemaru's PSG sidewall, because

both are used to fabricate LDD structures using a similar, well-known, and routine process. *Id.* at 9–10. Finally, Petitioner argues that other well-known sidewall materials were known to be suitable for the Yonemaru combination, such as silicon dioxide or TEOS oxide. *Id.* at 10.

Petitioner also replies that Patent Owner's unsatisfactory-for-its-intended-purpose argument fails because it was well known in the prior art how to control phosphorus diffusion when forming LDD regions. *Id.* at 11. According to Petitioner, Patent Owner ignores that selection of the phosphorus material and process conditions control phosphorus diffusion. *Id.* at 11–12. Petitioner argues that none of the references on which Patent Owner relies shows or suggests that the combination's phosphorus sidewalls would require a "barrier layer" under the sidewalls. *Id.* at 13. Next, Petitioner argues that an oxide layer does not necessarily prevent phosphorus diffusion and thus cannot be presumed to function as a barrier, and that controlling phosphorus diffusion without an oxide layer was well known in the art. *Id.* at 15–19 (relying on Ex. 1026 (Foster); Ex. 1027 (Ono); Ex. 1031 ¶¶ 55–59). Finally, Petitioner argues that controlling phosphorus diffusion without an oxide layer can create LDD devices that are satisfactory for Yonemaru's intended purpose. *Id.* at 20–21 (citing Ex. 1031 ¶¶ 60–65).

Regarding Patent Owner's not-the-claimed-invention argument, Petitioner argues that Patent Owner's argument mischaracterizes the Petition, in that the "same anisotropic etching" portion of the Petition quoted by Patent Owner refers to the type of etching, not to a particular etch step. *Id.* at 22 (citing Pet. 32, 60; Ex. 1031 ¶ 67).

4. Patent Owner's Sur-Reply Arguments

In its Sur-Reply, Patent Owner argues that the Reply improperly modifies the asserted ground. Sur-Reply 1. More particularly, Patent Owner argues that "the ground asserted in the Petition [is]: that the Yonemaru combination would have PSG sidewalls as disclosed in Yonemaru," and that the Petition "confirms that no modification of the sidewall material was intended." *Id.* Thus, Patent Owner argues, Petitioner's argument that the sidewall material or process of Yonemaru could be modified is "new and improperly shift the basis of the ground asserted in the Petition." *Id.* at 2, 3. Additionally, Patent Owner alleges that Petitioner fails to provide a reason that one of ordinary skill in the art would have been motivated to make the alleged substitution of the sidewall material. *Id.* at 4.

In addition, Patent Owner argues that Petitioner also presents the new argument "that a POSA would have selected process conditions to avoid significant phosphorous diffusion that would occur if the gate oxide layer between gates were removed." *Id.* Patent Owner relies on Dr. Bottoms's opinion that "such control would require extensive experimentation due to three independent sources of dopants in Yonemaru." *Id.* at 4–5 (citing Ex. 2008 ¶¶ 9–10). Patent Owner criticizes Petitioner's reliance on Foster and Ono as failing to suggest that one of ordinary skill in the art would be motivated to modify Yonemaru to introduce another doping source. *Id.* at 5–6. Patent Owner also criticizes Petitioner's reliance on Dr. Banerjee's "hypothetical process" that it alleges "relies upon new prior art for support" and "fails to show that phosphorus diffusion would not be an issue when

Yonemaru is modified solely to remove the gate oxide layer as proposed in the Petition." *Id.* at 6–7 (citing Ex. 1031 ¶¶ 61–65; Ex. 2008 ¶¶ 13–14.)

5. Petitioner's Reply to Sur-Reply Arguments

In its reply to Patent Owner's Sur-Reply, Petitioner argues that its Reply properly rebuts Patent Owner's Response. Reply to Sur-Reply 1. Petitioner maintains that "the Reply asserts only what the Petition disclosed (Yonemaru, Ohshima, and the state of art)" and "nothing about [Petitioner's reply arguments is inconsistent with Yonemaru because Yonemaru discloses PSG merely as an exemplary material." *Id.* at 4.

Petitioner also argues that one of ordinary skill in the art would have been motivated to use undoped sidewalls if phosphorus diffusion were an issue, which Petitioner maintains is not. *Id.* at 4–5. More particularly, Petitioner argues, the "Petition and Reply establish that the selection of a sidewall material, either with or without underlying oxide, is simply a choice from 'a finite number of identified, predictable means.'" *Id.* at 5 (quoting Pet. 61, Reply 5–11).

Finally, Petitioner argues that one of ordinary skill in the art would have been motivated to remove Yonemaru's gate oxide layer. *Id.* More particularly, Petitioner argues that neither Patent Owner nor Dr. Bottoms "denies that Dr. Banerjee's straight-forward example of controlling phosphorus diffusion using textbook equations would, in fact, control diffusion even if the oxide were removed." *Id.* at 6.

6. Discussion

Having considered the arguments and evidence of record in the complete record before us, we find persuasive Petitioner's showing, as summarized above, that the combination of Yonemaru, Ohshima, and Narita

teaches the limitations of independent claims 1, 8, and 15, and that one of ordinary skill in the art would have been motivated to combine the references in the manner proposed by Petitioner, with a reasonable expectation of success. We are persuaded by Petitioner's arguments and reasoning as to the disclosure of the limitations by the prior art references and the reasons to combine them.

As Petitioner noted at the oral hearing, "there's really a single claim limitation at issue here," namely, the claim 1 limitation "wherein each of the plurality of spacers physically contacts . . . the substrate." Tr. 96:20–97:1; Ex. 1001, 8:9–11; *see also* PO Resp. 14. In view of this, we discuss the arguments and evidence of record with more particularity below.

i. Yonemaru Allegedly Unsatisfactory for its Intended Purpose

The Petition presented explanation and reasoning that the proposed combination discloses the limitation "wherein each of the plurality of spacers physically contacts . . . the substrate." Pet. 31–34; *see supra* Section II.D.1. In the Reply, addressing Patent Owner's Response arguments, Petitioner expounds on its explanation and reasoning for this limitation, summarizing: "(1) Yonemaru discloses phosphorus-containing sidewalls merely as an exemplary sidewall material, (2) the diffusion would not be uncontrolled even if the sidewalls were made from a phosphorus-containing material, and (3) the Petition clearly explains that the Yonemaru combination does not include oxide beneath its sidewalls." Reply 4.

Regarding the first enumerated item, we are persuaded that Yonemaru's identification of PSG as a sidewall material was exemplary, rather than fixed or unalterable. *Id*.; Ex. 1005, 1 ("a designated quantity of, *e.g.*, PSG (Phospho Silicate Glass) film is deposited") (emphasis added), 3

("PSG film, *for example*, is deposited") (emphasis added); *id.* ("Furthermore, this invention is not limited to these embodiment examples, and may be altered variously within the scope of this invention."). Nothing in Yonemaru's discussion of PSG or other sidewall materials indicates that any particular sidewall material is important to the process disclosed therein. Rather, Yonemaru appears to be directed to the importance of the shape of the side walls 4, rather than the material from which they are formed. *See* Ex. 1005, 2 ("Moreover, the *shape of side wall 4*, in particular the width, determines the width of the low-concentration diffusion layer 5, and the width of this low-concentration diffusion layer 5 *determines the transistor characteristics*.") (emphases added); *id.* ("The objective of this invention is to provide a manufacturing method for semiconductor device that, while forming of a plurality of transistors on a semiconductor substrate, is able to form transistors with the same characteristics *by forming side walls with the same shape* at the side wall portion of each gate electrode of these transistors, even if the design is such that this group of transistors is clustered at a certain portion and interspersed as another portion.") (emphasis added).

Taken as a whole, Yonemaru does not require use of PSG, or even "phosphorus-doped polycrystalline silicon film," another material mentioned as a PSG alternative. *Id.* at 3. Rather, as Petitioner has shown, the sidewall material may be PSG, phosphorus-doped polycrystalline silicon film, or another material "within the scope of the invention" (*id.*), such as Ohshima's undoped silicon dioxide (Reply 9–10 (citing Ex. 1006, 5:63–6:14; Ex. 1031 ¶ 36)), or TEOS oxide (Reply 10–11 (citing Ex. 1031 ¶¶ 30–36)). Petitioner also shows that one of ordinary skill in the art would have been motivated by

Yonemaru itself, Ohshima, and/or well-known prior art to substitute, for example, an undoped, non-phosphorus-containing material as the material for the sidewall spacers in Yonemaru, with a reasonable expectation of success. Reply 9–11 (citing Ex. 1031 ¶¶ 30–36). As Petitioner notes, use of such alternative materials would obviate the alleged phosphorus diffusion problem raised by Patent Owner. Reply 11.

We have considered Patent Owner's arguments presented in the Response (*supra* Section II.D.2) and in the Sur-Reply (*supra* Section II.D.4), which are directed to the timeliness and quality of Petitioner's Reply arguments. As we discuss below, however, we do not find the Reply arguments to be improper. *See infra* Section II.D.6.iii. Regarding the motivation to combine articulated by Petitioner, we are persuaded that the choice of sidewall material in Yonemaru is a matter of selecting a material from a finite number of predictable alternatives, as Petitioner argued in its Reply and its Reply to Sur-Reply. *See* Reply to Sur-Reply 5 (citing Ex. 1033, 40:15–41:7); Reply 5–11 (citing Ex. 1031 ¶¶ 30–36).

Even if Yonemaru were read to require the sidewalls to be made of PSG or phosphorus-doped polycrystalline silicon film, which we do not read Yonemaru to require, we are persuaded by Petitioner's arguments that use of such materials would not present the phosphorus diffusion problem posed by Patent Owner. Reply 11–21. In the Petition, as discussed above, Petitioner provides persuasive reasons that a person of ordinary skill in the art "would have been motivated to apply Ohshima's teaching to Yonemaru to remove the exposed portions of gate oxide film 3 during the gate formation step." Pet. 60–62; *see supra* Section II.D.1. As further discussed by Petitioner in the Reply, "it was well known that phosphorus diffusion—with or without

an underlying oxide layer—can be controlled and that such control is a matter of process conditions." *Id.* at 11 (citing Ex. 1026, Fig. 3, 2:34–39; Reply Section II.B.3). Based on the evidence and arguments presented by Petitioner, and because Yonemaru does not appear to place restrictions on the concentration of phosphorus or the temperature of the anneal step, we find that one of ordinary skill in the art would have understood that "Yonemaru's process is suitable for a low-concentration-phosphorus film and a low-temperature anneal," as Petitioner argues, "which would result in negligible diffusion." *Id.* at 13 (citing Ex. 1031 ¶¶ 37–42; Reply Section II.B.5). We also find, based on Petitioner's evidence and argument, that, contrary to Patent Owner's assertions, "an oxide layer between PSG sidewalls and the substrate does not 'inherently perform[] as a phosphorus barrier layer'" and that an "oxide layer can be ineffective as a barrier." *Id.* at 16 (citing PO Resp. 20; Ex. 1025, 4:57–59). We also are persuaded by Petitioner's argument, supported by Dr. Banerjee's calculations, that one of ordinary skill in the art would have recognized that phosphorus diffusion can be controlled in Yonemaru, and would have had a reasonable expectation of success in applying well-known techniques, such as those used by Foster and Ono, to control phosphorus diffusion from sidewalls into the substrate in the Yonemaru combination. *Id.* at 17–19 (relying on Ex. 1026 (Foster); Ex. 1027 (Ono); Ex. 1031 ¶¶ 55–59), 20 (citing Ex. 1031 ¶¶ 60–65 (calculating the negligible distance of phosphorus diffusion under optimized conditions)).

We have considered Patent Owner's Sur-Reply arguments and evidence responding to Petitioner's Reply arguments on this matter. Sur-Reply 4–7; Ex. 2008 ¶¶ 6–14; *supra* Section II.D.2, Section II.D.4.

Particularly, Patent Owner argues in its Sur-Reply that it may be technically possible to control such diffusion, but that it would require extensive experimentation. Sur-Reply 4 (citing Ex. 2008 ¶¶ 9–10). Petitioner avers that this argument now supplants Patent Owner's Response argument that removal of the gate oxide would lead to uncontrolled diffusion, and notes that Patent Owner and its expert do not address the merits of Dr. Banerjee's examples and calculations. Reply to Sur-Reply 6 & n.4. We agree that Petitioner has demonstrated, through its examples and evidence, that an ordinarily skilled artisan would have been able to control phosphorus diffusion, and we are unpersuaded that Dr. Bottoms's rebuttal testimony establishes a need for extensive experimentation to achieve such control. Having reviewed Patent Owner's Sur-Reply arguments and evidence, we do not find the extensive experimentation argument supported by sufficient evidence, or persuasive testimony by Dr. Bottoms, who does not provide citations or evidence to support his assertions of the extensive experimentation allegedly required. Ex. 2008 ¶¶ 9–10. After weighing the respective evidence and arguments of the parties, we are persuaded that Petitioner has demonstrated there is not a need for a gate oxide layer under the sidewalls in Yonemaru to control phosphorus diffusion. Petitioner persuasively demonstrates that not only is phosphorus diffusion controllable, but that a gate oxide layer, even if present, may not necessarily prevent phosphorus diffusion. Thus, we are persuaded that Yonemaru need not use an oxide "barrier layer" to control phosphorus diffusion.

ii. Whether the Combination Results in the Claimed Invention

Patent Owner takes issue with Petitioner's contention that "[t]o the extent that Yonemaru does not disclose that the side walls 4 physically

contact the substrate because they are separated from the substrate by the gate oxide film 3," it would have been obvious to one of ordinary skill in the art "to apply Ohshima's teaching to Yonemaru to remove the excess gate oxide film 3 in Yonemaru by the same anisotropic etching that is used to form the **side walls 4**." PO Resp. 27 (quoting Pet. 32) (modifications by Patent Owner). Patent Owner contends that Petitioner's proposed modification of Yonemaru would require "several extra steps . . . to add a second set of sidewalls after removing the first set of sidewalls." *Id.* at 29.

Petitioner argues that Patent Owner's argument mischaracterizes the Petition. Reply 22. More particularly, Petitioner argues that the "same anisotropic etching" portion of the Petition quoted by Patent Owner refers to the type of etching, not to a particular etch step, as shown by the next sentence in the Petition: the "side walls 4 formed in subsequent steps would then directly contact the semiconductor substrate 1." *Id.* (citing Pet. 32, 60; Ex. 1031 ¶ 67 (Dr. Banerjee's declaration, explaining where the process was originally described in his opening Declaration at ¶¶ 190–194). Patent Owner does not appear to address this argument in its Sur-Reply.

We agree with Petitioner that the two sentences to which it refers (Pet. 32), when read together, mean that one of ordinary skill in the art "would have found it obvious to apply the same type of anisotropic etching used to form sidewalls in Yonemaru's step (D) to remove the gate oxide," and "would have applied this first etch before the (subsequent) steps of sidewall formation." Reply 22. As we noted in our Institution Decision (Inst. Dec. 21–22), in Section 10.12.1 of the Petition, Petitioner makes clear that its asserted ground is based on the contention that a person of ordinary skill in the art "would have been motivated to apply Ohshima's teaching to

Yonemaru to remove the exposed portions of gate oxide film 3 *during the gate formation step* for several reasons." Pet. 60 (emphasis added). Accordingly, we are persuaded by Petitioner's arguments and explanation on this issue.

iii. Allegedly New Reply Arguments

Patent Owner requested, and was granted, leave to file a Sur-Reply to address allegedly new arguments in Petitioner's Reply. Sur-Reply 1. In the Sur-Reply, Patent Owner argues that Petitioner's Reply arguments "that the asserted ground does not require sidewalls including phosphorus, and that phosphorus diffusion into the substrate would be controllable," both "could have been asserted in the Petition, but were not, and should be disregarded." *Id.*

We are persuaded, on this record, that Petitioner's Reply arguments are properly responsive. We are cognizant of the requirement "that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the ground for the challenge to each claim.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (quoting 35 U.S.C. § 312(a)(3)). We also note, however, that when "[t]he Board's final written decisions [are] based on the same combinations of references that were set forth in its institution decisions," a "new ground" or "new ground of rejection" argument does not apply. *Genzyme Therapeutic Prods. Ltd. v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1366 n.1 (Fed. Cir. 2016). We also have been cautioned that reply arguments should not be parsed "with too fine a filter." *Ericsson Inc. v. Intellectual Ventures I LLC*, 901 F.3d 1374, 1380 (Fed. Cir. 2018).

We have evaluated the evidence and arguments in the Petition, as well as those in the Reply, and conclude that Petitioner did not introduce any additional grounds relying on any new references, or propose any new theories, in its Reply. The Petition and the Institution Decision identified that Yonemaru uses PSG as an exemplary material meeting the limitation of claim 1. Pet. 31–34; Inst. Dec. 20. Patent Owner responded to this analysis in its Response. PO Resp. 16–18. Accordingly, Petitioner's arguments regarding use of alternative sidewall materials falling within the category of exemplary materials allowed by Yonemaru, and reasons that one of ordinary skill in the art would use alternative sidewall materials, were proper rebuttal arguments in the Reply, because they responded to an argument raised by Patent Owner in its Response and did not introduce new references or new grounds.

We also find that Petitioner, in response to Patent Owner's arguments regarding the alleged problems of phosphorus diffusion, presents proper rebuttal arguments as to why Patent Owner's arguments are inapposite. The Institution Decision recognized Patent Owner's arguments regarding potential problems caused by possible diffusion of phosphorus into the substrate if portions of Yonemaru's gate oxide film are removed. Inst. Dec. 20–21. Patent Owner included its arguments directed to this analysis in its Response. PO Resp. 16–27. We view Petitioner's arguments as properly responsive to Patent Owner's quite specific and narrow arguments focusing on the one disputed phrase in claim 1. Although Patent Owner argues, in relation to Petitioner's phosphorus diffusion Reply argument, that this "belated argument could have been provided in the Petition as part of a proper obviousness analysis" (Sur-Reply 4), it would be difficult if not

impossible for a petitioner to anticipate every argument it could have made in a petition.

We also note that Patent Owner requested and received a full and fair opportunity to respond to Petitioner's Reply arguments in its Sur-Reply. Patent Owner had notice of Petitioner's obviousness arguments as presented in the Petition, as analyzed in the Institution Decision, and as argued in the Reply. The Institution Decision found that PSG was exemplary and not critical to Yonemaru's process, and that Yonemaru does not require the presence of gate oxide along the entire surface of the substrate. Inst. Dec. 20–21. Patent Owner had opportunities to respond to our analysis in the Patent Owner Response and to respond to Petitioner's Reply arguments in the Sur-Reply. Both parties have been afforded additional opportunities to develop and respond to the respective arguments, and we have had sufficient opportunity to evaluate the parties' arguments and responses. Because of the additional briefing afforded the parties, we are persuaded that these arguments were adequately discussed and considered, allowing for a fair and just resolution of the dispute.

For the reasons given above, having considered the parties' arguments and evidence on the complete record now before us, we determine that Petitioner has shown by a preponderance of the evidence that independent claims 1, 8, and 15 would have been obvious over the combination of Yonemaru, Ohshima, and Narita.

iv. Dependent Claims 2–5 and 9–12

We also have reviewed Petitioner's contentions and supporting evidence regarding claims 2–5 and 9–12, each of which depends from claims 1 or 8. Pet. 40–44, 51–53. Other than arguments directed to the

independent claims, which we have discussed above, Patent Owner does not present additional arguments as to these claims. *See* PO Resp. 29. Based on the record now before us, we are persuaded that Petitioner has shown by a preponderance of the evidence that the combination of Yonemaru, Ohshima, and Narita renders obvious claims 2–5 and 9–12.

III. CONCLUSION

After considering the parties' arguments and evidence, we are persuaded that Petitioner has shown by a preponderance of the evidence that a person having ordinary skill in the art would have combined the teachings of Yonemaru, Ohshima, and Narita in the manner proposed by Petitioner. We conclude that Petitioner has satisfied its burden of demonstrating, by a preponderance of the evidence, that the subject matter of claims 1–5, 8–12, and 15 of the '611 patent is unpatentable under 35 U.S.C. § 103(a) as obvious in view of Yonemaru, Ohshima, and Narita.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner establishes, by a preponderance of the evidence, that claims 1–5, 8–12, and 15 of U.S. Patent No. 6,103,611 are unpatentable; and

FURTHER ORDERED that this is a Final Written Decision; therefore, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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