

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

Case IPR2017-01781
Patent 8,161,344 B2

Before MINN CHUNG, DANIEL J. GALLIGAN, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, NVIDIA Corporation (“Petitioner”) challenges the patentability of claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of U.S. Patent No. 8,161,344 B2 (“the ’344 patent,” Ex. 1001), which is assigned to Polaris Innovations Limited (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has not proven by a preponderance of the evidence that claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of the ’344 patent are unpatentable in this proceeding. See 35 U.S.C. § 316(e) (“In an *inter partes* review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.”).

A. Procedural History

On July 25, 2017, Petitioner requested *inter partes* review of claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of the ’344 patent. Paper 2 (“Pet.”). Patent Owner filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). We instituted trial on all grounds of unpatentability, which are as follows:

1. Whether claims 1, 8–12, 14, 16, 19, 26–31, 43, and 48–51 are unpatentable under 35 U.S.C. § 102(e) over Yoon;¹
2. Whether claims 16 and 18 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Yoon and Wickeraad;²

¹ US 2008/0082900 A1, filed Dec. 28, 2006, issued Apr. 3, 2008 (Ex. 1020).

² US 2007/0234182 A1, filed Mar. 31, 2006, issued Oct. 4, 2007 (Ex. 1022).

3. Whether claims 2, 20, and 44 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Yoon and LaBerge;³
4. Whether claims 4, 5, 22, 23, and 45 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Yoon and Hancock;⁴
5. Whether claims 1–3, 8–10, 12, 16–21, 26–28, 30, 43, 44, 48, 49, and 51 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Raz⁵ and Wickeraad; and
6. Whether claims 4, 5, 11, 22, 23, 29, 45, and 50 are unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Raz, Wickeraad, and Hancock.

Paper 9 (“Dec. on Inst.”), 37.

During the trial, Patent Owner filed a Request for Rehearing (Paper 11), which we denied (Paper 15). Patent Owner also filed a Response (Paper 18, “PO Resp.”), and Petitioner filed a Reply (Paper 26, “Pet. Reply”).⁶ With our authorization (Paper 31), Patent Owner filed a sur-reply addressing prior conception and diligent reduction to practice (Paper 37), and Petitioner filed a responsive brief (Paper 41). Each party also filed a Motion to Exclude evidence. Papers 32, 34.

An oral hearing was held on August 17, 2018, a transcript of which appears in the record. Paper 45 (“Tr.”). Following the hearing, with our authorization (Paper 46), the parties filed additional briefing addressing the

³ US 2003/0158981 A1, issued Aug. 21, 2003 (Ex. 1024).

⁴ US 4,277,844, issued July 7, 1981 (Ex. 1023).

⁵ US 2005/0066110 A1, issued Mar. 24, 2005 (Ex. 1021).

⁶ Paper 26 is a redacted version of Paper 25. For this Final Written Decision, we do not rely on any material that was filed under seal, and, therefore, we refer to the public, redacted version of Petitioner’s Reply.

broadest reasonable interpretation of “data arrangement alteration.”
Papers 47, 48.

B. Real Parties in Interest

Patent Owner identifies itself, Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 6, 2.

C. Related Matters

Petitioner and Patent Owner cite the following judicial matter involving the '505 patent: *Polaris Innovations Ltd. v. Dell Inc. & NVIDIA Corp.*, Case No. 4:16-cv-07005 (N.D. Cal.). Pet. 93; Paper 4, 2–3. The '344 patent is also at issue in IPR2017-01346, in which we are issuing a final written decision concurrently with this Decision.

D. The '344 Patent and Illustrative Claim

The '344 patent generally relates to circuits for error coding. Ex. 1001, Abstract, 1:11–12. Figure 1A, reproduced below, illustrates an embodiment of such a circuit.

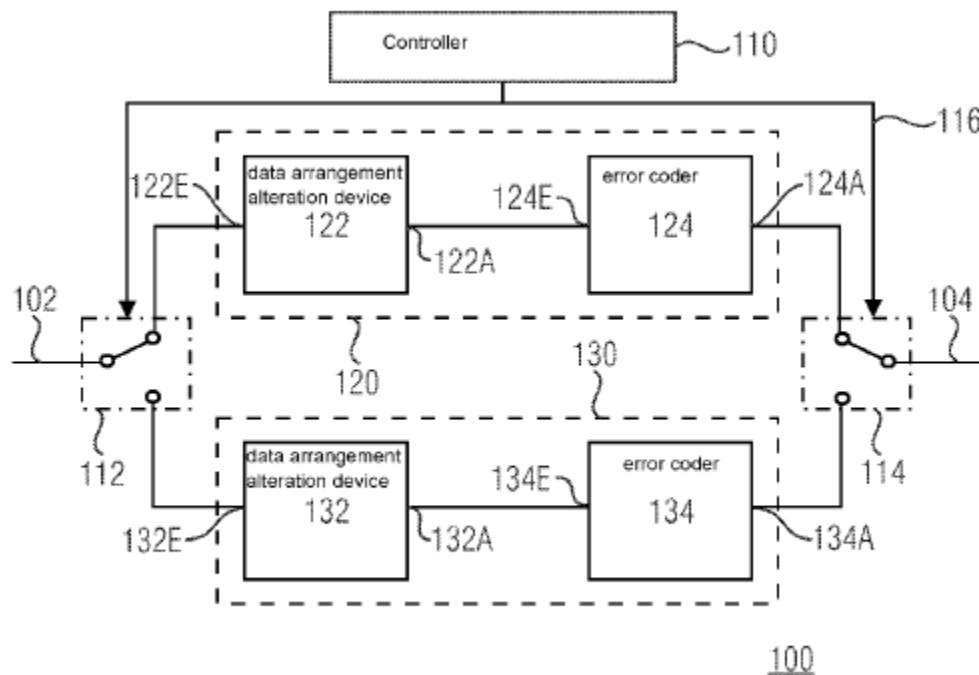


FIG 1A

Figure 1A illustrates an error coding circuit having controller 110, input 102, first error coding path 120, second error coding path 130, and output 104.

Ex. 1001, 3:27–30. As illustrated in Figure 1A, each of error coding paths 120 and 130 has a data arrangement alteration device and an error coder.

Ex. 1001, 3:30–34. The '344 patent explains that control indicator 116 is used to select between the first and second error coding paths. Ex. 1001, 4:41–47.

Of the claims at issue in the present proceeding, claims 1, 16, 19, and 43 are independent claims. Claim 1 is illustrative and is reproduced below.

1. A circuit for creating an error coding data block for a first data block, the circuit comprising:
 - a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding;
 - and

a second error coding path adapted to selectively create a second error coding data block in accordance with a second error coding;

the first error coding path and the second error coding path being selected as a function of a control indicator, and at least the first error coding path comprising a data arrangement alteration device.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Tredennick, testifies that "[a] person of ordinary skill in the art as of the time of the '344 patent (POSITA) would have had a Bachelor's degree in Electrical Engineering and at least 2 years of experience working in the field of semiconductor logic design." Ex. 1019

¶ 13. Neither Patent Owner, nor its declarant, Dr. Przybylski, offers a different assessment of the level of ordinary skill in the art. See Ex. 2003 ¶ 36 ("I am applying the definition of the level of experience of a person of ordinary skill in the art that has been put forward by Dr. Tredennick in his declaration. I do not necessarily agree with the definition offered there, but I do not presently believe that the exact level of experience of a person of ordinary skill impacts my opinions offered herein.").

Based on the evidence of record, we adopt Dr. Tredennick's statement of the level of ordinary skill in the art with the exception of the language "at least." Thus, we determine that the skill level of a person of ordinary skill in the art would have been that of a person with a bachelor's degree in electrical engineering and two years of experience working in the field of semiconductor logic design.

B. Claim Interpretation

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2016). In applying a broadest reasonable construction, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). This presumption may be rebutted when a patentee, acting as a lexicographer, sets forth an alternate definition of a term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Furthermore, only terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). We determine it is necessary to construe expressly only the claim terms discussed below to resolve the disputed issues before us in this proceeding.

1. Data Arrangement Alteration

Each of the challenged claims recites a “data arrangement alteration device” or a “data arrangement alteration algorithm.” The broadest reasonable interpretation of “data arrangement alteration” is at issue in this case and in IPR2017-01346, but the disputes in each proceeding are different. Here, the question is whether inverting data bits is an alteration of the arrangement of those data bits, as Petitioner contends. *See* Pet. 33 (“Yoon’s DBI [(data bus inversion)] is a technique for inverting – re-

arranging – the bits of a data block”). In our Decision on Institution, we agreed with Petitioner’s position. Dec. on Inst. 13 (“On this record and for purposes of this Decision, we are persuaded that data bus inversion is within the broadest reasonable interpretation of ‘data arrangement alteration’ and, therefore, that a device that performs data bus inversion is within the broadest reasonable interpretation of ‘data arrangement alteration device.’”). Following oral argument, we authorized the parties to file additional briefing addressing the broadest reasonable interpretation of “data arrangement alteration.” Papers 46, 47, 48.

Having considered the entire record developed during trial, we determine Petitioner has not shown that data bus inversion is within the broadest reasonable interpretation of data arrangement alteration consistent with the specification.

Petitioner argues that “data arrangement alteration” encompasses “changes in data order as well as other ways of rearranging data, such as inversion,” and that the “[t]he ’344 patent imposes no requirements on how ‘data arrangement alteration’ is achieved.” Paper 47, 2. In support, Petitioner cites the following disclosure in the ’344 patent: “Any implementations which may change an arrangement of data such that these data will be processed in an optimum manner for a subsequent error detection or correction algorithm may be considered as a potential data arrangement alteration device 222.” Ex. 1001, 10:34–38, *cited in* Paper 47, 3. According to Petitioner, “[t]hrough this disclosure, the ’344 patent places no limit on how ‘data []arrangement alteration’ is achieved, and covers any rearrangement whether it is achieved through bit reordering, inversion, or other types of logical bit operations.” Paper 47, 3.

Even if so, the *arrangement* of the data must be altered to give full effect to the claim language. The portions of the specification of the '344 patent cited by Petitioner confirm this.

In one instance, the '344 patent states:

In the first error coding path 120, the first data arrangement alteration device 122 is adapted to create a second data block on the basis of the first data block, which comprises the given number of data *in a second arrangement*, and to output it to the first error coder 124.

Ex. 1001, 3:63–67 (emphasis added), *cited in* Paper 47, 2. Another passage states:

The data arrangement alteration device 222 is adapted to receive, at the input 222E or 102, a first data block comprising a given number of data in the first arrangement, and to generate, on the basis of the first data block, a second data block comprising the given number of data *in a second arrangement*

Ex. 1001, 6:14–18 (emphasis added), *cited in* Paper 47, 2. These passages show that data arrangement alteration takes data and puts those data into a different arrangement. Petitioner also cites the '344 patent's disclosure of a deserializer changing the "representation" of data. Paper 47, 2–3 (citing Ex. 1001, 8:58–62, 9:2–7). But, in this operation, "the second data block 440 . . . *comprises the same data*, namely the 72 bits of the first data block 435 in a second arrangement which is different from the first arrangement of the first data block." Ex. 1001, 9:32–35 (emphasis added). Petitioner also cites an example in the '344 patent in which the burst length is halved from eight time pulses to four time pulses. Ex. 1001, 11:52–61, *cited in* Paper 47, 4. The '344 patent describes that, in this scenario, only half of the bits (36 out of 72) "will be occupied with processable data."

Ex. 1001, 11:59–60. Petitioner contends that this describes an output of 72 bits that is larger and different than the input of only 36 bits. Paper 47, 4. The '344 patent, however, describes providing “a further subarea of the matrix 420 for this mode, and to control the multiplexer 430, via the mode register 110, *such that this subarea will be read out*, so that, for example, only 36 of the 72 bits will be occupied with processable data.” Ex. 1001, 11:56–60 (emphasis added). Thus, it is the subarea having the 36 bits of processable data that is read out. But even if Petitioner is correct that the output is larger than the input in this example, data *arrangement* alteration still requires an alteration of the arrangement of the input data, even if the output contains additional data.

In all of the examples in the specification of the '344 patent, therefore, the arrangement of the data is altered. We see nothing in the intrinsic record to support a conclusion that merely altering data satisfies the requirement of data arrangement alteration. Petitioner also cites testimony from its declarant, Dr. Tredennick, and Patent Owner's declarant, Dr. Przybylski, that Petitioner contends supports its contention that data arrangement alteration encompasses inverting data. Paper 47, 2 (citing Ex. 1019 ¶¶ 60–61; Ex. 1029, 50:12–51:5; Ex. 1030, 148:13–150:1). Dr. Tredennick's cited testimony quotes Yoon's disclosure of inverting data and states, “Thus, Yoon's write [read] data path comprises a data arrangement alteration device – the first [second] data bus inversion unit.” Ex. 1019 ¶¶ 60–61. This testimony, however, does not explain why data arrangement alteration, as described in the '344 patent, encompasses data inversion. Dr. Przybylski testifies, “I believe that a selective inversion of data could be viewed as a data arrangement. I believe I could prove that to be the case. I don't believe

that such a proof is before the board in this case.” Ex. 1029, 50:12–51:5. Dr. Przybylski also testifies that “[i]nversion in a structured way where the output bits are an inverted form of input bits can be viewed as a rearrangement.” Ex. 1030, 149:4–6. This extrinsic evidence, however, fails to explain how “data arrangement alteration,” as described in the ’344 patent, would have been understood. In light of the intrinsic record discussed above, we do not find this extrinsic evidence to be particularly useful in determining the broadest reasonable interpretation of “data arrangement alteration.” *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (en banc) (authorizing the consideration of extrinsic evidence in determining the meaning of claims but noting that it is “in general . . . less reliable than the patent and its prosecution history in determining how to read claim terms”).

For its part, Patent Owner argues that “a ‘data arrangement alteration device’ should be interpreted as a device that *can* alter the arrangement of data in a data block.” IPR2017-01346, Paper 14, 8–9 (emphasis added). As explained above, however, the specification of the ’344 patent describes a data arrangement alteration device as a device that alters the arrangement of data, not a device that merely has the capability to do it. Consider a data block of eight bits, having four 0s and four 1s, that goes into a device that inverts each bit. The result of the inversion operation will be eight bits having 1s where the 0s were and 0s where the 1s were. Although the device alters the data by inverting each bit, the *arrangement* of the data is also changed because the input data were evenly divided between 0s and 1s. This, arrangement alteration, however, is merely a circumstance of the input data. Patent Owner’s proposed construction would encompass seemingly

any data alteration device because there likely will be some input to the device that will result in the data's arrangement being altered. This is not consistent with the description of the claimed subject matter in the specification of the '344 patent. See *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1382–83 (Fed. Cir. 2017) (quoting *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997)) (stating that the broadest reasonable interpretation “is an interpretation that corresponds with what and how the inventor describes his invention in the specification, i.e., an interpretation that is ‘consistent with the specification.’”).

Patent Owner also contends that data arrangement alteration must be performed on data “blocks.” Paper 48, 1–4. Petitioner disagrees.

Paper 47, 5. The following passage from the '344 patent is instructive:

A piece of data may be, for example, a bit, and a data word may consist of several bits, for example. It is possible for a data word to be formed of several bits which are received in a serial manner, i.e., successive in time, or to be formed by several bits which are received at the same time (parallel interface). In this context, what is meant by data block is a serial data word, a parallel data word, or a serial sequence of parallel data words, as is depicted, for example, by reference numeral 435 in FIG. 4. Embodiments of the data arrangement alteration device 222 are adapted to change any of these types of data blocks or all of them in accordance with at least one data arrangement alteration algorithm so as to optimize error detection, or at least to improve error detection as compared to an approach without any change in the data arrangement, by means of the subsequent error coding algorithms.

Ex. 1001, 11:66–12:14. A data word may be several bits and a “data block” may be a data word. Thus, the '344 patent uses the term “data block” to refer to a grouping of data.

Determining whether an arrangement of data is altered requires looking at a particular grouping of data from input to output. To that extent, we agree with Patent Owner that the '344 patent describes performing data arrangement alteration on data blocks. The term "data block," however, is not limited by the '344 patent to any particular structure or length.

Based on the foregoing, we determine that "data arrangement alteration device" is a device that alters the *arrangement* of data in a grouping of data. A "data arrangement alteration algorithm," similarly, is an algorithm that specifies how to alter an arrangement of data in a grouping of data.

2. Means for Performing a Data Arrangement Alteration Algorithm

Petitioner contends that "[t]he corresponding structure for 'performing a data arrangement alteration algorithm' is described in the '344 patent as a 'data arrangement alteration device,' which is part of the 'one or more devices' of the first means of claim 19. Thus, the corresponding structure is 'a data arrangement alteration device.'" Pet. 10 (citing Ex. 1001, 6:14–25, 6:42–65, 7:10–24; Ex. 1019 ¶ 32). In the Decision on Institution, we addressed Petitioner's proposed construction for "means for performing a data arrangement alteration algorithm," but we did not adopt it. Dec. on Inst. 11–12. Rather, we set out the following construction of this term:

Limitation	Function and Structure
Claim 19: means for performing a data arrangement alteration algorithm	<u>Function:</u> performing a data arrangement alteration algorithm <u>Structure:</u> data arrangement alteration devices 122, 132, and 222 and equivalents. <i>See id.</i> at 3:27–34, 5:65–6:25, 6:42–65, 8:55–57, 10:34–45, Figs. 1–4.

During the trial in this proceeding, neither party further disputed this interpretation. Having considered the entire record developed during trial, we determine that this is the proper interpretation for “means for performing a data arrangement alteration algorithm.” Thus, we apply this interpretation in our analysis below.

C. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Anticipation by Yoon
(Claims 1, 8–12, 14, 16, 19, 26–31, 43, and 48–51)

Petitioner contends claims 1, 8–12, 14, 16, 19, 26–31, 43, and 48–51 of the '344 patent are unpatentable under 35 U.S.C. § 102(e) as anticipated by Yoon. Pet. 2, 11–65.

1. Prior Art Status of Yoon

Patent Owner argues that Yoon is not prior art because the claimed subject matter was conceived prior to Yoon's filing date of December 28, 2006, and the applicant was diligent in reducing the invention to practice. PO Resp. 12–31. Because Petitioner has not established Yoon describes the “data arrangement alteration” limitations of each challenged claim, as discussed below, we need not reach the issue of conception and diligent reduction to practice.

2. Yoon

Yoon is directed to “a semiconductor memory apparatus capable of detecting an error in data input/output.” Ex. 1020 ¶ 2. Yoon describes a memory apparatus that is connected to a graphic processing unit (GPU) and that has an error correction code generator (EDC) and two global data lines each having a data bus inversion unit (DBI). *Id.* ¶¶ 15, 54–57, Fig. 4.

3. Data Arrangement Alteration

Each challenged independent claim recites “data arrangement alteration.” Claims 1 and 16 recite “at least the first error coding path

comprising a data arrangement alteration device.” Claim 19 recites “at least the first means for performing the first error coding comprising a means for performing a data arrangement alteration algorithm.” Claim 43 recites “performing a data arrangement alteration algorithm.” For each of these limitations, Petitioner relies on Yoon’s disclosure of a data bus inversion unit. Pet. 30–33 (citing Ex. 1020 ¶¶ 15, 54–57; Ex. 1019 ¶¶ 58–65), 48, 55, 65. Petitioner contends that, “[d]uring write operation, DBI_1 440 inverts (i.e., alters) some portion of the bits of the data block based on values in an 8-bit DBI signal.” Pet. 32 (citing Ex. 1020 ¶¶ 15, 54–57; Ex. 1019 ¶ 63). According to Petitioner, “Yoon uses DBI to alter data during read/write operations.” Pet. 33. As to claim 19, Petitioner asserts that Yoon’s data bus inversion devices describe “a means for performing a data arrangement alteration algorithm.” Pet. 48.

As discussed above in the section addressing claim interpretation, “data arrangement alteration” requires alteration of the *arrangement* of data, not merely alteration of data. Petitioner’s allegation that Yoon’s data bus inversion alters some portion of the data is insufficient to show that Yoon describes altering the arrangement of data, as required by the claims. For the same reasons, we are not persuaded that Yoon’s data bus inversion devices describe the same or equivalent structure as that set forth in the specification of the ’344 patent, namely data arrangement alteration devices 122, 132, and 222, as set forth in our claim interpretation discussion above.

Because Petitioner has not shown Yoon describes the “data arrangement alteration” limitations of independent claims 1, 16, 19, and 43, Petitioner has not proven, by a preponderance of the evidence, that Yoon anticipated these claims.

Dependent claims 8–12, 14, 26–31, and 48–51 incorporate the “data arrangement alteration” limitations by virtue of their dependency from their respective independent claims, and, therefore, Petitioner has not proven, by a preponderance of the evidence, that Yoon anticipated these claims.

*E. Obviousness over Yoon and Wickeraad
(Claims 16 and 18)*

Petitioner contends claims 16 and 18 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combined teachings of Yoon and Wickeraad. Pet. 2, 65–73. Petitioner's contentions with respect to these claims rely on Yoon to teach “a data arrangement alteration device” for the same reasons discussed with respect to anticipation. Pet. 65. Because Petitioner has not shown Yoon describes “data arrangement alteration,” Petitioner has not proven, by a preponderance of the evidence, that claims 16 and 18 would have been obvious over the combined teachings of Yoon and Wickeraad.

*F. Obviousness over Yoon and LaBerge
(Claims 2, 20, and 44)*

Petitioner contends claims 2, 20, and 44 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combined teachings of Yoon and LaBerge. Pet. 2, 76–79, 81, 82. Each of these claims requires the same data arrangement alteration algorithm to be used in both error coding paths. Petitioner argues LaBerge uses the same data bus inversion algorithm for both read and write operations. Pet. 78. LaBerge discloses that its data bus inversion algorithm inverts the data bits in a byte if certain conditions are met. Ex. 1024 ¶ 10. Thus, Petitioner's contentions with respect to these claims also rely on inverting data to teach “data arrangement alteration.” As discussed above in the section addressing

claim interpretation, “data arrangement alteration” requires alteration of the *arrangement* of data, not merely alteration of data. Petitioner’s contentions in this ground, therefore, are insufficient to show that the combination of Yoon and LaBerge teaches altering the arrangement of data, as required by the claims.

Thus, Petitioner has not proven, by a preponderance of the evidence, that claims 2, 20, and 44 would have been obvious over the combined teachings of Yoon and LaBerge.

*G. Obviousness over Yoon and Hancock
(Claims 4, 5, 22, 23, and 45)*

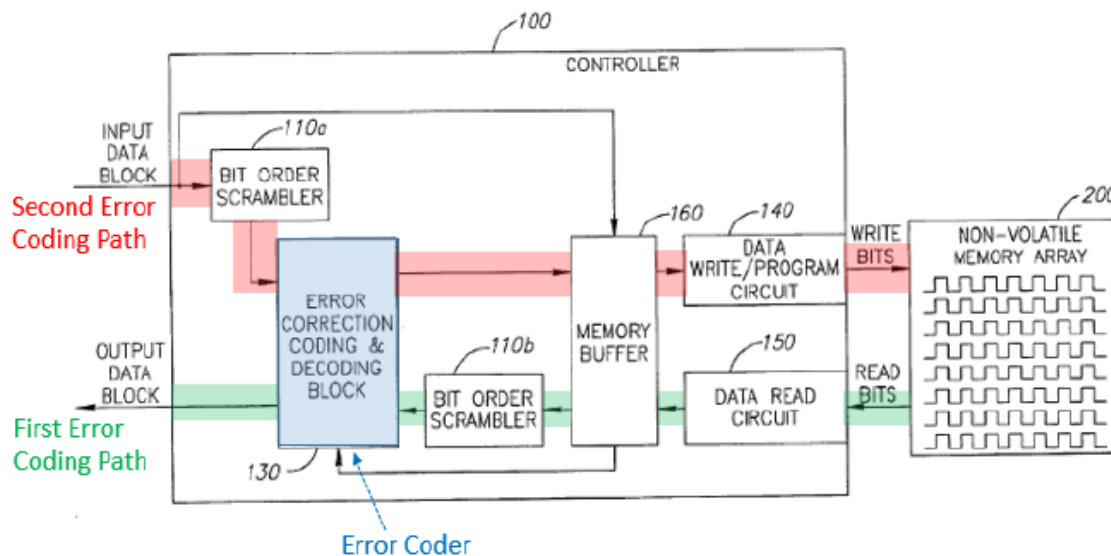
Petitioner contends claims 4, 5, 22, 23, and 45 of the ’344 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combined teachings of Yoon and Hancock. Pet. 2, 83–86, 89–92. These dependent claims incorporate the “data arrangement alteration” limitations of their respective independent claims, and Petitioner’s contentions in this ground do not remedy the deficiencies of Yoon’s teachings discussed above. Therefore, Petitioner has not proven, by a preponderance of the evidence, that claims 4, 5, 22, 23, and 45 would have been obvious over the combined teachings of Yoon and Hancock.

*H. Obviousness over Raz and Wickeraad
(Claims 1–3, 8–10, 12, 16–21, 26–28, 30, 43, 44, 48, 49, and 51)*

Petitioner contends claims 1–3, 8–10, 12, 16–21, 26–28, 30, 43, 44, 48, 49, and 51 of the ’344 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combined teachings of Raz and Wickeraad. Pet. 2, 13–83.

Petitioner relies on Raz to teach much of the subject matter recited in the independent claims. See Pet. 13–36. With its obviousness analysis,

Petitioner provides the annotated version of Raz's Figure 3 reproduced below.

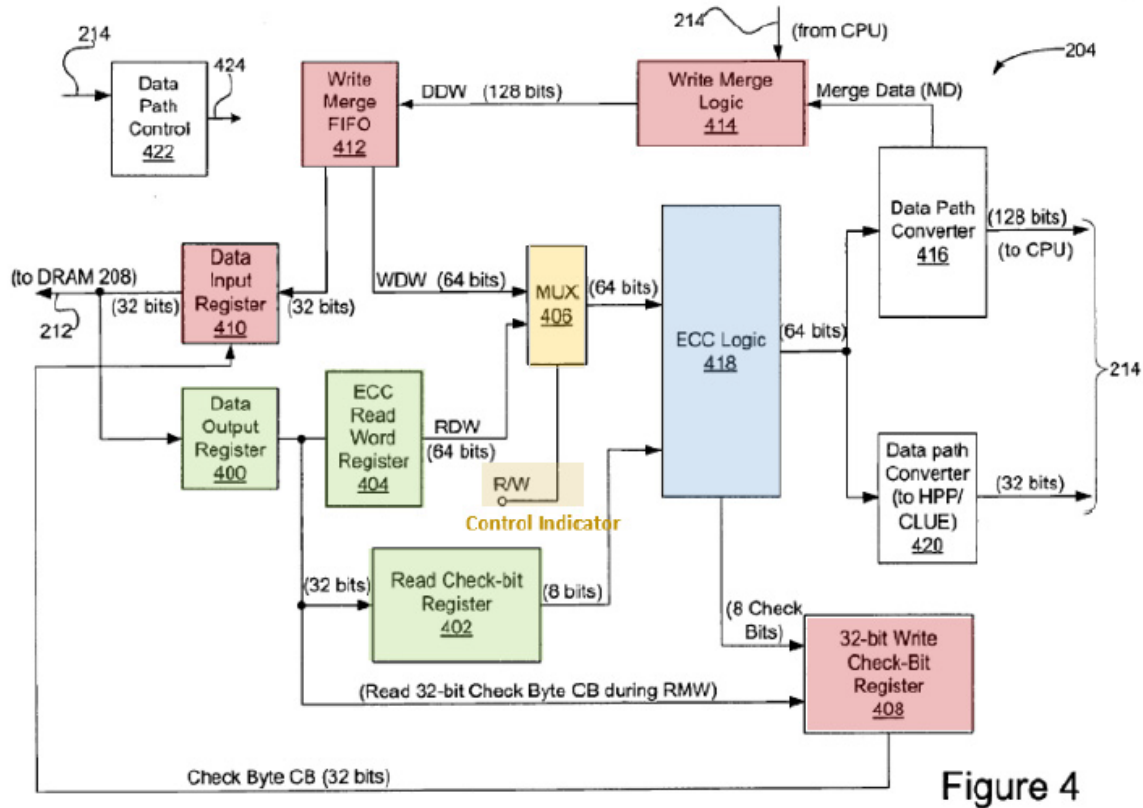


Pet. 13. In this annotated version of Figure 3 of Raz, Petitioner identifies a read path in green and a write path in red and contends these paths disclose the claimed “first error coding path” and “second error coding path,” respectively. Pet. 13, 17, 23–24.

Independent claims 1 and 16 recite “the first error coding path and the second error coding path being selected as a function of a control indicator.” Similarly, independent claim 19 recites “the first means and the second means being selected as a function of a control indicator,” and claim 43 recites “the first error coding data block for the first data block and the second error coding data block being selectively created as a function of a control indicator.”

Petitioner acknowledges that “Raz does not explicitly disclose a ‘control indicator’ for selecting between read/write operation.” Pet. 27. Petitioner argues “control indicators for selecting between read/write operations were well-known” and cites Wickeraad in support of this

contention. *Id.* (citing Ex. 1022 ¶¶ 5, 10, 15–17, 34–51; Ex. 1019 ¶¶ 177–184). With its obviousness analysis, Petitioner provides the annotated version of Wickeraad’s Figure 4 reproduced below.



In this annotated version of Figure 4 of Wickeraad, Petitioner labels “R/W” signal to multiplexer (or mux) 406 as a “Control Indicator.” Pet. 29. Petitioner contends that, “depending on the read/write signal, Wickeraad’s multiplexer 406 applies either write or read data to the ECC logic.” *Id.* For example, Wickeraad discloses that, “[i]n response to a read/write signal R/W being active, which defines a write operation, the multiplexer 406 applies the write data words WDW to the ECC logic 418” and that, “[w]hen the read/write signal is inactive, which defines a read operation, the multiplexer 406 applies the read data words RDW to the ECC logic 418.” Ex. 1022 ¶ 39.

Petitioner contends:

[A person of ordinary skill in the art] would have found it obvious to modify Raz's controller circuit to use Wickeraad's read/write signal for selecting between read/write path inputs to the ECC logic. [Ex.]1019, ¶183. Indeed, a [person of ordinary skill in the art] would have understood that Raz's memory controller would have required some technique for selecting between read/write paths to enable error correction block 130 to know the proper operation to perform and proper output to provide. *Id.* A [person of ordinary skill in the art] would have had a finite number of options for selecting between read/write paths and would have found use of a control indicator, such as Wickeraad's, a suitable option that was commonly employed. *Id.* In fact, a [person of ordinary skill in the art] would have found use of Wickeraad's control indicator (read/write signal) to select between Raz's read/write paths to have been use of a known technique to improve a similar device in the same way to yield predictable results. [Ex.]1019, ¶¶177-184.

Pet. 29–30. Dr. Tredennick testifies similarly. Ex. 1019 ¶ 183.

Patent Owner points out that, for Petitioner's alleged first and second error coding paths, Figure 3 of Raz shows separate read and write circuits and input and output data blocks that go into and come out of different parts of controller 100. PO Resp. 50. Dr. Przybylski testifies that, in Raz's Figures 1, 2, and 3, the input and output data paths are shown as separate unidirectional paths and there would be no indicator needed to select between these paths. Ex. 2003 ¶¶ 78, 79, 81, 83, 84. Dr. Przybylski also testifies that error correction coding and decoding block 130 is shared between the paths but has separate inputs and outputs for the input data block path and the output data block path. Ex. 2003 ¶¶ 78, 81, 84. Patent Owner argues there is no disclosure in Raz indicating a need to select between the two separate paths and, thus, there is no control indicator disclosed and no reason to add one. PO Resp. 50 (citing Ex. 2003 ¶ 84).

Petitioner argues that Raz's two paths share error correction coding and decoding block 130 and memory buffer 160 and that a person of ordinary skill in the art "would have understood that Raz used the more common technique of read/write paths that share circuitry and operate one at a time." Pet. Reply 24 (citing Ex. 1019 ¶ 183). Dr. Tredennick testifies that a person of ordinary skill in the art "would have understood that Raz's memory controller would have required some technique for selecting between read and write paths to enable error correction block 130 to know the proper operation to perform and proper output to provide." Ex. 1019 ¶ 183. But Dr. Przybylski explains that "the input data block path and the output data block paths are explicitly shown as separate unidirectional paths instead of a more traditional single, bidirectional I/O bus," which "further supports the implicit idea that the paths are separate with block 130 and it is capable of handling reads and writes into and out of controller 100 simultaneously." Ex. 2003 ¶ 79. Although this testimony from Dr. Przybylski relates to Figure 1, Dr. Przybylski provides testimony that refers to Figure 2 with reference to his discussion of Figure 1, explaining the differences, and does the same thing for Figure 3 with reference to Figure 2. Ex. 2003 ¶¶ 81–84. Thus, this testimony regarding the separate and unidirectional paths applies to Figures 1, 2, and 3. We credit Dr. Przybylski's testimony because Figure 3 of Raz shows separate unidirectional paths. In the annotated version of Figure 3 provided by Petitioner, the red path, which is alleged to be the "second error coding path," goes from left to right with arrows pointing right; the green path, which is alleged to be the "first error coding path," goes from right to left with arrows pointing left. Pet. 13.

The separate paths into and out of error correction coding and decoding block 130 undermine not only the reason to combine but also the actual proposed combination of the teachings of Raz and Wickeraad.

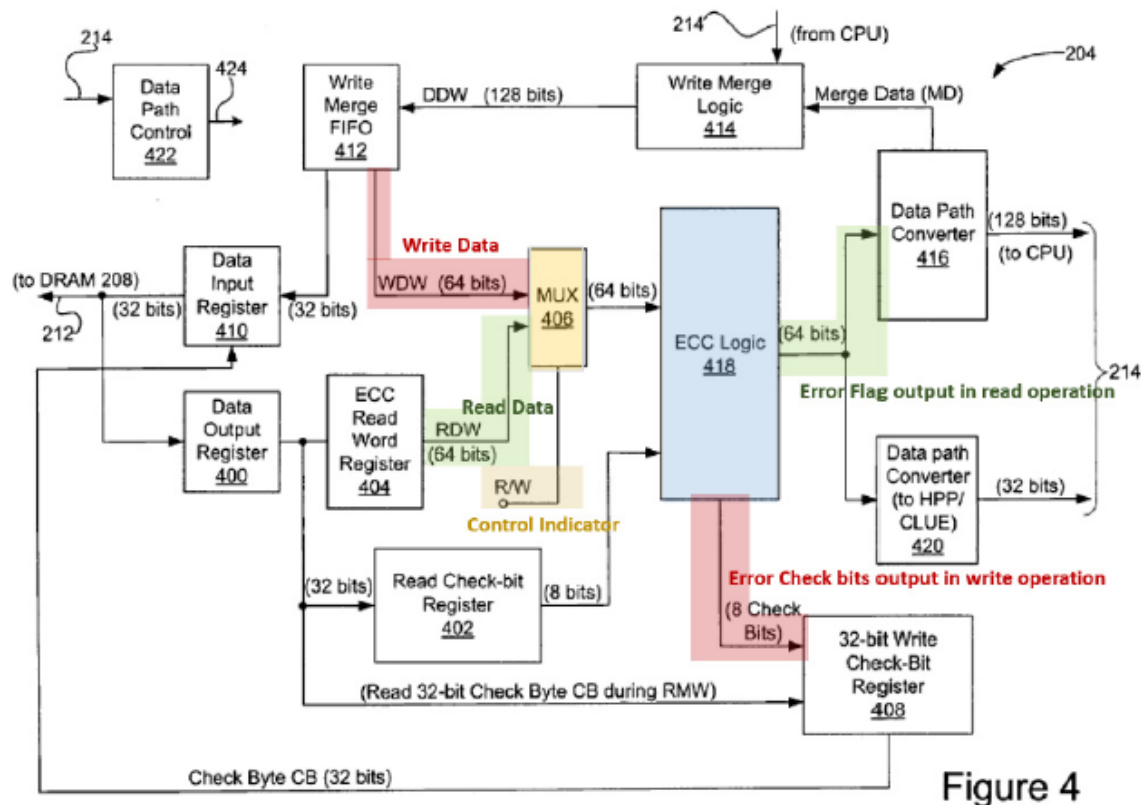
Petitioner argues that, “[b]y placing the Mux 406 [in Wickeraad’s Figure 4] in conjunction with Raz’s error correction coding and decoding block 130, the Mux 406 would be able to select either the read path (green) or write path (red) in Raz the same way it does for Wickeraad.” Pet. Reply 28.

Wickeraad uses multiplexer 406 to select one of two data words to be input to error checking and correction (ECC) logic 418, as described in the following passage:

In response to a read/write signal R/W being active, which defines a write operation, the multiplexer 406 applies the write data words WDW to the ECC logic 418. This occurs during standard write operations and during the write portion of a read-modify-write operation. When the read/write signal is inactive, which defines a read operation, the multiplexer 406 applies the read data words RDW to the ECC logic 418. This occurs during standard read operations and during the read portion of a read-modify-write operation.

Ex. 1022 ¶ 39. Thus, in Wickeraad, both read and write data words go into multiplexer 406, which then chooses which of the two data words to send to ECC logic 418. Figure 4 of Wickeraad shows one input on ECC logic for receiving both read and write data words.

Petitioner argues “Wickeraad discloses exactly that ability to route to two different destinations: a read path and a write path.” Pet. Reply 27 (emphasis omitted). In support, Petitioner provides the annotated version of Wickeraad’s Figure 4 reproduced below.



In this annotated version of Figure 4 of Wickeraad, Petitioner identifies various segments of data paths as write paths in red or read paths in green. Pet. Reply 28. According to Petitioner, ECC logic 418 outputs an error flag during a read operation but outputs eight error check bits from a different location during a write operation. Pet. Reply 27 (citing Ex. 1022 ¶¶ 43–46, 49; Ex. 1019 ¶¶ 180–183). Petitioner argues that, “as shown in [Wickeraad’s] FIG. 4 . . . and contrary to Polaris’s contention, Wickeraad’s ECC has two outputs, just like Raz.” Pet. Reply 27. Irrespective of Petitioner’s arguments regarding ECC outputs, multiplexer 406 is used to select between a write data word and a read data word to be *input* to ECC logic 418, which Figure 4 shows as having one input that is shared for read and write data words. Petitioner’s contention, however, is that one of ordinary skill in the art would have used “Mux 406 in conjunction with

Raz's error correction coding and decoding block 130" (Pet. Reply 28 (emphasis added)), which Raz depicts as having a separate input for each of the two separate paths. Petitioner's assertion that "Wickeraad's ECC has two outputs, just like Raz" fails to explain the need for multiplexer 406 on the input side of Raz's error correction coding and decoding block 130.

Based on the foregoing and upon considering the complete record, we find Petitioner has not provided sufficient "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). In particular, Petitioner has not provided persuasive reasoning why a person of ordinary skill in the art would have been motivated to combine the teachings of Wickeraad's multiplexer 406 with Raz's error correction coding and decoding block 130. Wickeraad's multiplexer 406 works in conjunction with ECC logic 418 to select one of two inputs to provide to ECC logic 418 based on the read/write signal R/W. Ex. 1022 ¶ 39. Raz, however, discloses that its error correction coding and decoding block 130 has a separate input for each of its read and write paths. Ex. 1021, Fig. 3. Thus, it is not evident why a person of ordinary skill in the art would have been motivated to combine the teachings of Wickeraad's multiplexer with Raz's error correction coding and decoding block 130 or even what such a combination would have accomplished.

Petitioner's challenges to each of the claims in this ground rely on combining Raz and Wickeraad for the reasons discussed above. Because Petitioner has not provided sufficient articulated reasoning for the combination of Raz and Wickeraad, Petitioner has not proven, by a preponderance of the evidence, that the combination of Raz and Wickeraad

renders obvious claims 1–3, 8–10, 12, 16–21, 26–28, 30, 43, 44, 48, 49, and 51.

*I. Obviousness over Raz, Wickeraad, and Hancock
(Claims 4, 5, 11, 22, 23, 29, 45, and 50)*

Petitioner contends claims 4, 5, 11, 22, 23, 29, 45, and 50 of the '344 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combined teachings of Raz, Wickeraad, and Hancock. Pet. 2, 42–44, 51, 56, 86–88, 90–92. Petitioner's challenges to each of the claims in this ground rely on combining Raz and Wickeraad for the reasons discussed above. Because Petitioner has not provided sufficient articulated reasoning for the combination of Raz and Wickeraad, Petitioner has not proven, by a preponderance of the evidence, that the combination of Raz, Wickeraad, and Hancock renders obvious claims 4, 5, 11, 22, 23, 29, 45, and 50.

III. MOTIONS TO EXCLUDE

Petitioner filed a Motion to Exclude Exhibits 2005–2010, 2013–2016, and 2023–2026 and certain portions of Exhibits 2003, 2046, and 2047 that rely on those exhibits. Paper 32. We do not rely on any of this material because it relates to the issue of conception and diligent reduction to practice, which we do not address. Therefore, we dismiss Petitioner's Motion to Exclude as moot.

Patent Owner filed a Motion to Exclude Exhibits 1025 and 1030 and certain portions of Exhibit 1029. Paper 34. Exhibit 1025 is an excerpt from Patent Owner's Preliminary Infringement Contentions in co-pending district court litigation. Exhibit 1029 is a transcript of Dr. Przybylski's deposition in this proceeding, and Exhibit 1030 is a transcript of Dr. Przybylski's

deposition in IPR2017-01346. We do not rely on Exhibit 1025 in any manner, and, although we discuss portions of Dr. Przybylski's deposition transcripts, we do not rely on this testimony in a manner adverse to Patent Owner. Thus, we dismiss Patent Owner's Motion to Exclude as moot.

IV. CONCLUSION

For the reasons discussed above, we determine Petitioner has not proven, by a preponderance of the evidence, that claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of the '344 patent are unpatentable on the grounds presented in this proceeding.

V. ORDER

Accordingly, it is:

ORDERED that Petitioner has not proven, by a preponderance of the evidence in this proceeding, that any one of claims 1–5, 8–12, 14, 16–23, 26–31, 43–45, and 48–51 of U.S. Patent No. 8,161,344 B2 is unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude Exhibits 2005–2010, 2013–2016, and 2023–2026 and certain portions of Exhibits 2003, 2046, and 2047 is dismissed as moot;

FURTHER ORDERED that Patent Owner's Motion to Exclude Exhibits 1025 and 1030 and certain portions of Exhibit 1029 is dismissed as moot; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01781
Patent 8,161,344 B2

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