

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION and
RENESAS ELECTRONICS AMERICA, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01872
Patent 6,103,611

Before GRACE KARAFFA OBERMANN, KRISTIN M. KALAN, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION

Finding Claims 1–5, 8–12, and 15 Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Renesas Electronics Corporation and Renesas Electronics America, Inc. (collectively, “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–5, 8–12, and 15 of U.S. Patent No. 6,103,611 (Ex. 1001, “the ’611 patent”). Paper 1 (“Pet.”). Lone Star Silicon Innovations, LLC¹ (“Patent Owner”) filed a Notice Waiving Preliminary Response. Paper 5. We instituted an *inter partes* review of claims 1–5, 8–12, and 15 on all grounds of unpatentability alleged in the Petition. Paper 6 (“Institution Decision” or “Inst. Dec.”).

After institution of trial, Patent Owner filed a Patent Owner Response. Paper 19 (“PO Resp.”). Petitioner filed a Reply. Paper 24 (“Reply”). An oral hearing was held on January 9, 2019. A transcript of the hearing is included in the record. Paper 29 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has established by a preponderance of the evidence that claims 1–5, 8–12, and 15 of the ’611 patent are unpatentable.

A. *Related Proceedings*

The parties identify a number of proceedings as related, including *Lone Star Silicon Innovations LLC v. Renesas Electronics Corp.*, Case No. 3:17-cv-03981 (N.D. Cal. Dec. 20, 2016) (dismissed without prejudice) and *Lone Star Silicon Innovations, LLC v. Renesas Electronics Corp.*, Appeal No. 2018-1580 (Fed. Cir. Feb. 15, 2018). Paper 22, 2; Paper 28, 6.

¹ Patent Owner identifies Longhorn IP LLC as an additional real party in interest. Paper 4, 1.

In Case IPR2017-01563, the Board found claims 1–5, 8–12, and 15 of the '611 patent unpatentable. *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, IPR2017-01563 (PTAB Dec. 17, 2018) (Paper 29).

B. The '611 Patent

The '611 patent, titled “Methods and Arrangements for Improved Spacer Formation Within a Semiconductor Device,” was filed December 18, 1997, and issued August 15, 2000. Ex. 1001, at [22], [45], [54]. The '611 patent relates to increasing the process control during the formation of spacers within a semiconductor device. *Id.* at [57].

As described in the '611 patent, a problem existed in the prior art in which uneven spacing between gate conductors could lead to spacers formed adjacent thereto having inconsistent widths, which “can have a deleterious effect on the semiconductor device being fabricated.” *Id.* at 5:22–62.

Figure 2b of the '611 patent is reproduced below.

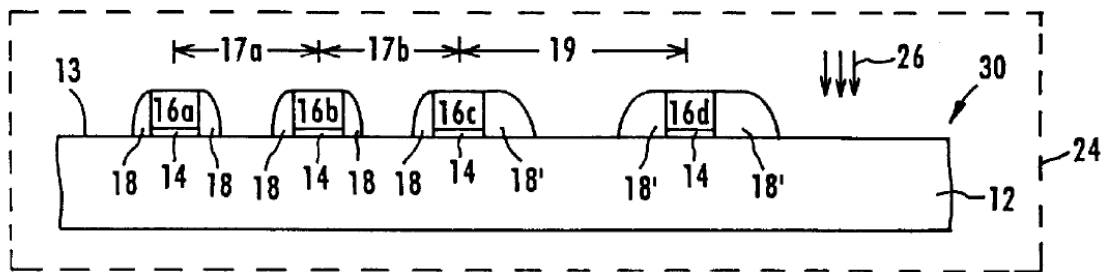


Fig. 2b (PRIOR ART)

Figure 2b, above, shows a portion of a prior-art semiconductor device following formation of spacers 18, 18'. *Id.* at 3:63–65. In the device of Figure 2b, gate conductors 16a, 16b, 16c, 16d are formed on substrate 12. *Id.* at 5:23–26. The center points of gate conductors 16a and 16b are separated by space 17a; the center points of gate conductors 16b and 16c are

separated by space 17b; the center points of gate conductors 16c and 16d are separated by space 19. *Id.* at 5:26–33. As seen in Figure 2b, space 19 is larger than spaces 17a and 17b. *Id.* at 5:31. As a result, “the spacers 18’ formed within second space 19 are differently shaped and have a wider width at their base than the spacers 18 formed, for example, in first spaces 17a and 17b.” *Id.* at 5:51–54 (emphasis omitted).

In order to solve this problem, the ’611 patent teaches using non-operational transistor gate arrangements to divide the larger space into more equal smaller spaces, “to provide more uniformity in the spaces/aspect ratios between gate conductors.” *Id.* at 6:9–25.

Figures 4a and 4b of the ’611 patent are reproduced below.

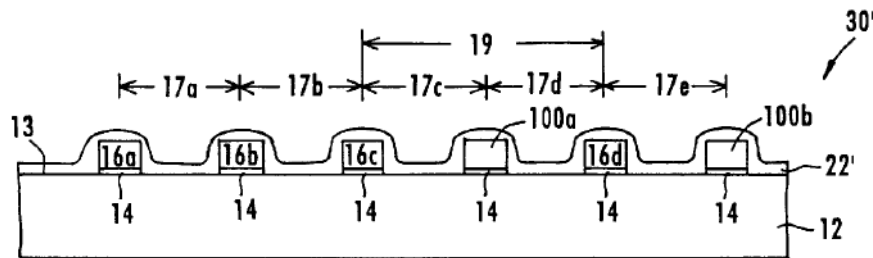


Fig. 4a

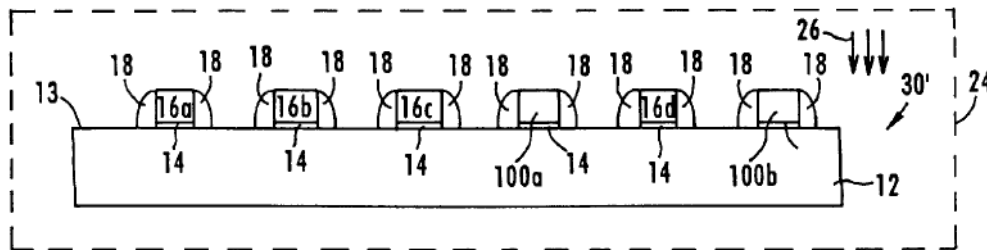


Fig. 4b

Figures 4a and 4b, above, show steps in a process for forming “substantially uniformly sized spacers” in a semiconductor device, in accordance with embodiments of the ’611 patent. *Id.* at 4:3–13. In the device of Figure 4a, gate conductors 100a, 100b are formed on substrate 12, in addition to gate

conductors 16a, 16b, 16c, 16d previously described with respect to the prior art device of Figure 2b. *Id.* at 6:9–14. The addition of gate conductor 100a, for example, “effectively divide[s] second space 19 into two first spaces 17c and 17d, which are each substantially equivalent to first spaces 17a and 17b.” *Id.* at 6:15–17 (emphasis omitted). As described in the ’611 patent, “[t]he result of adding these additional non-operational transistor gate arrangements is that the topology . . . has been altered to provide more uniformity in the spaces/aspect ratios between gate conductors.” *Id.* at 6:21–25.

Shown in Figure 4a, dielectric layer 22’ is deposited over substrate 12 and gate conductors 16a, 16b, 16c, 16d, 100a, 100b, using conventional processes. *Id.* at 6:26–30. Shown in Figure 4b, dielectric layer 22’ is subjected to anisotropic etching plasma 26, resulting in the formation of spacers 18. *Id.* at 6:34–40. Due to the uniformity in the spaces/aspect ratios between gate conductors in this embodiment, spacers 18 “have substantially uniformly sized widths.” *Id.* at 6:47–49. In turn, “the source and drain regions 20a and 20b [of the semiconductor device] (not shown in FIG. 4b) will be more uniformly shaped and sized.” *Id.* at 6:49–51 (emphasis omitted). Non-operational gate conductors 100a, 100b may be removed (*id.* at 6:52–63, Fig. 5a), or may remain in the complete semiconductor device (*id.* at 6:64–7:2).

C. Illustrative Claim

Of the challenged claims, claims 1, 8, and 15 are independent. Claims 2–5 depend, directly or indirectly, from claim 1, and claims 9–12

depend directly from claim 8. Independent claim 1 of the '611 patent is illustrative of the challenged claims and is reproduced below.

1. A method for forming substantially uniformly sized spacers on transistor gate arrangements within semiconductor devices on a common substrate, the method comprising:

forming a plurality of gate arrangements on a top surface of the substrate, wherein two of the plurality of gate arrangements are positioned parallel to one another and separated by a defined space;

forming a dielectric layer over at least a portion of the two gate arrangements and at least a portion of the defined space;

removing portions of the dielectric layer to form a plurality of spacers, wherein each of the plurality of spacers physically contacts one of the two gate arrangements and the substrate, and wherein the spacers located within the defined space each have a base width that is approximately the same;

configuring one of the two gate arrangements to control an electrical current between a source region and a drain region formed in the substrate; and

configuring the remaining one of the two transistor gate arrangements to be non-operational.

Ex. 1001, 7:65–8:18.

D. References Relied Upon by Petitioner

Petitioner relies on the following references. Pet. 19–20.

Reference	Publication Date / Issue Date	Exhibit
JP Pub. No. H02-37725 (“Yonemaru”)	Feb. 7, 1990	Ex. 1005; Ex. 1006 ²

² Petitioner provides the original Japanese language document (Ex. 1005) and a certified translation thereof (Ex. 1006). Citations to Yonemaru are to the translation.

Reference	Publication Date / Issue Date	Exhibit
JP Publ. No. H09-64195 (“Haribuchi”)	Mar. 7, 1997	Ex. 1007; Ex. 1008 ³
U.S. Patent No. 5,019,527 (“Ohshima”)	May 28, 1991	Ex. 1009
U.S. Patent No. 5,183,771 (“Mitsui”)	Feb. 2, 1993	Ex. 1010
JP Publ. No. H08-213605 (“Nishikakawa”)	Aug. 20, 1996	Ex. 1011; Ex. 1012 ⁴

Petitioner groups the references into Dummy Gate References⁵ and Spacer References⁶ when presenting its grounds. Pet. 10–19, 20–66. Petitioner relies on Admitted Prior Art (“APA”)⁷ to support its assertions. Petitioner also relies on the Declarations of Dean Neikirk, Ph.D. (Ex. 1004; Ex. 1020)

³ Petitioner provides the original Japanese language document (Ex. 1007) and a certified translation thereof (Ex. 1008). Citations to Haribuchi are to the translation.

⁴ Petitioner provides the original Japanese language document (Ex. 1011) and a certified translation thereof (Ex. 1012). Citations to Nishikakawa are to the translation.

⁵ Petitioner characterizes Yonemaru and Haribuchi as the “Dummy Gate” references. See Pet. 10–15. Petitioner cites to each of these references as disclosing the relevant claim features. See *id.* at 23–43. As stated in the Institution Decision, we view Petitioner’s asserted ground as being in view of the Admitted Prior Art and Yonemaru or Haribuchi. Inst. Dec. 9 n.8. Below, we address Patent Owner’s challenge to that finding.

⁶ Petitioner characterizes the Admitted Prior Art, Haribuchi, Ohshima, Mitsui, and Nishikakawa as the “Spacer References.” See Pet. 15–19.

⁷ Petitioner relies on Figures 2a and 2b of the ’611 patent, which are identified as prior art, and the corresponding discussion thereof. See Pet. 4–5, 9, 21–66. Patent Owner does not contest Petitioner’s reliance on Figures 2a and 2b as prior art forming the basis of Petitioner’s Ground 1 challenge. Tr. 23:12–17; see generally PO Resp.

to support its positions. Patent Owner relies on the Declaration of W. R. Bottoms, Ph.D. (Ex. 2001) to support its positions.

E. Instituted Grounds of Unpatentability

We instituted an *inter partes* review of claims 1–5, 8–12, and 15 of the '611 patent on the following grounds:

Whether claims 1–4, 8–11, and 15 would have been obvious under 35 U.S.C. § 103(a) in view of the Admitted Prior Art and Yonemaru or Haribuchi;

Whether claims 5 and 12 would have been obvious under 35 U.S.C. § 103(a) in view of the Admitted Prior Art and Yonemaru; and

Whether claims 1–5, 8–12, and 15 would have been obvious under 35 U.S.C. § 103(a) in view of Yonemaru and the Admitted Prior Art, Haribuchi, Ohshima, Mitsui, or Nishikakawa.

Inst. Dec. 22–23.

II. ANALYSIS

A. Claim Construction

The parties agree that the '611 patent expired during this proceeding, and that the claim construction principles outlined in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) apply. Pet. 8; PO Resp. 13–14; *see also* Inst. Dec. 4, 9–10. We, therefore, adopt a district court-type claim construction approach. *In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (“[T]he Board’s review of the claims of an expired patent is similar to that of a district court’s review.”); *see also Black & Decker, Inc. v. Positec USA, Inc.*, 646 F. App’x 1019, 1024 (Fed. Cir. 2016) (holding that in an *inter partes* review, “[c]laims of an expired patent are given their ordinary and customary meaning in accordance with our opinion in [*Phillips*]”).

Under the *Phillips* standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

Petitioner indicates that the “claims’ terms should be construed or understood consistent with their plain and ordinary meanings.” Pet. 8. Patent Owner “agrees with Petitioner[] that all claim terms should be accorded their plain and ordinary meaning as understood by a person having ordinary skill in the art and as consistent with the intrinsic record.” PO Resp. 14. After considering the parties’ arguments and evidence, we determine that it is not necessary to provide an express construction for any claim term for purposes of resolving the controversy. *See, e.g., Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have had a graduate’s degree with some emphasis in semiconductor device fabrication in physics, material science, electrical engineering, or a related degree, or an undergraduate degree in one of these fields and two to three years’ experience in semiconductor device design and fabrication. Such a person would have also had at least a basic understanding, through education or experience, of how different fabrication methods can alter the electrical characteristics of transistors.

Pet. 7–8 (citing Ex. 1004 ¶¶ 21–24).

Patent Owner asserts that a person of ordinary skill in the art would have held a master's degree in physics, electrical engineering or a related field and three years or more experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. (See Ex. 2001 at ¶ 29.) Design experience is necessary with respect to changes in process and parameters in the semiconductor device and to the effects of those changes on the device as a whole. (See, e.g., *id.* at ¶ 36.)

PO Resp. 13.

For the purposes of our Institution Decision, we accepted Petitioner's contentions regarding the level of ordinary skill in the art. Inst. Dec. 11–12. Neither party argues that the outcome of this case would differ based on our adoption of one party's definition over the other, and we see little difference between the parties' definitions. PO Resp. 13; *see generally* Reply. In light of the record now before us and consistent with the Institution Decision, we adopt Petitioner's definition of one of ordinary skill in the art. The level of ordinary skill in the art is also reflected by the references themselves. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (“[T]he absence of specific findings on the level of skill in the art does not give rise to reversible error ‘where the prior art itself reflects an appropriate level and a need for testimony is not shown.’”); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (finding that the Board of Patent Appeals and Interferences did not err in concluding that the level of ordinary skill in the art was best determined by the references of record).

C. Overview of the Asserted References

Below we provide an overview of the Admitted Prior Art, Yonemaru, and Haribuchi. An overview of the remaining references is unnecessary for purposes of this Decision.

1. Admitted Prior Art

As noted above, Petitioner relies on Figures 2a and 2b of the '611 patent, which are expressly identified as prior art, and the corresponding discussion thereof as Admitted Prior Art. *See* Pet. 4–5, 9, 21–66; Ex. 1001, 3:55–4:2, 5:2–6:2, Figs. 1, 2a, 2b, 3. The prior art described in the '611 patent, as illustrated in Figures 2a and 2b, is discussed above. *See supra* Section I.B.

2. Yonemaru (Ex. 1006)

Yonemaru relates to a manufacturing method for a semiconductor device. Ex. 1006, 1. In particular, Yonemaru describes forming a plurality of transistors, each having the same characteristics, by forming side walls (or, in other words, spacers) having the same shape at the sides of each gate electrode. *Id.* at 2. Yonemaru accomplishes this by using dummy gate electrodes between the gate electrodes. *Id.*

The manufacturing process of Yonemaru is discussed in more detail with respect to Figures 1(A)–1(E). Figure 1(A) is reproduced below.

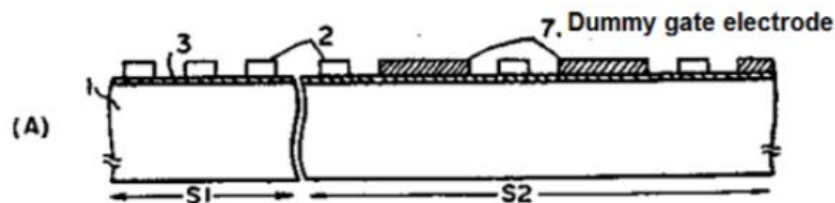


Figure 1(A), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* Gate electrodes 2 and dummy gate electrodes 7 are formed over gate oxide film 3 on semiconductor substrate 1. *Id.* As described in Yonemaru, the spacing between gate electrodes 2 may be 0.9 μm in closely spaced portion S1 and 4.5 μm in widely spaced portion S2. *Id.* Dummy gate electrode 7 is

positioned in such a way as to intervene between gate electrodes 2 at widely spaced portion S2, and, furthermore, is positioned such that its distance from gate electrodes 2 is $0.9\mu\text{m}$, or the distance between gate electrodes 2 at closely positioned portion S1. *Id.* Yonemaru notes that dummy gate electrode 7 serves no purpose in the semiconductor integrated circuit, and is not used as wiring. *Id.* at 3.

After formation of source/drain zone 5 (see *id.* at Fig. 1(B)), a PSG (Phospho Silicate Glass) film, for example, is deposited over the entire surface (*id.* at 2–3), as seen in Figure 1(C), reproduced below.

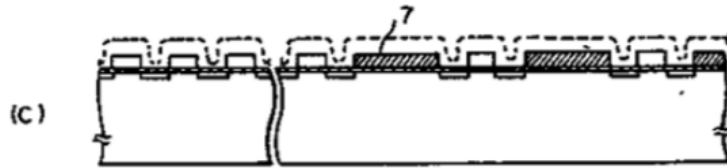


Figure 1(C), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* at 2. As seen in Figure 1(C), the “placement of a dummy gate electrode 7 causes PSG film to be deposited in the same shape at closely spaced portion S1 and widely spaced portion S2.” *Id.* at 3.

Figure 1(D) is reproduced below.

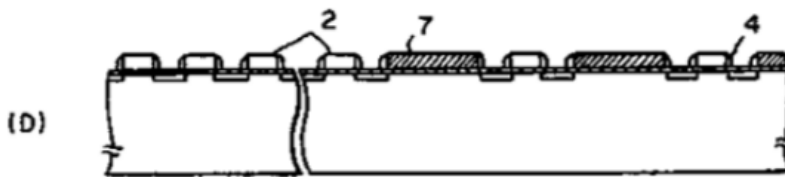


Figure 1(D), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* at 2. As shown in Figure 1(D), side walls 4 are formed at the sides of gate electrodes 2 and dummy gate electrodes 7, by anisotropically etching the

PSG film. *Id.* at 3. Because PSG film has already been deposited in the same shape at both the closely and widely spaced portions S1 and S2 during the above-described process, side wall 4 is also formed to the same shape. *Id.* Source/drain zone 6 (*see id.* at Figure 1(E)) is subsequently formed. *Id.*

3. *Haribuchi (Ex. 1008)*

Haribuchi relates to a method of manufacturing a “semiconductor device having elements with uniform properties . . . irrespective of gate electrode layout.” Ex. 1008, Abstract. Haribuchi accomplishes this goal using “dummy gate electrodes that do not function as gate electrodes” in order to “mak[e] widths of side wall spacers [] of the gate electrodes [] equal . . . , irrespective of the layout density of the gate electrodes.” *Id.*; *see also id.* ¶ 29 (“With the method for manufacturing a field effect semiconductor device as in claim 1, the width of the side wall spaces of the gate electrodes is the same in the first and second areas even if the gate electrode layout density is different in the first and second areas, making it possible to form so-called LDD layers or pocket layers, etc., that have equal channel-length widths in the first and second areas, which makes it possible to manufacture a field effect semiconductor device having elements with uniform properties in an integrated circuit, irrespective of gate electrode layout.”).

The manufacturing process of Haribuchi is discussed in more detail with respect to Figures 1(a)–1(c). Figure 1(a) is reproduced below.

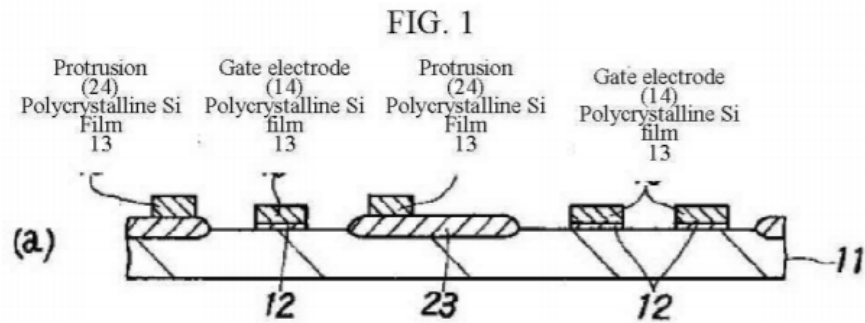


Figure 1(a), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Haribuchi. Gate electrodes 14 and protrusions 24 are formed over SiO₂ gate oxidation film 12 and SiO₂ film 23, respectively, on Si substrate 11. *Id.* ¶¶ 18–19. As described in Haribuchi, “protrusions 24 . . . serve as dummy gate electrodes that do not function as gate electrodes [and] are formed together with gate electrodes 14 . . . resulting in a uniform overall layout density for the gate electrodes 14 and the protrusions 24 in all MOS transistor formation areas. *Id.* ¶ 19.

Thereafter, SiO₂ film 16 is deposited on the entire surface (*see id.* at Fig. 1(b)), and then the entire surface of SiO₂ film 16 is subjected to anisotropic etching, thereby forming side wall spacers 17, as shown in Figure 1(c), reproduced below.

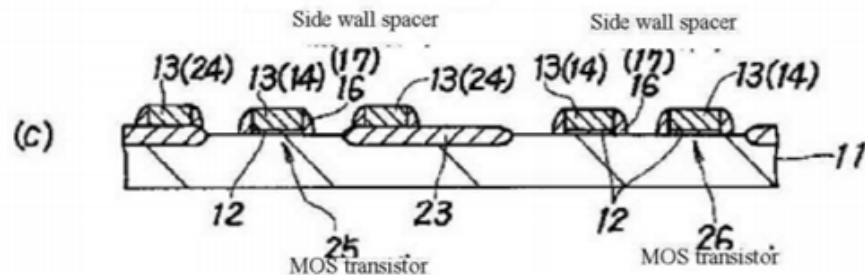


Figure 1(c), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Haribuchi. As described in Haribuchi, “the layout density of the gate electrodes 14 is different between the MOS transistors 25 and 26, but the overall layout density of the gate electrodes 14 and the protrusions 24 is the same where the MOS transistors 25 and 26 are formed, and therefore the width of the side wall spacers 17 is the same in the MOS transistors 25 and 26.” *Id.* ¶ 22. This uniformity of the width of side wall spacers 17 results in MOS transistors 25, 26 “having uniform properties.” *Id.* ¶ 23.

D. Analysis

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We note that, during this proceeding, the parties did not direct our attention to any objective evidence of non-obviousness.

An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic*

Tech., Inc., 504 F.3d 1249, 1259 (Fed. Cir. 2007). A prima facie case of obviousness is established when the prior art, itself, would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. See *In re Rinehart*, 531 F.2d 1048, 1051 (CCPA 1976).

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Petitioner must demonstrate obviousness by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); see also *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). A party that petitions the Board for a determination of obviousness must show that “a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *Procter & Gamble Co. v. Teva Pharm. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (quoting *Pfizer, Inc. v. Apotex, Inc.*, 408 F.3d 1348, 1361 (Fed. Cir. 2007)). We analyze both parties’ arguments, below, in accordance with the above-stated principles.

1. Instituted Grounds

Patent Owner argues that the Board instituted trial on grounds not identified in the Petition. PO Resp. 18–20. More particularly, Patent Owner argues that the Board deviated from the grounds asserted in the Petition by instituting on three grounds, rather than two, and by allegedly redefining the grounds as based on the Dummy Gate References and Spacer References in

the alternative, rather than in combination. *Id.* at 18–19. Petitioner responds that the Board, rather than redefining Petitioner’s arguments, merely accepted Petitioner’s arguments based on Yonemaru and Haribuchi redundantly teaching the same technique to create uniformly-sized sidewall spacers. Reply 10.

Because we do not reach Petitioner’s challenge based on Yonemaru in view of the Spacer References, we limit our discussion to Petitioner’s challenge based on the APA and the Dummy Gate References, i.e., Petitioner’s Ground 1. We instituted *inter partes* review as we did because Petitioner’s challenge, as presented in the Petition, is based on the APA in view of the Dummy Gate references, where the Dummy Gate References—Yonemaru and Haribuchi—are relied upon as each disclosing the relevant claimed features. Pet. 21–43; Inst. Dec. 9 n.8. Petitioner relies on the combination of APA and Yonemaru to teach the limitation of claims 5 and 12. Pet. 30–31, 37–38; Inst. Dec. 19. Given that claim 5 depends from claim 1, Petitioner’s challenge against claim 5 incorporates by reference the challenge against claim 1, which includes arguments based on the disclosures of each of Yonemaru and Haribuchi. Pet. 24–28 (for claim 1), 30–31 (for claim 5). The same is true for the challenge raised against claim 12, which depends from claim 8 and, thereby, incorporates by reference arguments made in connection with the independent claim. *Id.* at 31–35 (for claim 8), 37–38 (for claim 12). Thus, our Institution Decision does not deviate from the grounds presented by Petitioner in the Petition.

2. Asserted Obviousness Based on the Admitted Prior Art and the Dummy Gate References

Petitioner asserts that claims 1–5, 8–12, and 15 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of the Admitted Prior Art and the Dummy Gate References. Pet. 21–43.⁸

According to Petitioner, one of ordinary skill in the art would have been motivated to modify the Admitted Prior Art in view of either Yonemaru or Haribuchi in order to overcome problems in the Admitted Prior Art design. *Id.* at 21. “All three references recognize a desire to fabricate transistors with uniform characteristics.” *Id.* (citing Ex. 1001, 1:37–39; Ex. 1006, 122 (Problem to be Solved); Ex. 1008, Abstract). Further, each of Yonemaru and Haribuchi teaches that “[u]niformity among spacers leads to uniform transistor characteristics.” *Id.* (citing Ex. 1006, 123 (Benefits of Invention); Ex. 1008 ¶ 23).

Petitioner provides an illustration of the resulting structure, when the teachings of the Dummy Gate References are applied to the Admitted Prior Art design (Pet. 22), reproduced below:

⁸ As discussed herein, Petitioner did not argue in its Petition that claims 5 and 12 would have been obvious over the APA and Haribuchi. We, therefore, instituted trial on the grounds of (1) whether claims 1–4, 8–11, and 15 would have been obvious under 35 U.S.C. § 103(a) in view of the Admitted Prior Art and Yonemaru or Haribuchi; and (2) whether claims 5 and 12 would have been obvious under 35 U.S.C. § 103(a) in view of the Admitted Prior Art and Yonemaru. Inst. Dec. 19, 22.

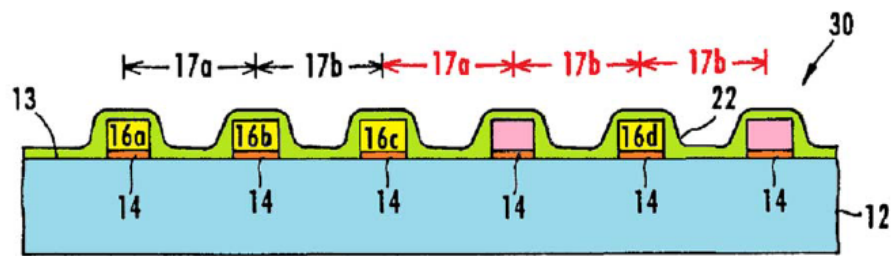


Fig. 2a (PRIOR ART)

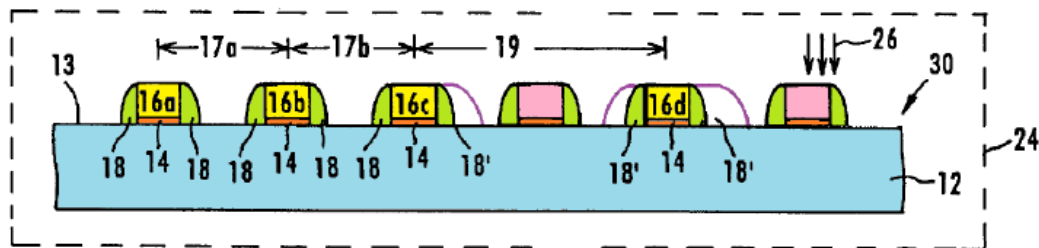


Fig. 2b (PRIOR ART)

Figures 2a and 2b, above, show a portion of the Admitted Prior Art semiconductor device as modified by Petitioner with the teachings of the Dummy Gate References. See Pet. 21–22. In Petitioner’s combination, “non-operational gates (pink) are interspersed among traditional operational gates 16a-16d [(yellow)] at uniform spacing 17a, 17b (red).” *Id.* at 21. According to Petitioner, when dielectric layer 22 (green, Fig. 2a) is formed over the gates and then etched to form side wall spacers 18 (green, Fig. 2b), the spacers have uniform size and shape due to the uniform spacing among operational and non-operational gates. *Id.* at 21–22 (citing Ex. 1004 ¶ 75). The purple lines in Petitioner’s modified and annotated Figure 2b show the size of spacers in the original, unmodified Figure 2b of the ’611 patent. *Id.* at 22.

Petitioner provides a claim chart identifying disclosures in the Admitted Prior Art, as well as in Yonemaru and Haribuchi, for each element

of claims 1–5, 8–12, and 15. *Id.* at 22–43.⁹ Petitioner also relies on the testimony of its declarant, Dr. Neikirk. *Id.*; Ex. 1004 ¶¶ 78–132, 135–168, 170–201, 203–229, 231–287. More particularly, Petitioner argues that all three references recognize a desire to fabricate transistors with uniform characteristics. Pet. 21 (citing Ex. 1001, 1:37–39; Ex. 1006, 122; Ex. 1008, Abstract). Because Yonemaru and Haribuchi both provide “dummy gates to create uniform spacing among all gates,” and because uniformity among spacers “leads to uniform transistor characteristics,” Petitioner argues that one of ordinary skill in the art “would recognize immediately that Yonemaru’s and Haribuchi’s solutions would overcome problems in the Admitted Prior Art design.” *Id.* (citing Ex. 1004 ¶ 74; Ex. 1006, 123; Ex. 1008 ¶ 23).

a. Patent Owner’s First Argument

Patent Owner argues that Petitioner fails to identify with particularity the grounds on which the challenge is based. PO Resp. 21. More specifically, Patent Owner argues that Petitioner fails “to identify with particularity the grounds on which the challenge to each claim is based” as well as “the evidence that supports the grounds for the challenge.” *Id.* at 20 (citing 35 U.S.C. § 312(a)(3)). Patent Owner also argues that Petitioner fails to “provide a limitation by limitation analysis that identifies what limitations are taught by the APA, what limitations are not taught by the APA, identifying where the missing limitations are disclosed in Yonemaru and Haribuchi,” and then fails to identify “why a POSA would be motivated to

⁹ As noted, for claims 5 and 12, Petitioner relies only on the combination of the Admitted Prior Art and Yonemaru (*see* Pet. 30–31, 37–38). Inst. Dec. 19, 22.

make the combination of the missing limitation supplied by Yonemaru and Haribuchi with the admitted prior art, along with establishing a reasonable expectation of success.” *Id.* at 22. Patent Owner also alleges that Petitioner arrives at its “altered figures” using “hindsight methodology” and ignoring the full teachings of Yonemaru and Haribuchi. *Id.* at 23.

Petitioner replies that the Petition presented a proper obviousness challenge. Reply 4. More particularly, Petitioner points to portions of the Petition that Petitioner asserts demonstrate “that Yonemaru and Haribuchi redundantly teach to intersperse dummy gates among operational gates in a manner that creates uniform density of the gates overall, which leads to uniform sidewall sizes,” and “this teaching would motivate a POSITA to modify the APA to cure the same problems.” *Id.* (citing Pet. 9–15, 21–22, 23–43). Petitioner denies that its challenges are based on hindsight reasoning, because “Yonemaru’s and Haribuchi’s teachings to provide uniform distribution among dummy gates and operational gates are repeated throughout each reference.” *Id.* at 5. Petitioner insists that the specific features of Yonemaru and Haribuchi emphasized by Patent Owner, such as Yonemaru’s oxide film, “have no role in creating uniformly-sized spacers,” but rather, “both references teach that uniformly-sized spacers results from a uniform distribution of dummy gates and operational gates.” *Id.* at 7. We agree with Petitioner.

Regarding Petitioner’s presentation of its obviousness challenge, we are persuaded that Petitioner has identified with sufficient particularity where and how the limitations of the claims are taught by the prior art, and that the Petition complies with § 312(a)(3). *See* Pet. 21–43. Petitioner’s case is premised for the most part on the disclosures of the APA. Petitioner,

however, relies on Yonemaru and Haribuchi to teach uniformly positioned gates. Petitioner’s claim chart identifies the portions of the APA that Petitioner asserts meet the limitations of the challenged claims, and the portions of Yonemaru and/or Haribuchi that meet the remaining limitations of the challenged claims. *See id.* at 23–43. We are also persuaded that Petitioner has articulated with sufficient particularity its contention as to why one of ordinary skill in the art would have been prompted to combine the references in the manner proposed by Petitioner. Pet. 21–22 (citing Ex. 1004 ¶¶ 73–75).

We, thus, are not persuaded by Patent Owner’s argument that the Petition fails to identify adequately the evidence that supports the challenge, or otherwise fails to comply with § 312(a)(3). Petitioner has made its case by a preponderance of the evidence, by clearly identifying the portions of the respective references on which it relies, and also by articulating “specific reasoning, based on evidence of record, to support the legal conclusion” that one of ordinary skill in the art, given the teachings of the APA, would have appreciated that more uniform distribution of gates explicitly shown by Yonemaru and Haribuchi is advantageous. *See Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

b. Patent Owner’s Second Argument

Patent Owner argues that the proposed combination “fails to disclose each limitation of the challenged claims,” namely, the limitation of “removing portions of the dielectric layer to form a plurality of spacers, wherein each of the plurality of spacers physically contacts one of the two gate arrangements and the substrate, and wherein the spacers located within the defined space each have a base width that is approximately the same.”

PO Resp. 30–31. More particularly, Patent Owner argues that “neither Yonemaru nor Haribuchi teaches the required dielectric removing step that results in spacers that physically contact the substrate,” and that neither Yonemaru nor Haribuchi discloses or suggests that non-operable gate arrangements are “freely applicable” to gate forming processes, such as the APA, where there is no gate oxide beneath the spacers. *Id.* at 31. Patent Owner argues that Haribuchi teaches away from forming non-operable gate arrangements having spacers directly contacting the substrate, because it teaches *operable* gates with spacers in direct contact with the substrate, not *non-operable* gates with spacers in direct contact with the substrate. *Id.* at 31–32.

Petitioner counters that Patent Owner “refuses to acknowledge that [the APA] provides sidewall spacers in physical contact with a semiconductor substrate.” Reply 6. Petitioner also criticizes Patent Owner for placing “undue emphasis on the individual implementations disclosed by Yonemaru and Haribuchi; implementations that have no role in creating uniformly sized spacers.” *Id.* at 7. Petitioner reiterates that the Petition explains that “the APA design forms sidewall spacers 18, 18’ in physical contact with operational transistor gates 16 and a substrate 12” but that the sidewall spacers 18, 18’ have non-uniform sizes. *Id.* at 8. Petitioner also notes, however, that “Yonemaru and Haribuchi each teach to distribute dummy gates among operational gates so that there is even spacing among the gates and that doing so causes sidewall spacers to have uniform sizes.” *Id.* (citing Pet. 26; Ex. 1001, Figs. 1, 2b; Ex. 1006, 122; Ex. 1008 ¶¶ 19, 22). Regarding Patent Owner’s teaching away argument, Petitioner counters that Haribuchi “places no significance on isolating protrusions from the

substrate,” but rather teaches that “uniform layout density among gate electrodes 14 and dummy gates 24 includes uniformly-sized sidewall spacers 17.” *Id.* at 9.

We agree that Petitioner’s case is premised on the APA’s teaching of nearly every limitation of the challenged claims, but that Petitioner relies on the Dummy Gate References to provide uniform spacing among all gates by using dummy gates, leading to equally sized sidewall spacers. *See, e.g.*, Pet. 21, 25–27; Reply 1, 8. Petitioner relies on the APA to disclose

removing portions of the dielectric layer 22 to form a plurality of spacers 18 (green), wherein each of the plurality of spacers physically contacts [one of] the [two] gate arrangements (yellow, pink) and the substrate 12 (blue), and wherein the spacers located within the spaces 17a, 17b each have a base width that is approximately the same.

Pet. 25–26 (citing Ex. 1001, 5:3–62, 5:41–48). Patent Owner does not dispute, and we find Petitioner has shown by a preponderance of the evidence, that the APA teaches all limitations of the claims, except for the non-operable gates. Petitioner relies on the teachings of Yonemaru and Haribuchi in combination with the APA, as shown in Petitioner’s modified Fig. 2b, to demonstrate that the resulting combination would result in spacers each having a base width that is approximately the same (*id.* at 22), and on Yonemaru to demonstrate that “sidewalls 4 are formed with the same shapes therein” (*id.* at 26 (emphasis omitted) (citing Ex. 1006, 123)).

We acknowledge Patent Owner’s arguments that the teachings of Yonemaru and Haribuchi are not “freely applicable” to gate arrangements such as those disclosed in the APA (PO Resp. 31) and that the combination does not result in the claimed invention because the dummy gates of

Yonemaru and Haribuchi have oxide beneath the spacers (*id.* at 32). Petitioner, however, argues that all three references “recognize a desire to fabricate transistors with uniform characteristics” (Pet. 21 (citing Ex. 1001, 1:37–39; Ex. 1006, 122 (Problem to be Solved); Ex. 1008, Abstract)), and Yonemaru and Haribuchi teach generally that “[u]niformity among spacers leads to uniform transistor characteristics.” *Id.* (citing Ex. 1006, 123 (Benefits of Invention); Ex. 1008 ¶ 23). We find that Petitioner’s reliance on Yonemaru and Haribuchi is directed to their teachings of spacing arrangements, which Petitioner has shown are applicable to the APA’s gate formation process. More particularly, Petitioner has demonstrated by a preponderance of the evidence that the “uniformity among spacers” teachings of Yonemaru and Haribuchi are directly applicable to the gate formation process of the APA, and that one of ordinary skill in the art would have been motivated to apply these teachings in the manner proposed by Petitioner. Pet. 21–22; Ex. 1004 ¶¶ 73–75 (describing fabrication of dummy gates in the proposed combination); Reply 3–4 (citing Ex. 1006, 122; Ex. 1008 ¶ 22). We also find that Petitioner has demonstrated that the gate oxide beneath the spacers is not critical for Yonemaru’s and Haribuchi’s teachings as they pertain to the proposed combination, because one of ordinary skill would have understood that spacers do not necessarily need to be isolated from a substrate by a gate oxide layer, as shown in the APA. Pet. 9 (citing Ex. 1004 ¶¶ 36–38); 21–22; annotated Figs. 2a, 2b; Reply 6. Petitioner also has demonstrated that neither Yonemaru nor Haribuchi place any specific emphasis on having a gate oxide layer between the spacers and the substrate vis-à-vis solving the problem of uniformly-sized spacers. Tr. 6:11–24; Reply 6–7 (citing Ex. 1006, 121; Ex. 1008 ¶¶ 19, 22). We

further find that Petitioner demonstrates that one of ordinary skill in the art would have been motivated to improve the APA design with the techniques taught by Haribuchi and Yonemaru, namely, providing dummy gates as a solution to non-uniform sidewall sizing in operational transistors, and that this combination proposed by Petitioner would result in the claimed invention. Pet. 21–22; Reply 3; Ex. 1004 ¶¶ 73–75. Thus, we find that Petitioner has proven by a preponderance of the evidence that Yonemaru and Haribuchi teach the limitations not provided by the APA, and that one of ordinary skill in the art would have been prompted to combine them with reasonable expectation of success. Pet. 21.

Additionally, we find that Haribuchi does not teach away from forming non-operable gate arrangements having spacers directly contacting the substrate. Specifically, we find that while Haribuchi does convey a particular method of forming operable and non-operable gates, it does not expressly criticize, discredit, or otherwise discourage forming non-operational gates having spacers directly contacting the substrate, as required for a “teaching away.” “A reference does not teach away ‘if it merely expresses a general preference for an alternative invention but does not “criticize, discredit, or otherwise discourage” investigation into the invention claimed.’” *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018) (citing *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009)).

We also have reviewed Petitioner’s contentions and supporting evidence regarding claims 2–5, 8–12, and 15. Pet. 21–22 (citing Ex. 1004 ¶¶ 73–75), 28–43. Other than arguments directed primarily to claim 1, which we have discussed above, Patent Owner does not present additional

arguments as to these remaining claims. See PO Resp. 33. Based on the record now before us, we are persuaded that Petitioner has shown by a preponderance of the evidence that the combination of the APA and Yonemaru or Haribuchi renders obvious claims 1–4, 8–11, and 15 (Pet. 21–43 (citing Ex. 1001, 5:3–62, Fig. 2a, 2b (modified); Ex. 1006, 121–123, Fig. 1D; Ex. 1008 ¶¶ 15, 18–20, Fig. 2; Ex. 1004 ¶¶ 78–132 (claim 1), 135–143 (claim 2), 144–151 (claim 3), 152–160 (claim 4), 170–201 (claim 8), 203–212 (claim 9), 213–219 (claim 10), 220–229 (claim 11), 236–287 (claim 15)), and that the combination of the APA and Yonemaru renders obvious claims 5 and 12. Pet. 30–31 (citing Ex. 1004 ¶¶ 161–168; Ex. 1006, Fig. 1D), 37–38 (citing Ex. 1004 ¶¶ 231–235; Ex. 1006, Fig. 1D).

3. Obviousness Based on Yonemaru and the Spacer References

Petitioner asserts that claims 1–5, 8–12, and 15 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Yonemaru and the Spacer References. Pet. 20, 43–66.

As discussed in Section II.D.2, *supra*, we conclude Petitioner has shown by a preponderance of evidence that claims 1–4, 8–11, and 15 are unpatentable as obvious over the APA and Yonemaru or Haribuchi, and that claims 5 and 12 are unpatentable as obvious over the APA and Yonemaru. This conclusion is dispositive of Petitioner’s challenge to the patentability of all challenged claims. Accordingly, we decline to address whether Petitioner has further shown, by a preponderance of evidence, that the challenged claims are also unpatentable as obvious over Yonemaru and the Spacer References. See *Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue because doing so “can not only save the

parties, the [agency], and [the reviewing] court unnecessary cost and effort,” but can “greatly ease the burden on [an agency] faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits”).

III. CONCLUSION

After considering the parties’ arguments and evidence, we are persuaded that Petitioner has shown by a preponderance of the evidence that a person having ordinary skill in the art would have combined the teachings of the APA and the Dummy Gate References in the manner proposed by Petitioner. We conclude that Petitioner has satisfied its burden of demonstrating, by a preponderance of the evidence, that the subject matter of claims 1–5, 8–12, and 15 of the ’611 patent is unpatentable under 35 U.S.C. § 103(a) as obvious in view of the APA and the Dummy Gate References.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner establishes, by a preponderance of the evidence, that claims 1–5, 8–12, and 15 of U.S. Patent No. 6,103,611 are unpatentable; and

FURTHER ORDERED that this is a Final Written Decision; therefore, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01872
Patent 6,103,611

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