

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION and
RENESAS ELECTRONICS AMERICA INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

IPR2017-01989
Patent 6,153,933

Before GRACE KARAFFA OBERMANN, KEVIN C. TROCK, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–4 (“the challenged claims”) of U.S. Patent No. 6,153,933 (Ex. 1001, “the ’933 patent”) are unpatentable.

A. Background

Renesas Electronics Corporation and Renesas Electronics America Inc. (collectively, “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–4 of the ’933 patent pursuant to 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Petitioner also filed the supporting Declaration of Dean Neikirk, Ph.D. (Ex. 1006) (“Neikirk Declaration”). Lone Star Silicon Innovations LLC (“Patent Owner”) filed a notice indicating an election to waive filing a preliminary response to the Petition. Paper 5. Pursuant to 35 U.S.C. § 314(a), on April 6, 2018, we instituted *inter partes* review on the following grounds:

whether claims 1–4 would have been anticipated under
35 U.S.C. § 102(e) by Kimura¹;

whether claims 1–4 would have been anticipated under
35 U.S.C. § 102(a) by Yoshihara²; and

¹ U.S. Patent No. 5,869,392, issued February 9, 1999 (Ex. 1011).

² Japanese Unexamined Patent Application Publication No. H08-293561, published November 5, 1996 (Ex. 1012). We refer to the English translation (Ex. 1013) of the original reference herein.

whether claims 1–4 would have been anticipated under
35 U.S.C. § 102(b) by Kubo³.

See Paper 6 (“Inst. Dec.” or “Dec.”).

In the Institution Decision, we declined to institute the ground for claims 1–4 under 35 U.S.C. § 103(a) in view of Admitted Prior Art and “Planarization References⁴” because we found that the Petition was deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a). Dec. 8–11.

On April 24, 2018, the Supreme Court held that a final written decision in an *inter partes* review must decide the patentability of all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (“SAS”). Pursuant to SAS, on May 3, 2018, we instituted *inter partes* review on all claims and all grounds. Paper 8.

Patent Owner filed a Patent Owner Response (Paper 20, “PO Resp.”). Patent Owner also filed the supporting Declaration of W.R. Bottoms, Ph.D. (“Bottoms Declaration”). Ex. 2001. Petitioner filed a Reply (Paper 22, “Pet. Reply”) to the Patent Owner Response. Petitioner also filed the supporting Reply Declaration of Dean Neikirk, Ph.D. (“Reply Neikirk Declaration”). (Ex. 1019).

³ Japanese Unexamined Patent Application Publication No. JPH08-153784, published June 11, 1996 (Ex. 1014). We refer to the English translation (Ex. 1015) of the original reference herein.

⁴ The Petition refers to the “Planarization References” as “Leidy, Tottori, Kimura, Yoshihara, and Kubo.” Pet. 12, 29. “Leidy” is U.S. Patent No. 5,710,460, issued January 20, 1998 (Ex. 1009). “Tottori” is U.S. Patent No. 5,479,054, issued December 26, 1995 (Ex. 1010).

An oral hearing was held on December 17, 2018. A transcript of the hearing is included in the record. Paper 28 (“Tr.”).⁵

B. Related Proceedings

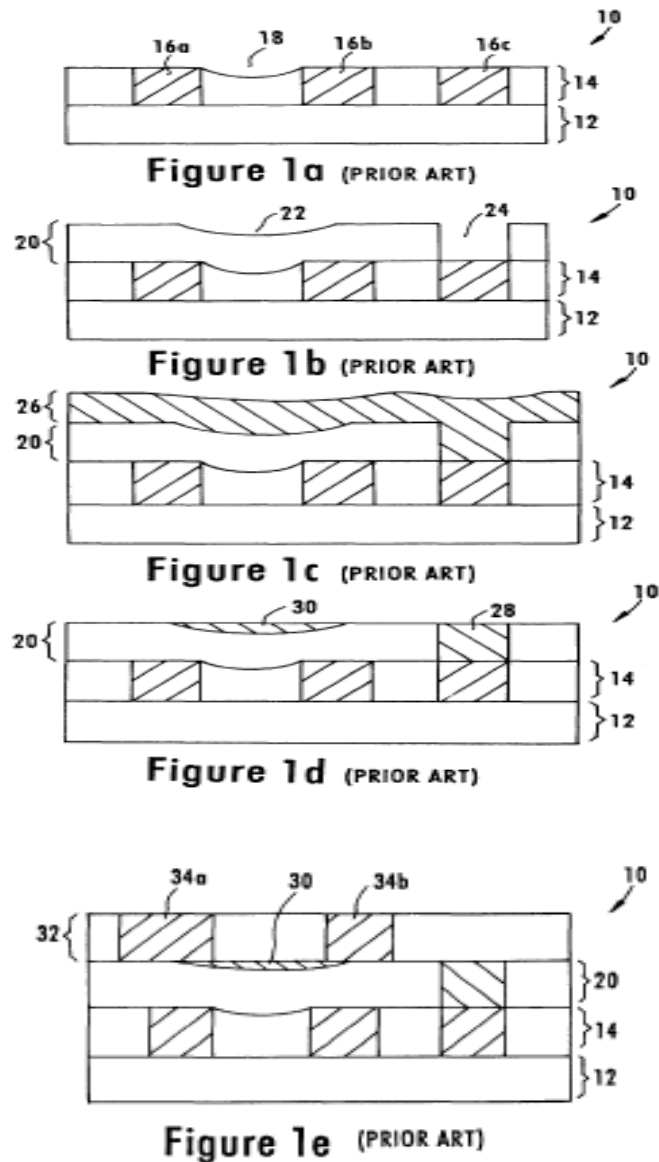
Petitioner indicates that the ’933 patent is asserted in *Lone Star Silicon Innovations, LLC v. Renesas Electronics Corp.*, C.A. No. 3:17-cv-0398 (N.D. Cal.). Pet. 2. Petitioner indicates that a petition for *inter partes* review of claims 5–12 of the ’933 patent (Case IPR2017-02123), has been filed. Pet. 2. The Final Written Decision in IPR2017-02123 is being issued concurrently with this decision.

C. The ’933 Patent

The ’933 patent is titled “Elimination of Residual Materials in a Multiple-Layer Interconnect Structure” and issued on November 28, 2000 from an application filed on September 5, 1997. Ex. 1001, [22], [45], [54].

The ’933 patent is directed generally to methods for forming multiple layer interconnect structures in an integrated circuit. Ex. 1001, Abstract. More specifically, the ’933 patent is directed to improvements to methods for forming multiple layers to avoid potential failure mechanisms due to irregularities in a lower interconnect structure being carried over to a higher interconnect layer. *Id.* at 1:47–53. Figures 1a to 1e, reproduced below, depict conventionally-known steps in forming multiple layer interconnect structures.

⁵ A consolidated hearing was conducted for this case and related Case IPR2017-02123, with a separate hearing for unrelated Case IPR2017-02124 conducted on the same day.



As depicted in Figure 1a, cross-section of portion 10 of a semiconductor wafer is fabricated with wafer stack 12, first dielectric layer 14, and first conductor plugs 16a, 16b, and 16c. Ex. 1001, 3:38–42. The surface of first dielectric layer 14 may have first layer depression 18. *Id.* at 4:8–12.

Figure 1b depicts patterned second layer dielectric layer 20 formed on first dielectric layer 14, that shows second layer depression 22 as formed by the conformable deposition over first layer depression 18. *Id.* at 4:17–24. As

shown in Figure 1c, second layer dielectric 20 is covered with second layer conductor 26 that fills etched opening 24. *Id.* at 4:26–30. As depicted in Figure 1d, second layer dielectric 20 is planarized, leaving second layer conductor plug 28 in etched opening 24, and second layer residual material 30 in second layer depression 22. *Id.* at 4:31–35. Second layer residual material 30, as shown in Figure 1e, can detrimentally affect the structure and resulting electrical properties of subsequently formed interconnect layers, such as a third layer interconnect that includes third layer dielectric 32, and can be a failure mechanism. *Id.* at 4:41–46, 4:52–55.

Figures 2a to 2e, reproduced below, depict fabrication steps for embodiments of the '933 patent.

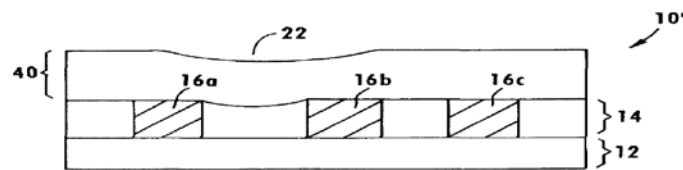


Figure 2a

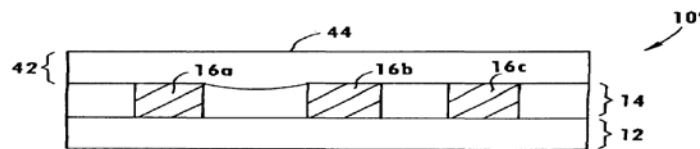


Figure 2b

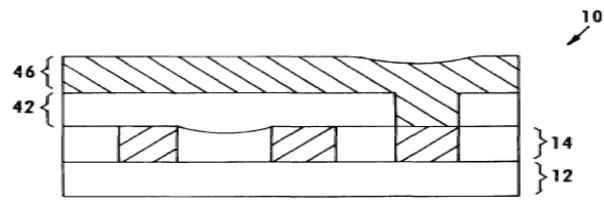


Figure 2c

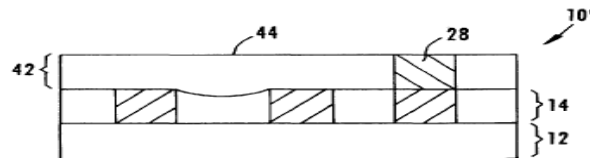


Figure 2d

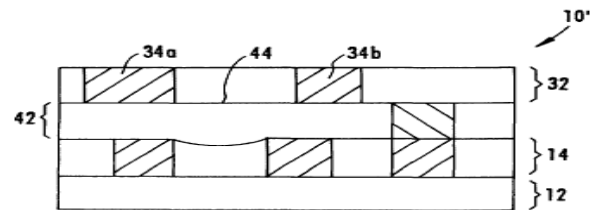


Figure 2e

Similarly to Figures 1a and 1b, Figure 2a depicts a cross-section of a portion 10' of a semiconductor wafer, fabricated with first interconnect layer 14, with first layer depression 18 between plugs 16a and 16b, and covered with second layer dielectric 40 that has second layer depression 22 caused by first layer depression 18. Ex. 1001, 4:56–65. As depicted in Figure 2b, second interconnect layer 40 is reduced in thickness, using planarization techniques, to form planarized second layer dielectric 42 that has substantially planar top surface 44, wherein second layer depression 22 has been eliminated. *Id.* at 5:6–14. In Figure 2c, second layer conductor 46 is deposited on top of planarized second layer dielectric 42, which has been patterned to reveal an etched opening 24, as in Figure 1b. *Id.* at 5:14–16. In Figure 2d, second layer conductor 46 has been planarized down to the planarized second layer dielectric to form second layer conductive plug 28. *Id.* at 5:17–20. “Thus, unlike portion 10 in FIG. 1d, the substantially flat top surface 44 of

planarized second layer dielectric 42 impedes the build-up or formation of any second layer residual materials.” *Id.* at 5:21–24.

Claim 1, the only independent claim of the ’933 patent at issue in the Petition, is reproduced below.

1. An arrangement comprising:
 - a wafer stack;
 - a first interconnect layer formed on the wafer stack, wherein the first interconnect layer includes at least one depression formed in a first dielectric layer; and
 - a second interconnect layer formed on the first interconnect layer, wherein the second interconnect layer includes a substantially planarized top surface located above the first interconnect layer and the depression in the first dielectric layer, the second interconnect layer being substantially free of residual conductive material, wherein the second interconnect layer includes a second dielectric layer and at least one second layer conductor that extends downwardly from the top surface through the second layer dielectric to the first layer interconnect.

Ex. 1001, 5:53–6:12.

II. ANALYSIS

A. The Parties’ Post-Institution Arguments

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 1–4 of the ’933 patent would have been unpatentable under 35 U.S.C. § 102 as anticipated by each of respectively, Kimura, Yoshihara, or Kubo. Dec. 7–21. We now determine whether Petitioner has established by a preponderance of the evidence that claims 1–4 are unpatentable. We previously instructed Patent Owner “that any arguments concerning patentability not raised in the response will be deemed waived.” Paper 7, 3;

see also 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record contains persuasive, un rebutted arguments and evidence presented by Petitioner regarding the manner in which some of the asserted prior art discloses corresponding limitations of claims 1–4. Based on the preponderance of the evidence before us, we conclude that some of the prior art identified by Petitioner discloses all of the limitations of the reviewed claims.

B. Claim Construction

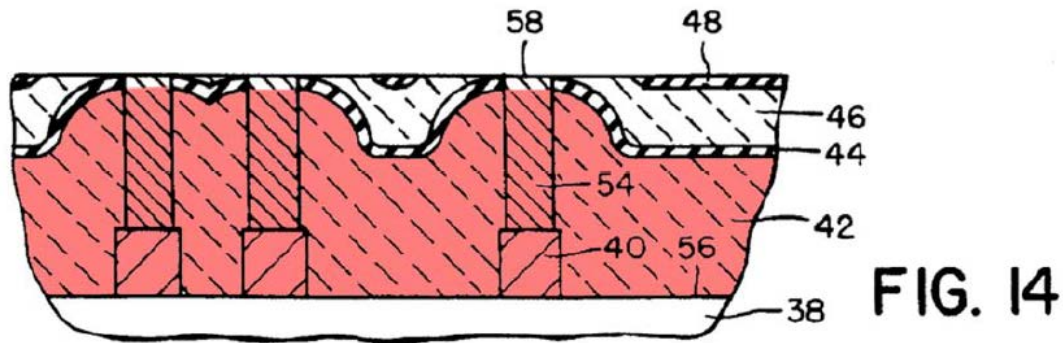
Petitioner indicates that the ’933 patent expired on September 5, 2017, and district court-type claim construction should be used. Pet. 11. Our review of the claims of an expired patent is similar to that of a district court’s review. *Wasica Finance GmbH v. Continental Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017). Specifically, because the expired claims of a patent are not subject to amendment, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed.

Cir. 1996)), that “words of a claim ‘are generally given their ordinary and customary meaning,’” as would be understood by a person of ordinary skill in the art in question at the time of the invention. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1015, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

“interconnect layer”

Petitioner proposes that the term “interconnect layer” be construed as “an interlayer dielectric having metal conductive interconnects therein or therethrough.” Pet. 11 (citing Ex. 1103, 88; Ex. 1006 § V.A). Patent Owner proposes that the correct construction of the term “does not include non-continuous portions of dielectric used to planarize another dielectric layer.” PO Resp. 27–28.

As the basis of its arguments in support of its claim construction, Patent Owner alleges that during the prosecution of the ’933 patent, the applicant distinguished U.S. Patent No. 5,510,652 (“Burke”), which used isolated portions of dielectric materials to fill materials in an interconnect layer. PO Resp. 24 (citing Exs. 1003, 1004). Patent Owner refers to annotated Figure 14 of Burke, reproduced below, arguing that applicant characterized layer 42 as an interconnect layer. *Id.* (citing Ex. 1003, 88).



(Ex. 1004 [FIG. 14] (red annotations illustrate layer 42).)

In view of the annotated cross-section of Figure 14 of Burke, Patent Owner asserts that applicant further argued “that Burke ‘fails to teach a second interconnect layer formed on the first interconnect layer’ and ‘merely describe[s] a complex method of forming a single interconnection layer.’” PO Resp. 24 (citing Ex. 1003, 61). Patent Owner further contends that in its arguments on appeal of the Examiner’s rejection, applicant distinguished structure 46 shown in annotated Figure 14 as not a layer, but as “isolated portions of a relatively soft dielectric material.” *Id.* at 25 (citing Ex. 1003, 88). Patent Owner asserts that applicant “clearly and unequivocally” distinguished Burke’s layer 46, and thereby disclaimed “non-continuous portions of dielectric used to planarize another dielectric layer from the meaning of interconnect layer.” *Id.* at 25–26.

Patent Owner additionally argues that its proposed construction is consistent with the language of claim 1, which includes “a substantially planarized top surface located above the first interconnect layer and the depression in the first dielectric layer.” PO Resp. 26. Patent Owner contends that a construction precluding non-continuous dielectric layers is also consistent with the embodiments disclosed in the specification. *Id.* at 26.

In Reply, Petitioner argues that Patent Owner's proposed interpretation of the claim term should be rejected because, during prosecution, applicant defined the claim "interconnect layer" as follows:

As used throughout the present application, the expression "interconnect layer" is manifestly intended to denote an interlayer dielectric having metal conductive interconnects therein or therethrough.

Pet. Reply 3 (citing Ex. 1003, 116).

Petitioner alleges that applicant never used any "continuous" language in prosecution, nor was there disavowal of any structure that was not continuous. Pet. Reply 3. Petitioner contends that applicant attempted to distinguish Burke on a host of disparate factors, so there can be no finding of a clear, unmistakable disclaimer of subject matter. *Id.* at 3–4. Petitioner further argues that Patent Owner's assertion that Burke's layer 46 is not continuous is incorrect because, besides where it is pierced by other structures, the layer is continuous. *Id.* at 4.

A prosecution history disclaimer must be clear and unambiguous. "[W]hile the prosecution history can inform whether the inventor limited the claim scope in the course of prosecution, it often produces ambiguities created by ongoing negotiations between the inventor and the PTO Therefore, the doctrine of prosecution disclaimer only applies to unambiguous disavowals." *Grober v. Mako Prods., Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012) (citing *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009)); see also *Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1322 (Fed. Cir. 2013). This standard is "exacting." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012).

We find no express disavowal of non-continuous portions of dielectric layers, such as that depicted in Burke, based on the prosecution history relating to interpretation of the claim term “interconnect layer.” We agree with Petitioner that applicant attempted to distinguish Burke on several different factors, including that Burke’s layer 46 is not a layer, Burke’s upper surface includes portions of layer 48 and interconnect 54 so it is not planarized, and also that the layer is not free of residual metal, as required by the claim. Ex. 1003, 88–89. We do not discern from the record that applicant limited the claim scope to a non-continuous layer such as that in Burke or that there was an express disavowal. Nor do we discern, and Patent Owner does not explain, how its arguments apply to embodiments in the specification of the ’933 patent that refer to structures such as “layer interconnects (i.e. dielectric 14 and plugs 16a-c),” which extend through layers, when under Patent Owner’s argument, such layers would appear to be “non-continuous.” See *e.g.*, Ex. 1001, 4:19–20. Similarly, Patent Owner also does not explain how its proposed “non-continuous” limitation could conform to the language of claim 1, which includes a “second layer conductor” extending through “second interconnect layer.”

Instead, we find the statement of applicant’s manifest intent in the prosecution history indicates that the interconnect layer is “an interlayer dielectric having metal conductive interconnects therein or therethrough,” and this represents how the claim term should be construed. See Ex. 1003, 88, 116. We therefore adopt the claim interpretation that an interconnect layer is “an interlayer dielectric having metal conductive interconnects therein or therethrough.”

“depression”

Patent Owner proposes that the term “depression” be interpreted under its plain and ordinary meaning as “a place or part that is lower than the areas which enclose it on all sides.” PO Resp. 28 (citing Ex. 2001 ¶ 116). Patent Owner argues that dictionary definitions support the proposed construction. *Id.* (citing Exs. 2014, 2015). Patent Owner contends that every embodiment in the ’933 patent supports this construction, referring, for instance, to the depression shown in Figure 2e of the ’933 patent. *Id.* Patent Owner also refers to the specification’s explanation that the ’933 patent solves “topographical irregularities carried over to the second interconnect layer from the first layer interconnect, such as for example, ‘depression[s] [are] caused by a scratch, dent, chip, or a previous process step.’” *Id.* at 29 (citing Ex. 1001, 1:65–2:5; Ex. 2001 ¶ 118); *see also* Ex. 1001, 2:48–53, 4:8–16).

Petitioner proposes that the claim term “depression” be interpreted as a “depressed place or part.” Pet. Reply 5. Petitioner argues that nothing in the ’933 patent specification suggests that a depression be surrounded by anything. *Id.* at 4–5. Petitioner further asserts that, when read in light of the specification, a person of ordinary skill in the art “would not conclude that the claimed depressions can refer only to those that are enclosed on all sides.” *Id.* at 5 (citing Ex. 1001, 3:28–30, 4:8–10; Ex. 1019 ¶¶ 16–22). For example, Dr. Neikirk refers to the specification’s disclosure of “topographical irregularities carried over to the second layer interconnect from the first layer interconnect, such as, for example, a depression caused by a scratch, dent, chip, or a previous process step.” Ex. 1019 ¶ 20 (citing Ex. 1001, 1:66–2:2).

Patent Owner’s proposed interpretation is more limited than the plain and ordinary meaning of the term “depression” and its description within the specification. The dictionary definition provided by Patent Owner defines “depression” as “a place or part that is lower than the surrounding area”—and this does not require that a “surrounding area” has to enclose the depression on all sides. Ex. 2014, 1 (definition (3)). The specification also does not require that a depression “caused by a scratch, dent, chip, or a previous process step” be enclosed on all sides. Ex. 1001, 1:66–2:2. For instance, if a scratch on the top of layer 14 of Figure 2b extends through an edge, that scratch or depression would not be enclosed on all sides. We therefore adopt Petitioner’s proposed interpretation that the claim term “depression” be interpreted as a “depressed place or part.”

Other Terms

We determine that no other claim term requires an express construction for the purposes of this Decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

C. Level of Ordinary Skill in the Art

Petitioner’s expert, Dr. Neikirk, testifies that a person of ordinary skill in the art at the time of the ‘933 invention “would have had a graduate’s degree with some emphasis in semiconductor device fabrication in physics, material science, electrical engineering, or a related degree, or an undergraduate degree in one of these fields and two to three years’ experience in semiconductor device design and fabrication,” as well as having “at least a basic understanding, through education or experience, of interconnect structures and techniques for making them.” Ex. 1006 ¶ 23; *see also* Pet. 10.

Patent Owner’s expert, Dr. Bottoms, testifies that one of ordinary skill in the art at the time of the invention of the ’933 patent “would have held a master’s degree in physics, electrical engineering or a related field and three years or more experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices.”

Ex. 2001 ¶ 30; *see also* PO Resp. 2.

The parties propose similar educational qualifications and experience levels. We find Petitioner’s proposed qualification of having at least a basic understanding of interconnect structures and techniques for making them to be applicable here in view of the ’933 patent. Therefore, to the extent necessary, we adopt Petitioner’s proposed qualifications as reflecting the level of ordinary skill in the art. In addition, we note that the art of record in this proceeding—namely, Kimura, Yoshihara, and Kubo—is indicative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Further, neither Dr. Neikirk nor Dr. Bottoms testifies that adoption of a different definition would change the outcome of this case.

D. Alleged Anticipation by Kimura

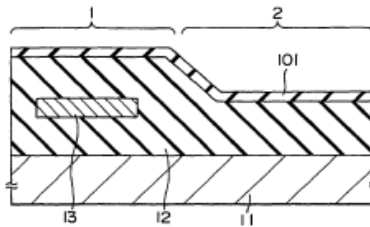
Petitioner contends that Kimura anticipates claims 1–4. Pet. 39–45. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1006, 1019) to support its positions. Patent Owner counters that Kimura does not anticipate the claims because it fails to disclose some claim limitations. PO Resp. 38–44. Patent Owner relies upon the Bottoms Declaration (Ex. 2001) to support its positions.

We begin our discussion with a brief summary of Kimura, and then address the evidence, analysis, and arguments presented by the parties.

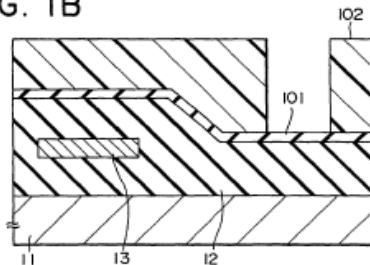
1. Kimura (Ex. 1011)

Kimura discloses a method for fabricating a semiconductor device that is capable of forming high reliability contacts. Ex. 1011, 2:18–21. Figures 1A–1G, reproduced below, depict cross-sectional drawings of the fabrication of a semiconductor device manufactured according to one embodiment of the invention. *Id.* at 3:7–12.

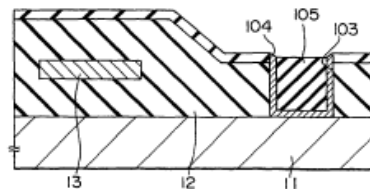
F I G. 1A

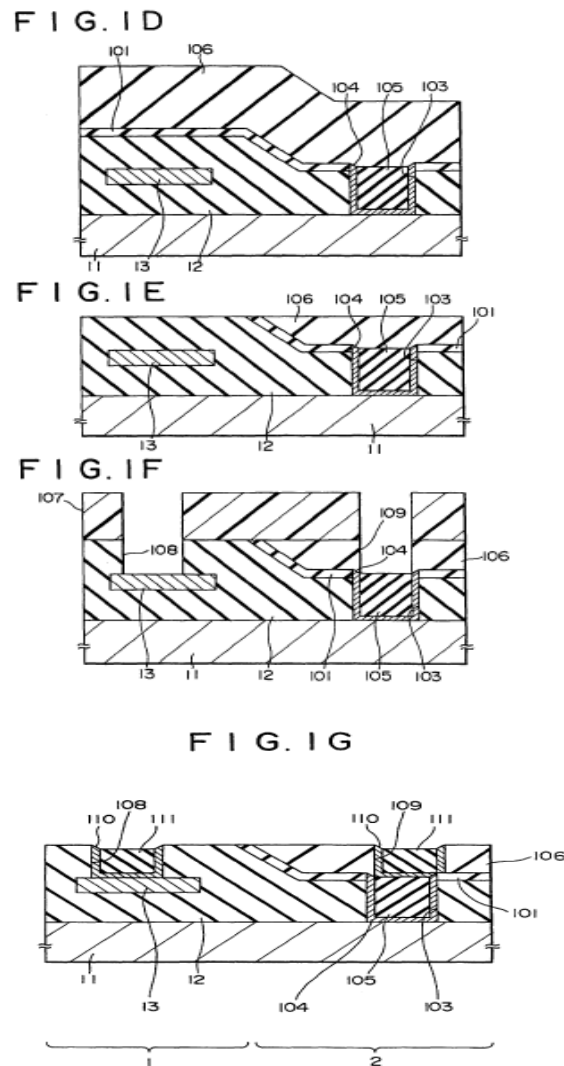


F I G. 1B



F I G. 1C





In the cross-section of Kimura's Figure 1C, semiconducting substrate 11 is formed with insulating layer 12 above it, polysilicon layer 13 is an interconnection layer, with tungsten layer 105 depicted. Ex. 1011, 3:28–51. As shown in Figure 1G, photoresist 107 is removed, and tungsten layer 111 is formed in two contact holes 108, 109. *Id.* at 4:54–57.

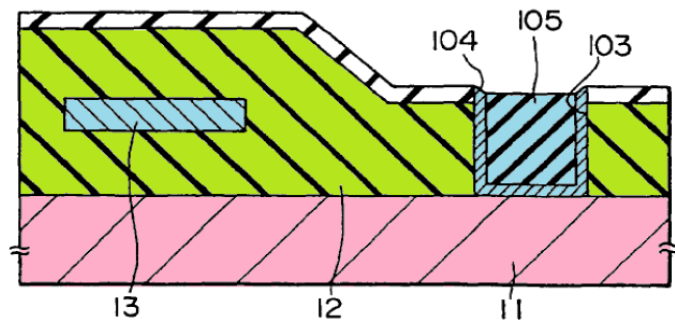
2. Analysis

A claim is unpatentable under 35 U.S.C. § 102 if a prior art reference discloses each and every limitation of the claimed invention, either explicitly or inherently. *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir.

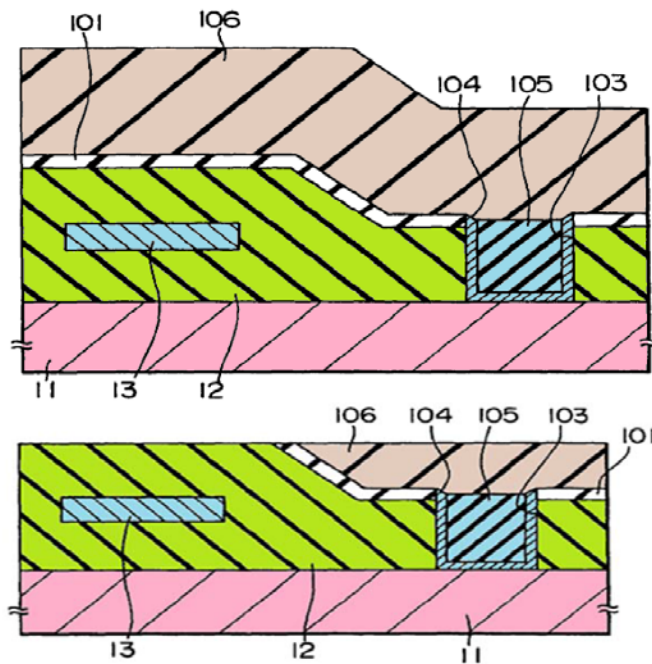
1995); see *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (“To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention . . . ;” any limitation not explicitly taught must be inherently taught and would be so understood by a person experienced in the field); *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991) (the dispositive question is “whether one skilled in the art would reasonably understand or infer” that a reference teaches or discloses all of the limitations of the claimed invention).

a. Independent Claim 1

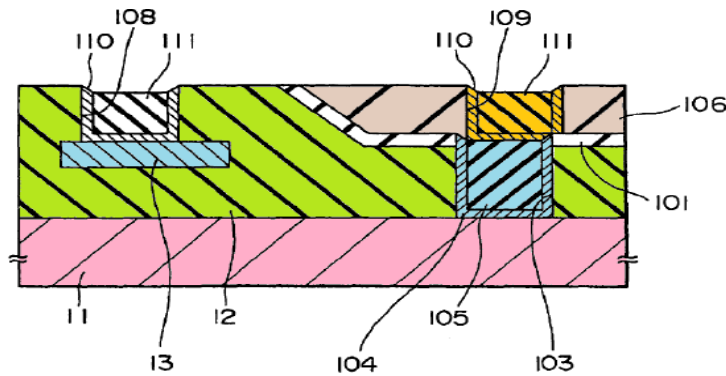
Petitioner presents evidence that Kimura discloses all the limitations of claims 1–4. See Pet. 39–45. In particular, Petitioner relies upon annotated Figures 1C–1G reproduced below. See *id.* at 41–42.



Ex. 1011, FIG. 1C (annotated)



Ex. 1110, FIGS. 1D-1E (annotated)



Ex. 1011, FIG. 1G (annotated)

Petitioner asserts, and we agree, that Kimura discloses a semiconductor substrate 11, shown in pink in the cross-section of Figure 1C, which is a wafer stack as claimed. Pet. 40–41. Petitioner contends, and we agree, that Kimura discloses a “first interconnect layer,” which is first dielectric layer 12, shown in green, that is formed on the wafer stack. *Id.* at 41–42. Petitioner contends that Kimura discloses that the first interconnect layer includes a depression formed within it by its structure with a “stepped portion,” such that it has a higher and lower portion. *Id.* In support,

Petitioner refers to Kimura’s disclosure that “a stepped portion is formed on the surface of the insulating layer 12 such that the cell region 1 is higher and a peripheral region 2 is lower.”⁶ *Id.* (citing Ex. 1011, 3:28–36). We agree with Petitioner that Kimura discloses a depression because the step down portion of first dielectric layer 12 is a depressed part of the structure.

We also agree with Petitioner that Kimura discloses the “second interconnect layer” recited in claim 1 with its layer 106, shown in tan in annotated Figures 1D and 1E. Pet. 42. Petitioner asserts that layer 106 is planarized, and its “substantially planarized top surface” is located above the first interconnect layer and the depression. *Id.* at 43 (citing Ex. 1011, 2:30–33, 2:54–56, 4:1–6); *see also* Ex. 1006 ¶ 168. Petitioner also argues, and we agree, that Kimura discloses that there is no residual conductive material on the surface of layer 106 by etching-back over the entire surface. *Id.* (citing Ex. 1011, 4:54–65). Petitioner further contends, and we agree, that Kimura discloses a second interconnect layer that includes a second dielectric layer, with a second layer conductor extending downwardly from the top surface down through the second layer dielectric to the first layer interconnect by its second dielectric layer 106, with its second layer conductor, shown in orange in annotated Figure 1G, extending to the first layer interconnect 103, shown in blue. *Id.* at 43–44.

Notwithstanding Patent Owner’s contrary arguments, which we discuss below, we agree that Kimura discloses every limitation of claim 1 of the ’933 patent and credit Dr. Neikirk’s supporting testimony on that point (Ex. 1006 ¶¶ 153–177), as it is consistent with the prior art disclosures.

⁶ See Figure 1G, *supra* 18, for depictions of the respective cell regions of Kimura.

Patent Owner argues that Kimura fails to disclose a second interconnect layer as recited in claim 1 because only an isolated portion of layer 106 is used to planarize the top surface of a single premetal dielectric layer 12. PO Resp. 39 (citing Ex. 2001 ¶ 111). Patent Owner analogizes Kimura's layer 106 to the alleged isolated portion of a dielectric of Burke, which was at issue in the prosecution history. *Id.* at 39–40. We do not agree with Patent Owner's argument because it is based on Patent Owner's proposed interpretation for the term “interconnect layer,” which we have not adopted. *See supra* Section II.B. Instead, we have construed the term “interconnect layer” as “an interlayer dielectric having metal conductive interconnects therein or therethrough,” and Kimura's layer 106, as depicted in Figure 1G, has a structure that falls within that definition. *See id.*

Patent Owner also argues that Kimura fails to disclose a depression in the first dielectric layer. PO Resp. 40–44. Patent Owner asserts that for Kimura's “stepped shape” of insulating layer 12, Petitioner does not show that other sides surrounding the peripheral region, besides cell region 1, are above the lower peripheral region. *Id.* at 42–43. Patent Owner contends that Dr. Neikirk confirmed that Kimura does not characterize its lower peripheral region as a depression. *Id.* at 43.

We do not agree with Patent Owner's argument that Kimura fails to disclose a depression because it is based on Patent Owner's proposed limited interpretation of the term, which we did not adopt, that would have required that it be “a place or part that is lower than the areas which enclose it on all sides.” *See supra*, Section II.2. Instead, the stepped down portion of Kimura's layer 12 meets the construction we have adopted for a depression as a “depressed place or part.” *See id.*

Patent Owner further contends that Kimura fails to disclose the “second interconnect layer” limitation under claim 1 of the ’933 patent because Kimura’s isolated portion of layer 106 is not located above a first interconnect layer and a depression. PO Resp. 40–42. Patent Owner argues that, as shown in Figure 1E, the top surface of layer 106 is even with the top of the alleged first interconnect layer formed by layer 12. *Id.* at 41 (citing Ex. 2001 ¶ 114). Patent Owner also argues that a person of ordinary skill in the art would not have understood that the region to the right of Kimura’s peripheral region 2 is necessarily higher than the peripheral region. *Id.* at 43 (citing Ex. 2001 ¶ 120). Patent Owner contends that Dr. Neikirk confirmed that Kimura does not disclose there is a higher surrounding region adjacent the lower peripheral region in Kimura’s disclosed embodiment. *Id.* (citing Ex. 2013, 16:16–19:9).

We do not agree with Patent Owner’s assertions. Claim 1 requires that “the second interconnect layer includes *a substantially planarized top surface located above the first interconnect layer and the depression* in the first dielectric layer.” Ex. 1001, 6:2–6 (emphasis added). As shown in Figure 1E of Kimura, planarized layer 106 (mapped as the second interconnect layer) has at least a significant portion of its top surface vertically above layer 12 (mapped as the “first interconnect layer”)—and there is nothing in the claim that requires that the entire top surface of the second interconnect layer be above the first interconnect layer.⁷ Further, Petitioner maps the “depression” of layer 12 to its “lower step.” Pet. 43. Kimura repeatedly refers to the left region as “higher” and in the stepped portion as “lower,” and additionally refers to the stepped portion as the

⁷ Patent Owner does not offer a claim construction for the term “above.”

“lower height area” of the insulating layer. *See* Ex. 1011, 2:50–56, 3:33–36. The configuration is shown in annotated Figure 1G. Kimura’s disclosures provide support that the stepped down portion of layer 12, which is mapped to the depression, is below the substantially planarized top surface of layer 106 (second interconnect layer). Moreover, we have declined to adopt Patent Owner’s proposed claim construction that “depression” is a lower part with areas that enclose it on all sides, so Petitioner does not have to demonstrate that the areas to the right of the mapped depression are higher than the depression in order to demonstrate anticipation.

Patent Owner also argues that Kimura does not anticipate claim 1 because it does not disclose using damascene techniques to form interconnect layers. PO Resp. 38 (citing Ex. 2001 ¶ 89). More specifically, Patent Owner asserts that Kimura does not disclose planarizing the tungsten metal used to form its contact plugs. *Id.* We do not agree with Patent Owner’s argument because claim 1 does not recite the use of “damascene techniques” and we do not discern a limitation in the claim that requires planarizing the metal in the contact plugs.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 1 of the ’933 patent is anticipated by Kimura.

b. Claim 2

Claim 2 recites “[t]he arrangement as recited in claim 1, wherein the second layer dielectric includes TEOS oxide.” Ex. 1001, 6:12–14. Petitioner alleges that Kimura discloses that the second layer dielectric includes a TEOS oxide. Pet. 45. In support, Petitioner refers to Kimura’s

disclosure that “[a] P-TEOS (Plasma Tetraethyl Orthosilicate) layer 106 is then formed over the entire surface.” *Id.* (citing Ex. 1011, 4:1–3).

We agree with Petitioner that Kimura discloses every limitation of claim 2 of the ’933 patent and credit Dr. Neikirk’s supporting testimony on that point (Ex. 1006 ¶¶ 178–182), as it is consistent with the prior art disclosures.

Patent Owner argues that dependent claim 2 is not anticipated by Kimura because Petitioner has not demonstrated that claim 1, from which claim 2 depends, is anticipated. PO Resp. 44. We do not agree with Patent Owner’s argument because, for the reasons discussed above, we have determined that Petitioner has demonstrated that Kimura anticipates claim 1.

Thus, Petitioner has shown by a preponderance of the evidence that claim 2 of the ’933 patent is anticipated by Kimura.

c. Claim 3

Claim 3 recites “[t]he arrangement as recited in claim 2, wherein the second layer conductor includes a metal.” Ex. 1001, 6:15–16. Petitioner alleges that Kimura discloses that its second layer conductor includes a metal. Pet. 45. In support, Petitioner refers to Kimura’s disclosure that a barrier metal layer 110 and a tungsten layer 111 are formed, as shown in Figure 1G. *Id.* (citing Ex. 1011, 4:54–57).

We agree that Kimura discloses every limitation of claim 3 of the ’933 patent and credit Dr. Neikirk’s supporting testimony on that point (Ex. 1006 ¶¶ 183–187), as it is consistent with the prior art disclosures.

Patent Owner argues that dependent claim 3 is not anticipated by Kimura because Petitioner has not demonstrated that claim 1, from which claim 3 depends, is anticipated. PO Resp. 44. We do not agree with Patent

Owner's argument because, for the reasons discussed above, we have determined that Petitioner has demonstrated that Kimura anticipates claim 1.

Thus, Petitioner has shown by a preponderance of the evidence that claim 3 of the '933 patent is anticipated by Kimura.

d. Claim 4

Claim 4 recites "[t]he arrangement as recited in claim 3, wherein the metal includes tungsten (W)." Ex. 1001, 6:17–18. Petitioner alleges that Kimura discloses that the second layer conductor includes tungsten. Pet. 45. In support, Petitioner refers to Kimura's disclosure that a tungsten layer 111 is formed as shown in Figure 1G. *Id.* (citing Ex. 1011, 4:54–57).

We agree that Kimura discloses every limitation of claim 3 of the '933 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1006 ¶¶ 188–192), as it is consistent with the prior art disclosures.

Patent Owner argues that dependent claim 4 is not anticipated by Kimura because Petitioner has not demonstrated that claim 1, from which claim 4 depends, is anticipated. PO Resp. 44. We do not agree with Patent Owner's argument because, for the reasons discussed above, we have determined that Petitioner has demonstrated that Kimura anticipates claim 1.

Thus, Petitioner has shown by a preponderance of the evidence that claim 4 of the '933 patent is anticipated by Kimura.

E. Alleged Anticipation by Kubo

Petitioner contends that Kubo anticipates claims 1–4. Pet. 52–58. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1006, 1019) to support its positions. Patent Owner counters that Kubo does not anticipate the claims

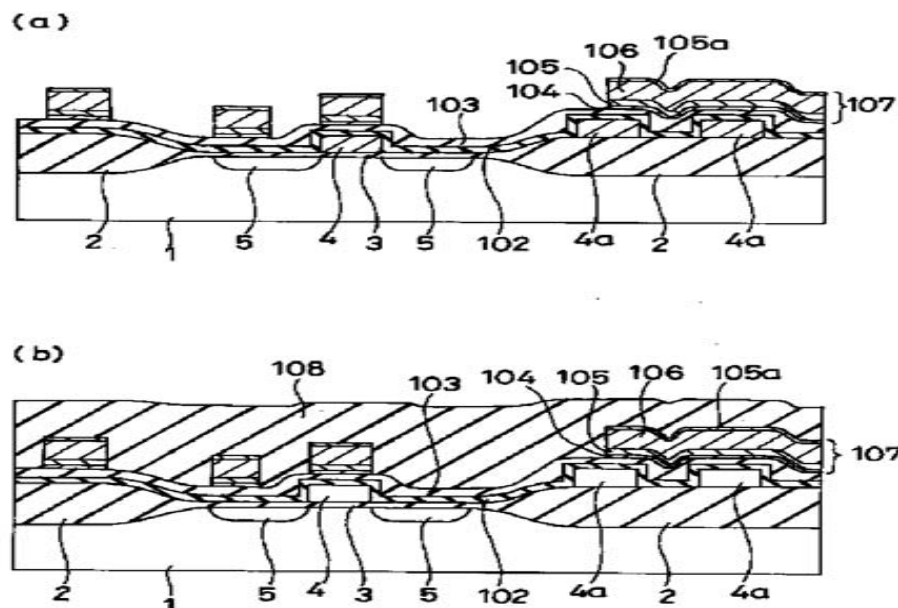
because it fails to disclose some claim limitations. PO Resp. 49–57. Patent Owner relies upon the Bottoms Declaration (Ex. 2001) to support its positions.

We begin our discussion with a brief summary of Kubo, and then address the evidence, analysis, and arguments presented by the parties.

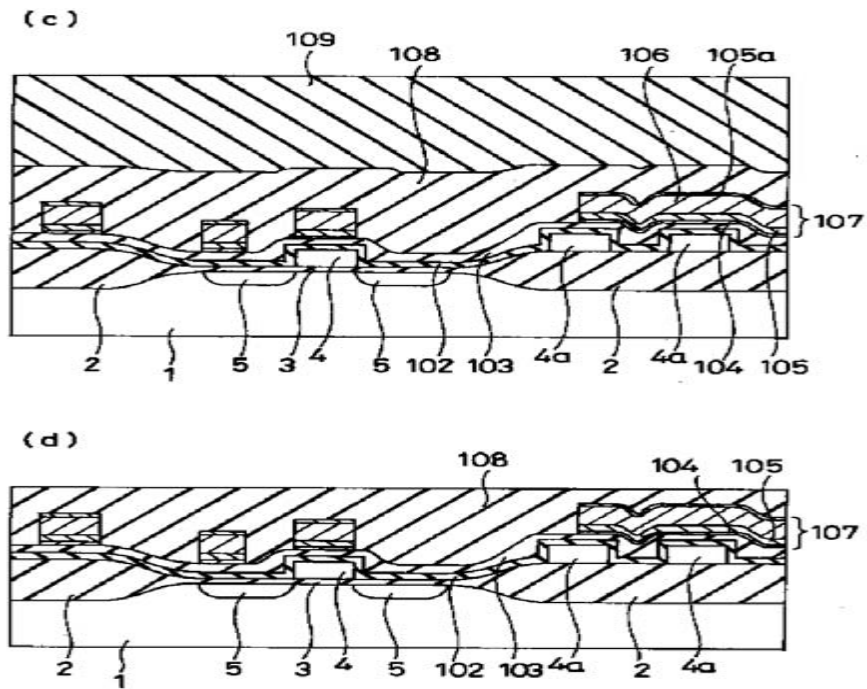
1. Kubo (Ex. 1015)

Kubo is directed to a manufacturing method for semiconductor devices that forms interlayer insulation film for multilayer wiring. Ex. 1015 ¶ 1. More specifically, Kubo is directed to improvements in an interlayer insulation film. *Id.* ¶ 2. Kubo discloses a method for forming a multiple-layer interconnect structure that includes embodiment 1, depicted in the manufacturing sequence reproduced below, with the cross-sections shown in Figure 2 continued from Figure 1, and the cross-sections shown in Figure 3 continued from Figure 2. *Id.* at [Brief Description of the Drawings].

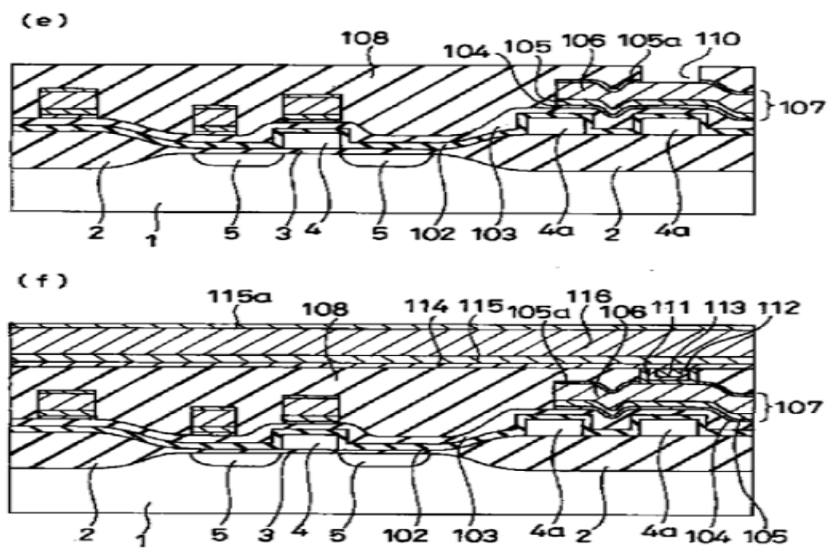
【図 1】



【图 2】



(FIG. 3)

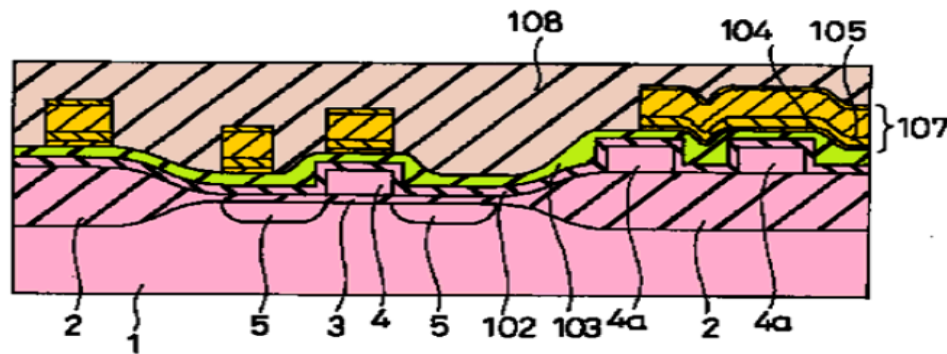


Cross sections of Figures 1, 2, and 3, above, depict silicon substrate 1, wire base insulation film 103 under laminated wiring 107, base insulation

film 103, titanium film 104, silicon oxide film 108, and tungsten film 113.
Ex. 1015 ¶¶ 22, 25, 27, 31.

2. Analysis

Petitioner presents evidence that Kubo discloses all the limitations of claims 1–4. *See* Pet. 52–58. In particular, Petitioner refers to annotated Figure 1(d) of Kubo, reproduced below. *See id.* at 55.



Ex. 1015, FIG. 1(d) (annotated)

Petitioner asserts, and we agree, that Kubo discloses a wafer stack as shown in pink in annotated cross-section Figure 1(d). Pet. 52. We also agree that Petitioner’s evidence demonstrates that Kubo discloses a first interconnect area, with a depression formed in dielectric layer 103, as shown in green. *Id.* at 53. Dr. Neikirk’s testimony on “depression” relies upon Kubo’s disclosure of “bumps” that correspond to steps in Kubo’s structure, which result in differences in the respective heights of the layers. *See* Ex. 1006 ¶¶ 241, 242 (citing Ex. 1015 ¶ 23).

Petitioner also asserts, and we agree, that organic silica film 108, which Petitioner maps as “second interconnect layer,” shown in tan in annotated Figure 1(d), is etched to remove upper layers. Pet. 55–56. We also agree Petitioner’s evidence demonstrates that Kubo discloses a second

layer conductor that extends downwardly from the top surface through the second layer dielectric to the first layer interconnect by its disclosure of conductors extending from the top surface of organic silica film 108 downwardly through second layer dielectric to layer 103. *Id.* at 56–57.

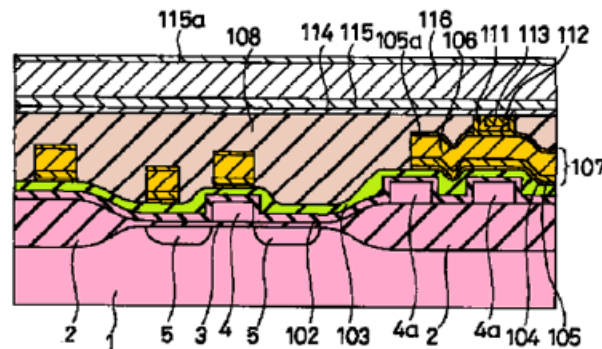
Notwithstanding Patent Owner’s contrary arguments, which we discuss below, we agree that Kubo discloses every limitation of claim 1 of the ’933 patent and credit Dr. Neikirk’s supporting testimony (Ex. 1006 ¶¶ 232–253), as it is consistent with the prior art disclosures.

Patent Owner argues that Kubo does not anticipate claim 1 because it does not mention the use of damascene techniques, etch-back used to form interconnects, or chemical-mechanical polishing (CMP). PO Resp. 50 (citing Ex. 2001 ¶ 98). We do not agree with Patent Owner’s arguments because claim 1 does not recite the use of “damascene techniques” or CMP, nor do we discern a limitation in claim 1 that requires planarizing the metal in contact plugs.

Patent Owner also argues that Petitioner fails to identify a second layer conductor disclosed in Kubo. PO Resp. 54–57. Patent Owner contends that Petitioner identifies silicon oxide film 108 as the dielectric portion of the second layer interconnect that is located and planarized above the first interconnect layer, and that is etched with through-hole 110, but it is etched just to the top of the lower layer laminated wiring 107 and not below to first interconnect layer 103. *Id.* at 54–55 (citing Pet. 55; Ex. 1015 ¶ 30, Fig. 3(e); Ex. 2001 ¶ 125). Patent Owner further alleges that in Kubo, titanium film 111, titanium oxide film 112, and tungsten film 113 do not extend all the way through silicon oxide film 108, which is alleged to be the second layer dielectric, nor does tungsten film 111 extend below to the first

interconnect layer 103. *Id.* at 55–56 (citing Ex. 1015 ¶ 31, Fig. 3(f); Ex. 2001, ¶ 127; Ex. 2013, 64:11–65:5).

We do not agree with Patent Owner’s arguments. For the “second layer conductor,” the Petition refers to Kubo’s statement that “silicon oxide film 108 was etched with a photoresist film as a mask, forming a through-hole 110 that reaches to the lower-layer laminated wiring 107, as shown in FIG. 3(e).” Pet. 56–57 (quoting Ex. 1015 ¶ 30). Petitioner then refers to the formation shown in annotated Figure 3(f), reproduced below, that includes titanium film 111, titanium oxide film 112, and tungsten film 113. *Id.* at 57 (citing Ex. 1015 ¶ 31).



Kubo, FIG. 3(f) (annotated)

Dr. Neikirk testifies that, as depicted in annotated the cross-section of Kubo’s Figure 3(f):

Kubo also shows conductors 107, 111 that extend through the dielectric layer 108 conductor. The conductor 107 extends laterally across the semiconductor device. The conductor, 111 form[s] a conductive plug that extends downwardly from a top surface of the dielectric layer 108 to make contact with conductor 107 and, by extension, conductors (now shown of the other interconnect layer).

Ex. 1006 ¶ 248.

Although Patent Owner argues that neither through-hole 110 nor titanium film 111, titanium oxide film 112, or tungsten film 113 (which fill

through-hole 110) extend all the way through silicon oxide film 108, that argument is based on an overly limited view of Petitioner's mapping of Kubo to the "second layer conductor." Petitioner asserts that lower layer laminated wiring 107 *and* titanium film 111 are both mapped to the claimed "second layer conductor" of claim 1. *See* Ex. 1006 ¶ 248; *see also* Pet. 56–57. Under this mapping, the evidence supports that Kubo discloses a "second layer conductor" that "extends downwardly from the top surface" of second interconnect layer, and "through the second layer dielectric to the first layer interconnect [103]." *See* Ex. 1006 ¶ 248; *see also* Pet. 56–57, Pet. Reply 8–11.

Patent Owner also suggests that not only does the second layer conductor have to extend through the second layer dielectric, but it also has to extend through the first layer interconnect and reach below it. *See* PO Reply 56. We discern no limitation in claim 1 that requires that the second layer conductor extend to below the first interconnect layer.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 1 of the '933 patent is anticipated by Kubo.

b. Claim 2

Petitioner alleges that Kubo discloses that the second layer dielectric includes a TEOS oxide. Pet. 57. In support, Petitioner refers to Kubo's disclosure that TEOS is injected into silicon oxide film 108. *Id.* (citing Ex. 1015, 1, [27]).

We agree that Kubo discloses every limitation of claim 2 of the '933 patent and credit Dr. Neikirk's supporting testimony (Ex. 1006 ¶¶ 254–259), as it is consistent with the prior art disclosures.

Patent Owner argues that dependent claim 2 is not anticipated by Kubo for the same reasons that it does not anticipate claim 1. PO Resp. 55. We do not agree with Patent Owner's argument because, for the reasons discussed above, we have determined that Petitioner has demonstrated that Kubo anticipates claim 1.

Thus, Petitioner has shown by a preponderance of the evidence that claim 2 of the '933 patent is anticipated by Kubo.

c. Claim 3

Petitioner alleges that Kubo discloses that the second layer conductor includes a metal. Pet. 58. In support, Petitioner refers to Kubo's disclosure of forming of tungsten film 113. *Id.* (citing Ex. 1015 ¶ 58).

We agree that Kubo discloses every limitation of claim 3 of the '933 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1006 ¶¶ 260–265), as it is consistent with the prior art disclosures.

Patent Owner argues that dependent claim 3 is not anticipated by Kubo for the same reasons that it does not anticipate claim 1. PO Resp. 55. We do not agree with Patent Owner's argument because, for the reasons discussed above, we have determined that Petitioner has demonstrated that Kubo anticipates claim 1.

Thus, Petitioner has shown by a preponderance of the evidence that claim 3 of the '933 patent is anticipated by Kubo.

d. Claim 4

Petitioner alleges that Kubo discloses that the second layer conductor includes tungsten. Pet. 45. In support, Petitioner refers to Kubo's disclosure that tungsten film 113 is formed. *Id.* (citing Ex. 1015 ¶ 31).

We agree that Kubo discloses every limitation of claim 4 of the '933 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1006 ¶¶ 266–270), as it is consistent with the prior art disclosures.

Patent Owner argues that dependent claim 4 is not anticipated by Kubo for the same reasons that it does not anticipate claim 1. PO Resp. 55. We do not agree with Patent Owner's argument because, for the reasons discussed above, we have determined that Petitioner has demonstrated that Kubo anticipates claim 1.

Thus, Petitioner has shown by a preponderance of the evidence that claim 4 of the '933 patent is anticipated by Kubo.

F. Alleged Anticipation by Yoshihara

Petitioner contends that Yoshihara anticipates claims 1–4. Pet. 46–51. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1006, 1019) to support its positions. Patent Owner counters that Yoshihara does not anticipate the claims because it fails to disclose some claim limitations. PO Resp. 44–49. Patent Owner relies upon the Bottoms Declaration (Ex. 2001) to support its positions.

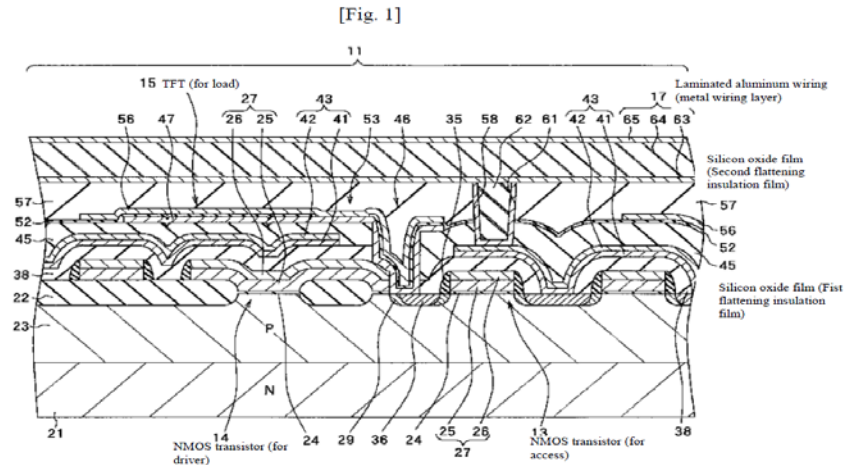
We begin our discussion with a brief summary of Yoshihara, and then we address the evidence, analysis, and arguments presented by the parties to the extent necessary.

1. Yoshihara (Ex. 1013)

Yoshihara discloses a method for manufacturing semiconductor memory devices. Ex. 1013 ¶ 1. Yoshihara discloses a cross-sectional view

of the semiconductor device shown in Figure 1, as reproduced below. *Id.*

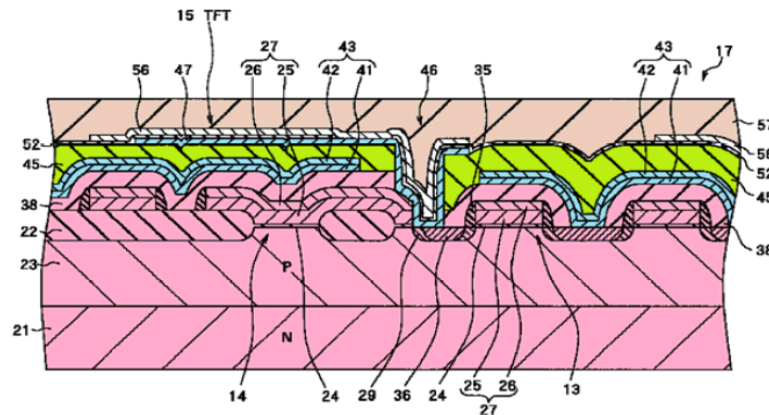
¶ 16, [Brief Description of the Figures].



In the cross-section of Yoshihara's Figure 1, silicon oxide layers 45 and 57 are depicted, as are poly side layer 43, poly layer crystal 47, which is a gate electrode formed on silicon oxide film 45, and silicon oxide films formed with a contact hole reaching to the poly side layer 43, which is filled by titanium/titanium nitride layer 61 and tungsten layer 62. Ex. 1013 ¶¶ 18–23.

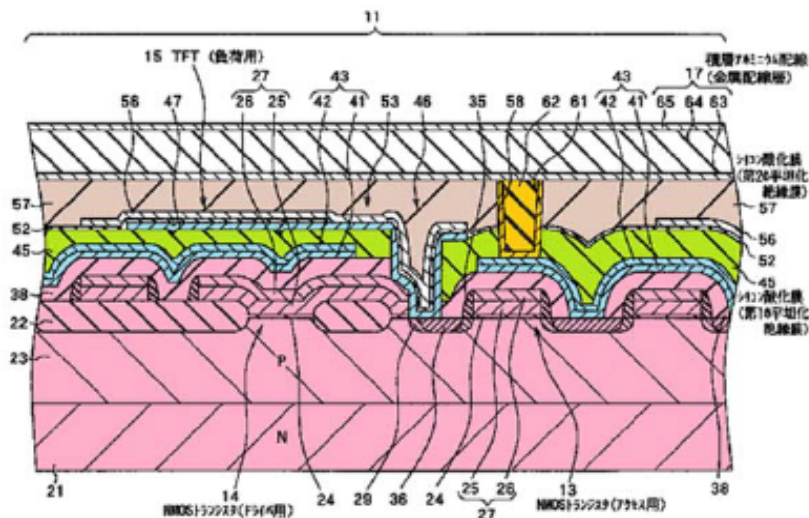
2. Analysis

Petitioner presents evidence that Yoshihara discloses all the limitations of claims 1–4. *See* Pet. 46–51. In particular, Petitioner relies upon annotated Figure 13, reproduced below. *See id.* at 49.



Ex. 1114, FIG. 13 (annotated)

Petitioner asserts, in part, that as shown in annotated Figure 13, Yoshihara discloses first interconnect layer (shown in green and blue in annotated Figure 13), on wafer stack (shown in pink), where there is a depression formed in first dielectric layer 45 (shown in green). Pet. 47. Patent Owner argues that although Petitioner asserts that the green and blue portions of Petitioner's annotated Figure 13 of Yoshihara are the first interconnect layer, there is no showing that there are any metal conductive interconnects in that layer, as required under Petitioner's proposed construction of the term "interconnect layer." PO Resp. 47–48. More specifically, Patent Owner asserts that the layer annotated by Petitioner in blue is poly crystal silicon layer 47, not a metal. *Id.* at 48 (citing Ex. 2001 ¶ 122). Patent Owner further asserts that poly side layer 43 does not extend in or through dielectric layer 45. *Id.* In Reply, Petitioner acknowledges that conductors 43 and 47 are not metal conductors. Pet. Reply 12. Petitioner then argues in Reply that Yoshihara's tungsten plug 62, as shown in orange in annotated Figure 1, reproduced below, extends through dielectric layer 45, so the structure of layer 45 with plug 62 would meet the construction of an interconnect layer. *Id.*



Ex. 1013, FIG. 1 (annotated)

Annotated Figure 1 of Yoshihara depicts a cross-section of an embodiment of the invention. Ex. 1013 ¶ 16; PO Reply 12.

We disregard Petitioner’s new argument in Reply on the issue of Yoshihara’s disclosure of a metal conductive interconnect in an interconnect layer because it presents a new theory of unpatentability that exceeds the proper scope of a Reply under 37 C.F.R. § 42.23(b). “[A] reply that raises a new issue or belatedly presents evidence will not be considered” and “[e]xamples of indications that a new issue has been raised in a reply include new evidence necessary to make out a *prima facie* case for the . . . unpatentability of an original . . . claim, and new evidence that could have been presented in a prior filing.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012). We also do not consider this new contention because Patent Owner was not afforded notice and full opportunity to respond to this new theory of unpatentability with briefing and evidence. *See generally Genzyme Therapeutic Prods. Ltd. v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1366–67 (Fed. Cir. 2016) (determining that the

Administrative Procedure Act and due process require notice to a party and the opportunity to submit facts and argument); *see also Intelligent Bio–Ays. v. Illumina Cambridge, Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’”).

Petitioner does not allege that there were any new unforeseen circumstances that would have necessitated a change in its position based on Yoshihara. *See* Pet. Reply 12. Here, we have adopted Petitioner’s own proposed construction of “interconnect layer” as “an interlayer dielectric having metal conductive interconnects therein or therethrough,” so Petitioner could not assert that there was changed position based on unforeseen claim construction.⁸ *See supra* Section II.B. Further, in light of Yoshihara’s failure to disclose the claim 1 element of a “first interconnect layer,” the Petition failed to make out a *prima facie* case for anticipation because there is no showing that there are any metal conductive interconnects in that layer, and Petitioner’s Reply cannot be used to introduce new evidence to provide that support. Thus, the argument and evidence presented in the Petition is insufficient to support that Yoshihara anticipates claim 1 of the ’933 patent.

Claims 2–4 depend from claim 1, and the Petition fails to remedy the deficiency of claim 1 with additional support from the evidence provided for claims 2–4. *See* Pet. 50–51.

Thus, we determine that Petitioner has not has shown by a preponderance of the evidence that claims 1–4 are anticipated by Yoshihara.

⁸ In the Decision to Institute, we also adopted, on a preliminary basis, the same proposed construction provided by Petitioner. Dec. 8.

G. Alleged Obviousness Based Upon Admitted Prior Art and Planarization References

Petitioner contends that claims 1–4 would have been obvious over Admitted Prior Art and the Planarization References, which are identified as Leidy, Tottori, Kimura, Yoshihara, and Kubo. Pet. 12, 29–39. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1006, 1019) to support its positions.

In the Institution Decision, we determined that because of the deficiencies under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a), Petitioner had not established a reasonable likelihood that it would prevail in showing that claims 1–4 were unpatentable. Dec. 9–11. Petitioner did not request rehearing on this issue. In Reply, Petitioner requests reconsideration of the denial of this ground.⁹ Pet. Reply. 12. Petitioner argues that its assertions relying on the Planarization References demonstrate that it was obvious to planarize a dielectric layer to solve problems in semiconductor manufacturing applications. *Id.* at 12–13. Petitioner contends that these techniques would have improved the structure of the Admitted Prior Art in the same way. *Id.* at 13. Petitioner argues that criticism of the Petition for failure to identify specific teachings of the planarization references does not apply because this type of combination adheres to *KSR*, in that it mandates that “[w]hat matters is the objective reach of the claims.” *Id.* (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007)). Petitioner alleges that

⁹ As discussed, *supra* Section I.A, this ground was subsequently instituted pursuant to SAS.

“claim 1 is directed not to a single fabrication technique but to a class of techniques: ‘planarization.’” *Id.* Petitioner further argues that the ‘933 patent admits that all elements described by claim 1 are disclosed by the prior art, with the exception of planarization of the top surface. *Id.* at 14. Petitioner alleges that because the planarization references are redundant, a person of ordinary skill in the art would have considered it obvious to planarize a second dielectric layer and apply this to the structure of the Admitted Prior Art. *Id.* at 14–15.

Patent Owner counters that the Petition lacks required sufficiency and particularity, and even if this challenge were considered, the prior art fails to teach some of the claim limitations. PO Resp. 57–67. Patent Owner relies upon the Bottoms Declaration (Ex. 2001) to support its positions.

Patent Owner asserts that the Board correctly determined that this ground was legally deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a), and there is no need for the Board to reconsider its initial determination on this issue. PO Resp. 57. Patent Owner argues that 35 U.S.C. § 312(a)(3) states that a petition may only be considered if it identifies the grounds and evidence with particularity. *Id.* at 59. Patent Owner also asserts that the Petition’s deficiencies cannot be cured because any new supplementation would constitute impermissible new arguments. *Id.* at 58–59 (citing 37 C.F.R. § 42.23(b)).

More specifically, Patent Owner alleges that the ground is legally deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a) because:

Petitioner[] improperly assert[s] that five different “Planarization References” should be combined with the admitted prior art described in the ‘933 patent. Petitioner[] fail[s] to explain whether the alleged ground of invalidity relies

on the combined teachings of the CMP references or should be based on one or more of the individual CMP References.

PO Resp. 59.

Patent Owner argues that Petitioner cites unrelated teachings of Leidy, Tottori, Kimura, Yoshihara, and fail to identify which of these teachings is to be relied on. PO Resp. 60. Patent Owner further argues that, to the extent that the teachings should be combined, Petitioner fails to identify how the combined references teach more than each individual reference. *Id.* Patent Owner also argues that grounds should be denied “when Petitioner[] fail[s] to articulate with reasonable clarity what specific elements from each of the references is to be combined, and in what manner, to meet each limitation of the claims.” *Id.* at 61. Moreover, Patent Owner asserts that each reference has unique teachings and rather than explaining the significance of specific facts for each reference, Petitioner “improperly pile[s] the references together.” *Id.* at 60–61. Patent Owner contends that this improperly imposes a burden upon Patent Owner and the Board. *Id.* at 61.

By statute, a Petition is required to identify “with particularity[] the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge.” 35 U.S.C. § 312(a)(3). The Petition shall also include “a full statement” with “a detailed explanation of the significance of the evidence, including material facts.” 37 C.F.R. § 42.22(a). Although *KSR* applies to an obviousness evaluation, a Petition must nonetheless meet the requirements of the statute and rules.

As we discussed in the Institution Decision, we found that the Petition was deficient in failing to present this obviousness challenge and the supporting evidence with particularity. Dec. 8–11. As discussed, Petitioner mixed and matched references in the claim charts, and particularly, mixed

and matched some of the prior art references identified as the Planarization References. *Id.* at 9 (citing Pet. 32–37). Dr. Neikirk did not testify in support of the teachings of specific references in the claim charts, but rather only referred to the grouping of prior art, identifying the group globally as “Planarization References.” *Id.* (citing Ex. 1006 § IX.B.1.a–e). Petitioner failed to articulate, with reasonable clarity, what specific elements from the individual Planarization References were combined with the specific elements of the other Planarization References to meet the limitations of independent claim 1. The Institution Decision also stated that, to the extent that the reference to “Leidy, Tottori, Kimura, Yoshihara, and Kubo” (Pet. 29) was intended to denote that all the named prior art should be considered for teaching the same limitation, it was unclear why Petitioner included all these references. Dec. 10 (citing Pet. 31–32). Here, we reiterate, for the same reasons expressed in the Institution Decision, that Petitioner’s assertions regarding the teachings of the prior art lack required particularity.

Moreover, we also determined in the Institution Decision that the rationale for the proposed combination(s) also lacks specificity and sufficient support in the Petition. *See* Dec. 10–11. Petitioner asserts that “Leidy and Tottori, for example, teach that dielectric layers having irregular surfaces can lead to short-circuits,” and “[b]oth references teach that creation of a second, planarized dielectric layer over the irregular dielectric surface can solve the shortcircuiting problem.” Pet. 29. Petitioner also contends that Kubo “recognizes that planarizing dielectric layers helps prevent the possibility of short-circuits among conductors.” *Id.* Petitioner referred to Yoshihara and Kimura as allegedly explaining “that planarization of interconnect layers [is needed to] satisfy focus requirements of

photolithography processes.” *Id.* at 29–30. Petitioner argues that “[w]ith so many benefits to be gained,” a person of ordinary skill in the art “would be keenly interested in techniques that planarize dielectric layers in interconnect structures.” *Id.* at 30. The stated basis for combining various teachings of the several references lacks required particularity and specificity of a rationale to combine these teachings with other prior art besides that in the Planarization References, much less an articulation of a rationale to combine with specific references within the grouping. *See id.* As we noted in the Institution Decision, it is unclear whether the rationale to combine is based on some form of a composite rationale across all of the Planarization References, that is, Leidy, Tottori, Kimura, Yoshihara, and Kubo, or whether it is based on a rationale to combine with each of the Planarization References individually, in the alternative. *See* Dec. 10–11. Here, we reiterate, for the same reasons expressed in the Institution Decision, that these assertions lack required particularity.

Thus, consistent with the Institution Decision and for the reasons expressed therein and reiterated herein, we determine that the Petition’s obviousness ground is deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a). Therefore, Petitioner has not shown by a preponderance of the evidence that claims 1–4 are obvious over Admitted Prior Art and the Planarization References.

III. CONCLUSION

For the foregoing reasons, we conclude Petitioner has demonstrated by a preponderance of the evidence, that claims 1–4 of the ’933 patent are unpatentable based on the following grounds: (1) anticipation by Kimura

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under 35 U.S.C. § 102(e); and (2) anticipation by Kubo under 35 U.S.C. § 102(b).

IV. ORDER

Accordingly, it is

ORDERED that claims 1–4 of the '933 patent are determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01989
Patent 6,153,933

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