

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HP INC.,
Petitioner,

v.

JAMES B. GOODMAN,
Patent Owner.

Case IPR2017-01994
Patent 6,243,315 B1

Before BRIAN J. McNAMARA, PATRICK M. BOUCHER, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, HP Inc. (“Petitioner”) challenges the patentability of claims 1, 5, 10, and 16 (“the challenged claims”) of U.S. Patent No. 6,243,315 B1 (Ex. 1001, “the ’315 patent”), owned by James B. Goodman (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during trial. For the reasons discussed below, we determine that Petitioner has shown by a preponderance of the evidence that claims 10 and 16 of the ’315 patent are unpatentable, but has not shown by a preponderance of the evidence that claims 1 and 5 of the ’315 patent are unpatentable.

A. Procedural History

On August 24, 2017, Petitioner filed a Petition requesting an *inter partes* review of claims 1, 5, 10, and 16 of the ’315 patent (Paper 2, “Pet.”), supported by the declaration testimony of Dr. Nader Bagherzadeh (Ex. 1002). Patent Owner filed a Preliminary Response. Paper 5 (“Prelim. Resp.”). On March 8, 2018, we instituted an *inter partes* review of the challenged claims. Paper 6 (“Decision on Institution” or “Dec. on Inst.”). On June 1, 2018, Patent Owner filed a Patent Owner Response (Paper 8) and later in the day, filed a second Patent Owner Response (Paper 9, “PO Resp.”). We refer herein to the second filed Patent Owner Response (Paper 9).¹ On August 24, 2018, Petitioner filed a Reply (Paper 10, “Reply”).

¹ Petitioner has not objected to our consideration of the second-filed Response.

A hearing was held on November 16, 2018. A transcript of the hearing has been entered into the record. Paper 15 (“Tr.”).

B. Related Proceedings

The parties identify the following litigations as related proceedings: *Goodman v. Hewlett-Packard Co.*, C.A. No. 16-CV-03195 (S.D. Tex.); *Goodman v. ASUS Computer International*, C.A. No. 17-CV-05542 (N.D. Cal.) (transferred from the S.D. Tex.); *Goodman v. Samsung Electronics America, Inc.*, C.A. No. 17-CV-05539 (S.D.N.Y.); and *Goodman v. Lenovo (United States) Inc.*, C.A. 17-CV-06782 (N.D. Cal.). Pet. 2; Paper 4 ¶ 2; Paper 4, 1.

In addition, we note that the ’315 patent is also the subject of current petitions for *inter partes* review by Samsung Electronics America, Inc. (IPR2017-02021) and by ASUS Computer International Inc. (IPR2018-00047²).

C. The ’315 patent

The ’315 patent is directed to memory systems having volatile solid state memory devices that retain information when an electrical power source is applied but lose their memory contents when power is removed. Ex. 1001, 2:54–58, 3:46–52. To reduce energy consumption and preserve memory contents, volatile memory devices are placed in low power “self-refresh mode” when the memory system is not receiving requests for access. *See id.* at 3:46–54 (stating the “low power mode utilizes

² Case IPR2018-00047 has been joined with IPR2017-02021.

significantly less electrical current than when the memory device is in the operating mode or powered up mode”), *id.* at 3:25–30 (stating “placing the memory devices into a power down self-refresh mode . . . will maintain the data using a minimum of electrical power”). The memory system of the ’315 patent has a control device interposed electrically between the memory devices and a central processing unit (“CPU”). *Id.* at 3:54–56. The control device senses CPU access of the memory devices and conditions the memory devices to an operating mode condition prior to allowing access to the information contained therein. *Id.* at 3:56–59. The control device also places the solid state memory devices into a low power standby mode when it “senses the termination of a memory cycle.” *Id.* at 3:59–62.

Figure 1 of the ’315 patent, reproduced below, illustrates a preferred embodiment in which address and control busses are electrically isolated from the memory devices when the memory devices are in a power down self-refresh mode. *Id.* at 5:60–63.

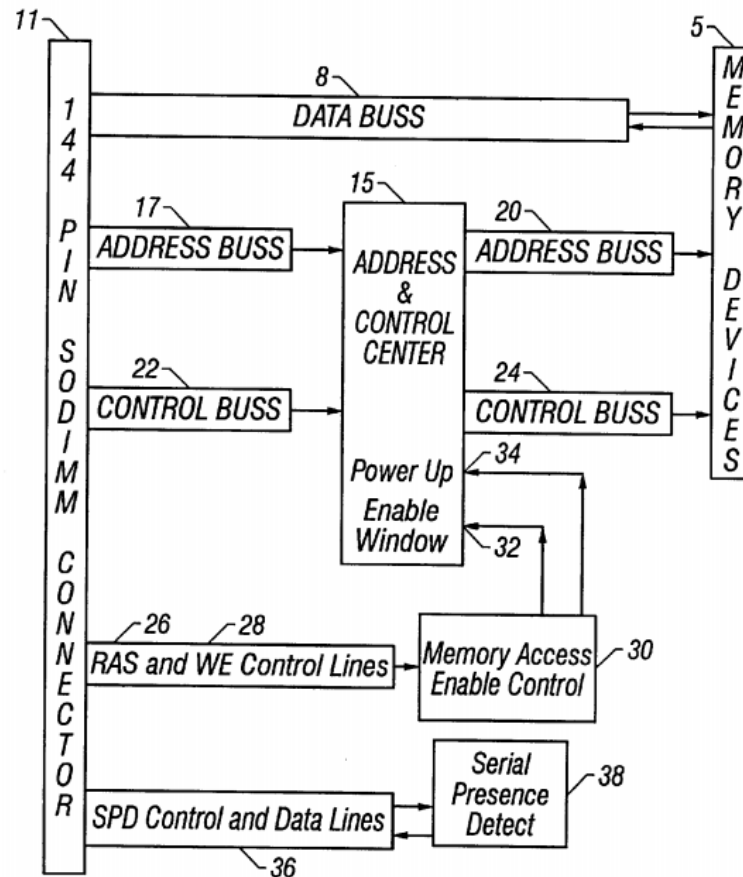


FIG. 1

As shown in Figure 1 of the '315 patent above, control device 15 is interdisposed between address bus³ 17 and address bus 20 (*id.* at 5:50–52) as well as between control bus 22 and control bus 24 (*id.* at 5:54–56). Control device 15 isolates address bus 17 and control bus 22 from memory devices 5 when the memory devices are in a power down self-refresh mode. *Id.* at 5:60–63. By isolating the memory devices from control bus 22 and address bus 17, control device 15 prevents errant signals from erroneously changing

³ The Decision uses the conventional spelling “bus” as opposed to “buss” as used in the '315 patent.

or affecting the data being retained by memory devices 5. *Id.* at 5:63–67.

Figure 1 also shows RAS control lines 26 and WE control lines 28, which are connected to memory access control device 30. *Id.* at 6:1–3. Memory access enable control device 30 receives signals from the CPU indicating that a memory access is pending. *Id.* at 6:3–5. Memory access enable control device 30 then signals control device 15 to bring memory devices 5 up to a normal operating mode. *Id.* at 5:56–59, 6:5–8. Memory access enable control device can also signal control device 15 to indicate when memory devices 5 are to be placed in a power down mode. *Id.* at 5:56–59.

Another preferred embodiment of the '315 patent is shown in the block diagram of Figure 4, reproduced below. *Id.* at 4:41–42.

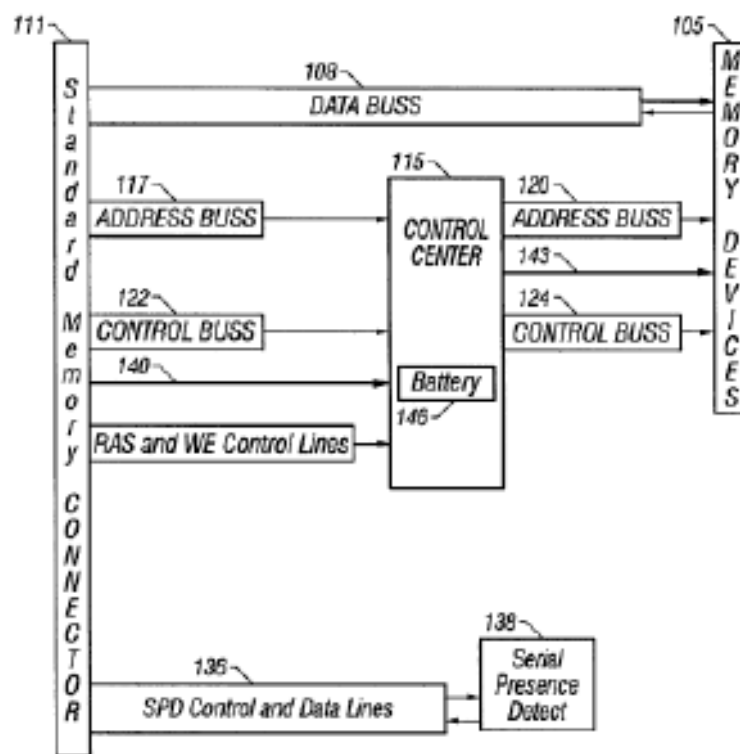


FIG. 4

Figure 4 of the '315 patent, shown above, is a block diagram of a preferred embodiment of the invention that switches the voltage source from the system electrical source input on line 140 to battery 146 when the input voltage level is less than a fixed amount and electrically isolates address and control lines. *Id.* at 9:41–46. As shown in Figure 4, control device 115 is interdisposed between address bus 117 and address bus 120 (*id.* at 9:16–20) and between control bus 122 and control bus 124 (*id.* at 9:20–23). Figure 4 “also shows RAS, row address select lines, 126 and WE, write enable, 128 lines connected to” control device 115. *Id.* at 9:24–26. Control device 115 compares the input voltage on line 140 against a fixed reference voltage; when the input voltage level is less than the fixed reference voltage, the output electrical voltage source is switched from the system electrical source input on line 140 to battery 146. *Id.* at 9:41–43. Control device 115 then electrically isolates the “memory devices 105 from . . . control lines 122 and address lines 117” to prevent errant signals. *Id.* at 9:43–47.

D. Illustrative Claims

Of the claims challenged by Petitioner, only claims 1 and 10 are independent and are reproduced below.⁴

1. [a] A memory system for use in a computer system, said memory system comprising:
[b] a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range

⁴ Paragraph breaks and bracketed letters have been added for ease of reference and for consistency with nomenclature utilized by Petitioner.

[c] and capable of being placed in a self refresh mode;

[d] said memory devices having address lines and control lines;

[e] a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and

[f] a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system

[g] wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.

Id. at 13:18–40.

10. [a] A memory system for use in a computer system, said memory system comprising:

[b] a plurality of volatile solid state memory devices that retain information when an electrical power source having a voltage greater than a predetermined voltage is applied to said devices;

[c] said memory devices having address lines and control lines;

[d] said computer system including a first electrical power source for operating said computer and being capable of producing a first voltage applied to said memory devices;

[e] a control device for monitoring said first voltage to determine when said first voltage is less than said predetermined voltage and for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said

memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and

[f] a second electrical power source operable for supplying a second voltage to said memory devices greater than said predetermined voltage;

[g] said control device being operable for disconnecting said first electrical power source from said memory devices and connecting said second electrical power source to said memory devices when said first voltage is less than said predetermined voltage;

[h] whereby, data in said memory devices is preserved by said second electrical power source when said first electrical power source fails to maintain at least said predetermined voltage on said memory devices, and said memory devices are isolated from errant signals.

Id. at 13:65–14:32.

E. Instituted Grounds

We instituted an *inter partes* review of claims 1, 5, 10, and 16 on all grounds of unpatentability set forth in the Petition, as summarized in the table below.

References	Basis	Challenged Claims
Schaefer ⁵ and Qureshi ⁶	§ 103(a)	1 and 5
Schaefer, Qureshi, and Mazur ⁷	§ 103(a)	10 and 16

⁵ U.S. Patent No. 5,600,605 (issued Feb. 4, 1997) (Ex. 1003, “Schaefer”)

⁶ U.S. Patent No. 5,793,776 (issued Aug. 11, 1998) (Ex. 1004, “Qureshi”)

⁷ U.S. Patent No. 5,204,840 (issued Apr. 20, 1993) (Ex. 1005, “Mazur”)

II. DISCUSSION

A. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). Petitioner contends a person of ordinary skill in the art at the time of the alleged invention of the '315 patent (a "POSITA") would have had at least a bachelor's degree in electrical, electronics, or computer engineering, or the equivalent training or experience in electrical, electronics, or computer engineering, or a related discipline, and would have had approximately 2 to 3 years of experience in computer systems, circuits, electronics, or a related discipline. Pet. 16. Petitioner's declarant, Dr. Bagherzadeh, generally agrees with this proposed level of ordinary skill in the art, but states that a POSITA would have had two *or more* years of experience in computer hardware, including the use of computer memory, and that the two or more years of experience would provide practical experience required to address issues such as low power backup for volatile memories. Ex. 1002 ¶¶ 31–32.

Patent Owner does not contest Petitioner's description of the level of ordinary skill in its Response. See PO Resp. 8. Based on our review of the '315 patent, the cited prior art, and Dr. Bagherzadeh's testimony, we determine a specific finding regarding ordinary skill level is not required as the prior art reflects an appropriate level. However, to the extent a specific finding regarding the level of skill is required, we adopt Dr. Bagherzadeh's description of a POSITA as it is consistent with the teachings of the prior art. Ex. 1002 ¶¶ 31–32.

B. Claim Construction

In an *inter partes* review filed before November 13, 2018, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b)(2017); Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018) (to be codified at 37 C.F.R. pt. 42). Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Prior to Institution, neither Petitioner nor Patent Owner identified any claim terms as warranting explicit construction. *See* Pet. 10; *see generally* Prelim. Resp. In its Preliminary Response, however, Patent Owner argued that the '315 patent requires that “*all* address and control lines are electrically isolated from the DRAM in the self refresh mode to avoid erratic signals from damaging or otherwise corrupting the data in the memory.” Prelim. Resp. 2 (emphasis added). Patent Owner argued because the cited art keeps one particular control line (i.e., control line CKE) active and connected to the memory devices during the self-refresh mode, the cited art does not teach electrically isolating *all* address and control lines. *See id.* at 8.

Our Decision on Institution states that we were not persuaded by Patent Owner’s argument because we did not understand the claims to

require electrically isolating memory devices from *all* address and control lines. Dec. on Inst. 13. We explained that the '315 patent identifies a number of address and control lines but only discusses electrically isolating certain of those address and control lines. *Id.* at 13–14. Specifically, we identified the embodiment of Figure 1, which the '315 patent describes as electrically isolating lines on control bus 22 and address bus 17 but does not describe as electrically isolating RAS and WE control lines 26 or 28. *Id.* We also identified the embodiment of Figure 4, which the '315 patent describes as electrically isolating control lines 122 and address lines 117 but does not describe as electrically isolating RAS and WE control lines 126 or 128. *Id.*

In its Response, Patent Owner again argues that “the phrase ‘selectively electrically isolating said memory devices from respective address lines and respective control lines’ must include *all* address and control signal lines.” PO Resp. 12 (emphasis added); *see generally id.* at 8–12 (citing Ex. 2001, 2). But Patent Owner clarifies in its Response, filed after institution, that the term *all* does not refer to address and control lines in general, but rather, refers to the address and control lines that communicate with the memory devices (i.e., “the respective address lines and the respective control lines”). *Id.* at 3; *see also id.* at 9–10. Specifically, Patent Owner contends that the:

only address and control lines which would need to be electrically isolated are the address and control lines which communicate to the memory devices because only those address and control lines could introduce errant signals which might adversely change data in the memory devices. Thus, the term “all” is referring to the class of address and control lines which

communicate with the memory devices, not address and control lines in general.

Id. at 9–10.

To support its claim construction, Patent Owner points to Figure 1 of the '315 patent. Patent Owner asserts RAS control line 26 and WE control line 28 of Figure 1 do not communicate with memory device 5 and, therefore “need not be electrically isolated from memory device 5 to protect the memory devices from any errant signals that might be on RAS and WE control lines, 26, 28.” *Id.* at 10. Patent Owner also asserts “Fig. 1 shows that the RAS and WE control lines 26, 28 must pass through control device 15 to reach the memory devices 5. Thus, control device 15 can also isolate . . . RAS 26 and WE 28 control lines consistent within the requirements of the '315 Patent, particularly the claims 1–9.” *Id.* at 19.

In addition, Patent Owner argues that the parties and the District Court in the *Goodman v. Hewlett-Packard Co.*, C.A. No. 16-CV-3195 (S.D. Tex.), adopted its proposed construction. *Id.* at 12 (stating “[a]ccordingly, the phrase ‘selectively electrically isolating said memory devices from respective address lines and respective control lines’ must include all address and control signal lines according to the address and control lines as construed by the parties and the District Court”).

Petitioner replies that the '315 patent does not disclose electrically isolating all address and control lines. Reply 4–5. Petitioner states the RAS and WE control lines of Figure 1 “are not included in control lines that make up ‘control buss 22’” and that the RAS and WE control lines of Figure 4 “are not part of ‘control buss 122.’” Reply 4–5 (citing Ex. 1001, 5:54–6:3, 9:7–26). Petitioner states that because Figure 1 identifies RAS and WE as

control lines, when Address & Control Center 15 electrically isolates control bus 22, there are at least two other control lines that are not electrically isolated. *Id.* at 4. Petitioner also states that RAS and WE of Figure 4 are not part of control bus 122, confirming that the claims do not require electrically isolating all address and control lines. *Id.* (citing Ex. 1001, 9:7–26).

Petitioner also argues Patent Owner’s proposed construction is narrower than that to which the parties agreed, and the District Court applied, because the agreed upon construction in the District Court did not include the word “all.” Reply 3 (identifying the District Court construction as “inhibiting signals on respective address and respective control lines from the memory devices such that signals on those lines do not arrive at the memory device”).

Based upon the full record, we agree with Patent Owner and determine the broadest reasonable construction consistent with the specification of a control device “for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices” as recited in independent claims 1 and 10, requires that the control device electrically isolate the memory devices from all address and control lines that communicate with the memory devices.

The plain language of the claims requires that the selected memory devices are electrically isolated from their *respective* address and control lines. Ex. 1001, 13:26–28, 14:11–18. In accordance with the plain and ordinary meaning, the reference in claim 1 to “respective address lines” and “respective control lines” is inclusive of all such lines for the selected

memory device. We further find that a claim construction limited to isolating all of a selected memory device's address and control lines is consistent with the purpose of such isolation expressed in claims 1 and 10, i.e. "so that when said memory devices are electrically isolated, *any* signals received on said respective address lines and said respective control lines do not reach said memory devices." *Id.* at 13:27–30, 14:15–18 (emphasis added).

Our construction is also consistent with the specification of the '315 patent, which explains that the invention prevents "errant control and address signals to the memory devices" by "electrically isolating the memory devices from signals received on the control lines and address lines." *Id.* at 3:15–24. The '315 patent states that when the memory devices are electrically isolated from the respective address lines and respective control lines, "*any* signals received on said respective address lines and respective control lines do not reach the memory devices." *Id.* at 4:16–24; *see also id.* at 3:25–30 (stating the "memory system maintains the integrity of the data retained by the memory devices by isolating the devices from the external power source, control lines and address lines").

Based upon a review of the full record, we also find that the '315 patent does not teach address or control lines that communicate with memory devices but are not electrically isolated from the memory devices. We are persuaded by Patent Owner's argument in its Response that the RAS and WE control lines 26, 28 of Figure 1 do not need to be electrically isolated from the memory devices because these lines connect to memory access enable control device 30 and therefore do not communicate with the memory devices. PO Resp. 10–11. The '315 patent states that RAS and WE

control lines 26, 28 are connected to memory access enable control device 30. Ex. 1001, 6:1–3. There is no express teaching that RAS control line 26 and WE control line 28 communicate with memory device 5. As such, there is no teaching in the '315 patent that memory devices 5 would need to be electrically isolated from RAS and WE control lines 26, 28 to prevent errant signals on these control lines from reaching the memory devices. Similarly, the '315 patent states that RAS and WE control lines 126 and 128 of Figure 4 are “connected to the control device” but does not state that the RAS and WE control lines communicate with memory devices. *Id.* at 9:24–26.

Rather, the '315 patent states that the outputs from the control device are address lines 120 and control lines 124 and that these outputs are inputs to the memory devices. *Id.* at 9:33–36. There is no disclosure in the '315 patent that the RAS and WE control lines are inputs to the memory devices. As such, there is no teaching in the '315 patent that memory devices 5 would need to be electrically isolated from RAS and WE control lines 26, 28 to prevent errant signals on these control lines from reaching the memory devices.

We also disagree with Petitioner’s argument that Patent Owner’s proposed construction is narrower than that applied in the District Court because the agreed upon construction in the District Court did not include the word “all.” Reply 3 (identifying the District Court construction as “inhibiting signals on respective address and respective control lines from the memory devices such that signals on those lines do not arrive at the memory device”). To focus on the presence or absence of the word “all” is too superficial because other language in the district-court construction has the same effect. That is, the language “inhibiting signals on *respective*

address and *respective* control lines” (emphasis added) includes all the address and control lines on the *selected* memory device. The District Court’s construction does not provide for inhibiting the signals on selected address and control lines of respective memories—it requires inhibiting signals on respective address and control lines of the selected memories.

Therefore, for the foregoing reasons, we construe a control device “for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices” as meaning that the control device electrically isolates the memory devices from all address and control lines that communicate with the memory devices.

We determine that no further claim construction is required to resolve the issues in dispute. See *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that only claims in controversy need to be construed and only to the extent necessary to resolve the controversy)).

C. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations⁸. See *Graham*, 383 U.S. at 17–18.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (*citing In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2016) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)).

To prevail on its challenges, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden never shifts to Patent Owner. See *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (*citing Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner does not

⁸ The parties have not provided any evidence or argument directed to secondary considerations, and therefore, secondary considerations do not constitute part of our analysis.

satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness. *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

D. Overview of the Asserted Art

1. Schaefer (Ex. 1003)

Schaefer describes a volatile memory device, such as a synchronous dynamic random access memory (“SDRAM”), “for storing data and responsive to command signals.” Ex. 1003, 1:57–60, 2:33–35. Schaefer’s SDRAM has memory arrays (i.e., bank 0 memory array 22 and bank 1 memory array 24) that comprise storage cells for storing data. *Id.* at 3:9–11. Command controller 28 controls the various circuitry for the SDRAM based on decoded commands, such as during controlled reads or writes from or to bank 0 memory array 22 and bank 1 memory array 24. *Id.* at 3:36–39. The SDRAM also has address lines A0–A10, control lines WE*, CAS*, and RAS*. *See id.* at 3:26–35, 3:43–45. Schaefer’s SDRAM has a self-refresh mode. *Id.* at 3:21–25. “All the input and output signals of SDRAM, with the exception of the CKE input signal during power down and self refresh modes, are synchronized to the active going edge . . . of the CLK signal.” *Id.* at 3:20–25 “A system clock (CLK) signal is provided through a CLK input pin and a clock enable signal (CKE) is provided through a CKE input pin to SDRAM 20. The CLK signal is activated and deactivated based on the state of the CKE signal.” *Id.* at 3:16–20.

2. Qureshi (Ex. 1004)

Qureshi is directed to, *inter alia*, a Joint Test Action Group (“JTAG”) test logic and memory controller for SDRAM chips, used for the *in situ* testing of integrated circuit chips mounted on a circuit board. Ex. 1004, 1:27–29. During JTAG testing of the chips, memory, such as SDRAMs, is put into a self-refresh mode. *Id.* at 1:63–65. “Self refresh is a refresh mode available in some memory and is preferred for data retention and low power operation.” *Id.* at 1:65–67. For an SDRAM in self-refresh mode, the SDRAM disables the system clock and all input buffers except CKE (clock enable). *Id.* at 1:65–2:2; *see also id.* at 5:49–51 (stating that “[o]nce the self refresh mode is entered, SDRAM 116 ignores all inputs other than a CKE (clock enable) pin while in self refresh state”). Qureshi states that the system has the “ability to dynamically enter and exit SDRAM self refresh before and after [JTAG] testing,” which saves debugging time. *Id.* at 2:54–56.

3. Mazur (Ex. 1005)

Mazur teaches a process “for preserving the RAM of an externally powered microprocessor on the occasion of a loss in external power.” Ex. 1005, [57]. According to Mazur, “[w]hen the power loss is detected, a signal is generated which initiates a sequence to isolate the RAM and refresh it with an independent power supply,” e.g., a rechargeable battery. *Id.*; *see also id.* at 2:8–11 (stating the “hardware comprises in coactive combination a power loss detection circuit, an independent power supply, a continuously rechargeable battery, . . . a standby refresh circuit, a switch-over circuit).

E. Asserted Obviousness of Claims 1 and 5 over Schaefer and Qureshi

Petitioner contends that independent claim 1 and dependent claim 5 are unpatentable under § 103(a) over the combined teachings of Schaefer and Qureshi. Pet. 3, 23–31, 39–44, 50. Patent Owner opposes. PO Resp. 15–21. Having considered the parties’ contentions and supporting evidence, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 1 and 5 are unpatentable under § 103 over Schaefer and Qureshi.

Our analysis focuses on claim element 1[e], which requires a control device “for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices.” As noted above in Section II.B, we construe claim element 1[e] as requiring that the control device electrically isolate the memory device from all address and control lines that communicate with the memory device.

Patent Owner contends that the combination of Schaefer and Qureshi does not teach all of the limitations of claim element 1[e] because control line CKE of the asserted art remains an input to the memory devices even during refresh, and therefore, the memory devices are not electrically isolated from *all* address and control lines as required by claim 1. See PO Resp. 20–21.

Petitioner replies that “CKE may be a control signal,” but because the claims do not require the control device “to electrically isolate all address

lines and control lines, it is irrelevant that CKE in Schaefer's DRAM is not electrically isolated." Reply 7.

We agree with Patent Owner that Petitioner has not persuasively shown that the combination of Schaefer and Qureshi teaches a control device that electrically isolates the memory devices as required under the claim construction set forth above in Section II.B. Specifically, because Petitioner has not shown that the CKE signal, which communicates with the claimed memory devices, is electrically isolated from the memory devices, Petitioner has not shown that memory devices are electrically isolated from "respective control lines" such that "any signals received on said . . . respective control lines do not reach said memory devices" as required by claim 1.

Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 1 of the '315 patent would have been obvious over the combination of Schaefer and Qureshi.

Claim 5 depends from claim 1 and, therefore, also includes this limitation. Petitioner's arguments regarding the unpatentability of claim 5 do not remedy the deficiency with regard to claim 1. Pet. 30, 20–51. As such, we also determine that Petitioner has not shown by a preponderance of the evidence that claim 5 of the '315 patent would have been obvious over the combination of Schaefer and Qureshi.

F. Asserted Obviousness of Independent Claim 10 over Schaefer, Qureshi, and Mazur

Petitioner contends that claim 10 is unpatentable under § 103 over the combined teachings of Schaefer, Qureshi, and Mazur. Pet. 3, 17–21, 31–39, 44–50. Patent Owner opposes. PO Resp. 22. Having considered the parties' contentions and supporting evidence, we disagree with Patent

Owner's arguments and determine that Petitioner has demonstrated by a preponderance of the evidence that claim 10 is unpatentable under § 103 over Schaefer, Qureshi, and Mazur.

1. Reason to Combine Schaefer, Qureshi, and Mazur

In general, claim 10 is directed to a memory system having volatile solid state memory devices having address and control lines, first and second electrical power sources, and a control device (1) for monitoring when the first voltage from the first power source is less than a predetermined voltage, (2) for selectively electrically isolating the memory devices from respective address and respective control lines, and (3) for disconnecting the first electrical power source from the memory devices and connecting the second electrical power source to the memory devices when the first voltage is less than the predetermined voltage. Claim 10 further states that the data in the memory devices is preserved by the second electrical power source when the first power source fails maintain a predetermined voltage, and the memory devices are isolated from errant signals.

Relying on the testimony of Dr. Bagherzadeh, Petitioner asserts that a POSITA would have been motivated to combine the teachings of Schaefer, Qureshi, and Mazur to arrive at the subject matter of claim 10. Pet. 17–19, 21–23, 44–45, 48, 50–51; Ex. 1002 ¶¶ 32–35, 48–53, 68–73. Petitioner explains that Qureshi teaches a memory controller that is configured to place SDRAM memory into a low power self-refresh mode for the purposes of testing data retention, while Schaefer teaches an SDRAM memory that is available for testing and includes a low power self-refresh mode that is used to retain data in low power situations. Pet. 17–18 (citing Ex. 1003, 3:3–6; Ex. 1004, 1:65–2:2; Ex. 1002 ¶ 48). Petitioner asserts that a POSITA would

have combined the teachings of Schaefer and Qureshi because “the functional electronic modules of Schaefer and Qureshi are configured to work together.” *Id.* at 17 (citing Ex. 1002 ¶ 48); *see also generally id.* at 17–21 (section of the Petition titled “Motivation to Combine References”); Ex. 1002 ¶¶ 32–35, 48–53. In the section of the Petition titled “Differences Between the Prior Art and the Patent Claims,” Petitioner also states that “a POSITA would seek to use the memory controller of Qureshi to place the DRAM memory of Schafer into the low power self-refresh mode so that existing data may be retained, while other signals may be ignored, and the amount of power consumed from the computer system is reduced.” Pet. 14 (citing Ex. 1002 ¶¶ 48–53).

Petitioner further asserts that Schaefer teaches that a power failure situation would require a reset of the components in the memory device and that Mazur teaches the use of a backup battery as an alternative power source to drive DRAM memory devices in the low power self-refresh mode. Pet. 9, 12–13, 19–20; Ex. 1002 ¶ 45; Ex. 1003, 4:4–7; Ex. 1005, 3:41–47. Petitioner further asserts a POSITA would have combined Mazur with Schaefer and Qureshi in order to, *inter alia*, enable retention of SDRAM data during testing phase without concern as to power losses. Pet. 20–21 (citing Ex. 1002 ¶¶ 67–73).

Patent Owner responds Petitioner has not articulated a reason to combine Schaefer and Qureshi because it is “not logical to conclude that Qureshi is suggesting that it should be combined with Schaefer to reduce power consumption.” PO Resp. 16–18 (citing Pet. 14; Ex. 1002 ¶¶ 48–53).

We disagree with this argument because it ignores Petitioner’s argument that a POSITA would have been motivated to combine Schaefer

with Qureshi because the functional electronic modules of Schaefer and Qureshi are configured to work together during testing of Schaefer's DRAMs using Qureshi's memory controller. Pet. 17; Ex. 1002 ¶ 48.

Indeed, even Patent Owner admitted on the preliminary record that "[t]here is no dispute that Schaefer and Qureshi can be combined." Prelim. Resp. 4; *see also id.* at 4–5 (arguing patentability of claims 10 and 16 over Schaefer, Qureshi, and Mazur by stating that although "[t]here is no dispute that Schaefer and Qureshi can be combined" . . . "Petitioner has failed to provide a technical argument for combining Mazur with the combination of Schaefer and Qureshi"). We have reviewed Petitioner's evidence and argument, including the testimonial evidence of Dr. Bagherzadeh, and agree with Petitioner. We find that a POSITA would have utilized Qureshi's memory controller for initiating a low power self-refresh mode during testing of Schaefer's SDRAM to ensure that data is retained during testing. *See* Pet. 18–19; Ex. 1002 ¶ 50.

Patent Owner also argues that Petitioner "has not provided any insight as to how the references can be combined to suggest claim 10" and therefore the proposed combination is "only speculation, and without merit." PO Resp. 22. This argument is not persuasive. The test for obviousness is "not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981); *see also In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) ("[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review."); *In re Nievelt*, 482 F.2d 965,

968 (CCPA 1973) (“Combining the *teachings* of references does not involve an ability to combine their specific structures.”). As the Supreme Court has explained, “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *KSR*, 550 U.S. at 417.

Petitioner has provided persuasive argument and evidence, supported by the unrebutted declaration testimony of Dr. Bagherzadeh, that a POSITA would have combined the teachings of Schaefer, Qureshi, and Mazur so as to enable retention of the SDRAM data during the testing phase without concern as to power losses. Pet. 17–19, 21–23, 44–45, 48, 50–51; Ex. 1002 ¶¶ 32–35, 48–53, 68–73, 78, 81. We credit Dr. Bagherzadeh’s unrebutted testimony that because “Qureshi’s memory controller is configured to force Schaefer’s memory device into a low power self-refresh mode for data retention during testing, a POSITA would recognize that this low power mode may be supported by a battery backup instead of the primary power source, thereby enabling failure of the primary power source without the need for resetting any components.” *Id.* ¶ 69.

We also agree with Petitioner’s argument, supported by the undisputed testimony of Dr. Bagherzadeh, that combining the teachings of the art merely brings together a unified overall function between the three modules and is within the capabilities of a POSITA. *See, e.g.*, Pet. 20–21; Ex. 1002 ¶¶ 35, 50, 68. We credit Dr. Bagherzadeh’s unrebutted testimony that a POSITA possesses the requisite skill to combine basic electrical components in an expected or natural way (as described in each reference) to meet the claimed limitations. Ex. 1002 ¶¶ 31–35, 52, 53, 73. We further

credit Dr. Bagherzadeh’s un rebutted testimony that a “POSITA would understand that the circuit of Mazur may be adapted to detect when the power supply falls below a range of 3.0 V to 4.8 V, if a different DRAM, with a different operating voltage is used to perform the functions of the ’315 patent.” *Id.* ¶ 78 (citing Ex. 1005, 3:9–16, 5:36–39, 7:21–22), 81; Pet. 49.

Accordingly, we find Petitioner has sufficiently articulated reasons with rational underpinning for why a POSITA would have combined the teachings of Schaefer, Qureshi, and Mazur and that such a combination was within the skill level of a POSITA.

2. Claim Elements 10[a]–10[h]

Petitioner asserts that the combination of Schaefer, Qureshi, and Mazur teaches each of the limitations of claim 10. Patent Owner has not presented any argument that the cited art does not teach the limitations of claim 10 in its Patent Owner Response; therefore, any such arguments are waived. *See Novartis AG v. Torrent Pharm. Ltd.*, 853 F.3d 1316, 1330 (Fed. Cir. 2017); *In re Nuvasive*, 842 F.3d 1376, 1381 (Fed. Cir. 2016).⁹ Nevertheless, in “an *inter partes* review, the burden of persuasion is on the petitioner to prove ‘unpatentability by a preponderance of the evidence,’ . . . and that burden never shifts to the patentee.” *Dynamic Drinkware*, 800 F.3d at 1378 (quoting 35 U.S.C. § 316(e)).

⁹ As in *Nuvasive*, the Scheduling Order in this proceeding cautioned Patent Owner that “any arguments for patentability not raised in the response will be deemed waived.” Paper 7, 3.

1. Preamble – claim element 10[a]

Preamble language that merely states the purpose or intended use of an invention generally is not treated as limiting the scope of a claim. *See Boehringer Ingelheim Vetmedica, Inc. v. Schering–Plough Corp.*, 320 F.3d 1339, 1345 (Fed. Cir. 2003). When the limitations in the body of the claim rely upon or derive essential structure from the preamble, however, then the preamble acts as a necessary component of the claimed invention and is limiting. *See Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003).

The preamble of claim 10 recites a “memory system for use in a computer system, said memory system comprising.” We find that this preamble merely states the purpose or intended use of the invention and, as such, does not limit the scope of the claim. To the extent the preamble is limiting, we agree with Petitioner’s undisputed assertions and find that the preamble limitations are taught by Schaefer, Qureshi, and Mazur. Pet. 31 (stating Mazur discloses hardware that may be implemented in a memory system), 39 (stating Schaefer’s SDRAM is a memory system capable of retaining data), 23–24 (stating Schaefer discloses an SDRAM memory device that is configured to receive signals from Qureshi’s memory controller); Ex. 1003, 2:33–35, 3:3–6, Fig. 1; Ex. 1004, 2:3–6, Fig. 1; Ex. 1005, 2:6–14, 3:27–29; Ex. 1002 ¶¶ 54–55.

2. Claim Element 10[b]

Claim element 10[b] recites “a plurality of volatile solid state memory devices that retain information when an electrical power source having a voltage greater than a predetermined voltage is applied to said devices.” Petitioner asserts Schaefer and Mazur teach this limitation. Pet. 24–25, 31–

32. Petitioner asserts Schaefer’s SDRAM device has two bank memory arrays, bank 0 and bank 1 (a plurality of volatile solid state memory devices) that retain information when an electrical power source is applied. Pet. 24–25, 39 (citing Ex. 1003, 2:36–37, 3:13–16; Ex. 1002 ¶¶ 54–55). Relying on the un rebutted testimony of Dr. Bagherzadeh, Petitioner asserts that the SDRAM of Schaefer is configured to work within a predetermined voltage range of 3 V to 3.6 V. *Id.* at 39 (citing Ex. 1002 ¶ 56; Ex. 1008, 1). Petitioner also relies on Mazur’s teaching that the Vcc signal of the computer supply is greater than at least 4.8V for the DRAM memory devices. *Id.* at 31 (citing Ex. 1005, 5:11–15).

We agree with Petitioner’s analysis of this limitation, which Patent Owner does not dispute, and find that Schaefer and Mazur teach the volatile solid state memory devices required by claim element 10[b].

4. Claim element 10[c]

Claim element 10[c] recites “said memory devices having address lines and control lines.” For this limitation, Petitioner relies on Schaefer’s disclosure of “address bits on input pins A0–A10” and “control signals including a row address strobe (RAS*) signal on a RAS* pin, column address strobe (CAS*) signal on a CAS* pin, and a write enable (WE*) signal on a WE* pin.” Pet. 25–26, 40 (emphasis omitted) (quoting Ex. 1003 3:30–33, 4:19–21); Ex. 1002 ¶ 58. We agree with Petitioner’s analysis of this claim element, which Patent Owner does not dispute, and find that Schaefer teaches memory devices having address and control lines, as required by claim element 10[c].

5. *Claim element 10[d]*

Claim element 10[d] recites “said computer system including a first electrical power source for operating said computer and being capable of producing a first voltage applied to said memory devices.” For this limitation, Petitioner relies on, *inter alia*, Mazur’s disclosure of a “power supply” that supplies at least 4.8V for the DRAM memory devices. Pet. 32–33 (citing Ex. 1005, 3:9–16, 5:11–15, 5:36–39). We agree with Petitioner’s analysis of this claim element, which Patent Owner does not dispute, and find that Mazur teaches a first electrical power source, as required by claim element 10[d].

6. *Claim element 10[e]*

Claim element 10[e] recites:

control device for monitoring said first voltage to determine when said first voltage is less than said predetermined voltage and for selectively electrically isolating said memory devices from respective address lines respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory device.

For this claim element, Petitioner relies on the combined teachings of Schaefer, Qureshi, and Mazur. Pet. 33–36, 47–48. Petitioner asserts that Mazur teaches a power loss detection circuit that detects when the power supply falls below 4.8V. Pet. 33–34 (citing Ex. 1005, 3:9–16, 5:36–39). Petitioner further asserts that Mazur teaches that when a drop in power is sensed, the refresh switch-over circuit provides control signals internal to the DRAM rather than from within the computer, thereby isolating the DRAM. *Id.* at 34–35 (citing Ex. 1005, 4:17–32).

Petitioner further contends that Qureshi teaches a memory controller (“control device”) that is configured to place SDRAM memory, such as the SDRAM of Schaefer, into a low power self-refresh mode, for the purposes of testing data retention, and that Schaefer teaches an SDRAM memory that is available for testing and includes a low power self-refresh mode that is used to retain data in low power situations. Pet. 17–18, 26–27, 40–41. Petitioner asserts that a POSITA would understand that the memory controller of Qureshi is a control device that may be modified to include the circuit components of Mazur so as to isolate the DRAM of Schaefer from errant signals on address and control lines in the low power self-refresh mode, while providing the signals internally so that no data is lost. *Id.* at 34–35, 47–48 (citing Ex. 1002 ¶¶ 68–69, 78–79; Ex. 1005, 4:17–32, 5:13–14). Petitioner asserts that because Mazur’s refresh switch-over circuit provides the control signals internal to the DRAM, external signals are not provided to the DRAM and therefore, any signals received on the respective address and control lines do not reach the memory devices. See Pet. 35, 47–48 (citing Ex. 1005, 4:17–32; Ex. 1002 ¶¶ 78–79).

We agree with Petitioner’s analysis of this claim element, which Patent Owner does not dispute, and find that Schaefer, Qureshi, and Mazur teach the control device required by claim element 10[e].

7. Claim element 10[f]

Claim element 10[f] recites “a second electrical power source operable for supplying a second voltage to said memory devices greater than said predetermined voltage.” For this claim element, Petitioner relies on Mazur’s teaching of a rechargeable battery that provides power to the

DRAM device at a voltage level greater than 4.8V. Pet. 35–36 (citing Ex. 1005, 3:9–16, 5:11–15, 5:36–39).

We agree with Petitioner’s analysis of this claim element, which Patent Owner does not dispute, and find that Mazur teach a second electrical power source, as required by claim element 10[f].

8. Claim element 10[g]

Claim element 10[g] recites a “control device being operable for disconnecting said first electrical power source from said memory devices and connecting said second electrical power source to said memory devices when said first voltage is less than said predetermined voltage.” For this claim element, Petitioner relies on the combined teachings of Schaefer, Qureshi, and Mazur. Pet. 36–37, 49–50. Petitioner asserts that Mazur teaches a “power switch-over circuit” that switches power from the computer circuit 16 to the power supply 18 when a power failure of less than 4.8V is detected. Pet. 49. Petitioner contends that a POSITA would understand that the memory controller of Qureshi (“control device”) can be modified to include the power switch-over components of Mazur that are configured to switch power from computer circuit 16 to power supply 18, when the power failure occurs. Pet. 49 (citing Ex. 1002 ¶ 81). Petitioner explains that both Qureshi and Schaefer teach that power failure would disrupt the data retention capabilities of the SDRAM and that use of Mazur’s backup battery would avoid the need to reset components in the event of a power failure. *Id.* at 19–20, 49–50 (citing Ex. 1003, 4:4–7, Ex. 1005, 5:13–14; Ex. 1002 ¶ 69).

We agree with Petitioner’s analysis of this claim element, which Patent Owner does not dispute, and find that Mazur teach the control device as required by claim element 10[g].

9. *Claim element 10[h]*

Claim element 10[h] recites that the “data in said memory devices is preserved by said second electrical power source when said first electrical power source fails to maintain at least said predetermined voltage on said memory devices, and said memory devices are isolated from errant signals.” For this claim element, Petitioner relies on the combined teachings of Schaefer, Qureshi, and Mazur. Pet. 38, 50. Petitioner cites to its arguments regarding claim elements 10[e]–10[f] and further asserts that Mazur teaches that when the rechargeable battery supply provides the power required to maintain the data in the DRAM, the refresh signals are then internally generated and that the low power self-refresh mode prevents corruption of the data by electrically isolating the DRAM from errant signals. *See id.* at 38, 50 (citing Ex. 1005, 4:17–32; Ex. 1002 ¶ 82).

We agree with Petitioner’s analysis of this claim element, which Patent Owner does not dispute, and find that the cited art teaches preserving the data in memory devices and isolating the memory devices from errant signals as required by claim element 10[h].

For the foregoing reasons, we find that the combination of Schaefer, Qureshi, and Mazur teach each of the limitations of claim 10 and that Petitioner has sufficiently articulated reasons with rational underpinning for why a POSITA would have combined the teachings of Schaefer, Qureshi, and Mazur to arrive at the claimed subject matter of claim 10. Accordingly,

we find Petitioner has shown by a preponderance of the evidence that claim 10 is unpatentable under § 103 over Schaefer, Qureshi, and Mazur.

G. Asserted Obviousness of Dependent Claim 16 over Schaefer, Qureshi, and Mazur

Claim 16, which depends from claim 10, requires that the memory devices are DRAM semiconductor chips. We agree with Petitioner's undisputed argument and evidence that the memory chips taught in both Schaefer and Qureshi are synchronous dynamic random access memory (SDRAM), which is a type of DRAM, and that Mazur teaches DRAM memory devices. Pet. 30, 50–51; Ex. 1003, 2:33–35; Ex. 1002 ¶¶ 65, 83. Accordingly, for these reasons as well as the reasons given in our analysis of independent claim 10 above, we find Petitioner has shown by a preponderance of the evidence that claim 16 is unpatentable over Schaefer, Qureshi, and Mazur.

III. CONCLUSION

Based on the evidence and arguments, we determine:

(1) Petitioner has not demonstrated by a preponderance of the evidence that claims 1 and 5 are unpatentable under 35 U.S.C. § 103(a) over the combination of Schaefer and Qureshi; and

(2) Petitioner has demonstrated by a preponderance of the evidence that claims 10 and 16 are unpatentable under 35 U.S.C. § 103(a) over the combination of Schaefer, Qureshi, and Mazur.

IV. ORDER

Accordingly, it is

ORDERED that claims 1 and 5 of U.S. Patent No. 6,243,315 B1 have not been shown to be unpatentable;

ORDERED that claims 10 and 16 of U.S. Patent No. 6,243,315 B1 are held to be unpatentable; and

FURTHER ORDERED that, because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-01994
Patent 6,243,315 B1

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