

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS AMERICA, INC. and
ASUS COMPUTER INTERNATIONAL, INC.,
Petitioner,

v.

JAMES B. GOODMAN,
Patent Owner

Case IPR2017-02021¹
Patent 6,243,315 B1

Before BRIAN J. McNAMARA, PATRICK M. BOUCHER, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Case IPR2018-00047, filed by ASUS Computer International, Inc. (“ASUS”), has been joined with this proceeding.

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Samsung Electronics America, Inc. and ASUS Computer International, Inc. (collectively “Petitioner”) challenge the patentability of claims 1–20 (“the challenged claims”) of U.S. Patent No. 6,243,315 B1 (Ex. 1001, “the ’315 patent”²), owned by James B. Goodman (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during trial. For the reasons discussed below, we determine that Petitioner has shown by a preponderance of the evidence that claims 1, 5, 10, and 16 of the ’315 patent are unpatentable but has not shown by a preponderance of the evidence that claims 2–4, 6–9, 11–15, and 17–20 are unpatentable.

A. Procedural History

On August 29, 2017, Samsung Electronics America, Inc. filed a Petition requesting an *inter partes* review of claims 1–20 of the ’315 patent. Paper 2 (“Pet.”). The Petition is supported by the declaration testimony of Dr. Andrew Wolfe. Ex. 1002. Patent Owner filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

On October 12, 2017, ASUS Computer International, Inc. (“ASUS”) filed a Petition requesting *inter partes* review of claims 1–20 of the ’315 patent on the same grounds and arguments presented in Case IPR2017-02021 and requested joinder with Case IPR2017-02021. *See* Case IPR2018-00047, Papers 2, 3. Patent Owner filed a Preliminary Response. Case IPR2018-00047, Paper 7.

² Citations are to IPR2017-02021 unless otherwise indicated.

On March 9, 2018, we instituted an *inter partes* review of the challenged claims in IPR2017-02021. Paper 7 (“Decision on Institution” or “Dec. on Inst.”). On March 20, 2018, we granted ASUS’s request for *inter partes* review and for joinder of the IPR2018-00047 proceeding with IPR2017-02021. IPR2018-00047, Paper 9. On June 1, 2018, Patent Owner filed a Patent Owner Response. Paper 10. On August 24, 2018, Petitioner filed a Reply. Paper 11 (“Reply”).

A hearing was held on November 16, 2018. A transcript of the hearing has been entered into the record. Paper 18 (“Tr.”).

B. Related Proceedings

Petitioner identifies the following litigations as related proceedings: *Goodman v. Samsung Electronics America, Inc.*, Case No. 1:17-cv-05539 (S.D.N.Y.); *Goodman v. Hewlett-Packard Co.*, Case No. 4:16-cv-03195 (S.D. Tex.); *Goodman v. ASUS Computer Int’l, Inc.*, Case No. 4:16-cv-03232 (S.D. Tex.). Pet. 2.

Patent Owner further identifies the following litigations as related proceedings: *Goodman v. ASUS Computer Int’l*, Case No. 17-cv-05542 (N.D. Cal.) (transferred from the S.D. Tex.); *Goodman v. Lenovo (United States) Inc.*, Case No. 17-cv-06782; and *Goodman v. Acer American Corp.*, Case No. 17-cv-07297. See Prelim. Resp. 2; IPR2018-00047, Prelim. Resp. 3.

We also note that the ’315 patent was the subject of a Final Written Decision in *HP Inc. v. Goodman* (Case IPR2017-01994) in which we determined claims 1 and 5 were not shown to be unpatentable but that claims 10 and 16 were shown to be unpatentable. IPR2017-01994, Paper 16. The ’315 patent was also the subject of a petition for *inter partes* review in

SMART Modular Technologies, Inc. v. Goodman, Case IPR2015-01675, in which the Board instituted *inter partes* review and subsequently granted the parties' joint motion to terminate. See IPR2015-01675, Paper 20.

C. The '315 patent

The '315 patent is directed to memory systems having volatile solid state memory devices that retain information when an electrical power source is applied but lose their memory contents when power is removed. Ex. 1001, 2:54–58, 3:46–52. To reduce energy consumption and preserve memory contents, volatile memory devices are placed in low power “self-refresh mode” when the memory system is not receiving requests for access. See *id.* at 3:46–54 (stating the “low power mode utilizes significantly less electrical current than when the memory device is in the operating mode or powered up mode”), 3:25–30 (stating “placing the memory devices into a power down self-refresh mode . . . will maintain the data using a minimum of electrical power”). The memory system of the '315 patent has a control device interposed electrically between the memory devices and a central processing unit (“CPU”). *Id.* at 3:54–56. The control device senses CPU access of the memory devices and conditions the memory devices to an operating mode condition prior to allowing access to the information contained therein. *Id.* at 3:56–59. The control device also places the solid state memory devices into a low power standby mode when it “senses the termination of a memory cycle.” *Id.* at 3:59–62.

Figure 1 of the '315 patent, reproduced below, illustrates a preferred embodiment in which address and control busses are electrically isolated from the memory devices when the memory devices are in a power down self refresh mode. *Id.* at 5:60–63.

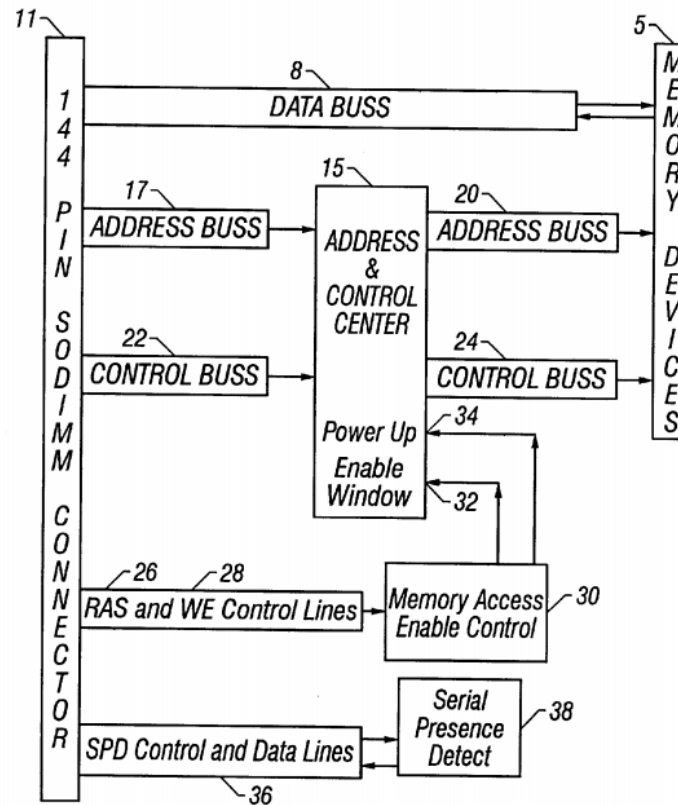


FIG. 1

As shown in Figure 1 of the '315 patent above, control device 15 is interdisposed between address buss 17 and address buss 20 (*id.* at 5:50–52) as well as in between control buss 22 and control buss 24 (*id.* at 5:54–56). Control devices 15 isolates address buss 17 and control buss 22 from memory devices 5 when the memory devices are in a power down self refresh mode. *Id.* at 5:60–63. By isolating the memory devices from control buss 22 and address buss 17, control device 15 prevents errant signals from erroneously changing or affecting the data being retained by memory devices 5. *Id.* at 5:63–67.

Figure 1 also shows row address select (“RAS”) control lines 26 and write enable (“WE”) control lines 28, which are connected to memory access enable control device 30. *Id.* at 6:1–3. Memory access enable control device 30 receives signals from the CPU indicating that a memory

access is pending. *Id.* at 6:3–5. Memory access enable control device 30 then signals control device 15 to bring memory devices 5 up to a normal operating mode. *Id.* at 5:56–59, 6:5–8. Memory access enable control device 30 can also signal control device 15 to indicate when memory devices 5 are to be placed in a power down mode. *Id.* at 5:56–59.

Another preferred embodiment of the '315 patent is shown in the block diagram of Figure 4, reproduced below. *Id.* at 4:41–42.

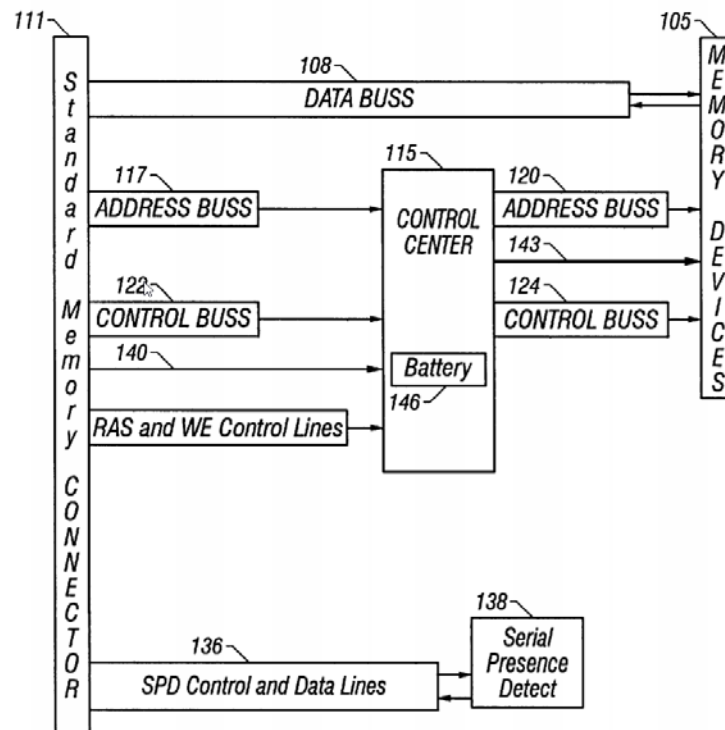


FIG. 4

Figure 4 of the '315 patent, shown above, is a block diagram of a preferred embodiment of the invention that switches the voltage source from the system electrical source input on line 140 to battery 146 when the input voltage level is less than a fixed amount and electrically isolates address and control lines. *Id.* at 9:41–46. As shown in Figure 4, control device 115 is interdisposed between address buss 117 and address bus 120 (*id.* at 9:16–20) and between control buss 122 and control buss 124 (*id.* at 9:20–23).

Figure 4 “also shows RAS, row address select lines, 126 and WE, write enable, 128 control lines connected to” control device 115. *Id.* at 9:24–26. The “system input electrical power source line 140 and control lines 122 and address lines 117 are inputs into control device 115.” *Id.* at 9:31–33. The outputs from control device 115 are address lines 120 control lines 124 and voltage line 143. *Id.* at 9:33–34. Voltage line 143 supplies power at a predetermined voltage level to the memory devices. *Id.* at 9:36–37.

Control device 115 compares the input voltage on line 140 against a fixed reference voltage; when the input voltage level is less than the fixed reference voltage, the output electrical voltages source is switched from the system electrical source input on line 140 to battery 146. *Id.* at 9:41–43. Control device 115 then electrically isolates the “memory devices 105 from . . . control lines 122 and address lines 177” to prevent errant signals. *Id.* at 9:43–47.

D. Illustrative Claims

Of the claims challenged by Petitioner, only claims 1 and 10 are independent and are reproduced below.³

1. A memory system for use in a computer system, said memory system comprising:

[a] a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh mode; said memory devices having address lines and control lines;

³ Paragraph breaks and bracketed letters have been added for ease of reference and for consistency with nomenclature utilized by Petitioner.

- [b] a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and
- [c] a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.

Id. at 13:18–40.

10. A memory system for use in a computer system, said memory system comprising:
 - [a] a plurality of volatile solid state memory devices that retain information when an electrical power source having a voltage greater than a predetermined voltage is applied to said devices; said memory devices having address lines and control lines;
 - [b] said computer system including a first electrical power source for operating said computer and being capable of producing a first voltage applied to said memory devices;
 - [c] a control device for monitoring said first voltage to determine when said first voltage is less than said predetermined voltage and for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and
 - [d] a second electrical power source operable for

supplying a second voltage to said memory devices greater than said predetermined voltage;

[e] said control device being operable for disconnecting said first electrical power source from said memory devices and connecting said second electrical power source to said memory devices when said first voltage is less than said predetermined voltage;

[f] whereby, data in said memory devices is preserved by said second electrical power source when said first electrical power source fails to maintain at least said predetermined voltage on said memory devices, and said memory devices are isolated from errant signals.

Id. at 13:65–14:32.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–20 are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Basis
1, 5	§ 102(e)	Dell ⁴
10, 16	§ 103	Dell and Abe ⁵
2–4, 6–9	§ 103	Dell and JESD21-C ⁶
11–15, 17–20	§ 103	Dell, Abe, and JESD21-C
1, 5	§ 103	Ooishi ⁷ and Palaniswami ⁸
10, 16	§ 103	Ooishi, Palaniswami, and Abe

⁴ U.S. Patent No. 6,327,664 (filed April 30, 1999, issued Dec. 4, 2001) (Ex. 1004, “Dell”)

⁵ U.S. Patent No. 5,590,082 (issued Dec. 31, 1996) (Ex. 1005, “Abe”)

⁶ *JEDEC STANDARD No. 21-C, Release 7, Configurations for Solid State Memories*, Electronics Indus. Assoc. Jan. 1997 (Ex. 1006, “JESD21-C”).

⁷ U.S. Patent No. 6,172,928 (issued Jan. 9, 2001) (Ex. 1008, “Ooishi”).

⁸ U.S. Patent No. 6,144,219 (issued Nov. 7, 2000) (Ex. 1009, “Palaniswami”).

II. DISCUSSION

A. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). Petitioner contends a person of ordinary skill in the art at the time of the alleged invention of the '315 patent (a "POSITA") would have had, *inter alia*, a bachelor's degree in electrical, electronics, computer engineering; or the equivalent training, and would have had approximately 2 to 3 years of experience in computer systems, circuits, electronics, or a related discipline. Pet. 9; Ex. 1002 ¶¶ 27–30. Patent Owner does not contest Petitioner's description of the level of ordinary skill. See PO Resp. 8.

Based on our review of the '315 patent, the cited prior art, and Dr. Wolfe's testimony, we determine a specific finding regarding ordinary skill level is not required as the prior art reflects an appropriate level. See *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown"). However, to the extent a specific finding regarding the level of skill is required, we find Petitioner's articulation of a person of ordinary skill in the art is consistent with the teachings of the prior art and adopt Petitioner's description of a POSITA as someone who "would have had a bachelor's degree in electrical, electronics, or computer engineering; or the equivalent training, and would have had approximately two to three years of experience in computer systems, circuits, electronics, or a related discipline." See Pet. 9.

B. Claim Construction

In an *inter partes* review filed before November 13, 2018, such as here, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2017)⁹; *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Petitioner asserts that under the broadest reasonable construction, the plain meaning of the phrase “selectively electrically isolating said memory devices from respective address lines and respective control lines,” found in independent claims 1 and 10, “in the context of conventional memory devices and signals is that such signals are inhibited from arriving at the given memory devices.” Pet. 10 (citing Ex. 1002 ¶ 47). In its Preliminary Response, Patent Owner did not identify any claim terms as warranting explicit construction but did argue the claims of the ’315 patent require that “*all* address and control lines are electrically isolated from the memory

⁹ This rule has been amended for later filed cases. See 37 C.F.R. § 42.100(b)(2018); see also Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,340 (Oct. 11, 2018) (stating “[t]his rule is effective on November 13, 2018 and applies to all IPR, PGR, and CBM petitions filed on or after the effective date”).

devices in the self refresh mode to avoid erratic signals from damaging or otherwise corrupting the data in the memory.” Prelim. Resp. 2 (emphasis added). Patent Owner argued, *inter alia*, the asserted prior art reference (i.e., Dell) did not anticipate the challenged claims of the ’315 patent because Dell did not isolate a control line (i.e., clock enable (“CKE”) line) from its memory bank, even when the memory bank is in a power down state. *See id.* at 11.

In our Decision on Institution, we disagreed with Patent Owner’s argument that the claims required electrically isolating *all* address and control lines from the memory device. Dec. on Inst. 12–13. We explained that the ’315 patent identifies a number of address and control lines but only discusses electrically isolating certain of those address and control lines. *Id.* at 13. Specifically, we identified the embodiment of Figure 1, which the ’315 patent describes as electrically isolating lines on control bus 22 and address bus 17 but does not describe as electrically isolating RAS and WE control lines 26 or 28. *Id.* We also identified the embodiment of Figure 4, which the ’315 patent describes as electrically isolating control lines 122 and address lines 117 but does not describe as electrically isolating RAS and WE control lines 126 or 128. *Id.*

In its Response, Patent Owner again argues that claims 1 and 10 require *all* address and control lines to be electrically isolated from the memory devices to avoid erratic signals from corrupting data in the memory devices. *See, e.g.*, PO Resp. 14–16. Patent Owner contends the ’315 patent “makes it clear that the claimed invention is to protect the data in the memory devices during self refresh from errant signals which might reach the memory devices.” PO Resp. 14 (citing Ex. 1001, 4:11–24, 5:63–67).

Petitioner replies the claims only require “isolation from ‘respective address lines and respective control lines’—not *all* address lines and *all* control lines.” Reply 9–10. Petitioner argues Patent Owner mischaracterizes the stated purpose of the ’315 Patent, which is to isolate the memory from only the specifically identified address lines and control lines—not every single conceivable signal. *Id.* at 7 (citing Ex. 1001, 5:63–67).

Based upon a review of the full record, we determine the broadest reasonable construction consistent with the Specification of a control device “for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices” as recited in independent claims 1 and 10 requires that the control device electrically isolate the memory devices from *all* address and control lines that communicate with the memory devices.¹⁰

The plain language of the claims requires that the selected memory devices are electrically isolated from their *respective* address and control lines. *See* Ex. 1001, 13:26–28, 14:11–18. In accordance with the plain and ordinary meaning, the reference in claim 1 to “respective address lines” and “respective control lines” is inclusive of *all* such lines for the selected memory device.

We further find that a claim construction limited to isolating *all* of a selected memory device’s address and control lines is consistent with the

¹⁰ We note that the same claim construction issue was presented in IPR2017-01994 and that we have adopted the same construction in both proceedings. IPR2017-01994, Paper 16, 11–17.

purpose of such isolation expressed in claims 1 and 10, i.e., “so that when said memory devices are electrically isolated, *any* signals received on said respective address lines and said respective control lines do not reach said memory devices.” *Id.* at 13:27–30, 14:15–18 (emphasis added).

Our construction is also consistent with the Specification of the ’315 patent, which explains that the invention prevents “errant control and address signals to the memory devices” by “electrically isolating the memory devices from signals received on the control lines and address lines.” *Id.* at 3:15–24. The ’315 patent states that when the memory devices are electrically isolated from the respective address lines and respective control lines, “any signals received on said respective address lines and respective control lines do not reach the memory devices.” *Id.* at 4:16–24; *see also id.* at 3:25–30 (stating the “memory system maintains the integrity of the data retained by the memory devices by isolating the devices from the external power source, control lines and address lines”); *id.* at 5:63–67 (“By isolating the memory devices from the control buss 22 and address buss 17 the control device 15 prevents errant signals from erroneously changing or affecting the data being retained by the memory devices 5.”). We are persuaded by Patent Owner’s argument that the purpose of the invention—to prevent errant control and address signals from reaching the memory devices—would not be achieved if errant signals on some control lines were able to reach the memory devices.

The ’315 patent states that RAS and WE control lines 26, 28 are connected to memory access enable control device 30. Ex. 1001, 6:1–3. There is no express teaching that RAS control line 26 and WE control line 28 communicate with memory device 5. As such, there is no teaching in the ’315 patent that memory devices 5 would need to be electrically

isolated from RAS and WE control lines 26, 28 to prevent errant signals on these control lines from reaching the memory devices.

Similarly, the '315 patent states that RAS and WE control lines 126 and 128 of Figure 4 are “connected to the control device” but does not state that the RAS and WE control lines communicate with memory devices. Ex. 1001, 9:24–26. Rather, the '315 patent states that the outputs from the control device are address lines 120 and control lines 124 and that these outputs are inputs to the memory devices. *Id.* at 9:33–36. There is no disclosure in the '315 patent that the RAS and WE control lines are inputs to the memory devices. As such, there is no teaching in the '315 patent that memory devices 5 would need to be electrically isolated from RAS and WE control lines 126, 128 to prevent errant signals on these control lines from reaching the memory devices.

Therefore, for the foregoing reasons, we determine the broadest reasonable construction consistent with the Specification of a control device “for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices” as recited in independent claims 1 and 10 requires that the control device electrically isolate the memory devices from all address and control lines that communicate with the memory devices. This construction is the same as our construction in Case IPR2017-01994. *See* IPR2017-01994, Paper 16, 14. We determine that no further claim construction is required to resolve the issues in dispute. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating that only claim terms in

controversy need to be construed and only to the extent necessary to resolve the controversy).

C. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Each element of the challenged claim must be found, either expressly or inherently, in the single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). While the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). Thus, the dispositive question is whether one skilled in the art would have reasonably understood or inferred from a prior art reference that every claim element is disclosed in that reference. *Eli Lilly v. Los Angeles Biomedical Research Inst. at Harbor–UCLA Med. Ctr.*, 849 F.3d 1073, 1074–75 (Fed. Cir. 2017). Still further, “it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains.” The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations¹¹. See *Graham*, 383 U.S. at 17–18. Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)).

To prevail on its challenges, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden never shifts to Patent Owner. See *Dynamic Drinkware, LLC. v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner does not satisfy its burden of proving obviousness by employing “mere conclusory

¹¹ The parties have not provided any evidence or argument directed to secondary considerations, and therefore, secondary considerations do not constitute part of our analysis.

statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

D. Overview of the Asserted Art

1. Dell (Ex. 1004)

Dell, titled “Power Management on a Memory Card Having a Signal Processing Element,” describes a memory module having individually addressable banks of memory chips that can be placed into a higher or lower power state by a system memory controller or digital signal processor (“DSP”). Ex. 1004, at [54], 1:48–63. The memory module of Dell is able to selectively and expeditiously reduce power to individual banks of memory (or portions thereof) when they are not being accessed. *Id.* at 1:40–45.

2. Abe (Ex. 1005)

Abe is directed to a memory control circuit for initiating a self-refresh mode for a dynamic random access memory (“DRAM”) when the power supply voltage is lowered and for the self-refresh mode to consume less power. Ex. 1005, 1:5–10, 1:48–56. Abe discloses a main power supply and an auxiliary power supply, wherein the auxiliary supply is used for self refresh functions when the main power supply is cut off. *Id.* at 3:5–8.

3. JESD21-C: Configurations for Solid State Memories (Ex. 1006)

Petitioner asserts JESD21-C is a January 1997 publication of a JEDEC industry standard for memory devices. *See* Pet. 37. As an initial matter, we must determine whether Petitioner has made a threshold showing that JESD21-C is a prior art printed publication under 35 U.S.C. § 102(b). To qualify as a printed publication, a document must have been sufficiently

accessible to the public interested in the art before the critical date. *In re Cronyn*, 890 F.2d 1158, 1160 (Fed. Cir. 1989). A reference is deemed publically accessible upon a satisfactory showing that such document has been disseminated or otherwise made available to the extent persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence can locate it. *Kyocera Wireless Corp. v. ITC*, 545 F.3d 1340, 1350–51 (Fed. Cir. 2008). Petitioner asserts JESD21-C was published January 1997 and is prior art under pre-AIA 35 U.S.C. § 102(b). Pet. 37–38. As support, Petitioner relies upon the Declaration of John J. Kelley (“the Kelley Declaration”), the current President of the Solid State Technology Association of the Joint Electron Device Engineering Council (“JEDEC”). See Ex. 1007 ¶ 2. Mr. Kelly states that JEDEC specification JESD21-C, Configurations for Solid State Memories, Release 7 (January 1997), a copy of which is attached to his declaration as Exhibit 17, “was made publicly available in January 1997.” *Id.* ¶¶ 4, 7. Mr. Kelley testifies that in January 1997 copies of the entire JESD21-C volume “would . . . have been available for purchase by anyone in the public” and that “pages comprising the specifically updated modules would have been sent to those who subscribed to the annual updating service for JESD21-C.” *Id.* ¶ 6.

Patent Owner does not dispute that JESD21-C qualifies as prior art under 35 U.S.C. § 102(b). See PO Resp. 7. Based on the current record, we determine JESD21-C qualifies as a prior art printed publication under § 102(b).

4. *Ooishi* (Ex. 1008)

Ooishi is directed to a semiconductor memory device that reduces power consumption during a self-refresh operation. Ex. 1008, 1:41–43. The memory device of Ooishi has both a normal mode and a power down mode,

and further includes a self-refresh circuit that generates a refresh address signal when in power down mode. *Id.* at 1:44–50; 1:56–58. Ooishi also discloses a first power supply that is used when the device is in normal mode and a second power supply that is used when the device is in a power down mode. *Id.* at 1:64–2:11.

5. *Palaniswami (Ex. 1009)*

Palaniswami is directed to an isolation mechanism located between a DSP and a DRAM controller that isolates DSP outputs from a DRAM controller upon occurrence of a low power condition. Ex. 1009, at [57], 2:65–3:15, Fig. 2. The stated goal of Palaniswami’s isolation mechanism is to prevent corruption of DRAM due to faulty DSP signals and attributable to lost or depleted battery supply. *Id.* at 2:1–5.

E. Asserted Unpatentability of Independent Claim 1 over Dell and Claim 10 over Dell and Abe

Petitioner contends that claim 1 is unpatentable as anticipated by Dell and that claim 10 is unpatentable as obvious over Dell and Abe. *See* Pet. 12–22, 26–37. Patent Owner opposes. *See generally* PO Resp. 10–19. Having considered the parties’ contentions and supporting evidence, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claim 1 is anticipated by Dell or that claim 10 would have been obvious over the combined teachings of Dell and Abe.

Our analysis focuses on the claim language found in claim element 1[b] and claim element 10[c], which require a “control device” “for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices.” As noted

above in Section II.B, we construe claim element 1[b] and 10[c] as requiring that the control device electrically isolate the memory device from *all* address and control lines that communicate with the memory device.

Patent Owner contends that Dell does not disclose all of the limitations of claim element 1[b] or 10[c] because Dell's CKE (clock enable) line is a "control line" that can remain connected to a memory bank even when the memory bank is in a power down state. *See* PO Resp. 14–15; *see also id.* at 15 (stating, *inter alia*, Dell's clock enable line 24 has four branches 54a–54d connected to the banks of memory chips 12a–12h and 13a–13h through FET switches 56a–56d to provide individual clock enable signals directly to the chips 12a–12h and 13a–13h without going through the bus controller 34 so that the chips can be addressed when they are in the lowest power state).

Petitioner acknowledges that the memory banks can be reached through a CKE signal even when the device is in a low-power and/or self-refresh mode. *See* Reply 5–6 (citing Pet. 2; Ex. 1004, 4:11–22) (stating that in the self refresh mode, only the clock enable signal is active, with all other receivers being turned off). Petitioner, however, argues that neither claim 1 nor claim 10 requires electric isolation of the memory from *all* address lines and *all* control lines. *See* Reply 4–5; *see also id.* at 9–10 (acknowledging the "CKE line in Dell can access the memory devices during low power/self-refresh mode, but this is irrelevant to the claim, which only requires isolation from 'respective address lines and control lines'—not *all* address lines and *all* control lines").

We agree with Patent Owner that Petitioner has not persuasively shown that Dell discloses a control device that electrically isolates the memory devices as required under the claim construction set forth above in

Section II.B. Specifically, because Dell’s CKE line can access the memory devices even when the devices are in a low-power or self-refresh mode, Petitioner has not shown that Dell’s memory devices are electrically isolated from “respective control lines” such that “any signals received on said . . . respective control lines do not reach said memory devices” as required by claims 1 and 10. Accordingly, we determine Petitioner has not shown by a preponderance of the evidence that claim 1 of the ’315 patent is unpatentable over Dell or that claim 10 is unpatentable over the combined teachings of Dell and Abe.

F. Asserted Unpatentability of Dependent Claims 2–9 and 11–20

Petitioner contends (1) dependent claim 5 is unpatentable under § 102 over Dell, (2) claim dependent 16 is unpatentable under § 103 over Dell and Abe, (3) dependent claims 2–4 and 6–9 are unpatentable under § 103 over Dell and JESD21-C, and (4) dependent claims 11–15 and 17–20 are unpatentable under § 103 over Dell, Abe, and JESD21-C. *See* Pet. 22–23, 37–49. Each of claims 2–9 depends directly or indirectly from claim 1 and each of claims 11–20 depends directly or indirectly from claim 10.

Petitioner’s arguments regarding the unpatentability of the dependent claims 2–9 and 11–20 do not remedy the deficiency with regard to the independent claims from which they depend. *See id.* As such, we also determine that Petitioner has not shown by a preponderance of the evidence that claims 2–9 and 11–20 of the ’315 patent are unpatentable.

G. Asserted Obviousness of Claims 1 and 5 over Ooishi and Palaniswami (Ground 5)

Petitioner contends that claims 1 and 5 are unpatentable under § 103 over the combined teachings of Ooishi and Palaniswami. Pet. 49–66. Patent Owner opposes. PO Resp. 19–23. Having considered the parties’

contentions and supporting evidence, we disagree with Patent Owner's arguments and determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 5 are unpatentable under § 103 over Ooishi and Palaniswami.

1. Claim 1

a. Preamble and Claim Element 1[a]

The preamble and claim element 1[a] recite a

memory system for use in a computer system, said memory system comprising [] a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh mode; said memory devices having address lines and control lines.

We agree with Petitioner's undisputed contention that both Ooishi and Palaniswami disclose memory systems for use in a computer system as recited in the preamble. *See* Pet. 52. Regarding claim element 1[a], Petitioner asserts Ooishi's DRAM memory cell arrays constitute a plurality of volatile solid state memory devices that are capable of being placed in a self-refresh mode. *See* Pet. 53–55 (citing, *inter alia*, Ex. 1008, 1:44–50, 1:56–58, 3:18–26, 5:3–15, 5:38–41). Petitioner further asserts the memory devices have address and control lines because Ooishi's memory bank arrays receive control signals (e.g., CLK, CKE, CS, RAS, CAS, WE) and address signals, as well as address and control lines. *See* Pet. 55–56 (citing Ex. 1008 5:3–15, Fig. 1; Ex. 1002 ¶ 99).

Patent Owner argues Ooishi does not teach the limitations of claim element 1[a] because “the word ‘volatile’, ‘address lines’, and ‘control lines’ do not appear in Ooishi.” PO Resp. 20.

We disagree with Patent Owner’s argument. The asserted art need not recite the exact language of the claims because an obviousness analysis is not an *ipsissimis verbis* test. *Gleave*, 560 F.3d at 1334. Rather, what a prior art reference discloses or teaches is determined from the perspective of one of ordinary skill in the art. *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1361 n.3 (Fed. Cir. 2008).

We are persuaded by Petitioner’s arguments, supported by the declaration testimony of Dr. Wolfe, that a person skilled in the art would have understood that Ooishi’s description of a DRAM unit with a plurality of memory cell arrays (Ex. 1008, 3:18–26), a self-refresh control circuit that generates refresh signals in a power down mode (*id.* at 1:44–50, 1:56–58, 5:38–41), and specifically identified control signals and address signals (*id.* at 5:3–15, Fig. 1), teaches the limitations of claim element 1[a]. See Pet 53–56; Reply 13; Ex. 1002 ¶¶ 95–99.

b. Claim Element 1[b]

Claim element 1[b] requires the memory system comprise “a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices.” Petitioner contends both Ooishi and Palaniswami teach or suggest this claim element. Pet. 56–63.

Petitioner contends Ooishi’s teaching that, during the power down mode, power is not supplied to circuitry that is not required for a self-refresh operation, renders obvious the “control device” limitation of claim element 1[b]. *Id.* at 56; see also *id.* at 57 (annotating the various components in Figure 1 of Ooishi that are “not required for a self refresh operation”).

Petitioner states that a POSITA would understand that because the components that connect to the address and control signals to the DRAM are not supplied with power, the address and control signals are electrically isolated from the DRAM during the self-refresh mode. *Id.* (citing Ex. 1002 ¶¶ 101–102).

To the extent Ooishi does not expressly disclose the control device of claim element 1[b], Petitioner argues such a control device is expressly disclosed in Palaniswami. *See* Pet. 57–63. Petitioner contends Palaniswami’s isolation mechanism 20 is a “control device” that selectively isolates DRAM 6 from output signals from DSP 4 to prevent memory corruption due to low power. *Id.* at 57–59 (citing Ex. 1009, 2:65–3:5, 3:8–14; Ex. 1002 ¶¶ 103–105). Petitioner asserts a POSITA would have been motivated to combine Palaniswami’s separate isolation mechanism 20 with the DRAM and address/control signals of Ooishi because of Ooishi’s explicit teaching to isolate DRAM from control and address signals in low-power situations. *See* Pet. 59 (citing Ex. 1002 ¶ 107; Ex. 1008, 6:23–28, 6:38–42); *see also id.* at 59–63. Petitioner explains that, to the extent Ooishi’s control and address signals are not already inhibited by virtue of those components being disconnected from power, a POSITA would have been motivated to use Palaniswami’s isolation mechanism to selectively inhibit the control and address signals from arriving at the memory banks in order to ensure that those signals did not corrupt the stored data. Ex. 1002 ¶ 108; *see also id.* ¶ 109 (stating a POSITA would have combined Ooishi and Palaniswami to provide selective control, such as allowing control signals to arrive at components that determine self refresh operation, such as the self-refresh control circuit (SRC) in Ooishi, but still be inhibited from arriving at the DRAM memory cells). Petitioner also relies on testimony

that electrically isolating DRAM was a well-known technique and that applying this technique to well-known DRAM systems would have yielded the predictable result of preventing errant signals from corrupting DRAM. Pet. 50–51; Ex. 1002 ¶ 55 (citing Ex. 1010, 1:50–65, [57]); Ex. 1009, at [57], 1:64–2:7.

Patent Owner makes a number of arguments in response. First, Patent Owner asserts the control device of claim element 1[b] would not have been obvious over the teachings of Ooishi because Petitioner errs in assuming that Ooishi’s address and control lines supply electrical power to its memory devices. See PO Resp. 20. We are not persuaded by this argument because Petitioner does not assert that the address and control lines supply power to the Ooishi’s memory devices. Rather, Petitioner asserts Ooishi’s address and control signals are electrically isolated from the DRAM when they are not supplied with power. Pet. 57. We are persuaded by Petitioner’s argument, supported by Dr. Wolfe’s unrebutted testimony, that a POSITA would understand that when components that connect the address and control signals of the DRAM are not supplied with power, they are electrically isolated from the DRAM during self-refresh mode. Pet. 56–57 (citing Ex. 1002 ¶¶ 101–102; Ex. 1008, 6:38–42).

Patent Owner also states that even if a line for electrical power were not supplied with power, the line would remain connected and “the line would be ‘floating’ thereby creating a path for erratic signals.” PO Resp. 21. Patent Owner, however, does not provide sufficient evidence to support this argument. Attorney arguments and conclusory statements that are unsupported by factual evidence are entitled to little probative value. *In re Geisler*, 116 F.3d 1465, 1470 (Fed. Cir. 1997). Rather, we are persuaded by Petitioner’s argument, supported by unrebutted expert testimony, that a

POSITA would understand that when power is not supplied to the address and control lines, the lines are electrically isolated from the memory, as claimed. Pet. 56–57 (citing Ex. 1002 ¶¶ 101–102).

Patent Owner does not dispute that Palaniswami teaches a control device that isolates DRAM memory devices from output signals to prevent corruption during low power. *See generally* PO Resp. Patent Owner does however argue “the reasoning for combining Ooishi and Palaniswami is illogical, and irrelevant.” *Id.* at 21. Patent Owner contends that because Petitioner alleges Ooishi already has a control device, there is no motivation to modify Ooishi to add the control device of Palaniswami. PO Resp. 21–22.

We are not persuaded by this argument. We agree with Petitioner’s argument that a POSITA would understand that Ooishi’s address and control signals are electrically isolated from the DRAM during self-refresh mode. *See* Pet. 56–57. We also agree with Petitioner that Palaniswami’s isolation mechanism 20 is a control device that selectively isolates DRAM from output signals to prevent corruption of DRAM due to low power. *See id.* at 57–59 (citing Ex. 1009, 2:65–3:5, 3:8–14; Ex. 1002 ¶¶ 103–105); *see also* Ex. 1002 ¶ 54 (stating the isolation by Palaniswami’s isolation mechanism “prevents corruption of dynamic random access memory due to low power”); Ex. 1009, at [57] (stating an “isolation mechanism serves to isolate digital signal processor outputs from a dynamic random access memory controller upon the occurrence of a low power condition” to prevent “corruption of dynamic random access memory due to low power”). We are also persuaded by Petitioner’s argument, supported by unrebutted expert testimony, (1) that one skilled in the art would have been motivated to interpose Palaniswami’s “isolation mechanism” between the logic unit 100

and DRAM 200 of Ooishi to yield the predictable result of preventing errant signals from corrupting DRAM, (2) that doing so would also allow for selective isolation of signals, (3) that electrically isolating DRAM was a well-known technique at the time of the invention, (4) that applying this technique to well-known DRAM systems would have yielded the predictable result of preventing errant signals from corrupting DRAM, and (5) that the isolation mechanism of Palaniswami could be interposed in Ooishi's system without otherwise disturbing the functionality of Palaniswami's embodiment. Ex. 1002 ¶¶ 51–59, 101–111. Therefore, based on our review the parties arguments and evidence, we determine the combined teachings of Ooishi and Palaniswami teach the limitations of claim element 1[b] and Petitioner has sufficiently shown that a POSITA would have reason to combine the teachings of the asserted art to arrive at the limitations of claim element 1[b].

c. Claim Element 1[c]

Claim element 1[c] recites

a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical powers supply for said computer system.

Petitioner contends that claim element 1[c] is taught by the combined teachings of Ooishi and Palaniswami. Petitioner contends Ooishi's "mode decoder," which acts as the "memory access enable control device," is coupled to both the control lines and the self-refresh control circuit that determines when the memory system is not being accessed, through a clock

enable signal CKE, and which then outputs a self-refresh set signal to initiate a self-refresh (i.e., low power) mode. Pet. 63–64 (citing Ex. 1008, 5:16–19, 6:38–44, 6:51–55, 7:34–45, Fig. 1; Ex. 1002 ¶¶ 114–116). Petitioner further asserts that isolation mechanism 20 of Palaniswami discloses the element “wherein said control device electrically isolates said memory devices and places said memory device in said self refresh mode.” *Id.* at 64. Relying on the declaration testimony of Dr. Wolfe, Petitioner contends a POSITA would have been motivated to interpose the “isolation mechanism” of Palaniswami between the logic unit 100 and DRAM 200 of Ooishi to obtain the predictable result of preventing errant signals from corrupting data stored in the DRAM when Ooishi’s mode decoder initiates a low power mode. *See id.* at 50–52 (citing Ex. 1002 ¶¶ 51–59). Petitioner explains that the combination applies a known technique (electrically isolating DRAM upon the occurrence of a low power condition) to a known device (computer system with DRAM) to yield predictable results (preventing errant signals from causing unintended results during a low power condition). *Id.* at 50–51 (citing Ex. 1002 ¶ 55; Ex. 1009, at [57], 1:8–10, 1:64–2:7, 2:65–66, 4:37–39); *see also id.* at 51 (stating Palaniswami teaches its isolation mechanism prevents faulty DSP output signals from reaching the DRAM to prevent corruption of the memory due to low power); *see also id.* at 65 (stating Ooishi discloses the amount of electrical energy being drawn from an electrical power supply for said computer system is reduced in a self-refresh mode) (citing Ex. 1008, at [57], 1:40–43; Ex. 1002 ¶ 118).

Patent Owner argues that Petitioner has not addressed the limitation requiring “the ‘control device’ to respond to the ‘memory access control [device].’” PO Resp. 20–21; *see also id.* at 21–22 (stating the Petition does not identify a “memory access enable control device” that communicates

with a “control device”). We disagree with this argument because Patent Owner is arguing language not found in the challenged claim. Claim element 1[c] recites, *inter alia*, the “memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode.” Petitioner explains how these limitations of claim element 1[c] are taught by the *combined* teachings of Ooishi and Palaniswami. See Pet. 63–65. For example, we are persuaded by Petitioner’s argument that the combination of Ooishi and Palaniswami teaches a “memory access enable control device” (i.e., Ooishi’s mode decoder) that is coupled to a control device (i.e., Palaniswami’s isolation mechanism 20). Petitioner explains that Ooishi’s mode decoder “determines when the memory system is not being accessed, through a clock enable signal CKE, . . . which then outputs a self-refresh set signal to initiate self-refresh (i.e., low power) mode.” Pet. 63–64 (citing Ex. 1008, Fig. 1, 5:16–19, 6:38–44, 6:51–55, 7:34–45; Ex. 1002 ¶¶ 114–116). We are persuaded by Petitioner’s argument, supported by the declaration testimony of Dr. Wolfe, that Ooishi’s mode decoder determines when the memory system is not being accessed and then outputs a self-refresh set signal to initiate self-refresh (i.e., low power) mode. See Pet. 63 (citing Ex. 1008, 5:16–19, 6:38–44; 6:51–55, 7:34–45, Fig. 1; Ex. 1002 ¶¶ 113–116). We also agree with Petitioner that Palaniswami’s isolation mechanism acts as the “control device.” We are persuaded by Petitioner’s argument that Palaniswami’s “isolation mechanism isolates digital signal processor outputs from a dynamic random access memory controller upon

the occurrence of a low power condition.” Pet. 51 (quoting Ex. 1009, at [57]).

We also agree with Petitioner that a person skilled in the art would have been motivated to combine Palaniswami’s isolation mechanism and Ooishi’s mode decoder within the DRAM to determine when memory is not being accessed and to selectively electrically isolate the memory from the respective address and control lines. *See* Pet. 63–65; Ex. 1002 ¶¶ 113–118. Accordingly, we determine the combined teachings of Ooishi and Palaniswami teach the limitations of claim element 1[c] and Petitioner has sufficiently shown that a POSITA would have reason to combine the teachings of the asserted art to arrive at the limitations of claim element 1[c].

e. Conclusion

After considering Petitioner’s and Patent Owner’ arguments and supporting evidence, we determine that Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over the combined teachings of Ooishi and Palaniswami.

2. Claim 5

Petitioner asserts the combination of Ooishi and Palaniswami teaches the limitations of claim 5, which recites “[t]he memory system as claimed in claim 1, wherein the memory devices are DRAM semiconductor microchips.” Pet. 65. We agree with Petitioner’s assertion that Ooishi teaches DRAM semiconductor microchips and that one skilled in the art would have been motivated to combine the DRAM of Ooishi and the isolation mechanism of Palaniswami to achieve electrical isolation of memory devices, wherein those memory devices are either (1) memory cell arrays within the DRAM, or (2) DRAM semiconductor memory chips. Pet. 65–66 (citing Ex. 1009, 2:65–66, Fig. 2; Ex. 1002 ¶ 121). Accordingly, we

find Petitioner has shown by a preponderance of the evidence that claim 5 is unpatentable over Ooishi and Palaniswami.

H. Asserted Obviousness of Claims 10 and 16 over Ooishi, Palaniswami, and Abe (Ground 6)

Petitioner contends that claims 10 and 16 are unpatentable under § 103 over the combined teachings of Ooishi, Palaniswami, and Abe. Pet. 66–72. Patent Owner opposes. PO Resp. 23–24. Specifically, Patent Owner states its arguments regarding claims 1 and 5 against combining Ooishi and Palaniswami also apply to claims 10 and 16 and further states Petitioner has not provided “technical information” as to “how Abe would be incorporated into the combination of Ooishi and Palaniswami.” PO Resp. 24. Having considered the parties’ contentions and supporting evidence, we disagree with Patent Owner’s arguments and determine that Petitioner has demonstrated by a preponderance of the evidence that claims 10 and 16 are unpatentable under § 103 over Ooishi, Palaniswami, and Abe.

1. Claim 10

a. Preamble and Claim Element 10[a]

The preamble and claim element 10[a] recite a “memory system for use in a computer system, said memory system comprising: a plurality of volatile solid state memory devices that retain information when an electrical power source having a voltage greater than a predetermined voltage is applied to said devices; said memory devices having address lines and control lines.” We are persuaded by Petitioner’s unrebutted argument that Ooishi as well as Ooishi and Palaniswami teach these limitations for the same reasons the cited art teaches the similar limitations recited in the preamble and element [a] of claim 1. See Pet. 67–68.

b. Claim Element 10[b]

Claim element 10[b] recites “said computer system including a first electrical power source for operating said computer and being capable of producing a first voltage applied to said memory devices.” We are persuaded by Petitioner’s un rebutted argument that Abe’s disclosure of a main power supply producing a first voltage to a main DRAM control circuit coupled to a DRAM teaches the limitations of claim element 10[b]. See Pet. 27–28, 67–68; Ex. 1005, 1:6–10, 2:55–62, 3:5–14, Fig. 1; Ex. 1002 ¶¶ 129–130.

c. Claim Element 10[c]

Claim element 10[c] recites:

a control device for monitoring said first voltage to determine when said first voltage is less than said predetermined voltage and for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices.

Petitioner asserts the power supply monitors of Abe combined with the isolation mechanism of Palaniswami teaches these limitations. Pet. 69–70. Petitioner explains Abe discloses two power supply monitors with predetermined detection voltages that can be set slightly higher than the minimum voltage at which the main circuit can operate normally. See Pet. 29–30 (citing Ex. 1005, 3:20–26, 3:40–60, Fig. 1; Ex. 1002 ¶ 134), 69. Petitioner contends that Palaniswami teaches the “selectively electrically isolating” limitations of claim element 10[b] for the same reasons as set forth with respect to claim element 1[b] and that a POSITA would have been motivated to substitute the isolation mechanism of Palaniswami into the

DRAM of Abe in order to inhibit address and control signals from reaching the memory devices. Pet. 70 (citing Ex. 1002 ¶ 156); *see also id.* at 66–67.

Patent Owner argues claims 10 and 16 are patentable for the same reasons argued “in connection with claims 1 and 6 [sic: claims 1 and 5]”. *See* PO Resp. 24. We are not persuaded by Patent Owner’s arguments for the same reasons set forth above in Section II.G.

d. Claim Element 10[d]

Claim element 10[d] recites “a second electrical power source operable for supplying a second voltage to said memory devices greater than said predetermined voltage.” Petitioner asserts Abe’s disclosure of an auxiliary power supply that supplies power for retaining the contents of DRAM when the main power supply is cut off, teaches the limitations of claim element 10[d]. Pet. 32–33, 70 (citing Ex. 1005, 2:55–62, 3:5–17; Ex. 1002 ¶ 139). We have reviewed and agree with Petitioner’s undisputed assertions that Abe teaches the limitations of claim element 10[d].

e. Claim Element 10[e]

Claim element 10[e] recites “said control device being operable for disconnecting said first electrical power source from said memory devices and connecting said second electrical power source to said memory devices when said first voltage is less than said predetermined voltage.” Petitioner asserts Abe’s disclosure of using diodes to switch between the main and auxiliary power supply when the first voltage falls below a predetermined voltage teaches this claim element. *See* Pet. 34–35, 70 (citing Ex. 1005, 3:5–19, Fig. 1; Ex. 1002 ¶ 142). We have reviewed and agree with Petitioner’s undisputed assertions that Abe teaches the limitations of claim element 10[e].

f. Claim Element 10[f]

Claim element 10[f] recites “whereby, data in said memory devices is preserved by said second electrical power source when said first electrical power source fails to maintain at least said predetermined voltage on said memory devices, and said memory devices are isolated from errant signals.”

Petitioner contends that the combined teachings of Abe and Palaniswami render the limitations of claim element 10[f] obvious. *See* Pet. 71. Specifically, Petitioner asserts Abe teaches an auxiliary power supply (second electrical power source) that powers the self-refresh mode when the main power supply is shut off meets the limitation of claim element 10[f]. *See* Pet. 36–37 (citing Ex. 1005, 1:48–56, 2:9–28), 71. Petitioner further asserts that Palaniswami discloses an isolation mechanism that selectively electrically isolates memory devices from errant signals for the same reasons set forth with respect to claim 1[b]. *See* Pet. 57–63, 71 (citing Ex. 1002 ¶ 163). We have reviewed, and agree with Petitioner’s undisputed assertions that Abe teaches the limitations of claim element 10[f].

g. Reasons to Combine

Petitioner asserts a POSITA would have been motivated to combine the memory system of Ooishi and Palaniswami with the auxiliary power supply control circuitry of Abe in order to prevent data loss when the battery’s charge is critically low. Pet. 66–67 (citing Ex. 1006 ¶¶ 66–68). Petitioner asserts that all three references are directed to DRAM systems that utilize a self refresh mode. *Id.* at 66. Petitioner contends that Ooishi’s teaching of first and second power supplies provide the same functionality as Abe’s two power supply control circuitry and a person skilled in the art would have been motivated to include Abe’s more explicit teaching of

threshold detection voltages to provide further detail on when the second power supply would be used. Pet. 66–67 (citing Ex. 1005, 3:21–31; Ex. 1002 ¶ 67). Citing Palaniswami’s teaching that battery power supply depletes over time, Petitioner also contends a POSITA would recognize that using Abe’s power control circuitry to switch the DRAM to an auxiliary power supply when battery charge is low would solve the known problem of unexpected power outage. *Id.* at 67 (citing Ex. 1002 ¶ 168; Ex. 1009, 1:15–16).

Patent Owner responds that Petitioner has not provided “technical information” to suggest how Abe would be incorporated into the combination of Ooishi and Palaniswami. PO Resp. 24. This argument is not persuasive. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). As the Supreme Court has explained, “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *KSR*, 550 U.S. at 417. Based on the current record, for the reasons stated in the Petition, we find Petitioner has established that a POSITA would have had reason to combine the teachings of Ooishi, Palaniswami, and Abe to achieve the claimed subject matter.

h. Conclusion

After considering Petitioner’s and Patent Owner’ arguments and supporting evidence, we determine that Petitioner has shown by a

preponderance of the evidence that claim 10 would have been obvious over the combined teachings of Ooishi, Palaniswami, and Abe.

2. Claim 16

Claim 16 depends from claim 10 and further requires that the memory devices are DRAM semiconductor chips. We agree with Petitioner's undisputed argument and evidence that Abe's memory system comprises DRAM semiconductor memory chips. Pet. 72 (citing Ex. 1005, Fig. 1; Ex. 1002 ¶165). For the reasons stated above, we also find Petitioner has established that a POSITA would have had reason to combine the teachings of Ooishi, Palaniswami, and Abe. Accordingly, we find Petitioner has shown by a preponderance of the evidence that claim 16 is unpatentable over Ooishi, Palaniswami, and Abe.

III. CONCLUSION¹²

In summary:

Claims	35 U.S.C. §	Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 5	§ 102	Dell		1, 5
10, 16	§ 103	Dell and Abe		10, 16
2–4, 6–9	§ 103	Dell and JESD21-C		2–4, 6–9

¹² Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

11–15, 17–20	§ 103	Dell, Abe, and JESD21-C		11–15, 17–20
1, 5	§ 103	Ooishi and Palaniswami	1, 5	
10, 16	§ 103	Ooishi, Palaniswami, and Abe	10, 16	
Overall Outcome			1, 5, 10, 16	2–4, 6–9, 11– 15, 17–20

IV. ORDER

Accordingly, it is

ORDERED that claims 1, 5, 10, and 16 of the '315 patent are determined to be *unpatentable*;

FURTHER ORDERED that claims 2–4, 6–9, 11–15, and 17–20 of the '315 patent have not been shown to be unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-02021
Patent 6,243,315 B1

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