

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION and
RENESAS ELECTRONICS AMERICA INC.,
Petitioners,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

IPR2017-02123
Patent 6,153,933

Before GRACE KARAFFA OBERMANN, KEVIN C. TROCK, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 5–12 (“the challenged claims”) of U.S. Patent No. 6,153,933 (Ex. 1101, “the ’933 patent”) are unpatentable.

A. Background

Renesas Electronics Corporation and Renesas Electronics America Inc. (collectively, “Petitioner”) filed a Petition requesting *inter partes* review of claims 5–12 of the ’933 patent pursuant to 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Petitioner also filed the supporting Declaration of Dean Neikirk, Ph.D. (Ex. 1105) (“Neikirk Declaration”). Lone Star Silicon Innovations LLC (“Patent Owner”) filed a Preliminary Response. Paper 5. Patent Owner also filed the supporting Declaration of W.R. Bottoms, Ph.D. (“Bottoms Declaration”). Ex. 2001. Pursuant to 35 U.S.C. § 314(a), on April 6, 2018, we instituted *inter partes* review on the following grounds:

whether claims 5–8, 10, and 11 would have been anticipated under § 102(b) by Kubo¹;

whether claim 9 would have been rendered obvious under § 103(a) over the combined teachings of Kubo and Jang²;

¹ Japanese Unexamined Patent Application Publication No. JPH08-153784, published June 11, 1996 (Ex. 1111). We refer to the English translation (Ex. 1112) of the original reference herein.

² U.S. Patent No. 5,674,783, issued October 7, 1997 (Ex. 1108).

whether claim 12 would have been rendered obvious under § 103(a) over the combined teachings of Kubo and Ito³;
whether claims 5–8, 10, and 11 would have been anticipated under § 102(e) by Kimura⁴;
whether claim 9 would have been rendered obvious under § 103(a) over the combined teachings of Kimura and Jang;
whether claim 12 would have been rendered obvious under § 103(a) over the combined teachings of Kimura and Ito;
whether claims 5, 7, and 9–11 would have been anticipated under § 102(a) by Yoshihara⁵; and
whether claims 6 and 12 would have been rendered obvious under § 103(a) over the combined teachings of Yoshihara and Admitted Prior Art.

See Paper 7 (“Inst. Dec.” or “Dec.”).

In the Institution Decision, we declined to institute the ground for claims 5–12 under 35 U.S.C. § 103(a) in view of Admitted Prior Art and “CMP References⁶” because we found that the Petition was deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a). Dec. 14–16.

³ Japanese Unexamined Patent Application Publication No. H08-306785, published November 22, 1996 (Ex. 1115). We refer to the English translation (Ex. 1116) of the original reference herein.

⁴ U.S. Patent No. 5,869,392, issued February 9, 1999 (Ex. 1110).

⁵ Japanese Unexamined Patent Application Publication No. H08-293561, published November 5, 1996 (Ex. 1113). We refer to the English translation (Ex. 1114) of the original reference herein.

⁶ The Petition refers to the “CMP References” as “Jang, Kimura, and Ito.” Pet. 33.

On April 24, 2018, the Supreme Court held that a final written decision in an *inter partes* review must decide the patentability of all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (“SAS”). Pursuant to SAS, on May 3, 2018, we instituted *inter partes* review on all claims and all grounds. Paper 9.

Patent Owner filed a Patent Owner Response (Paper 21, “PO Resp.”). Patent Owner also filed the supporting Declaration of W.R. Bottoms, Ph.D. (“Response Bottoms Declaration”). Ex. 2013. Petitioner filed a Reply (Paper 23, “Pet. Reply”) to the Patent Owner Response. Petitioner also filed the supporting Reply Declaration of Dean Neikirk, Ph.D. (“Reply Neikirk Declaration”). (Ex. 1121).

An oral hearing was held on December 17, 2018. A transcript of the hearing is included in the record. Paper 29 (“Tr.”).⁷

B. Related Proceedings

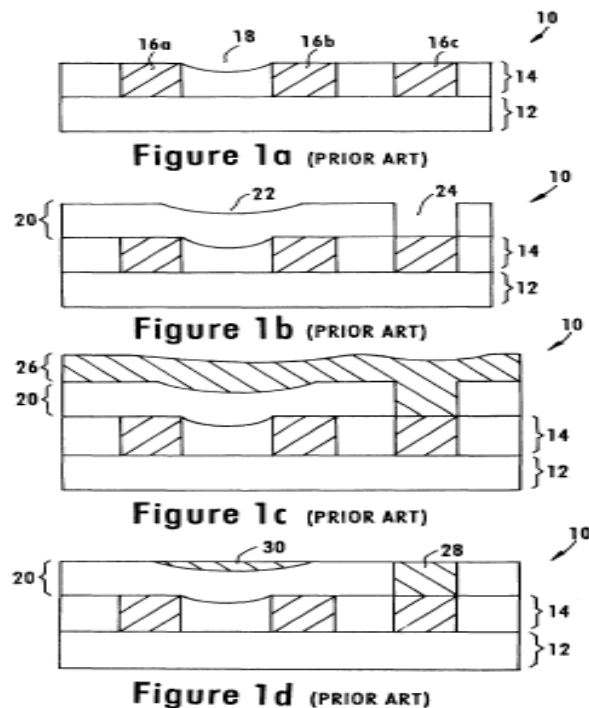
The parties indicate that the ’933 patent is asserted in *Lone Star Silicon Innovations, LLC v. Renesas Electronics Corp.*, C.A. No. 3:17-cv-0398 (N.D. Cal.). Pet. 2, Paper 4, 2. Petitioner indicates that a petition for *inter partes* review of claims 1–4 of the ’933 patent (Case IPR2017-01989), has been filed. Pet. 2. The Final Written Decision in IPR2017-01989 is being issued concurrently with this decision.

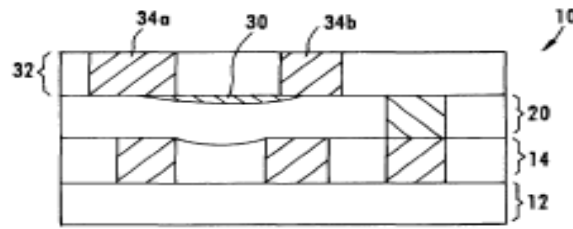
⁷ A consolidated hearing was conducted for this case and related Case IPR2017-01989, with a separate hearing for unrelated Case IPR2017-02124 conducted on the same day.

C. The '933 Patent

The '933 patent is titled “Elimination of Residual Materials in a Multiple-Layer Interconnect Structure” and issued on November 28, 2000 from an application filed on September 5, 1997. Ex. 1101, [22], [45], [54].

The '933 patent is directed generally to methods for forming multiple layer interconnect structures in an integrated circuit. Ex. 1101, Abstract. More specifically, the '933 patent is directed to improvements to methods for forming multiple layers to avoid potential failure mechanisms due to irregularities in a lower interconnect structure being carried over to a higher interconnect layer. *Id.* at 1:47–53. Figures 1a to 1e, reproduced below, depict conventionally-known steps in forming multiple layer interconnect structures.





As depicted in Figure 1a, cross-section of portion 10 of a semiconductor wafer is fabricated with wafer stack 12, first dielectric layer 14, and first conductor plugs 16a, 16b and 16c. Ex. 1101, 3:38–42. The surface of first dielectric layer 14 may have first layer depression 18. *Id.* at 4:8–12. Figure 1b depicts patterned second layer dielectric layer 20 formed on first dielectric layer 14, that shows second layer depression 22 as formed by the conformable deposition over first layer depression 18. *Id.* at 4:17–24. As shown in Figure 1c, second layer dielectric 20 is covered with second layer conductor 26 that fills etched opening 24. *Id.* at 4:26–30. As depicted in Figure 1d, second layer dielectric 20 is planarized, leaving second layer conductor plug 28 in etched opening 24, and second layer residual material 30 in second layer depression 22. *Id.* at 4:31–35. Second layer residual material 30, as shown in Figure 1e, can detrimentally affect the structure and resulting electrical properties of subsequently formed interconnect layers, such as a third layer interconnect that includes third layer dielectric 32, and can be a failure mechanism. *Id.* at 4:41–46, 4:52–55.

Figures 2a to 2e, reproduced below, depict fabrication steps for embodiments of the '933 patent.

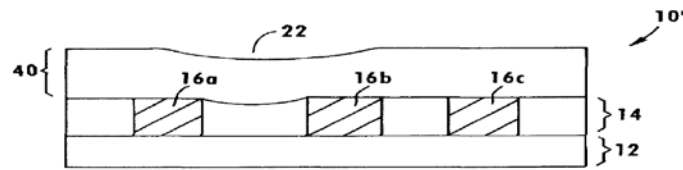


Figure 2a

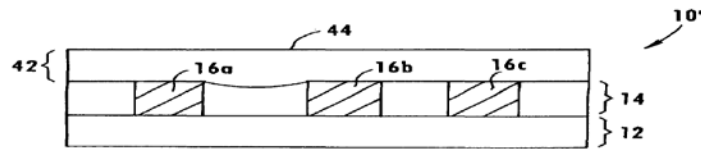


Figure 2b

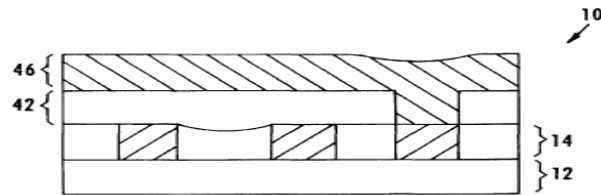


Figure 2c

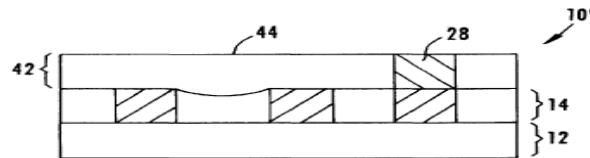


Figure 2d

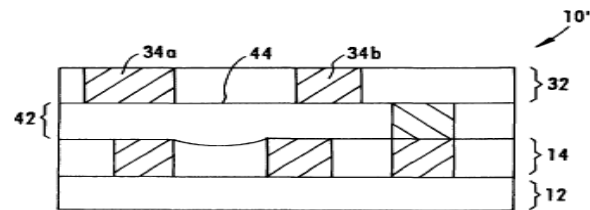


Figure 2e

Similarly to Figures 1a and 1b, Figure 2a depicts a cross-section of a portion 10' of a semiconductor wafer, fabricated with first interconnect layer 14, with first layer depression 18 between plugs 16a and 16b, and covered with second layer dielectric 40 that has second layer depression 22 caused by first layer depression 18. Ex. 1101, 4:56–65. As depicted in Figure 2b, second interconnect layer 40 is reduced in thickness, using planarization techniques,

to form planarized second layer dielectric 42 that has substantially planar top surface 44, wherein second layer depression 22 has been eliminated. *Id.* at 5:6–14. In Figure 2c, second layer conductor 46 is deposited on top of planarized second layer dielectric 42, which has been patterned to reveal an etched opening 24, as in Figure 1b. *Id.* at 5:14–16. In Figure 2d, second layer conductor 46 has been planarized down to the planarized second layer dielectric to form second layer conductive plug 28. *Id.* at 5:17–20. “Thus, unlike portion 10 in FIG. 1d, the substantially flat top surface 44 of planarized second layer dielectric 42 impedes the build-up or formation of any second layer residual materials.” *Id.* at 5:21–24.

Claim 5, the only independent claim of the '933 patent at issue in the Petition, and dependent claim 6 are reproduced below.

5. A method for forming a multiple-layer interconnect structure in an integrated circuit using damascene techniques, the method comprising:

forming a first layer interconnect having a first dielectric layer through which at least one first layer conductor extends;

forming a second layer interconnect on the first layer interconnect, the second layer interconnect having a second layer dielectric through which at least one second layer conductor extends, by forming the second layer dielectric to a first thickness and substantially planarizing the second layer dielectric to reduce the first thickness to a second thickness prior to patterning the second layer dielectric;

patterning the second layer dielectric to form an etched opening; and

filling the etched opening with a conductive material to form the second layer conductor.

6. The method as recited in claim 5⁸, wherein forming the second layer interconnect further includes planarizing the conductive material to be substantially level with the top surface of the second layer dielectric.

Ex. 1101, 6:19–42.

II. ANALYSIS

A. *The Parties’ Post-Institution Arguments*

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 5–12 of the ’933 patent would have been unpatentable under 35 U.S.C. § 102 and/or § 103 under asserted prior art. Dec. 7–36. We now determine whether Petitioner has established by a preponderance of the evidence that claims 5–12 are unpatentable. We previously instructed Patent Owner “that any arguments concerning patentability not raised in the response will be deemed waived.” Paper 8, 3; *see also* 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have before us arguments and evidence advanced by Petitioner to support its unpatentability

⁸ A Certificate of Correction issued on November 28, 2000, which corrected some claim numbering. *See* Ex. 1101, Certificate of Correction, 1.

contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record contains persuasive, un rebutted arguments and evidence presented by Petitioner regarding the manner in which some of the asserted prior art discloses corresponding limitations of claims 5–12. Based on the preponderance of the evidence before us, we conclude that some of the prior art identified by Petitioner discloses or teaches all of the limitations of the reviewed claims.

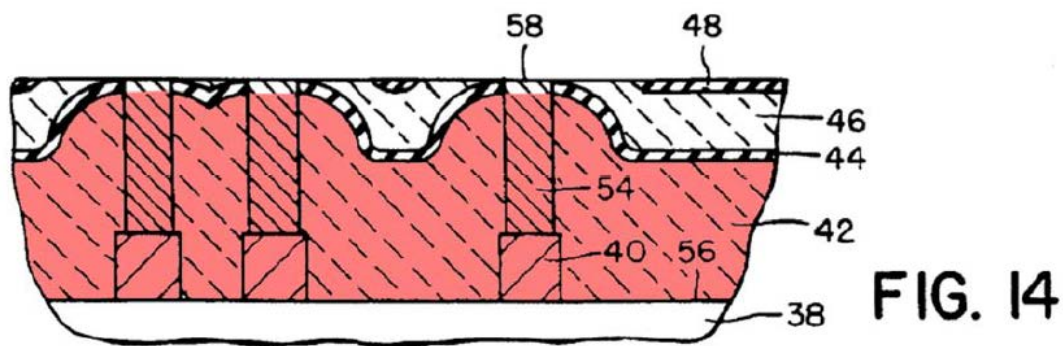
B. Claim Construction

Petitioner indicates that the '933 patent expired on September 5, 2017, and district court-type claim construction should be used. Pet. 11. Our review of the claims of an expired patent is similar to that of a district court's review. *Wasica Finance GmbH v. Continental Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017). Specifically, because the expired claims of a patent are not subject to amendment, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)), that "words of a claim 'are generally given their ordinary and customary meaning,'" as would be understood by a person of ordinary skill in the art in question at the time of the invention. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1015, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

“layer interconnect”

Petitioner proposes that the term “interconnect layer” be construed as “an interlayer dielectric having metal conductive interconnects therein or therethrough.” Pet. 11 (citing Ex. 1103, 88; Ex. 1105 § V.A). Patent Owner proposes that the correct construction of the term “does not include non-continuous portions of dielectric used to planarize another dielectric layer.” PO Resp. 24.

As the basis of its arguments in support of its claim construction, Patent Owner alleges that during the prosecution of the '933 patent, the applicant distinguished U.S. Patent No. 5,510,652 (“Burke”), which used isolated portions of dielectric materials to fill materials in an interconnect layer. PO Resp. 24–26 (citing Exs. 1103, 1004). Patent Owner refers to annotated Figure 14 of Burke, reproduced below, arguing that applicant characterized layer 42 as an interconnect layer. *Id.* at 24–25 (citing Ex. 1103, 88).



(Ex. 1004 [FIG. 14] (red annotations illustrate layer 42).)

In view of the annotated cross-section of Figure 14, Patent Owner asserts that applicant argued “that Burke ‘fails to teach a second interconnect layer formed on the first interconnect layer’ and ‘merely describe[s] a complex method of forming a single interconnection layer.’” PO Resp. 25 (citing Ex.

1103, 61). Patent Owner further contends that in its arguments on appeal of the Examiner's rejection, applicant distinguished structure 46 shown in annotated Figure 14 as not a layer, but as "isolated portions of a relatively soft dielectric material." *Id.* (citing Ex. 1103, 88). Patent Owner asserts that applicant "clearly and unequivocally" distinguished Burke's layer 46, and thereby disclaimed "non-continuous portions of dielectric used to planarize another dielectric layer from the meaning of interconnect layer." *Id.* at 26.

Patent Owner additionally argues that its proposed construction is consistent with the language of claim 5. PO Resp. 26. Patent Owner also contends that a construction precluding non-continuous dielectric layers is also consistent with the embodiments disclosed in the specification. *Id.* at 26–27.

In Reply, Petitioner argues that Patent Owner's proposed interpretation of the claim term should be rejected because, during prosecution, applicant defined the claim "interconnect layer" as follows:

As used throughout the present application, the expression "interconnect layer" is manifestly intended to denote an interlayer dielectric having metal conductive interconnects therein or therethrough.

Pet. Reply 5–6 (citing Ex. 1103, 116).

Petitioner alleges that applicant never used any "continuous" language in prosecution, nor was there disavowal of any structure that is not continuous. Pet. Reply 6. Petitioner contends that applicant attempted to distinguish Burke on a host of disparate factors, so there can be no finding of a clear, unmistakable disclaimer of subject matter. *Id.* at 6–7. Petitioner further argues that Patent Owner's assertion that Burke's layer 46 is not

continuous is incorrect because, besides where it is pierced by other structures, the layer is continuous. *Id.* at 7.

A prosecution history disclaimer must be clear and unambiguous. “[W]hile the prosecution history can inform whether the inventor limited the claim scope in the course of prosecution, it often produces ambiguities created by ongoing negotiations between the inventor and the PTO Therefore, the doctrine of prosecution disclaimer only applies to unambiguous disavowals.” *Grober v. Mako Prods., Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012) (citing *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009)); *see also Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1322 (Fed. Cir. 2013). This standard is “exacting.” *Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012).

We find no express disavowal of non-continuous portions of dielectric layers, such as that depicted in Burke, based on the prosecution history relating to interpretation of the claim term “layer interconnect.” We agree with Petitioner that applicant attempted to distinguish Burke on several different factors, including that Burke’s layer 46 is not a “layer,” its upper surface includes portions of layer 48 and interconnect 54 so it is not planarized, and also that the layer is not free of residual metal, as required by the claim. Ex. 1103, 88–89. We do not discern from the record that applicant limited the claim scope to a non-continuous layer such as that in Burke or that there was an express disavowal. *See id.* Nor do we discern, and Patent Owner fails to explain, how its arguments apply to embodiments in the specification of the ’933 patent that refer to structures such as “layer interconnects (i.e. dielectric 14 and plugs 16a-c)” which extend through layers, when under Patent Owner’s argument the layer would appear to be

“non-continuous.” *See e.g.*, Ex. 1101, 4:19–20. Similarly, Patent Owner also does not explain how its proposed “non-continuous” limitation could conform to the claim 5 language itself, which includes a “first layer interconnect . . . through which at least one first layer conductor extends” as well as “second layer interconnect” that has a “second layer conductor” extending through it.

Instead, we find the statement of applicant’s manifest intent in the prosecution history indicates that the “interconnect layer” is “an interlayer dielectric having metal conductive interconnects therein or therethrough,” and this represents how the claim term “layer interconnect” should be construed.⁹ *See* Ex. 1103, 88, 116. We therefore adopt the claim interpretation that a “layer interconnect” is “an interlayer dielectric having metal conductive interconnects therein or therethrough.”

“damascene techniques”

Petitioner proposes that the term “damascene techniques” should be construed as “patterning opening(s) in a dielectric layer and filling the patterned opening with conductor material.” Pet. 11 (citing Ex. 1101, 3:59–64; Ex. 1105 § V.B). Petitioner alleges that the claims do not require that all layers of an interconnect structure be made by damascene techniques. *Id.*

Patent Owner argues that “[i]n view of the claim language as a whole, the specification, and the knowledge of one of ordinary skill in the art, the phrase ‘using damascene techniques’ adds a limitation to claim 5 and requires the ‘forming’ steps to use damascene techniques.” PO Resp. 15–16.

⁹ The parties agreed that the terms “interconnect layer” and “layer interconnect” are used interchangeably and should be interpreted in the same manner. Tr. 11:14–20, 50:1–8.

Patent Owner contends that the claim requires three steps: “1) patterning a layer of dielectric material to form an etched opening; 2) filling the etched opening with a conductive material; and 3) planarizing the conductive material using etching or [chemical-mechanical polishing] CMP so that the top surface of the conductive material is significantly level with the top of the dielectric material.” *Id.* at 16 (citing Ex. 2013 ¶ 75). Patent Owner alleges that the phrase “using damascene techniques” in the preamble serves to “breath[] life and meaning into the claims,” so it is “an additional ‘necessary limitation to them.’” *Id.* at 16–17 (citing *Loctite Corp v. Ultraseal Ltd.*, 781 F.2d 861, 866 (Fed. Cir. 1985)). Patent Owner further asserts that the specification states repeatedly that forming interconnect layers using damascene techniques is part of the invention. *Id.* at 18 (citing Ex. 1101, 1:50–53, 3:30–34, 5:35–45). Patent Owner argues that the preamble defines the invention by limiting the methods that satisfy the claim. *Id.* Patent Owner asserts that under the “conventional damascene techniques” described in the ’933 patent, it requires that the plugs are significantly level with the top of the dielectric layer. *Id.* at 19. Patent Owner alleges that, although Petitioner apparently agrees that “using damascene techniques” is a claim limitation, its proposed definition is overbroad because it omits the step of planarizing the conductive material by etching or CMP. *Id.* Patent Owner further argues that a person of ordinary skill in the art would not understand that any one of the three steps may be omitted because all three steps are needed to form a functional interconnect layer. *Id.* (citing Ex. 2013 ¶ 80).

Patent Owner further asserts that claim differentiation need not be applied to the interpretation of claim 5 in light of the limitations of

dependent claim 6. PO Resp. 21. Patent Owner argues that “the doctrine of claim differentiation does not *require* each claim to have a different scope, but rather merely creates a *presumption* that each claim has a different scope.” *Id.* (citing *Free Motion Fitness, Inc. v. Cybex Int’l, Inc.*, 423 F.3d 1343, 1351 (Fed. Cir. 2005)). Patent Owner further contends that claim 6 is not rendered superfluous by its proposed construction because it “only further limits the forming of the second layer interconnect and not the first step of forming the first layer interconnect.” *Id.* This argument is based on Patent Owner’s assertion that under the ’933 patent specification, “the first interconnect layer is formed using damascene techniques, including planarization, as was admittedly known in the art, but adds new, previously unused process steps for forming the second layer interconnect.” *Id.* at 21–22 (citing Ex. 2013 ¶ 59). Patent Owner further argues that, even under the alleged claim differentiation with claim 6, this does not serve as a reason to exclude the planarization step from “using damascene techniques” because “the specification makes clear that the invention pertains exclusively to interconnect structures made using damascene techniques, including the planarization step.” *Id.* at 22.

To require that the step of “planarizing the conductive material . . .” be included in the steps of claim 5 constitutes impermissible importation of a limitation into the claim. This would be so even if we were to find that the use of the term “using damascene techniques” in the preamble is limiting. There is no dispute that the steps of claim 5 as recited, that is, “patterning” and “filling” steps, are steps used in “damascene techniques.” The performance of any one of the steps of a damascene technique would fall within the scope of the “using damascene techniques” of the preamble. In

other words, the performance of any of the steps of a damascene technique could be considered to be “the use of damascene techniques” because “patterning” and “filling” are steps that are part of “damascene techniques.”

We discern nothing in claim 5 that requires the inclusion of all steps employed in damascene techniques be included as recited steps, as Patent Owner advocates. Claim 5 recites “forming the second layer interconnect” includes “patterning . . . to form an etched opening,” and “filling the etched opening with a conductive material to form the second layer conductor,” with dependent claim 6 reciting “planarizing the conductive material to be substantially level with the top surface of the second layer dielectric.” See Ex. 1101 6:19–42. Because claim 6 further limits claim 5, the doctrine of claim differentiation supports a conclusion that claim 5 should not include a planarizing step. *Free Motion Fitness, Inc. v. Cybex Int’l, Inc.*, 423 F.3d 1343, 1351 (Fed. Cir. 2005). To view the claims otherwise would impermissibly make one of the claims superfluous. See *id.*

Moreover, the disclosures of the specification do not support that the recitation of the use of “damascene techniques” requires that there be a step included for planarizing the conductive material. For instance, the specification describes patterning to form an etched opening in both the first and second layers, without any planarizing of conductive materials, and these steps are described as using damascene techniques or processes. See Ex. 1101, 3:49–52, 4:21–26, Figs. 1a, 1b. Nor is there support for Patent Owner’s argument that claim 5’s use of the term “damascene techniques” should result in an interpretation that no planarizing of the conductive material is required for the first interconnect layer, but planarizing is required for the second interconnect layer. See PO Resp. 21. Patent

Owner's argument is inherently inconsistent because it would apply the use of "damascene techniques" in two different ways within the same claim. Patent Owner is also trying to limit the claim to an embodiment of the specification, despite broader language in the claim itself and support for such breadth in the specification.

On the other hand, we determine that Petitioner's proposed construction is consistent with the language of claim 5 and the disclosures in the '933 patent specification. Accordingly, we adopt Petitioner's proposed construction of "damascene techniques" as "patterning opening(s) in a dielectric layer and filling the patterned opening with conductor material."

Other Terms

We determine that no other claim term requires an express construction for the purposes of this Decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

C. Level of Ordinary Skill in the Art

Petitioner's expert, Dr. Neikirk, testifies that a person of ordinary skill in the art at the time of the '933 invention "would have had a graduate's degree with some emphasis in semiconductor device fabrication in physics, material science, electrical engineering, or a related degree, or an undergraduate degree in one of these fields and two to three years' experience in semiconductor device design and fabrication," as well as having "at least a basic understanding, through education or experience, of fabrication methods for interconnect structures." Ex. 1105 ¶ 25; *see also* Pet. 10.

Patent Owner's expert, Dr. Bottoms, testifies that one of ordinary skill in the art at the time of the invention of the '933 patent "would have held a

master's degree in physics, electrical engineering or a related field and three years or more experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices.” Ex. 2001 ¶ 30; *see also* PO Resp. 2.

The parties propose similar educational qualifications and experience levels. We find Petitioner's proposed qualification of having at least a basic understanding of fabrication methods for interconnect structures to be applicable here in view of the '933 patent. Therefore, to the extent necessary, we adopt Petitioner's proposed qualifications as reflecting the level of ordinary skill in the art. In addition, we note that the primary art of record in this proceeding—namely, Kimura, Yoshihara, and Kubo—is indicative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Neither Dr. Neikirk nor Dr. Bottoms testifies that adoption of a different definition would change the outcome of this case.

D. Alleged Anticipation by Kimura

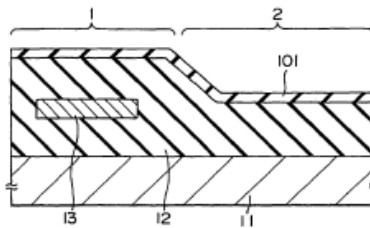
Petitioner contends that Kimura anticipates claims 5–8, 10, and 11. Pet. 58–65. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1105, 1121) to support its positions. Patent Owner counters that the Kimura does not anticipate the claims because it fails to disclose some claim limitations. PO Resp. 62–64. Patent Owner relies upon the Bottoms Declaration (Ex. 2001) and Response Bottoms Declaration (Ex. 2013) to support its positions.

We begin our discussion with a brief summary of Kimura, and then address the evidence, analysis, and arguments presented by the parties.

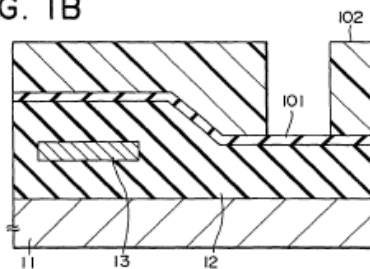
1. Kimura (Ex. 1110)

Kimura discloses a method for fabricating a semiconductor device that is capable of forming high reliability contacts. Ex. 1110, 2:18–21. Figures 1A–1G, reproduced below, depict cross-sectional drawings of the fabrication of a semiconductor device manufactured according to one embodiment of the invention. *Id.* at 3:7–12.

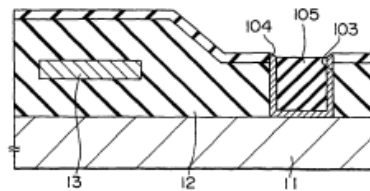
F I G. 1A

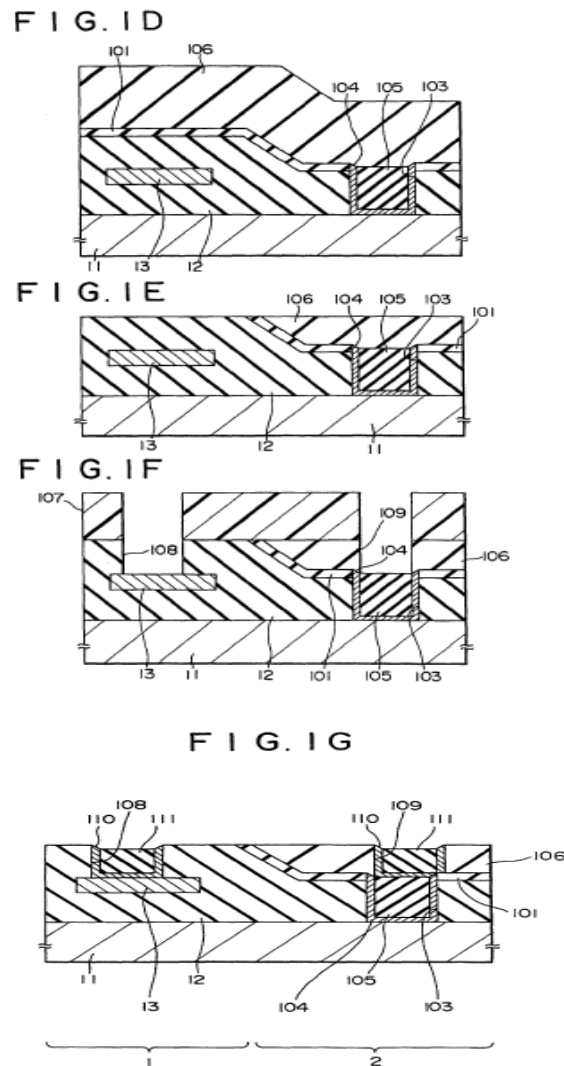


F I G. 1B



F I G. 1C





In the cross-section of Figure 1C, semiconducting substrate 11 is formed with insulating layer 12 above it, polysilicon layer 13 is an interconnection layer, with tungsten layer 105 depicted. Ex. 1110, 3:28–51. As shown in Figure 1G, photoresist 107 is removed, and tungsten layer 111 is formed in two contact holes 108, 109. *Id.* at 4:54–57.

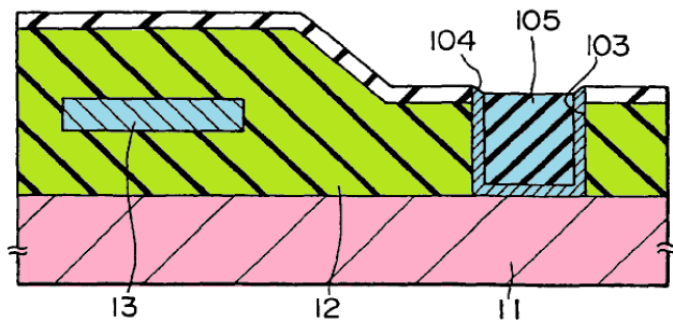
2. Analysis

A claim is unpatentable under 35 U.S.C. § 102 if a prior art reference discloses each and every limitation of the claimed invention, either explicitly or inherently. *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir.

1995); see *MEHL/Biophile Int’l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (“To anticipate, a claim a prior art reference must disclose every limitation of the claimed invention . . .;” any limitation not explicitly taught must be inherently taught and would be so understood by a person experienced in the field); *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991) (the dispositive question is “whether one skilled in the art would reasonably understand or infer” that a reference teaches or discloses all of the limitations of the claimed invention).

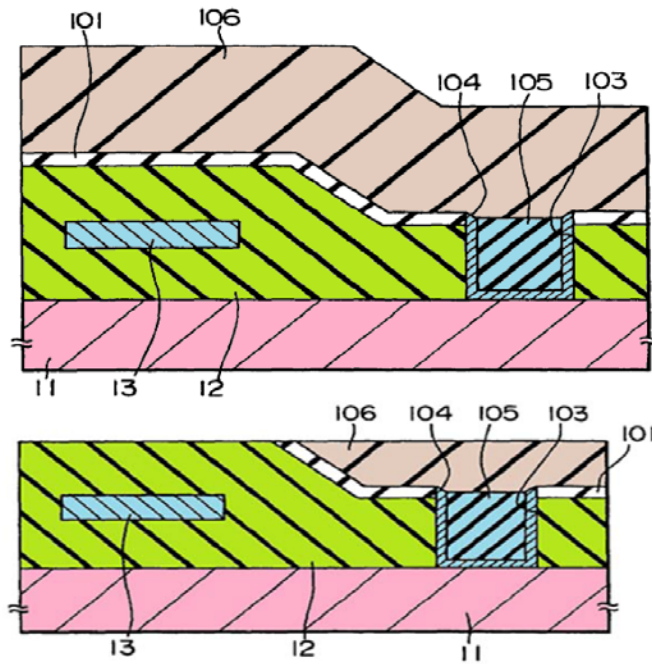
a. Independent Claim 5

Petitioner presents evidence that Kimura discloses all the limitations of claims 5–8, 10, and 11. See Pet. 58–65. In particular, Petitioner relies upon annotated Figures 1C–1G reproduced below.¹⁰ See *id.* at 58–63.

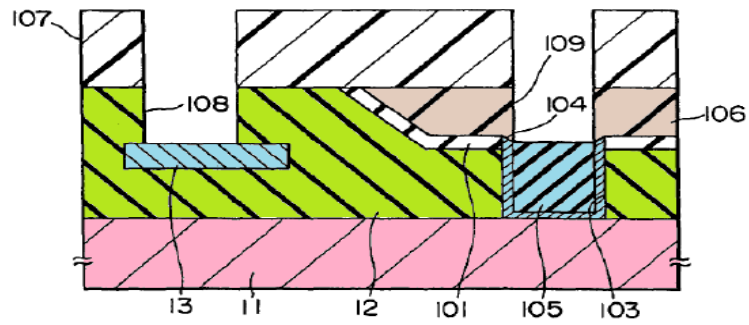


Ex. 1011, FIG. 1C (annotated)

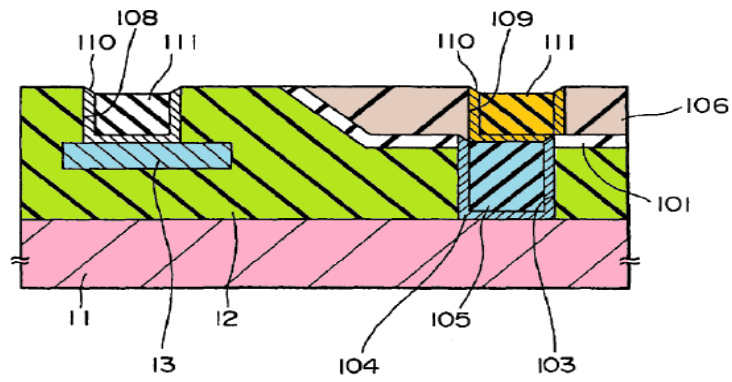
¹⁰ Annotated Figures 1C–1G refer to “Ex. 1011,” and should instead refer to Ex. 1110.



Ex. 1110, FIGS. 1D-1E (annotated)



Ex. 1110, FIG. 1F (annotated)



Ex. 1011, FIG. 1G (annotated)

Petitioner asserts, and we agree, that Kimura discloses a method for forming a multilayer structure in an integrated circuit, as depicted in the cross-section in annotated Figure 1G, using damascene techniques. Pet. 58–59. More specifically, Petitioner contends, and we agree, that Kimura teaches the use of damascene techniques by its disclosure that contact holes 103, 108, and 109 are formed in dielectric layers 12 and 106 and then are filled with conductor materials. *Id.* at 59 (citing Ex. 1110, 3:41–59, 4:24–65).

Petitioner contends, and we agree, that Kimura discloses formation of a “first interconnect layer,” which is first dielectric layer 12, shown in green, with first layer conductors 13 and 105, shown in blue, extending through the layer, as depicted in annotated Figure 1C. *Id.* at 59–60 (citing Ex. 1110, 3:28–36, 3:47–51).

Petitioner also contends, and we agree, that Kimura discloses forming a second layer interconnect on the first layer interconnect, the second layer interconnect having a second layer dielectric 106 (shown in tan) through which at least one second layer conductor 111 (shown in orange) extends, as depicted in annotated Figure 1G. Pet. 60 (citing Ex. 1110, 4:1–3, 4:26–65). Petitioner also provides evidence that Kimura discloses substantially planarizing the second layer dielectric to reduce the thickness by polishing the surface of second layer dielectric (shown in tan), as depicted in annotated Figures 1D and 1E. *Id.* at 60–61 (citing Ex. 1110, 4:1–6). We agree with Petitioner that Kimura also discloses patterning the second dielectric to form an etched opening and filling it with conductive material as depicted in annotated Figures 1F and 1G. *Id.* at 62–63 (citing Ex. 1110, 4:26–34, 4:54–57).

Notwithstanding Patent Owner's contrary arguments, which we discuss below, we agree that Kimura discloses every limitation of claim 5 of the '933 patent and credit Dr. Neikirk's supporting testimony (Ex. 1105 ¶¶ 295–324) on that point, as it is consistent with the prior art disclosures.

Patent Owner argues that Kimura fails to disclose a first and second interconnect layer as recited in claim 5 because only an isolated portion of layer 106 is used to planarize a single interconnect layer. PO Resp. 62 (citing Ex. 2013 ¶ 147). Patent Owner argues that Burke distinguished an interconnect layer and disclaimed similar isolated portions of materials, which was at issue in the prosecution history. *Id.* We do not agree with Patent Owner's argument because it is based on Patent Owner's proposed interpretation for the term “interconnect layer,” which we have not adopted. *See supra* Section II.B. Instead, we have construed the term “interconnect layer,” as “an interlayer dielectric having metal conductive interconnects therein or therethrough,” and Kimura's layer 106, as depicted in Figure 1G, has a structure that falls within that definition. *See id.*

Patent Owner also asserts that in Kimura, contact plugs in the array region 1 shown in Fig. 1G (*see supra* 21) need to be shallow, while contact plugs in region 2 need to be substantially deeper, so they are formed in a two-step process. PO Resp. 63. Patent Owner argues that the contact plugs reach the top surface of a single interconnect layer. *Id.* We do not agree with Patent Owner that Kimura discloses only a single interconnect layer. As mapped, and as discussed above, Kimura's structure has two interconnect layers (shown in green and tan), each having its own metal conductive interconnects (shown in blue and orange), as depicted in annotated Figure 1G. Patent Owner also alleges that Kimura does not disclose

depressions formed in the insulator layer. *Id.* at 64. We do not agree with Patent Owner’s argument because claim 5 does not recite a “depression” limitation.

Patent Owner also argues that Kimura does not disclose the use of “damascene techniques.” Patent Owner asserts that Kimura does not use the word “damascene,” and the contact plugs disclosed by Kimura are not formed using damascene techniques because there is no disclosure of planarizing the tungsten metal used to form its contact plugs. PO Resp. 64. We do not agree with Patent Owner’s arguments. We have declined to adopt Patent Owner’s proposed claim construction that “damascene techniques” requires “planarizing the conductive material,” so Petitioner does not have to show this disclosure in the prior art in order to demonstrate anticipation. Additionally, a prior art reference does not have to use the exact wording as the claim; rather, the dispositive question is whether one skilled in the art would reasonably understand that each claim element is disclosed by the reference. *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990); *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991). As discussed above, we determined that Petitioner has sufficiently demonstrated that Kimura discloses the claimed “patterning” and “filling” using damascene techniques.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 5 of the ’933 patent is anticipated by Kimura.

b. Claim 6

Claim 6 recites “[t]he method as recited in claim 5, wherein forming the second layer interconnect further includes planarizing the conductive

material to be substantially level with the top surface of the second layer dielectric.” Ex. 1101, 6:39–42. Petitioner alleges that Kimura discloses that the conductive material 11 (shown in orange) is planarized to be substantially level with the top surface of second layer dielectric 106 (shown in tan), as depicted in annotated Figure 1G reproduced above. Pet. 63–64 (citing Ex. 1110, 4:54–65).

We agree with Petitioner that Kimura discloses every limitation of claim 6 of the ’933 patent and credit Dr. Neikirk’s supporting testimony (Ex. 1105 ¶¶ 325–330) on that point, as it is consistent with the prior art disclosures. Patent Owner presents no arguments for claim 6, beyond its assertions for independent claim 5, which we have addressed above. PO Resp. 62–64.

Thus, Petitioner has shown by a preponderance of the evidence that claim 6 of the ’933 patent is anticipated by Kimura.

c. Claim 7

Claim 7 recites “[t]he method recited in claim 5, wherein the second layer dielectric includes TEOS oxide.” Ex. 1101, 6:43–44. Petitioner alleges that Kimura discloses that the second layer dielectric includes TEOS oxide. Pet. 64. In support, Petitioner refers to Kimura’s disclosure that a “P-TEOS (Plasma Tetraethyl Orthosilicate) layer” is formed. *Id.* (citing Ex. 1110, 4:1–3).

We agree that Kimura discloses every limitation of claim 7 of the ’933 patent and credit Dr. Neikirk’s supporting testimony (Ex. 1105 ¶¶ 331–335) on that point, as it is consistent with the prior art disclosures. Patent Owner presents no arguments for claim 7, beyond its assertions for independent claim 5, which we have addressed above. PO Resp. 62–64.

Thus, Petitioner has shown by a preponderance of the evidence that claim 7 of the '933 patent is anticipated by Kimura.

d. Claim 8

Claim 8 recites “[t]he method as recited in claim 7, wherein the first thickness is greater than approximately 10,000 Å.” Ex. 1110, 6:45–46. Petitioner alleges that Kimura discloses this claim limitation by stating that the “P-TEOS (Plasma Tetraethyl Orthosilicate) layer 106 is then formed over the entire surface to a thickness of about 1.5 μm by CVD,” which is 15,000 Å. Pet. 64 (citing Ex. 1110, 4:1–3).

We agree that Kimura discloses every limitation of claim 8 of the '933 patent and credit Dr. Neikirk's supporting testimony (Ex. 1105 ¶¶ 336–341) on that point, as it is consistent with the prior art disclosures. Patent Owner presents no arguments for claim 8, beyond its assertions for independent claim 5, which we have addressed above. PO Resp. 62–64.

Thus, Petitioner has shown by a preponderance of the evidence that claim 8 of the '933 patent is anticipated by Kimura.

e. Claim 10

Claim 10 recites “[t]he method as recited in claim 5, wherein the conductive material is a metal.” Ex. 1110, 6:49–50. Petitioner alleges that Kimura discloses this claim limitation by its “barrier metal layer 110 and a tungsten layer 111,” which are formed in the two contact holes. Pet. 65 (citing Ex. 1110, 4:54–57).

We agree that Kimura discloses every limitation of claim 10 of the '933 patent and credit Dr. Neikirk's supporting testimony (Ex. 1105 ¶¶ 342–346) on that point, as it is consistent with the prior art disclosures. Patent

Owner presents no arguments for claim 10, beyond its assertions for independent claim 5, which we have addressed above. PO Resp. 62–64.

Thus, Petitioner has shown by a preponderance of the evidence that claim 10 of the '933 patent is anticipated by Kimura.

f. Claim 11

Claim 11 recites “[t]he method as recited in claim 10, wherein the metal includes tungsten.” Ex. 1110, 6:51–52. Petitioner alleges that Kimura discloses this claim limitation by “a barrier metal layer 110 and a tungsten layer 111” that are formed in the two contact holes. Pet. 65 (citing Ex. 1110, 4:54–57).

We agree that Kimura discloses every limitation of claim 11 of the '933 patent and credit Dr. Neikirk’s supporting testimony (Ex. 1105 ¶¶ 347–351) on that point, as it is consistent with the prior art disclosures. Patent Owner presents no arguments for claim 11, beyond its assertions for independent claim 5, which we have addressed above. PO Resp. 62–64.

Thus, Petitioner has shown by a preponderance of the evidence that claim 11 of the '933 patent is anticipated by Kimura.

E. Alleged Obviousness of Claim 9 over Kimura and Jang

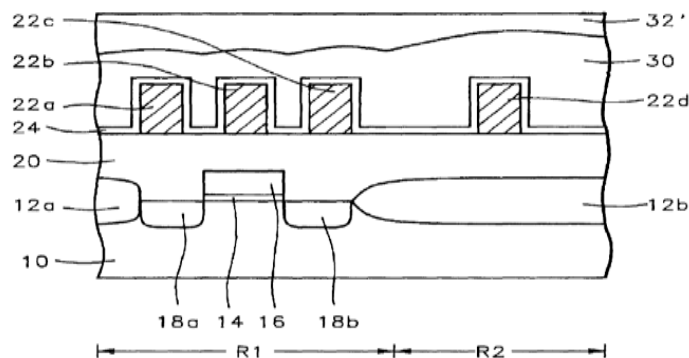
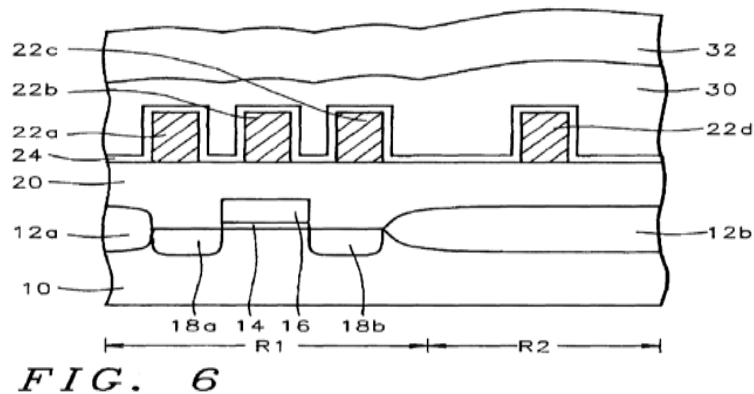
Petitioner asserts that claim 9 is obvious over the combination of Kimura and Jang. Pet. 65–67. To support its contentions, Petitioner provides evidence and explanations as to how the prior art teaches each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declarations (Ex. 1105, 1121) to support its positions. Patent Owner counters that the prior art does not render claim 9 obvious because the prior art fails to teach

or suggest some limitations of the claim and the prior art is incompatible.
PO Resp. 64–66.

Based on the evidence in this entire trial record, we are persuaded by Petitioner’s explanations and evidence in support of the obviousness grounds asserted under Kimura and Jang for claim 9. We begin our discussion with a brief summary of Jang, and then address the evidence, analysis, and arguments presented by the parties.

1. Jang (Ex. 1108)

Jang is directed to methods for forming integrated circuits. Ex. 1108, 2:65–67. Jang discloses forming methods that are depicted in cross-sections shown below in reproduced Figures 6 and 7.



Figures 6 and 7 are schematic cross-sectional diagrams illustrating progressive stages in forming an integrated circuit, which include formed CMP planarized layers of an embodiment of the invention, conductive layers 22a-22d, blanket first gap filling insulator layer 30, and interconductor dielectric layer 32. Ex. 1108, 4:44–49, 11:9–17, 11:19–25. Interconductor dielectric layer 32 is planarized to be uniform by CMP planarization to form planarized inter-conductor dielectric layer 32 as shown in Figure 7. *Id.* at 11:22–25, 11:44–48.

2. Analysis

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.¹¹ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Claim 9 recites “[t]he method as recited in claim 7, wherein the second thickness is less than or equal to approximately 5,000 Å.” Ex. 1110, 6:43–44. Petitioner asserts that Kimura teaches that its TEOS layer is approximately 7,000 Å after planarizing, which is close to the thickness range claim. Pet. 65–66. Dr. Neikirk testifies that Kimura and Jang disclose

¹¹ Patent Owner does not argue on this record that there are objective indicia of nonobviousness.

similar manufacturing techniques. Ex. 1105 ¶ 358. Dr. Neikirk further testifies that Jang teaches that its inter-connector dielectric layer is planarized to a reduced thickness of 3,000–5,000 Å. *Id.* ¶ 358 (citing Ex. 1108, 11:38–40, 12:1–5). Dr. Neikirk testifies that “Jang’s disclosure also reinforces my opinion that a person having ordinary skill [], who considers interrelated teachings of the art would recognize that planarization techniques may yield a planarized layer 106 at a thickness less than or equal to 5,000 Å.” *Id.* ¶ 358.

We agree with Petitioner that the evidence supports that one of skill in the art would have considered Kimura and Jang’s teachings to be interrelated—both references are directed to methods for forming integrated circuits, and, more specifically, they disclose similar formations of dielectric layers with interconnect structures and CMP polishing. *See* Ex. 1110, 1:37–40, 2:18–21, 4:1–24; Ex. 1108, 1:38–40, 2:65–3:4, 12:1–5. Dr. Neikirk’s testimony that a person having ordinary skill in the art would have recognized that planarization techniques yield a layer thickness less than or equal to 5,000 Å is consistent with and supported by the teachings of Kimura and Jang. *See* Ex. 1105 ¶ 358.

Notwithstanding Patent Owner’s contrary arguments, which we discuss below, we agree that Kimura and Jang teach every limitation of claim 9 of the ’933 patent and that there is sufficient rationale to combine the references, and we credit Dr. Neikirk’s supporting testimony (Ex. 1105 ¶¶ 352–374) on that point, as it is consistent with the prior art disclosures.

Patent Owner argues that Kimura does not disclose forming both first and second layer interconnects using damascene techniques. PO Resp. 65. We do not agree with Patent Owner’s argument on this issue because it is

based on Patent Owner's proposed interpretation for the application of the term "damascene techniques," which we have not adopted. *See supra* Section II.B.

Patent Owner also asserts that Jang's alleged teaching of reducing the thickness of an interconductor dielectric layer "is not properly combinable with Kimura's disclosed process." PO Resp. 65. Patent Owner contends that in Kimura, layer 106 is polished down to a thickness equivalent to the height difference between the top of the insulating layer minus the thickness of the silicon nitride layer 101. *Id.* Patent Owner argues that there is no suggestion in Kimura that the thickness of layer 106 could be freely modified. *Id.*

We do not agree with Patent Owner's argument on this issue because it is based on a bodily incorporation of Jang into Kimura; however, "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Here, Jang teaches that the inter-connector dielectric layer can be planarized to a reduced thickness of less than 5,000 Å, and Kimura teaches a second layer with a thickness close to the range claim in the view of one of ordinary skill in the art. *See* Ex. 1108, 12:1–5; Ex. 1105 ¶¶ 354–357. Therefore, we find sufficient support for Dr. Neikirk's testimony that a skilled artisan would have found the interrelated teachings of Kimura and Jang's planarization techniques to suggest thicknesses of less than or equal to 5,000 Å in a second layer in a formation of dielectric layers. *See* Ex. 1105 ¶¶ 358–359.

Thus, Petitioner has shown by a preponderance of the evidence that claim 9 of the '933 patent is unpatentable as obvious over Kimura and Jang.

F. Alleged Obviousness of Claim 12 over Kimura and Ito

Petitioner asserts that claim 12 is obvious over the combination of Kimura and Ito. Pet. 56–65. To support its contentions, Petitioner provides evidence and explanations as to how the prior art teaches each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declarations (Exs. 1105, 1121) to support its positions. Patent Owner counters that the prior art would not have rendered claim 12 obvious because the prior art fails to teach or suggest some limitations of the claim. PO Resp. 66.

Based on the evidence in this entire trial record, we are persuaded by Petitioner's explanations and evidence in support of the obviousness grounds asserted under Kimura and Ito for claim 12. We begin our discussion with a brief summary of Ito, and then address the evidence, analysis, and arguments presented by the parties.

1. Ito (Ex. 1116)

Ito discloses techniques for manufacture of interconnects in semiconductor devices directed to reduction in capacitance effects and reflection. Ex. 1116 ¶¶ 5–6. Figure 1, reproduced below, shows a cross-sectional drawing of a semiconductor device manufactured according to an example of the invention. *Id.* at [Brief Explanation of the Drawing].

[Figure 1]

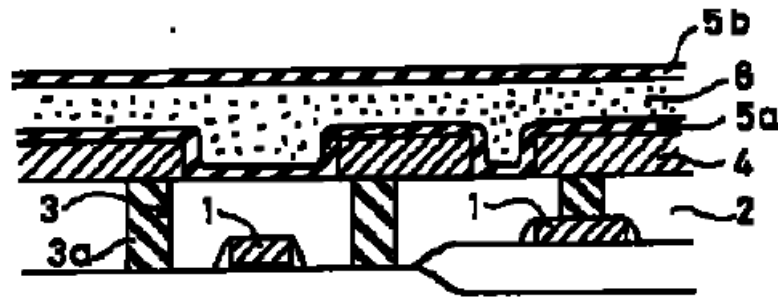


Figure 1 depicts wires 4, plugs 3, substrate 1, and insulating layers 2 and 6. Ex. 1116 ¶¶ 14–17. Ito discloses planarization of layer 6 by a CMP process. *Id.* ¶ 26.

2. Analysis

Claim 12 recites “[t]he method as recited in claim 6, wherein the planarizing of the conductive material includes the step of chemical-mechanical polishing.” Ex. 1110, 6:53–55. Petitioner asserts that Kimura discloses planarizing its tungsten plugs by surface etch-back. Pet. 67. Petitioner directs us to Ito, which discloses semiconductor manufacture techniques with tungsten plugs, where removal of excess tungsten may be performed by etch-back technique or by CMP. *Id.* at 68 (citing Ex. 1116 ¶ 15). Petitioner refers to Ito’s discussion of the respective methods as disclosing advantages of CMP over etch back:

As an embedding method of the plug metal 3a, a method that combines W-CVD and etching or a method that only leaves plug metal 3a in the contact hole by a CMP process replacing etch back may be adopted. If the thickness of the wiring metal extending over the entire wafer is made uniform, ***the elimination of unnecessary W from CMP yields more excellent results than with etch back.***

Ex. 1116 ¶ 15 (cited in Pet. 68) (emphasis in Petition).

Petitioner argues that “Ito teaches CMP is a better technique than etch-back, [and] Ito would motivate a worker of skill to replace Kimura’s etch-back technique with CMP planarization.” Pet. 68 (citing Ex. 1105 ¶ 380).

Notwithstanding Patent Owner’s contrary argument, which we discuss below, we agree that Kimura and Ito teach every limitation of claim 12 of the ’933 patent, and we credit Dr. Neikirk’s supporting testimony (Ex. 1105 ¶¶ 375–380) on that point, as it is consistent with the prior art disclosures. We also agree that there is sufficient rationale to combine the references because they are both directed to semiconductor manufacturing techniques with tungsten plug formation, and Ito’s method of removing excess tungsten using CMP offers an improvement to Kimura’s method. See Ex. 1105 ¶¶ 377–380; KSR, 550 U.S. at 417 (noting that “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill”).

Patent Owner argues that Kimura does not disclose forming both first and second layer interconnects using damascene techniques. PO Resp. 66. We do not agree with Patent Owner’s argument because it is based on Patent Owner’s proposed interpretation for the application of the term “damascene techniques,” which we have not adopted. See *supra* Section II.B.

Thus, Petitioner has shown by a preponderance of the evidence that claim 12 of the ’933 patent is obvious over Kimura and Ito.

G. Alleged Anticipation by Kubo

Petitioner contends that Kubo anticipates claims 5–8, 10, and 11. Pet. 44–54. To support its contentions, Petitioner provides explanations as to

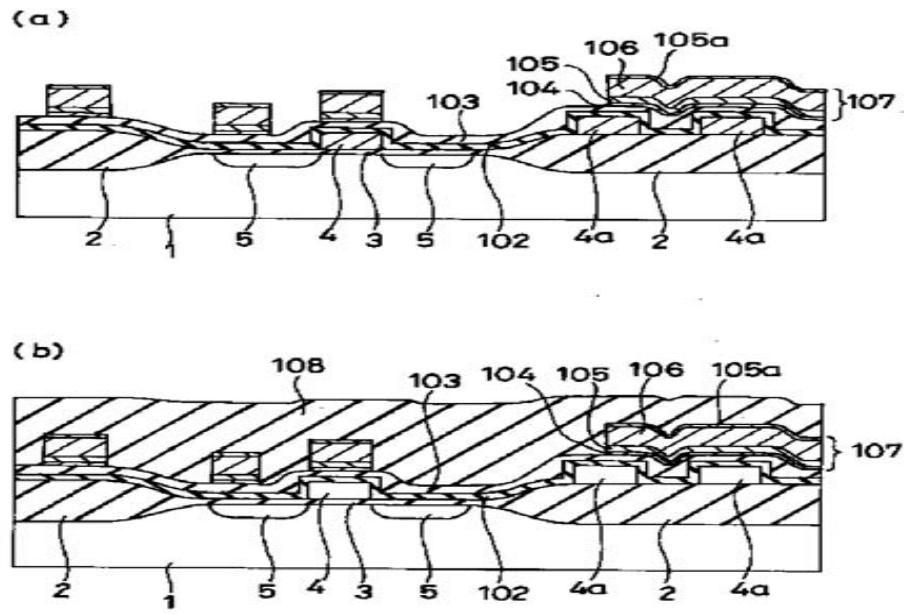
how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1105, 1121) to support its positions. Patent Owner counters that the Kubo does not anticipate the claims because it fails to disclose some claim limitations. PO Resp. 52–60.

We begin our discussion with a brief summary of Kubo, and then address the evidence, analysis, and arguments presented by the parties.

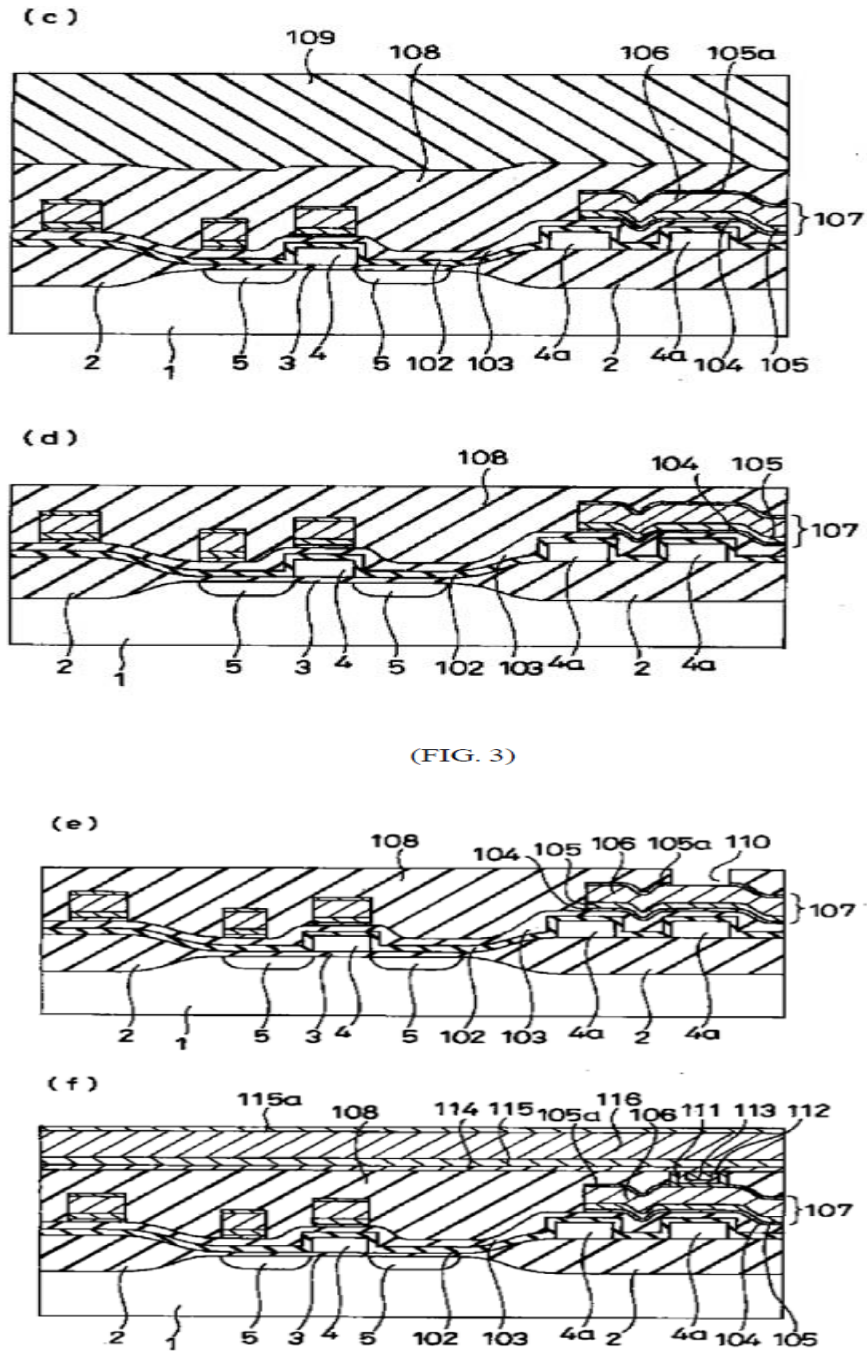
1. Kubo (Ex. 1112)

Kubo is directed to a manufacturing method for semiconductor devices that forms interlayer insulation film for multilayer wiring. Ex. 1112 ¶ 1. More specifically, Kubo is directed to improvements in an interlayer insulation film. *Id.* ¶ 2. Kubo discloses a method for forming a multiple-layer interconnect structure that includes embodiment 1, depicted in the manufacturing sequence reproduced below, with the cross-sections shown in Figure 2 continued from Figure 1, and the cross-sections shown in Figure 3 continued from Figure 2. *Id.* at [Brief Description of the Drawings].

【図 1】



【図 2】



(FIG. 3)

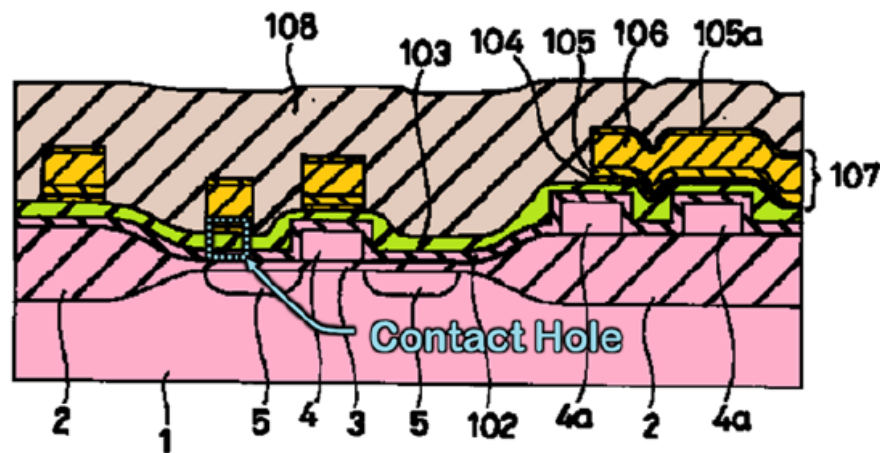
Cross sections of Figures 1, 2, and 3, above, depict silicon substrate 1, wire base insulation film 103 under laminated wiring 107, base insulation film

103, titanium film 104, silicon oxide film 108, and tungsten film 113. Ex. 1112 ¶¶ 22, 25, 27, 31.

2. Analysis

Petitioner presents evidence that Kubo discloses all the limitations of claims 5–8, 10, and 11. *See* Pet. 44–54.

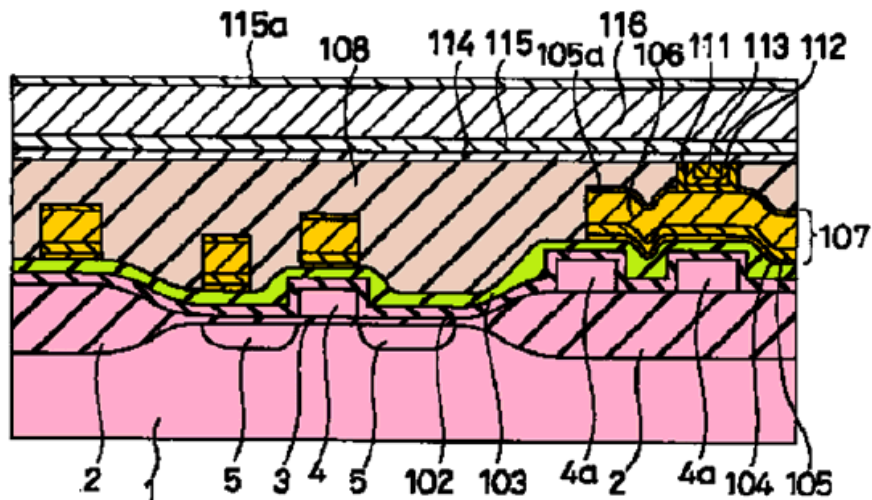
For claim 5, Petitioner asserts, and we agree, that Kubo teaches a method for forming a multiple-layer interconnect structure in an integrated circuit using damascene techniques by its disclosure of forming contact holes in dielectric layers 103 and 108, and then filling them with conductor materials. Pet. 45 (citing Ex. 1112, ¶¶ 25, 30–31). Petitioner asserts, and we agree, that Kubo discloses a “first interconnect having a first dielectric layer” as depicted in green in the annotated version of Figure 1(b), reproduced below.



Ex. 1112, FIG. 1(b) (annotated)

Annotated Figure 1(b) also depicts contact holes shown in blue that are formed in layer 103, where, as Petitioner asserts and we agree, the contact hole accommodates an electric connection between wiring layer 107 and semiconductor elements on substrate 1. Pet. 45–46 (citing Ex. 1112 ¶ 25).

Petitioner asserts, and we agree, that Kubo discloses forming the second layer interconnect having a second layer dielectric 108 (shown in tan) through which second layer conductors 107, 113 (shown in orange) extends, as shown in annotated Figure 3(f) reproduced below.



Ex. 1112, FIG. 3(f) (annotated)

In support, Petitioner refers to Kubo's disclosures shown in the cross-section of annotated Figure 3(f) of silicon oxide film 108 deposited on a surface incorporating laminated wiring 107, with silicon film 108 etched with through-hole formed reaching lower-level laminated wiring 107, and sputtering with titanium film. Pet. 46–47 (citing Ex. 1112 ¶¶ 27, 30–31). Petitioner asserts, and we agree, that Kubo discloses planarizing second layer dielectric 108 (shown in tan) and patterning it. *Id.* at 47–49 (citing Ex. 1112 ¶¶ 15, 28–29, 30). Petitioner asserts, and we agree, that Kubo discloses filling the etched openings with conductive material to form second layer conductor (shown in orange). *Id.* at 49–50 (citing Ex. 1112 ¶ 31).

Notwithstanding Patent Owner's contrary arguments, which we discuss below, we agree that Kubo discloses every limitation of claim 5 of the '933 patent and credit Dr. Neikirk's supporting testimony (Ex. 1105 ¶¶ 205–233) on that point, as it is consistent with the prior art disclosures.

Patent Owner argues that Kubo does not mention the use of damascene techniques, or CMP or etch-back to planarize a conductor layer when using damascene techniques, as required under claim 5. PO Resp. 57–60 (citing Ex. 2013 ¶ 140–145). We do not agree with Patent Owner's arguments on claim 5 because they are based on Patent Owner's proposed interpretation of the application of the term “damascene techniques,” which we have not adopted. *See supra* Section II.B.

For dependent claim 6, Petitioner asserts, and we agree, that Kubo discloses planarizing the conductive material 113 (shown in orange in annotated Figure 3(f)) to be substantially level with the top surface of the second layer dielectric 108, with “tungsten film 113 and the like [] etched back by performing plasma etching.” Pet. 50–51 (citing Ex. 1112 ¶ 31–32).

For dependent claim 7, Petitioner asserts, and we agree, that Kubo discloses that the second layer dielectric includes TEOS oxide by the use of silicon oxide film referred to as ozone TEOS film. Pet. 51–52 (citing Ex. 1112, 1, ¶¶ 3–5, 26–27, 35–36).

For dependent claim 8, Petitioner asserts, and we agree, that Kubo discloses that the thickness of the second layer dielectric is greater than approximately 10,000 Å, with a thickness of 1.5 µm (15,000 Å) disclosed. Pet. 52 (citing Ex. 1112 ¶ 27).

For dependent claim 10, Petitioner asserts, and we agree, that Kubo discloses that the claimed conductive material is a metal, that is, tungsten film. Pet. 52–53 (citing Ex. 1112 ¶¶ 31–32).

For dependent claim 11, Petitioner asserts, and we agree, that Kubo discloses that the metal includes tungsten. Pet. 53.

For dependent claims 6–8, 10, and 11, Patent Owner argues that Petitioner fails to carry its burden of showing that claim 5 is anticipated by Kubo. PO Resp. 60. We do not agree with Patent Owner because, for the reasons discussed above, we find that Petitioner has sufficiently demonstrated that claim 5 is anticipated by Kubo.

Thus, Petitioner has shown by a preponderance of the evidence that claims 5–8, 10, and 11 of the '933 patent are anticipated by Kubo.

H. Obviousness of Claim 9 over Kubo and Jang

Petitioner asserts that Kubo discloses layer 108, which is deposited initially at a thickness of 1.5 μm , and is planarized by etchback. Pet. 54 (citing Ex. 1112 ¶¶ 26–27). In addition, Petitioner contends that Kubo also teaches that layer 106 has a final thickness of 2,600 Å based on thickness of the films 111-113 placed in a contact hole 110 etched into the layer 108. *Id.* (citing Ex. 1112 ¶¶ 30–31). Dr. Neikirk testifies that “Kubo teaches that the layer 108 is planarized to a thickness of 2,600 Å, and this range falls within the range described by claim 9.” Ex. 1105 ¶ 270. Petitioner also argues that Jang discloses similar manufacturing techniques for interconnect structures at similar thicknesses, with inter-conductor dielectric layer 32 formed initially at a thickness of 13,000-17,000 Å, which is then planarized to a reduced thickness of 3,000-5,000 Å. Pet. 54–55 (citing Ex. 1108, 11:38–40, 12:1–5). Dr. Neikirk testifies that a person of ordinary skill “who considers

these interrelated teachings would recognize that Kubo's etchback techniques would yield a planarized layer 108 at a thickness similar to Jang's, at or about 3,000-5,000 Å." Ex. 1105 ¶ 271.

We agree with Petitioner that one of skill in the art would have considered that Kubo and Jang teach the limitation of a "second thickness that is less than or equal to approximately 5,000 Å."

Notwithstanding Patent Owner's contrary arguments, which we discuss below, we agree that Kubo and Jang teach every limitation of claim 9 of the '933 patent and that there is sufficient rationale to combine the references, and we credit Dr. Neikirk's supporting testimony (Ex. 1105 ¶¶ 267–272) on that point, as it is consistent with the prior art disclosures.

Patent Owner argues that claim 9 would not have been not obvious because Kubo does not disclose the multiple-layer interconnect structure or damascene technique requirements of claim 5, and Petitioner fails to supply arguments that Jang fills this gap. PO Resp. 61. We do not agree with Patent Owner's arguments for claim 5 because they are based on Patent Owner's proposed interpretation for the application of the term "damascene techniques," which we have not adopted. *See supra* Section II.B. Because we find Petitioner's arguments and evidence sufficient to demonstrate that claim 5 was anticipated, we do not agree with Patent Owner's arguments on claim 9 because they are solely based on alleged deficiencies as to claim 5.

Thus, Petitioner has shown by a preponderance of the evidence that claim 9 of the '933 patent is unpatentable as obvious over Kubo and Jang.

I. Obviousness of Claim 12 over Kubo and Ito

Similarly to its arguments regarding Ito in combination with Kimura, which we discuss *supra* in Section II.F, Petitioner asserts that Ito discloses

semiconductor manufacture techniques with tungsten plugs, where removal of excess tungsten may be performed by etch-back technique or by CMP. Pet. 57 (citing Ex. 1116 ¶ 15). Petitioner contends that Kubo discloses that conductive plugs are formed on dielectric layers, and the conductor materials are planarized by etching the conductors back until the top surface of the dielectric layer 108 is exposed. *Id.* at 56 (citing Ex. 1112 ¶¶ 25, 30–32). Petitioner argues that “Ito teaches CMP is a better technique than etch-back, [and] Ito would motivate a worker of skill to replace Kubo’s etch-back technique with CMP planarization.” *Id.* at 57 (citing Ex. 1105 ¶ 289).

Notwithstanding Patent Owner’s contrary arguments, which we discuss below, we agree that Kubo and Ito teach every limitation of claim 12 of the ’933 patent and that there is sufficient rationale to combine the references, and we credit Dr. Neikirk’s supporting testimony (Ex. 1105 ¶¶ 285–289) on that point, as it is consistent with the prior art disclosures.

Patent Owner argues that Kubo does not disclose the multiple-layer interconnect structure requirement of claim 5, including disclosing forming a first layer interconnect using damascene techniques, and Petitioner does not provide any arguments that Ito fills the gap. PO Resp. 61. We do not agree with Patent Owner’s argument because it is based on Patent Owner’s proposed interpretation for the application of the term “damascene techniques,” we have not adopted. *See supra* Section II.B.

Thus, Petitioner has shown by a preponderance of the evidence that claim 12 of the ’933 patent is unpatentable as obvious over Kubo and Ito.

J. Alleged Anticipation by Yoshihara

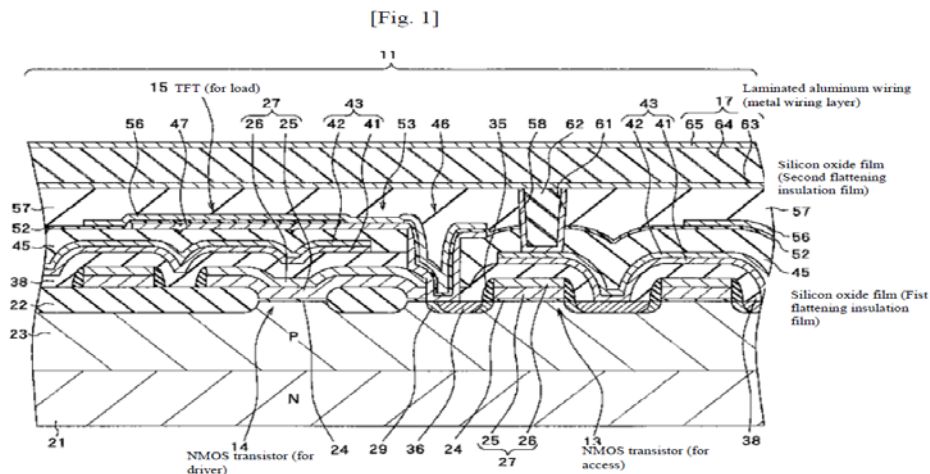
Petitioner contends that Yoshihara anticipates claims 5, 7, and 9–11. Pet. 69–79. To support its contentions, Petitioner provides explanations as

to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1105, 1121) to support its positions. Patent Owner counters that the Yoshihara does not anticipate the claims because it fails to disclose some claim limitations. PO Resp. 69–73. Patent Owner relies upon the Bottoms Declarations (Exs. 2001, 2013) to support its positions.

We begin our discussion with a brief summary of Yoshihara, and then we address the evidence, analysis, and arguments presented by the parties to the extent necessary.

1. Yoshihara (Ex. 1114)

Yoshihara discloses a method for manufacturing semiconductor memory devices. Ex. 1114 ¶ 1. Yoshihara discloses a cross-sectional view of the semiconductor device shown in Figure 1, as reproduced below. *Id.* ¶ 16, [Brief Description of the Figures].

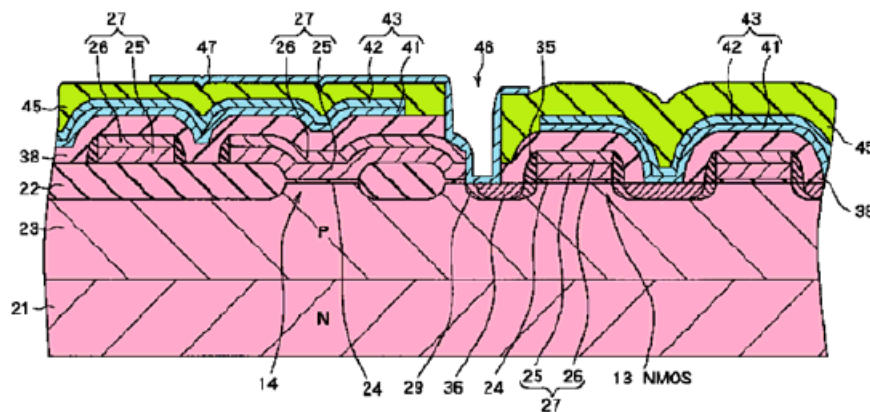


In Figure 1, silicon oxide layers 45 and 57 are depicted, as are poly side layer 43, poly layer crystal 47, which is a gate electrode formed on silicon oxide film 45, and silicon oxide films formed with a contact hole reaching to

the poly side layer 43, which is filled by titanium/titanium nitride layer 61 and tungsten layer 62. Ex. 1114 ¶¶ 18–23.

2. Analysis

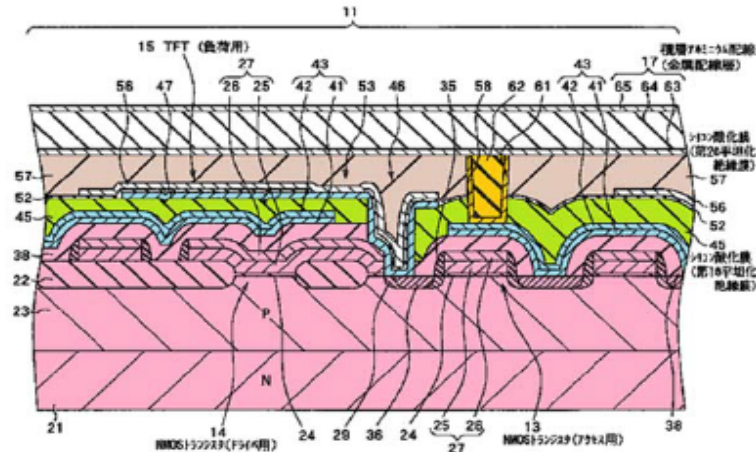
Petitioner presents evidence that Yoshihara discloses all the limitations of claims 5, 7, and 9–11. See Pet. 69–79. In particular, Petitioner relies upon annotated Figure 9, reproduced below. See *id.* at 72.



Ex. 1114, FIG. 9 (annotated)

Petitioner asserts, in part, that Yoshihara discloses first interconnect layer having a first dielectric layer (shown in green in annotated Figure 9), through which at least one first layer conductor 43, 47 (shown in blue) extends. Pet. 70. Patent Owner argues that although Petitioner asserts that the green and blue portions of Yoshihara are the first interconnect layer, there is no showing that there are any metal conductive interconnects in that layer as required under Petitioner’s proposed construction of the term “interconnect layer.” PO Resp. 71. More specifically, Patent Owner asserts that the blue layer is poly crystal silicon layer 47, not a metal. *Id.* (citing Ex. 2013 ¶ 159). In Reply, Petitioner acknowledges that conductors 43 and 47 are not metal conductors. Pet. Reply 16. Petitioner then argues in Reply

that Yoshihara's tungsten plug 62, as shown in orange in annotated Figure 1, reproduced below, extends through dielectric layer 45, so this structure of layer 45 with plug 62 would meet the construction of a first interconnect layer. *Id.*



Ex. 1013, FIG. 1 (annotated)

Annotated Figure 1 of Yoshihara depicts a cross-section of an embodiment of the invention. Pet. Reply 15.

We disregard Petitioner's new argument in Reply on the issue of Yoshihara's disclosure of a metal conductive interconnects in a first interconnect layer because it presents a new theory of unpatentability that exceeds the proper scope of a Reply under 37 C.F.R. § 42.23(b). "[A] reply that raises a new issue or belatedly presents evidence will not be considered" and "[e]xamples of indications that a new issue has been raised in a reply include new evidence necessary to make out a prima facie case for the . . . unpatentability of an original . . . claim, and new evidence that could have been presented in a prior filing." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012). We also do not consider this new contention because Patent Owner was not afforded notice and full

opportunity to respond to this new theory of unpatentability with briefing and evidence. *See generally Genzyme Therapeutic Prods. Ltd. v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1366–67 (Fed. Cir. 2016) (determining that the Administrative Procedure Act and due process require notice to a party and the opportunity to submit facts and argument); *see also Intelligent Bio–Ays. v. Illumina Cambridge, Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’”).

Petitioner does not allege that there were any new unforeseen circumstances that would have necessitated a change in its position based on Yoshihara. *See* Pet. Reply 14–16. Here, we have adopted Petitioner’s own proposed construction of “interconnect layer” as “an interlayer dielectric having metal conductive interconnects therein or therethrough,” so Petitioner could not assert that there was changed position based on unforeseen claim construction.¹² *See supra*, Section II.B. Further, in light of Yoshihara’s failure to disclose the claim 5 elements of a “first layer interconnect” and “first layer conductor,” the Petition failed to make out a *prima facie* case for anticipation because there is no showing that there are any metal conductors or metal conductive interconnects in the layer, and Petitioner’s Reply cannot be used to introduce new evidence to provide that support. Thus, the argument and evidence presented in the Petition is insufficient to support that Yoshihara anticipates claim 5 of the ’933 patent.

¹² In the Decision to Institute, we also adopted, on a preliminary basis, the same proposed construction provided by Petitioner. Dec. 10.

Claims 7 and 9–11 depend, directly or indirectly, from claim 5, and the Petition fails to remedy the deficiencies in the disclosures of the prior art for claim 5 with additional support from the evidence provided for claims 7 and 9–11. *See* Pet. 76–79.

Thus, we determine that Petitioner has not has shown by a preponderance of the evidence that claims 5, 7, and 9–11 are anticipated by Yoshihara.

K. Alleged Obviousness over Yoshihara and Admitted Prior Art

Petitioner contends that claims 6 and 12 would have been obvious over Yoshihara and Admitted Prior Art. Pet. 79–81. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration and Reply Declaration (Exs. 1105, 1121) to support its positions. Patent Owner counters that Yoshihara and Admitted Prior Art do not render claims 6 and 12 obvious because Petitioner relies on Admitted Prior Art to meet this planarization of the conductive material limitation, and fails to remedy the deficiencies of Yoshihara’s disclosures of the limitations of claim 5. PO Resp. 73.

We agree with Patent Owner that Petitioner’s reliance on Admitted Prior Art is limited to planarization of conductive plugs. Pet. 79–81. Claims 6 and 12 depend, directly or indirectly, from claim 5, and the Petition fails to remedy the deficiencies of Yoshihara for claim 5 with additional support from the evidence provided for claims 6 and 12.

Thus, we determine that Petitioner has not has shown by a preponderance of the evidence that claims 6 and 12 are obvious over Yoshihara and Admitted Prior Art.

*L. Alleged Obviousness Based Upon Admitted Prior Art
And Planarization References*

Petitioner contends that claims 5–12 would have been obvious over Admitted Prior Art and the CMP References, which are identified as Jang, Kimura, and Ito. Pet. 33–44. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration (Ex. 1105) to support its positions.

In the Institution Decision, we determined that because of the deficiencies under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a), Petitioner had not established a reasonable likelihood that it would prevail in showing that claims 5–12 were unpatentable. Dec. 13–16. Petitioner did not request rehearing on this issue. In Reply, Petitioner requests reconsideration of the denial of this ground.¹³ Pet. Reply. 16. Petitioner argues that its assertions based on the CMP References demonstrate that forming planarized dielectric layers was a well-known technique in semiconductor fields and solved a host of problems. *Id.* at 17. Petitioner contends that these techniques would have improved the structure of the Admitted Prior Art in the same way. *Id.* Petitioner argues that this ground should be reconsidered in light of *KSR*’s mandate that the interrelated teachings of the patents should be considered. *Id.* at 18 (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)). Petitioner alleges that “[c]laim 5 does not recite the various elements that Patent Owner attempts to import from the specification and the claim,” but that the art “describes many different advantages to be obtained by the

¹³ As discussed, *supra* Section I.A, this ground was subsequently instituted pursuant to SAS.

technique.” *Id.* at 18–19. Petitioner further argues that the ‘933 patent admits that all elements described by claim 5 are disclosed by the prior art, with the exception of planarization. *Id.* at 19. Petitioner alleges that because the planarization references are redundant, a person of ordinary skill in the art would have considered it obvious to planarize a second dielectric layer and apply this to the structure of the Admitted Prior Art. *Id.*

Patent Owner counters that the Petition lacks required sufficiency and particularity, and even if this challenge were considered, the prior art fails to teach some of the claim limitations. PO Resp. 32–52. Patent Owner relies upon the Bottoms Declarations (Exs. 2001, 2013) to support its positions.

Patent Owner asserts that the Board correctly determined that this ground was legally deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a), and there is no need for the Board to reconsider its initial determination on this issue. PO Resp. 32–33. Patent Owner argues that 35 U.S.C. § 312(a)(3) states that a petition may only be considered if it identifies the grounds and evidence with particularity. *Id.* at 33.

Patent Owner argues that Petitioner cites unrelated teachings of Jang, Kimura, and Ito, and fails to identify which of these teachings is to be relied on. PO Resp. 34. Patent Owner further argues that, to the extent that the teachings should be combined, Petitioner fails to identify how the combined references teach more than each individual reference. *Id.* Patent Owner also argues that grounds should be denied “when Petitioners fail to articulate with reasonable clarity what specific elements from each of the references is to be combined, and in what manner, to meet each limitation of the claims.” *Id.* at 33. Moreover, Patent Owner asserts that each reference has unique teachings and rather than explaining the significance of specific facts for

each reference, Petitioner “improperly pile the references together.” *Id.* at 34. Patent Owner contends that this improperly imposes a burden upon the Patent Owner and the Board. *Id.*

By statute, a Petition is required to identify “with particularity[] the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge.” 35 U.S.C. § 312(a)(3). The Petition shall also include “a full statement” with “a detailed explanation of the significance of the evidence, including material facts.” 37 C.F.R. § 42.22(a). Although *KSR* applies to an obviousness evaluation, a Petition must nonetheless meet the requirements of the statute and rules.

As we discussed in the Institution Decision, we found that the Petition was deficient in presenting its challenge and the evidence with particularity for this ground. Dec. 13–16. As discussed, Petitioner mixed and matched references in the claim charts, and, particularly mixed and matched some of the prior art references identified as the CMP References. *Id.* at 14–16 (citing Pet. 33–37). Dr. Neikirk did not testify in support of the teachings of specific references in the claim charts, but rather only referred to the grouping of prior art, identifying the group globally as “Planarization References.” *Id.* at 16 (citing Ex. 1105 § VIII.F). Petitioner failed to articulate, with reasonable clarity, what specific elements from the individual CMP References were combined with the specific elements of the other CMP References to meet the limitations of independent claim 5. *Id.* The Institution Decision also stated that, to the extent that the reference to “Jang, Kimura, and Ito” (Pet. 33), was intended to denote that all the named prior art should be considered for teaching the same limitation, it was unclear why Petitioner included all these references to the extent that they

teach the same limitation. Dec. 15. Here, we reiterate, for the same reasons discussed in the Institution Decision, that Petitioner’s assertions lack required particularity.

Moreover, the Institution Decision determined that the rationale for the proposed combination(s) also lacked specificity and sufficient support. Dec. 15–16. The Institution Decision referred to Petitioner’s assertion that “Jang ‘states that formation of interconnection studs within planarized insulator layers have gained wide acceptance, and discloses thicknesses within the ranges identified in claims 8 and 9.’” *Id.* at 15 (citing Pet. 29). Petitioner also contended that Kimura explains “that planarization of interconnect layers is needed to satisfy focus requirements of photolithography processes,” and Ito’s planarization of insulation layers “helps achieve desired anti-reflection properties.” *Id.* (citing Pet. 29). Petitioner argued that the “collection of prior art” offers advantages such that one of skill in the art would have reason to have reason to adopt “each of the planarization techniques described,” and one of skill also would have been “keenly interested” in planarization techniques. *Id.* at 15–16 (citing Pet. 29–30). The Institution Decision determined that the stated basis lacked required particularity and specificity of a rationale to combine. *See id.* at 16. The Institution Decision also determined that it was unclear whether the rationale to combine was based on some form of a composite rationale based upon all of the CMP References, that is, Jang, Kimura, and Ito, or whether it was based upon each of the CMP References’ alleged rationale individually presented as alternative bases. *Id.* Here, we reiterate, for the same reasons expressed in the Institution Decision, that these assertions lack required particularity.

Thus, consistent with the Institution Decision and for the reasons expressed therein and reiterated herein, we determine that the Petition's obviousness ground is deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a). Therefore, Petitioner has not has shown by a preponderance of the evidence that claims 5–12 are obvious over Admitted Prior Art and the CMP References.

III. CONCLUSION

For the foregoing reasons, we conclude Petitioner has demonstrated by a preponderance of the evidence, that claims 5–12 of the '933 patent are unpatentable based on the following grounds: (1) anticipation of claims 5–8, 10, and 11 by Kubo under § 102(b); (2) obviousness of claim 9 over Kubo and Jang under § 103(a); (3) obviousness of claim 12 over Kubo and Ito under § 103(a); (4) anticipation of claims 5–8, 10, and 11 by Kimura under § 102(e); (5) obviousness of claim 9 over Kimura and Jang under § 103(a); and (6) obviousness of claim 12 over Kimura and Ito under § 103(a).

IV. ORDER

Accordingly, it is

ORDERED that claims 5–12 of the '933 patent are determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-02123
Patent 6,153,933

PETITIONER:

Robert L. Hails
Michael J. Riesen
Theresa M. Weisenberger
BAKER HOSTETLER LLP
rhails@bakerlaw.com
mriesen@bakerlaw.com
tweisenberger@bakerlaw.com

PATENT OWNER:

Nicholas T. Peters
David A. Gosse
Timothy P. Maloney
FITCH, EVEN, TABIN & FLANNERY LLP
ntpete@fitcheven.com
dgosse@fitcheven.com
tim@fitcheven.com