

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION and
RENESAS ELECTRONICS AMERICA INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

IPR2017-02124
Patent 6,046,089

Before GRACE KARAFFA OBERMANN, KEVIN C. TROCK, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1 and 5 of U.S. Patent No. 6,046,089 (Ex. 1001, “the ’089 patent”) are unpatentable.

A. Background

Renesas Electronics Corporation and Renesas Electronics America Inc. (collectively, “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–3 and 5 of the ’089 patent pursuant to 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Petitioner also filed the supporting Declaration of Dean Neikirk, Ph.D. (Ex. 1004) (“Neikirk Declaration”). Pursuant to 35 U.S.C. § 314(a), on April 6, 2018, we instituted *inter partes* review on the following grounds:

whether claims 1 and 5 would have been anticipated under § 102(b) by Yamanaka¹;

whether claims 1 and 5 would have been anticipated under § 102(b) by Mitsui²; and

whether claims 1 and 5 as would have been rendered obvious under § 103(a) over the combined teachings of Urabe³, Yamanaka, and Mitsui.

¹ Japanese Unexamined Patent Application Publication No. H08-130306, published May 21, 1996 (Ex. 1005). We refer to the English translation (Ex. 1006) of the original reference herein.

² U.S. Patent No. 5,296,401, issued March 22, 1994 (Ex. 1009).

See Paper 6 (“Inst. Dec.” or “Dec.”).

In the Institution Decision, we declined to institute on the ground of anticipation of claim 2 by Yamanaka or by Mitsui. Dec. 14, 18–19. We declined to institute on the ground of obviousness of claim 2 over the combination of Urabe, Yamanaka, and Mitsui. *Id.* at 24. We also declined to institute on the ground that claim 3 would have been obvious under 35 U.S.C. § 103(a) in view of “Spacer Art”⁴ and “RTA Art”⁵ because we found that the Petition was deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a). *Id.* at 25–27.

On April 24, 2018, the Supreme Court held that a final written decision in an *inter partes* review must decide the patentability of all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (“SAS”). Pursuant to SAS, on May 3, 2018, we instituted *inter partes* review on all claims and all grounds. Paper 8.

Patent Owner did not file a Patent Owner Response. Petitioner filed a Supplemental Claim Construction Brief (Paper 22) (“Pet. Supp. Br.”), and

³ Japanese Unexamined Patent Application Publication No. No. H07-176729, published July 14, 1995 (Ex. 1007). We refer to the English translation (Ex. 1008) of the original reference herein.

⁴ The Petition identifies “Spacer Art” as “Yamanaka, Mitsui, and Urabe.” Pet. 11, *see also id.* at 68–69.

⁵ The Petition identifies “RTA Art” (Rapid Thermal Anneal Art) as “Vasudev, Hayden 2, Grim, and Rodder.” Pet. 17. “Vasudev” is U.S. Patent No. 4,617,066, issued October 14, 1986 (Ex. 1013). “Hayden 2” is U.S. Patent No. 5,407,847, issued April 18, 1995 (Ex. 1014). “Grim” is U.S. Patent No. 5,011,794, issued April 30, 1991 (Ex. 1015). “Rodder” is European Patent Application No. EP 0 776 034 A2, published May 28, 1997 (Ex. 1016).

Patent Owner filed a Response to Petitioners' Supplemental Claim Construction Brief (Paper 23 ("PO Supp. Resp. Br.")).

An oral hearing was held on December 17, 2018. A transcript of the hearing is included in the record. Paper 28 ("Tr.").⁶

B. Related Proceedings

The parties indicate that the '089 patent is asserted in *Lone Star Silicon Innovations, LLC v. Renesas Electronics Corp.*, C.A. No. 3:17-cv-03981 (N.D. Cal.). Pet. 2; Paper 3, 2. Patent Owner indicates that several petitions for *inter partes* reviews have been filed by Petitioner against patents owned by Lone Star, but it appears that no other pending review involves the '089 patent. Paper 3, 1–2.

C. The '089 Patent

The '089 patent is entitled "Selectively Sized Spacers" and issued on April 4, 2000 from an application filed on January 5, 1998. Ex. 1001, [22], [45], [54].

The '089 patent is directed generally to formation of selectively sized spacers in integrated circuit manufacturing. Ex. 1001, 1:4–6, 1:63–64. Maximizing performance of gate transistors can be achieved by etching of spacers for specific geometries of gates. *Id.* at 2:11–20. Figure 1D, reproduced below, depicts a cross-section of an insulated-gated field-effect transistor ("IGFET") having selectively sized spacers. *Id.* at 2:39–42.

⁶ A separate hearing for unrelated Cases IPR2017-01989 and IPR2017-02123 was conducted on the same day.

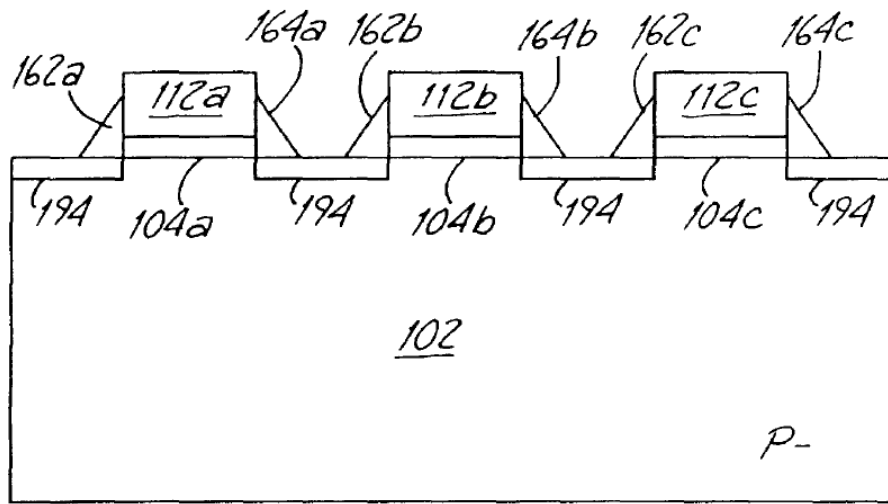


Fig. 1D

Figure 1D depicts substrate 102; polysilicon gates 112a, 112b, and 112c; gate oxide 104a, 104b, and 104c; lightly doped regions 194; and spacers 162a, 162b, 162c, 164a, 164b, and 164c are formed. Ex. 1001, 3:23–25, 3:57–65, 4:8–9. Figure 1E, reproduced below, depicts the application of mask 192 over gate 112a, including associated spacer 162a and 164a. *Id.* at 4: 22–23.

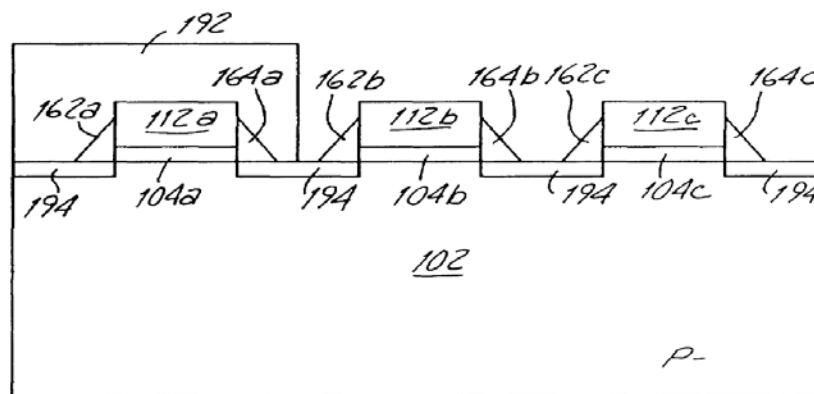


Fig. 1E

Figure 1E depicts mask 192 placed over gate 112a. The top of the structure shown in Figure 1E is then etched, resulting in selective etching from gates

112b and 112c and their associated spacers. Ex. 1001, 4:22–28. Figure 1F, reproduced below, illustrates the results of etching.

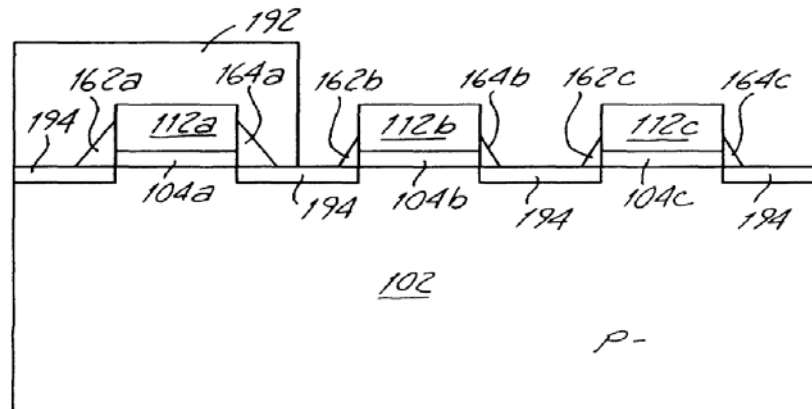
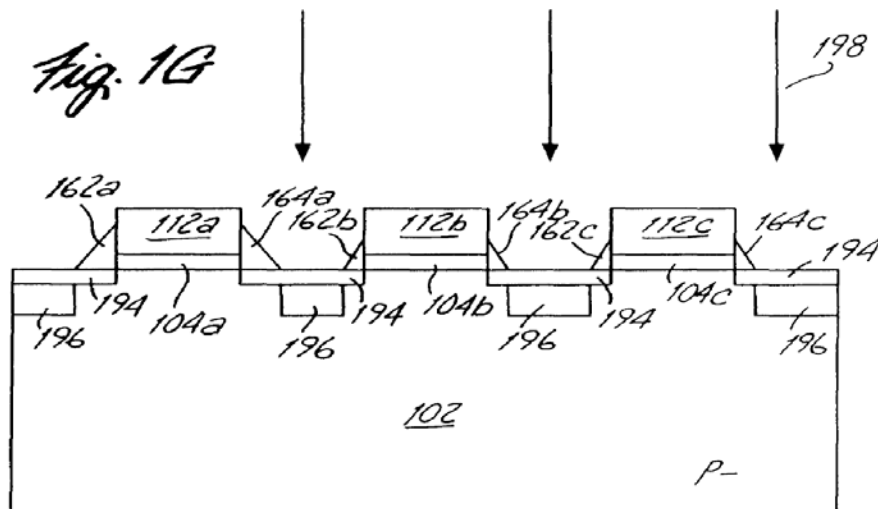


Fig. 1F

Figure 1F depicts spacers 162b and 164b, associated with gate 112b, and spacers 162c and 164c, associated with gate 112c, that have been anisotropically etched to reduce their profiles and to reduce their length. Ex. 1001, 4:31–35. Regions of the substrate may be subject to additional doping as shown in Figure 1G below.



As depicted in Figure 1G, highly doped regions 196 are introduced in substrate 102 by subjecting the structure to ion implantation as indicated by

arrows 198. Ex. 1001, 4:36–39. Polysilicon gates 112a, 112b, and 112c provide an implant mask for substrate 102. *Id.* at 4:40–42. Although highly doped regions 196 are depicted as distinct from lightly doped regions 194, “as those of ordinary skill in the art can appreciate, in reality, regions 194 and 196 are intermingled.” *Id.* at 4:42–46.

Claims 1 and 2 of the ’089 patent are reproduced below.

1. A method for forming a device comprising:
 - forming at least one spacer adjacent to an edge of each of a plurality of gates on a substrate, the plurality of gates including a first gate and at least one remaining gate;
 - applying a mask to the first gate, including at least a portion of said at least one spacer for the first gate;
 - etching and therein sizing said at least one spacer for each of the at least one remaining gate into a geometry that is smaller than the at least one spacer for the first gate;
 - removing the mask from the first gate; and
 - applying an ion implantation and forming a highly doped region within the substrate adjacent to the sized at least one spacer.
2. The method of claim 1, wherein applying an ion implantation and forming a highly doped region further includes forming a lightly doped region within the substrate underneath each spacer.

Ex. 1001, 5:43–59.

II. ANALYSIS

A. The Parties’ Post-Institution Arguments

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that

claims 1 and 5 of the '089 patent would have been unpatentable under 35 U.S.C. § 102 and/or § 103 over the asserted prior art. Dec. 7–36. We now determine whether Petitioner has established by a preponderance of the evidence that claims 1–3 and 5 are unpatentable. We previously instructed Patent Owner “that any arguments concerning patentability not raised in the response will be deemed waived.” Paper 7, 3; *see also* 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

As discussed above, Patent Owner declined to file a Patent Owner Response. With the record now complete, we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions. In this regard, the record contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which some of the asserted prior art discloses or teaches corresponding limitations of claims 1 and 5. Based on the preponderance of the evidence before us, we conclude that some of the prior art identified by Petitioner discloses or teaches all of the limitations of claims 1 and 5 of the '089 patent.

B. Claim Construction

In the Petition, Petitioner contended that the '089 patent would expire before an *inter partes* review would reach a final written decision. Pet. 10.

Petitioner, therefore, asserted that a district-court type claim construction should be used. *Id.* (citing 37 C.F.R. § 42.100(b)). In its Supplemental Claim Construction Brief, Petitioner reiterates that *Phillips*-type claim construction should be used. *See* Supp. Pet. Br. 3. Patent Owner also relies upon district-court type claim construction. PO Supp. Resp. Br. 3–4. We note that the filing date of the patent is January 5, 1998, therefore, it appears that the patent has expired. Accordingly, we will use district-court type construction for the claims of this patent.

Our review of the claims of an expired patent is similar to that of a district court’s review. *Wasica Finance GmbH v. Continental Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017). Because the expired claims of a patent are not subject to amendment, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)), that “words of a claim ‘are generally given their ordinary and customary meaning,’” as would be understood by a person of ordinary skill in the art in question at the time of the invention. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

The only claim construction in dispute is for the claim 2 term “wherein applying an ion implantation and forming a highly doped region further includes forming a lightly doped region within the substrate underneath each spacer” as it relates to the claim 1 “high[] dop[ing]” step, that is, the step of

“applying an ion implantation and forming a highly doped region.” Pet. 10, Pet. Supp. Br. 1–5; PO Supp. Resp. Br. 1–5. Petitioner argues that claims 1 and 2 would “permit[] intervening manufacturing steps to occur between the formation of the lightly doped region(s) and the formation of the highly doped region(s).” Pet. 10–11 (citing Ex. 1004 § IV.A; Ex. 1001 at 3:65–4:7, 5:56–59, Figs. 1C–1G; Ex. 1012 at 86). In support of its construction, Petitioner relies on the Neikirk Declaration (Ex. 1004) and portions of the ’089 patent specification (the “specification”). *See id.* Dr. Neikirk testifies that “a person of ordinary skill in the art as of January 5, 1998, would understand that intervening steps may separate the formation of the lightly doped region from the formation of the highly doped region, as is described in the specification.” Ex. 1004 ¶ 31. Dr. Neikirk identifies portions of the specification that describe a light doping step followed by a heavy doping step. *Id.* Dr. Neikirk further testifies that “[t]he ’089 Patent has no disclosure to suggest that the lightly doped regions and the highly doped regions are formed in a continuous, uninterrupted operation.” *Id.* ¶ 32.

Petitioner also argues that under legal precedent the use of “includes” does not foreclose intervening steps. Pet. Supp. Br. 1. Petitioner refers to cases that support that the term “includes” means “comprising,” where other elements may be added within the scope of the claim. *Id.* at 2–3. Petitioner asserts that under *Phillips*-type construction the Board should look to the intrinsic evidence of the record and extrinsic evidence in the form of dictionaries, and expert testimony can also be considered, and further argues that unrebutted evidence supports that the “further includes” language of claim 2 allows for intervening manufacturing steps. *Id.* at 3–4. More

specifically, Petitioner refers to the specification's description of the steps of forming the lightly doped and highly doped regions as discrete operations that are separated by several intervening steps. *Id.* at 4; *see also* Pet. 7–8. Petitioner argues that “a claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct.” *Id.* at 4–5 (citing *Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F.3d 1318, 1326 (Fed. Cir. 2013)). Petitioner also refers to Dr. Neikirk's testimony regarding the embodiment in the specification as well as a contemporaneous dictionary definition that defines “lightly doped drain” as “a reduced doping of the drain region in very small geometry MOS/CMOS transistor,” the “implementation” of which includes “moderate implant before spacer formation, heavy implant after spacer formation.” *Id.* at 5 (citing Ex. 1004 ¶¶ 31–33 (quoting Ex. 1012, 86)).

Patent Owner argues that claim 1 recites ordered steps and the limitations recited in claim 2 must be performed within the order recited in claim 1. PO Supp. Resp. Br. 1. Patent Owner asserts that a method claim requires an ordering of steps when claim language, as a matter of logic or grammar, requires that the steps be performed as literally written. Patent Owner argues that under that the claim 1 and 2 language the method requires applying ion implementation after the spacer has been sized by the etching step. *Id.* at 2–3. Patent Owner also argues that the originally filed claims support two different methods of forming the lightly doped region, referencing claim 2 as originally filed, which recites that the same ion implantation step forms both the highly doped region and the lightly doped region. *Id.* at 4 (citing Ex. 1003, 26). Patent Owner contrasts and

differentiates this with claim 6, as originally filed, which recites that lightly doping is performed prior to forming the spacer. *Id.* at 5.

We agree with Patent Owner that a claim “requires an ordering of steps when the claim language, as a matter of logic or grammar, requires that the steps be performed in the order written, or the specification directly or implicitly requires” an order of steps. *TALtech Ltd. v. Esquel Apparel, Inc.*, 279 Fed. Appx. 974, 978 (Fed. Cir. 2008); *see also Function Media, LLC v. Google, Inc.*, 708 F.3d 1310, 1320 (Fed. Cir. 2013) (concluding that a claim that recites “processing” an “electronic advertisement” necessarily indicates that “the creation of the ad must happen before the processing begins”).

Claim 2 recites “[t]he method of claim 1, *wherein applying an ion implantation and forming a highly doped region further includes forming a lightly doped region within the substrate underneath each spacer.*” Ex. 1001, 5:56–59 (emphasis added). Claim 1 includes an “ion implementation and forming a highly doped region” step. Applying grammatical conventions, the proper reading of the limitation of claim 2 would be that the step of applying an ion implantation and forming a highly doped region would further include forming a lightly doped region, that is, where lightly doping would be done with the highly doping step. We note also that applying an ion implantation and forming a highly doped region is performed “adjacent to the sized at least one spacer,” which indicates that the ion implantation would occur after the “sizing,” that is, the result of the masking and etching steps of claim 1.

We note, however, that a literal reading of the claim 2 step would appear to be at odds with the disclosure of the embodiment of the specification, which, as Petitioner argues, only discloses a light doping step

followed by a heavy doping step. *See* Pet. Supp. Br. 3–4. We agree with Petitioner that “there is a strong presumption against a claim construction that excludes a disclosed embodiment.” *See In re Katz Interactive Call Processing Patent Litig.*, 639 F.3d 1303, 1324 (Fed. Cir. 2011). However, the Federal Circuit has also “expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment.” *Phillips*, 415 F.3d at 1323 (citing *Gemstar-TV Guide Int’l, Inc. v. ITC*, 383 F.3d 1352, 1366 (Fed. Cir. 2004)). In this instance, the prosecution history shows that the originally filed claims included different recited steps for the respective high and low doping. Reproduced below is a copy of page 8 of the prosecution history, which includes some of the original claims that were part of the original application. Ex. 1003, 26.

- We claim:
1. A method for forming a device comprising:
forming at least one spacer for each of a plurality of gates on a substrate, the plurality of gates including a first gate and at least one remaining gate, each spacer adjacent to an edge of the gate;
applying a mask to the first gate, including the at least one spacer for the first gate;
etching the at least one spacer for each of the at least one remaining gate; and,
removing the mask from the first gate, including from the at least one spacer for the first gate.
 2. The method of claim 1, further comprising applying an ion implantation to form a highly doped region within the substrate adjacent to each spacer.
 3. The method of claim 2, wherein applying an ion implantation further forms a lightly doped region within the substrate underneath each spacer.
 4. The method of claim 2, further comprising applying a rapid thermal anneal (RTA) to cure the ion implantation.
 5. The method of claim 2, further comprising forming a metal silicide within the substrate adjacent to each spacer.
 6. The method of claim 1, further comprising, prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation to form a lightly doped region within the substrate adjacent to each edge of each gate.
 7. The method of claim 1, wherein each spacer has a triangular geometry.
 8. The method of claim 1, wherein forming at least one spacer comprises using a high-

As shown in the reproduction of originally filed claims above, originally filed claim 1 includes steps for forming and etching spacers and claims 2 and 3 recite “applying an ion implantation to form a highly doped region within the substrate adjacent to each spacer” and “applying an ion implantation further forms a lightly doped region within the substrate underneath each spacer.” Ex. 1003, 26. Originally-filed claim 6 discloses “[t]he method of claim 1,” where “prior to forming at least one spacer for each . . . gate . . . , applying an ion implementation to form a lightly doped

region within the substrate adjacent to each edge of each gate.”⁷ *Id.* Thus, under a literal reading, the originally filed claims support a method where the lightly doping step is applied prior to forming the spacers (claim 6), and also support a method that would include the circumstance where ion implantation includes the steps of highly doping and lightly doping, and those steps occur after the spacers are formed (claims 2 and 3). Because the originally filed claims are part of the original filed disclosure, this bolsters support of a literal grammatical reading of claim 2, which is that the step of applying an ion implantation and forming a highly doped region would further include forming a lightly doped region, that is, where lightly doping would be done with the highly doping step. *See In re Anderson*, 471 F.2d 1237, 1238–39 (CCPA 1973) (An original claim is part of the disclosure at the time of filing.).

Moreover, interpreting claim 2 as limited to the embodiment in the specification, as Petitioner advocates, would be inconsistent with the principle of claim differentiation with respect to issued claim 5. Claim 5 includes similar steps to claim 1, with the last additional recitation of “prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation and forming a lightly doped region within the substrate adjacent to each edge of each gates.” *See Ex. 1001*, 6:10–13. If we were to interpret claim 2 as Petitioner advocates to conform to only the embodiment of the specification, this would result in claim 2 being interpreted so that it is essentially the same as claim 5, which would

⁷ Original claim 3 was amended and issued as claim 2, the dependent claim at issue. *Ex. 1003*, 61. Original dependent claim 6 was amended and issued as independent claim 5. *Id.*

impermissibly render one of the claims superfluous. *See Free Motion Fitness, Inc. v. Cybex Int’l, Inc.*, 423 F.3d 1343, 1351 (Fed. Cir. 2005).

For the reasons discussed above, we determine that the grammatically correct application of the wording of claims 1 and 2 should be applied, and this interpretation is supported by the intrinsic record. *Phillips*, 415 F.3d at 1317. We interpret the step of claim 2 to mean that applying ion implantation and forming a highly doped region further includes forming a lightly doped region, that is, where lightly doping would be done with the highly doping step.

Other Terms

We determine that no other claim term requires an express construction for the purposes of this Decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

C. Level of Ordinary Skill in the Art

Petitioner’s expert, Dr. Neikirk, testifies that a person of ordinary skill in the art at the time of the claimed invention “would have had a graduate’s degree with some emphasis in semiconductor device fabrication in physics, material science, electrical engineering, or a related degree, or an undergraduate degree in one of these fields and two to three years’ experience in semiconductor device design and fabrication,” as well as having “at least a basic understanding, through education or experience, of interconnect structures and techniques for making them.” Ex. 1004 ¶ 22; *see also* Pet. 9–10.

Patent Owner provides no proposed qualifications for one of ordinary skill in the art. *See* PO Supp. Resp. Br. 1–5.

We adopt Petitioner’s proposed qualifications. In addition, we note that the primary art of record in this proceeding—namely, Yamanaka, Mitsui, and Urabe—is indicative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Further, neither party argues that adoption of different proposed qualifications would change the outcome of this case.

D. Alleged Anticipation by Yamanaka

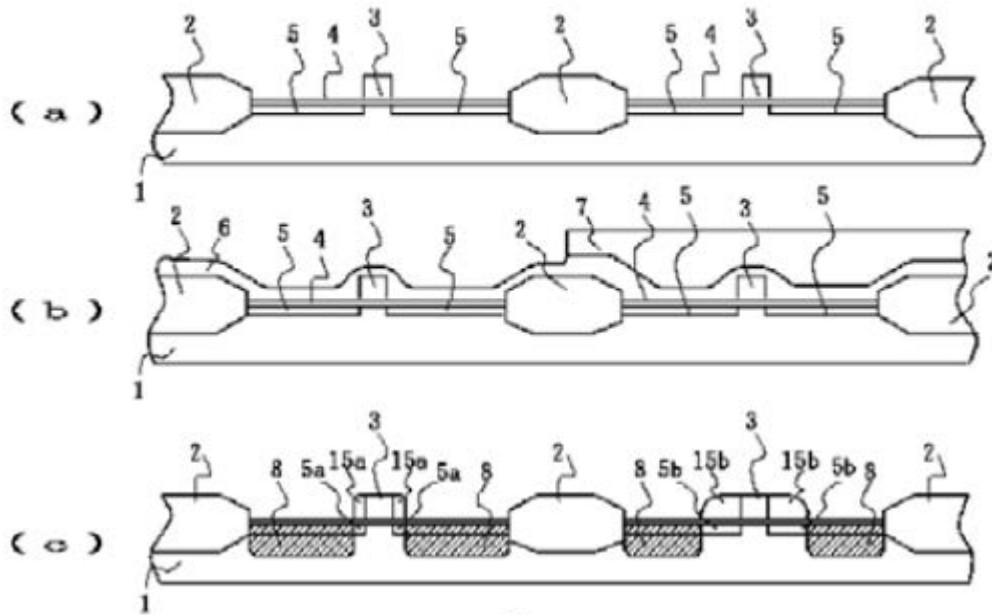
Petitioner contends that Yamanaka anticipates claims 1, 2, and 5. Pet. 21–36. To support its contentions, Petitioner provides explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration (Ex. 1004) to support its positions.

We begin our discussion with a brief summary of Yamanaka, and then address the evidence and arguments presented.

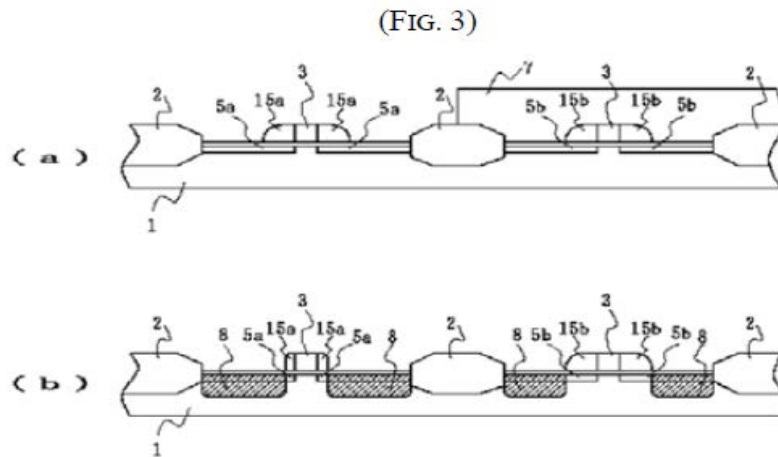
1. Yamanaka (Ex. 1006)

Yamanaka is directed to a method for semiconductor device manufacture that includes changing the length of low-density diffusion layers associated with transistors. Ex. 1006 ¶¶ 3, 4, Abstract. More specifically, Yamanaka discloses manufacturing methods that include forming gate electrodes, then ion-implanting to form a first diffusion layer with the gate electrodes acting as a mask. *Id.* ¶ 20. Figure 1a–c, reproduced below, are cross-sections of Yamanaka showing manufacturing processes for semiconductor devices:

(FIG. 1)



As shown in Figure 1(c), gate oxide film is formed, with doping, and gate electrode 3 is formed by photoetching. Ex. 1006 ¶ 20. Ion implanting is done relative to substrate 1 to form a first diffusion region 5 to serve as the drain/source region of transistors. *Id.* ¶ 22. This manufacturing method allows the formation of transistors having a lightly doped drain (LDD) structure, with low-density diffusion regions, 5a and 5b, having different widths between the transistors. *Id.* ¶¶ 1, 24. Figures 3(a) and 3(b) are reproduced below.



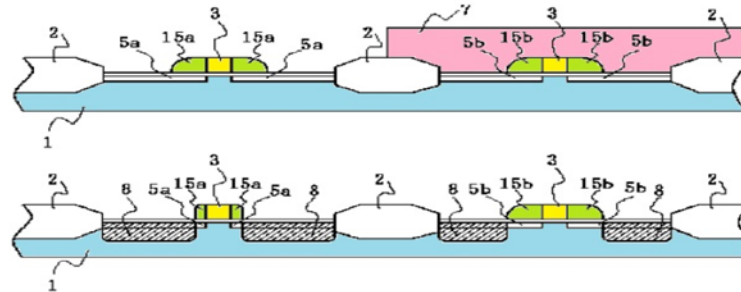
As depicted in Figure 3(a), photoresist 7 is formed over gate electrode 3 and low density diffusion areas 5b and side wall oxide film 15b. Ex. 1006 ¶¶ 24, 27, 31. Further etching is done forming thin side wall oxide fill 15a. *Id.* ¶ 31.

2. Analysis

a. Claim 1

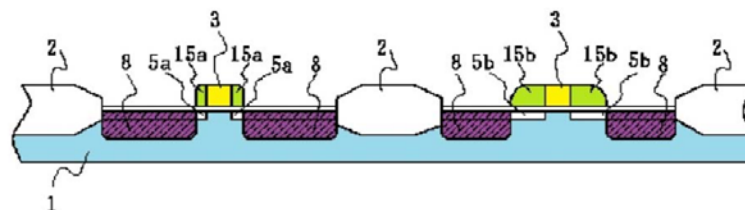
A claim is unpatentable under 35 U.S.C. § 102 if a prior art reference discloses each and every element of the claimed invention, either explicitly or inherently. *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir. 1995); see *MEHL/Biophile Int'l Corp. v. Milgram*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (“To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, . . .”; any limitation not explicitly taught must be inherently taught and would be so understood by a person experienced in the field.); *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991) (the dispositive question is “whether one skilled in the art would reasonably understand or infer” that a reference teaches or discloses all of the elements of the claimed invention).

Petitioner asserts that Yamanaka discloses every limitation of claim 1. Pet. 21–27. Annotated Figures 3(a) and 3(b) are reproduced below.



Ex. 1006, FIGS. 3(a), 3(b) (annotated)

As depicted in annotated Figures 3(a) and 3(b), Petitioner asserts, and we agree, that Yamanaka discloses forming at least one spacer (shown in green) adjacent to an edge of each of gates (shown in yellow) on a substrate (shown in blue), and the gates include a first gate and at least one remaining gate. Pet. 21–22. Petitioner asserts, and we concur, that the claimed “mask” to element 7, shown in pink, is applied to the “first gate,” shown in yellow (element 3), that includes at least one spacer. *Id.* at 23–24. Petitioner asserts, and we agree, that Yamanaka discloses “sizing least one spacer for each of the at least one remaining gate into a geometry that is smaller than the at least one spacer for the first gate,” by an etching process, along with mask removal, as disclosed and as shown in annotated Figures 3(a) and 3(b). *Id.* at 23–35 (citing, *inter alia*, Ex. 1006 ¶¶ 21, 22, 31). Petitioner refers to another version of annotated Figure 3(b), reproduced below.



Ex. 1006, FIG. 3(b) (annotated)

In annotated Figure 3(b), Petitioner further asserts, and we agree, that regions 8, that is, second diffusion areas, shown in purple, are areas within substrate 1 which have been subjected to additional implantation of high-density impurity, and Petitioner relies upon this disclosure for teaching the step of “applying an ion implantation and forming a highly doped region.” Pet. 25–27 (citing, *inter alia*, Ex. 1006 ¶¶ 3, 13, 22, 31).

Patent Owner waived opposition to this challenge to claim 1. See Paper 20, 2.⁸

We agree with Petitioner that Yamanaka discloses every limitation of claim 1 of the '089 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1004 ¶¶ 72–99), as it is consistent with the prior art disclosures.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 1 of the '089 patent is anticipated by Yamanaka.

b. Claim 2

Claim 2 depends from claim 1, and additionally recites “wherein applying an ion implantation and forming a highly doped region further includes forming a lightly doped region within the substrate underneath each spacer.” Ex. 1001, 5:56–59. As the basis of its anticipation challenge to claim 2, Petitioner relies solely on its proposed claim construction and on Yamanaka's disclosure wherein the step of forming a lightly doped region is performed in an earlier separate step from the step of forming a highly doped regions. Pet. 27–28; Ex. 1004 ¶¶ 104–108. As discussed, *supra* Section

⁸ The September 4, 2018 Order notes Patent Owner's acknowledgment of waiver of challenges to claims 1 and 5 of the '089 patent.

II.B, we do not adopt Petitioner's proposed claim construction for claim 2, which would permit intervening manufacturing steps to occur between the formation of the lightly doped regions and the formation of the highly doped regions. Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 2 of the '089 patent is anticipated by Yamanaka.

c. Claim 5

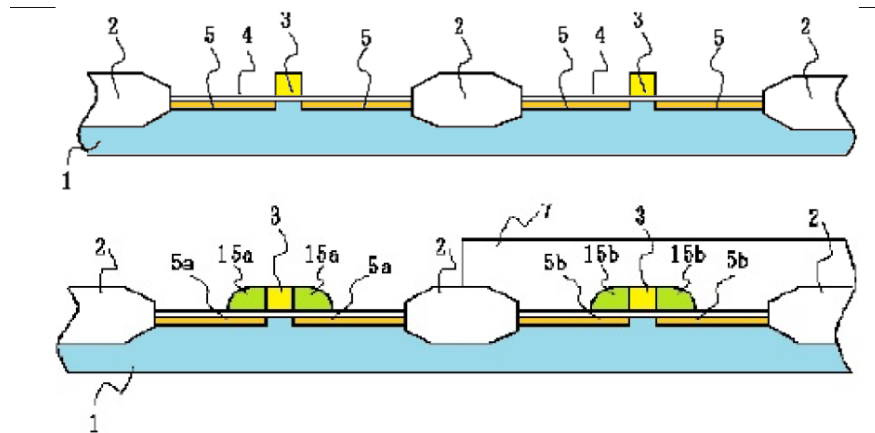
Claim 5 is a method claim that has similar steps to claim 1, however, the final two steps which differ are

removing the mask from the first gate; and applying an ion implantation and forming a highly doped region within the substrate adjacent to the sized at least one spacer; and

prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation and forming a lightly doped region within the substrate adjacent to each edge of each gate.

Ex. 1001, 6:6–13.

We agree with Petitioner that Yamanaka discloses the claim 5 steps that are similar to claim 1 for the reasons discussed above. *See* Pet. 29–34; *see also* Ex. 1004 ¶¶ 120–146. Petitioner also asserts, and we agree, that Yamanaka discloses that the step of applying ion implantation and forming the lightly doped region is performed prior to spacer formation. Pet. 34–36, Ex. 1004 ¶¶ 147–153. This is depicted in annotated Figures 3(a) and 3(b) reproduced below.



Ex. 1006, FIGS. 3(a), (b) (annotated)

As depicted in annotated Figures 3(a) and 3(b), Yamanaka discloses, prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation and forming a lightly doped region (with first diffusion region shown in orange) within the substrate (shown in blue) in a location adjacent to each edge of each gate (shown in yellow). Pet. 34–35 (citing Ex. 1006 ¶ 3).

Patent Owner waived opposition to this challenge to claim 5. See Paper 20, 2.

We agree with Petitioner that Yamanaka discloses every limitation of claim 5 of the '089 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1004 ¶¶ 119–153), as it is consistent with the prior art disclosures.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 5 of the '089 patent is anticipated by Yamanaka.

E. Alleged Anticipation by Mitsui

Petitioner contends that Mitsui anticipates claims 1, 2, and 5. Pet. 36–50. To support its contentions, Petitioner provides explanations as to how

the prior art discloses each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration (Ex. 1004) to support its positions.

We begin our discussion with a brief summary of Mitsui, and then address the evidence and arguments presented.

1. Mitsui (Ex. 1009)

Mitsui is directed to a semiconductor device including two metal oxide semiconductor field-effect transistors (“MOSFETs”) on a single substrate, each MOSFET having sidewall spacers that act as masks for forming impurity regions within the substrate. Ex. 1009, Abstract. Figures 2A, 2G, and 2H of Mitsui are reproduced below.

FIG.2A

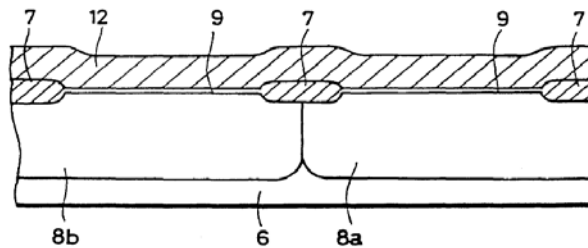


FIG. 2G

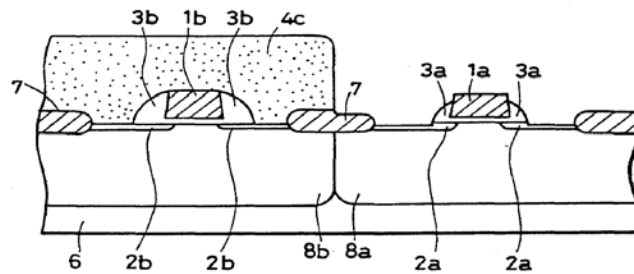


FIG. 2H

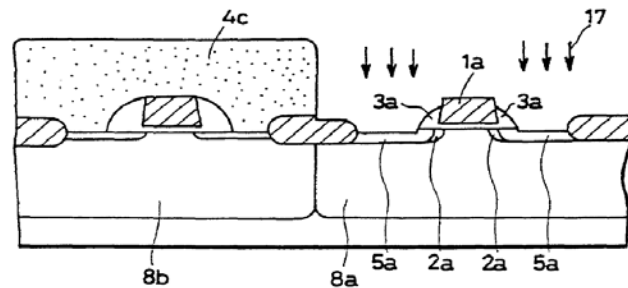
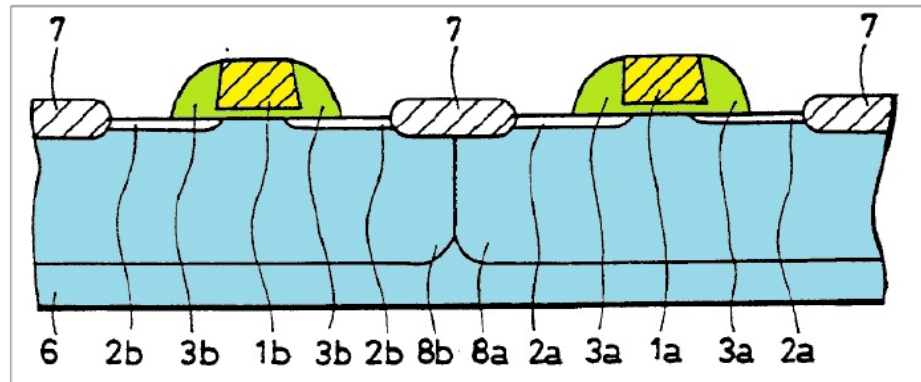


Figure 2A depicts substrate 6, with the formation of gate electrode in p-well region 8a and second gate electrode in n-well region 8b of the substrate, and with thin gate insulating film 9 and polysilicon layer 12 shown. Ex. 1009, 8:4–6, 8:15–19, 8:67–9:15. Mitsui discloses implanting boron ions to form p⁻ impurity regions of low concentration. *Id.* at 8:40–51, 9:29–34. Sidewall spacers 3a, 3b are formed on the sidewalls of the gate electrodes 1a, 1b. *Id.* at 9:11–13. As shown in Figure 2G, resist pattern 4c is used as a mask and applied to one of gate electrodes 1b and its spacers 3b. *Id.* at 8:30, 9:16–20. With the mask in place, Mitsui discloses “partially etching and removing using anisotropic etching” of a portion of spacer 3a “to a predetermined thickness,” resulting in a smaller spacer. *Id.* at 9:13–35. Then, arsenic ions are implanted to form high concentration n⁺ impurity regions 5a. *Id.* at 9:29–34.

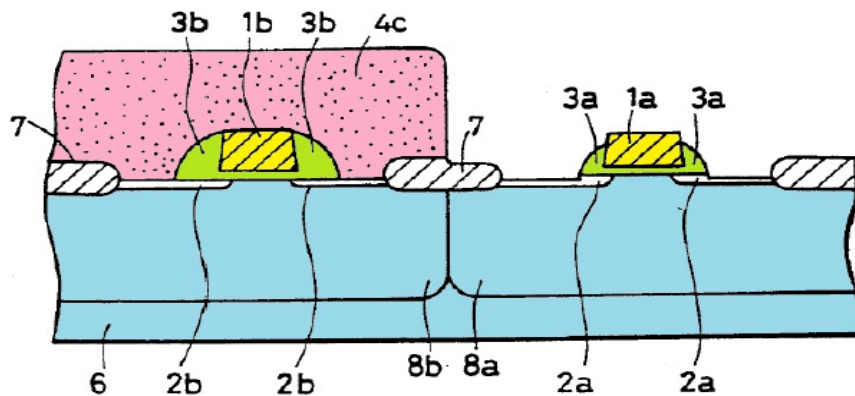
2. Analysis

a. Claim 1

Petitioner asserts that Mitsui discloses every limitation of claim 1. Pet. 36–41. Annotated Figures 2F and 2G are reproduced below.



Ex. 1009, FIG. 2F (annotated)



Ex. 1009, FIG. 2G (annotated)

As depicted in annotated Figures 2F and 2G, Petitioner asserts, and we agree, that Mitsui discloses the claimed gates shown in yellow and forming the “spacers” shown in green (element 3a, 3b). Pet. 36–37. Petitioner asserts, and we agree, that Mitsui discloses the use of a mask shown in pink, applied to a spacer for a “first gate.” *Id.* at 38. Petitioner also contends, and we agree, that Mitsui discloses “sizing least one spacer for each of the at least one remaining gate into a geometry that is smaller than the at least one

spacer for the first gate,” by an etching process, along with mask removal, resulting in smaller spacer 3a. *Id.* at 37–40. Petitioner also asserts, and we agree, that the claimed implantation to form a highly doped regions is disclosed in Mitsui. *Id.* at 40–41.

Patent Owner waived opposition to this challenge to claim 1. *See* Paper 20, 2.

We agree with Petitioner that Mitsui discloses every limitation of claim 1 of the '089 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1004 ¶¶ 154–185), as it is consistent with the prior art disclosures.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 1 of the '089 patent is anticipated by Mitsui.

b. Claim 2

Claim 2 depends from claim 1 and additionally recites “wherein applying an ion implantation and forming a highly doped region further includes forming a lightly doped region within the substrate underneath each spacer.” Ex. 1001, 5:56–59. As the basis of its anticipation challenge to claim 2, Petitioner relies solely on its proposed claim construction and on Mitsui's disclosure where the step of forming a lightly doped region is performed in an earlier separate step from the step of forming a highly doped regions. Pet. 42–43; Ex. 1004 ¶¶ 189–193. As discussed, *supra* Section II.B, we have not adopted Petitioner's proposed claim construction, which would permit intervening manufacturing steps to occur between the formation of the lightly doped regions and the formation of the highly doped

regions. Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 2 of the '089 patent is anticipated by Mitsui.

c. Claim 5

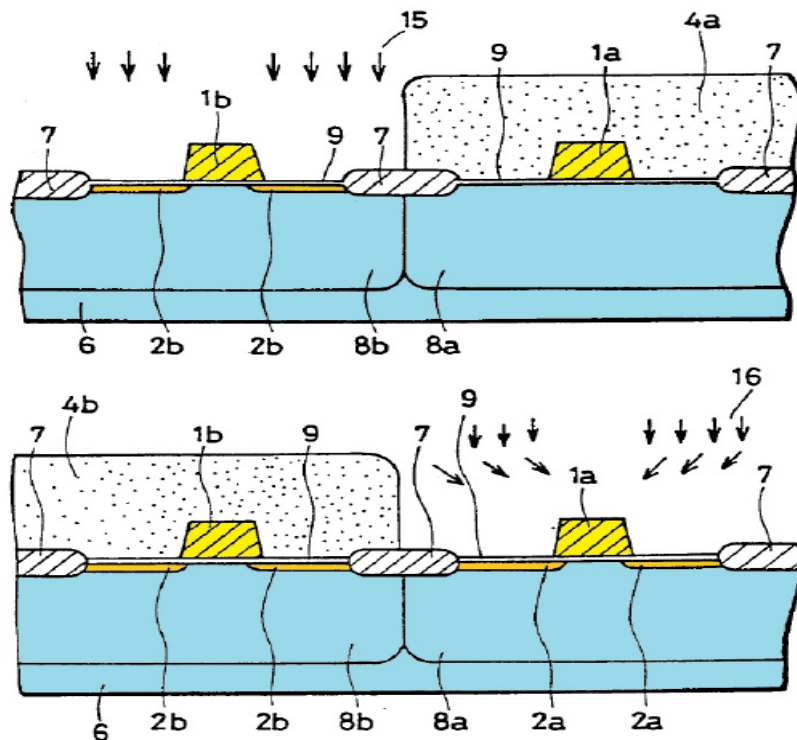
Claim 5 is a method claim that has similar steps to claim 1, however, the final two steps which differ are

removing the mask from the first gate; and applying an ion implantation and forming a highly doped region within the substrate adjacent to the sized at least one spacer; and

prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation and forming a lightly doped region within the substrate adjacent to each edge of each gate.

Ex. 1001, 6:6–13.

We agree with Petitioner that Mitsui discloses the claim 5 steps that are similar to claim 1, for the reasons discussed above. *See* Pet. 44–49; *see also* Ex. 1004 ¶¶ 120–146. Petitioner also asserts, and we agree, that Mitsui discloses that the step of applying ion implantation and forming the lightly doped region is performed prior to spacer formation. Pet. 34–36, Ex. 1004 ¶¶ 147–153. This is depicted in annotated Figures 2C and 2D of Mitsui reproduced below.



Ex. 1009, FIGS. 2C, 2D (annotated)

As depicted in annotated Figures 2C and 2D, Mitsui discloses, prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation and forming a lightly doped region (with first diffusion region shown in orange) within the substrate (shown in blue) in a location adjacent to each edge of each gate (shown in yellow). Pet. 49–50 (citing Ex. 1009, 8:39–66).

Patent Owner waived opposition to this challenge to claim 5. See Paper 20, 2.

We agree with Petitioner that Mitsui discloses every limitation of claim 5 of the '089 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1004 ¶¶ 207–244), as it is consistent with the prior art disclosures.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 5 of the '089 patent is anticipated by Mitsui.

F. Alleged Obviousness over Urabe, Yamanaka, and Mitsui

Petitioner contends that claims 1, 2, and 5 would have been obvious over Urabe, Yamanaka, and Mitsui. Pet. 51–66. To support its contentions, Petitioner provides explanations as to how the prior art teaches each claim limitation. *Id.* Petitioner also relies upon the Neikirk Declaration (Ex. 1004) to support its positions.

We begin our discussion with a brief summary of Urabi, and then address the evidence and arguments presented.

1. Urabe (Ex. 1008)

Urabe is generally directed to a method of manufacturing transistors with different spacer film sizes on the same chip. Ex. 1008, Abstract. Urabe discloses that this method and device provides different source/drain resistance on the same chip to improve chip performance. *Id.* ¶ 13, Abstract. Urabe discloses narrowing the width of spacer oxide film on transistors “thereby making it possible to prevent decrease in the source/drain breakdown voltage and increase the source/drain current of the transistor without narrowing the LDD oxide film of transistors that require source/drain breakdown voltage.” *Id.* ¶ 14.

Urabe discloses formation of gate electrodes on a substrate as shown in Figure 15 reproduced below.

【図 15】

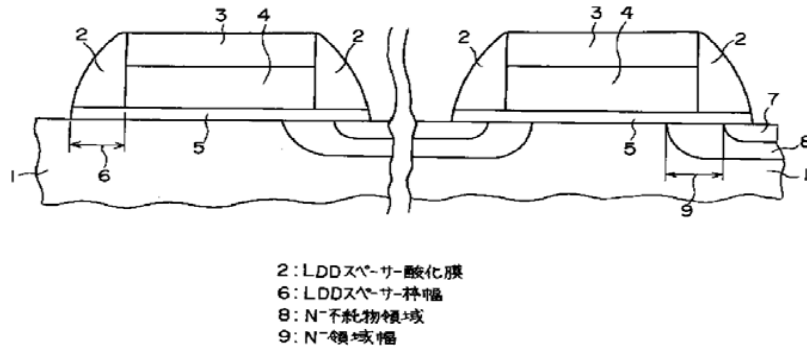
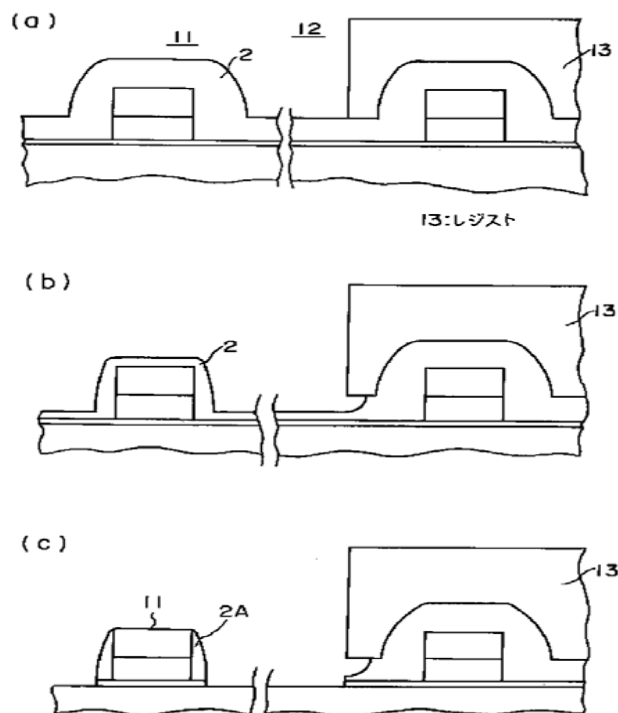


Figure 15 depicts silicon substrate 1, spacer oxide film (side wall) 2, oxide film 3, doped polysilicon gate electrode 4, and N⁺ impurity region 8. Ex. 1008 ¶ 3. Urabe discloses applying a resist to cover a gate and spacers, as shown in Figures 4(a) to 4(c), reproduced below. *Id.* ¶¶ 3, 32.

【図 4】



Figures 4(a) to 4(c) depict spacer oxide film (side walls) 2, transistor 11, and resist 13. Ex. 1008 ¶¶ 3, 31, 32. Urabe discloses that “[i]n FIG. 4, (a) indicates the state after resist 13 has been patterned, (b) indicates the state after oxide film 2 of the second transistor portion has been isotropically etched, and (c) indicates the state after oxide film 2 has similarly been anisotropically etched after (b).” Ex. 1008 ¶ 32.

Urabe further discloses that the resist is removed. Ex. 1008 ¶ 40. Once the spacers are etched to their final shape, an N⁺ source/drain 7 is implanted in the substrate adjacent to the spacers. *Id.*, Figs. 3, 15.

2. Analysis

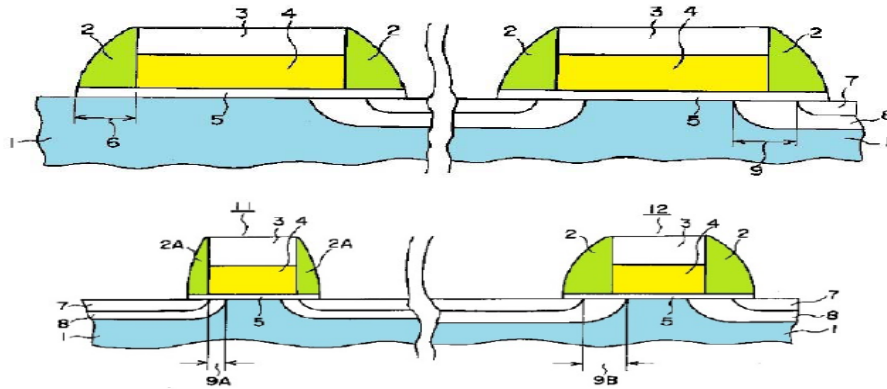
A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁹ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

a. Claim 1

Petitioner asserts that Urabe discloses every limitation of claim 1, but contends that if alternative interpretations of its teachings are applied, there is rationale to modify certain teaching of Urabe in accordance with the

⁹ Patent Owner presents no objective indicia of nonobviousness on this record.

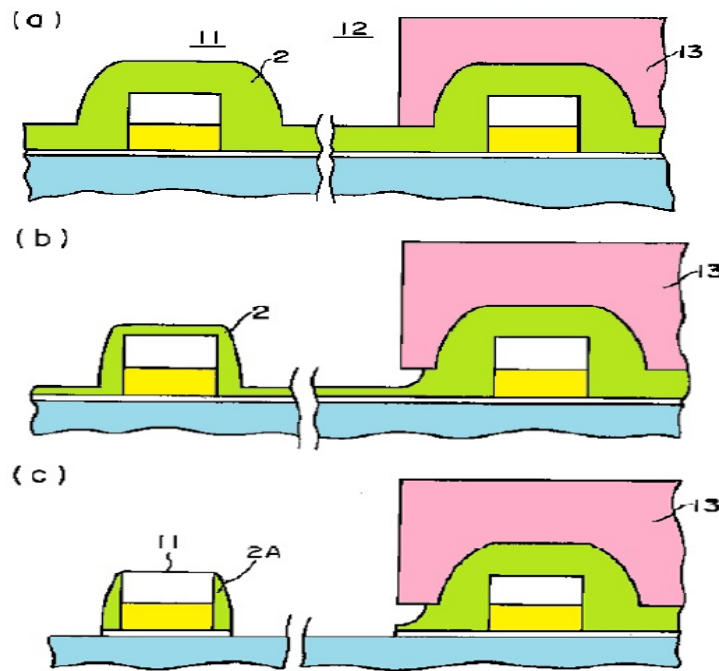
teachings of Yamanaka and Mitsui. Pet. 51–58. Petitioner refers to annotated Figures 1 and 15 depicted below.



Ex. 1008, FIGS. 15, 1 (annotated)

Pet. 53.

As depicted in annotated Figures 1 and 15, Petitioner asserts, and we agree, that Urabe teaches forming spacers (shown in green), adjacent to gates (shown in yellow) on a substrate (shown in blue). Pet. 53–54. Petitioner also relies on annotated Figures 4(a) to 4(c), reproduced below.



Ex. 1008, FIGS. 4(a)-4(c) (annotated)

As depicted in annotated Figures 4(a) to 4(c), Petitioner contends, and we agree, that Urabe teaches the application of a mask (shown in pink) to a first gate, including a portion of at least one spacer. Pet. 54–55. Petitioner asserts, and we agree, that the sequence of steps shown in annotated Figures 4(a) to 4(c) teach the “etching” and “sizing” step of claim 1. *Id.* at 55–57. Petitioner further contends, and we agree, that Urabe teaches the application of ion implantation to form a highly doped region adjacent to a sized spacer. *Id.* at 57–58.

As shown in Figures 4(a) to 4(c) of Urabe, a mask is applied only to a portion of the mapped spacer of the first gate, and the formation of this spacer is completed only after the masking step. Claim 1 does not indicate that the order of the respective “forming” and “applying [or removing] a mask” steps must be performed in a particular order, so we find Urabe sufficiently teaches the limitations of claim 1. *See Interactive Gift Express, Inc. v. CompuServe Inc.*, 256 F.3d 1323, 1342 (Fed. Cir. 2001) (“[u]nless the

steps of a method [claim] actually recite an order, the steps are not ordinarily construed to require one.”). Although not required, Petitioner additionally relies upon Yamanaka and Mitsui for their teachings of the formation of the spacer. *See* Pet. 51–52. Dr. Neikirk presents testimony and evidence that Yamanaka and Mitsui teach the “forming,” “applying a mask,” and “etching” claim limitations. Ex. 1004 ¶¶ 250–271. Petitioner argues that all the prior art references are directed to similar subject matter and “the references are not just analogous art, they belong to the exact same field of endeavor—varying spacer sizes to control operational characteristics of transistors.” Pet. 51. Dr. Neikirk testifies that a variation to complete formation of the larger spacer before or after the application and removal of the mask is an obvious alternative. Ex. 1004 ¶ 63. He further testifies that the combination of the prior art references requires nothing more than using known methods to yield predictable results. *Id.* Dr. Neikirk also testifies that Urabe, Yamanaka, and Mitsui’s approaches to solving the same problem are so similar to one another that one with ordinary skill in the art would find it obvious to substitute one for the other. *Id.* ¶ 64. We determine that the evidence is sufficient to support a conclusion that the prior art, Urabe, Yamanaka, and Mitsui, teach obvious variations of techniques of “forming,” “applying a mask,” and “etching.”

Patent Owner waived opposition to this challenge to claim 1. *See* Paper 20, 2.

We agree with Petitioner that Urabe, Yamanaka, and Mitsui teach every limitation of claim 1 of the ’089 patent, and that there is sufficient showing of rationale that the references can be combined, and we credit Dr.

Neikirk's supporting testimony on those points (Ex. 1004 ¶¶ 61–65, 246–282).

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 1 of the '089 patent is obvious over Urabe, Yamanaka, and Mitsui.

b. Claim 2

As the basis of its obviousness challenge to claim 2, Petitioner solely relies on its proposed claim construction and on Urabe's disclosure wherein the step of forming a lightly doped region is performed in an earlier separate step from the step of forming a highly doped regions. Pet. 58–59; Ex. 1004 ¶¶ 286–293. We have not adopted Petitioner's proposed claim construction, which would permit intervening manufacturing steps to occur between the formation of the lightly doped regions and the formation of the highly doped regions. As discussed above, Yamanaka and Mitsui also fail to disclose this limitation. Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 2 of the '089 patent would have been obvious over Urabe, Yamanaka, and Mitsui.

c. Claim 5

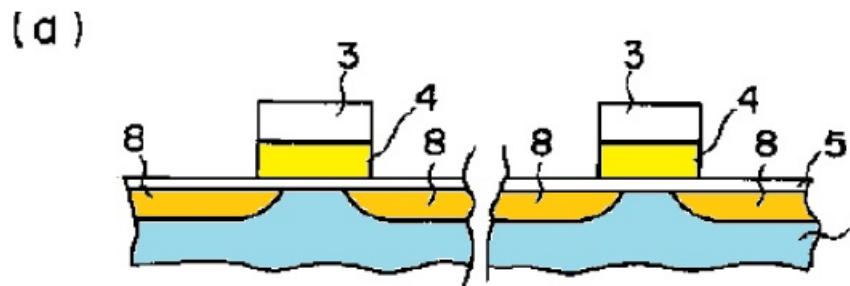
Claim 5 is a method claim that has similar steps to claim 1, however, the final two steps which differ are

removing the mask from the first gate; and applying an ion implantation and forming a highly doped region within the substrate adjacent to the sized at least one spacer; and

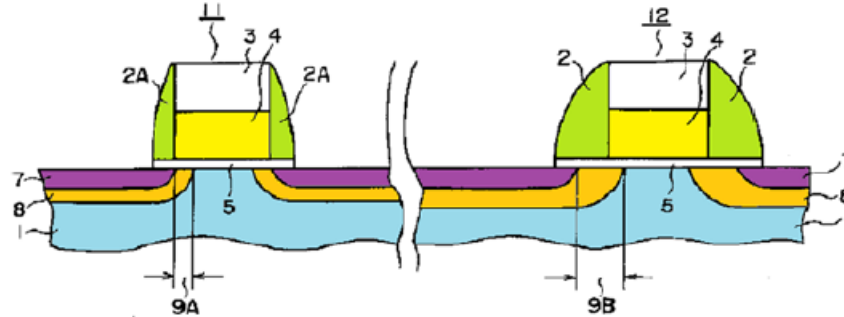
prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation and forming a lightly doped region within the substrate adjacent to each edge of each gate.

Ex. 1001, 6:6–13.

We agree with Petitioner that Urabe, Yamanaka, and Mitsui teach the steps of claim 5 that are similar to claim 1, for the reasons discussed above. *See* Pet. 59–66. Petitioner also asserts, and we agree, that Urabe teaches the step of applying ion implantation and forming the lightly doped region performed prior to spacer formation. *Id.* at 65–66. This is depicted in annotated Figures 17(a) and 1 reproduced below.



Ex. 1008, FIG. 17(a) (annotated)



Ex. 1008, FIG. 1 (annotated)

As depicted in annotated Figures 1 and 17(d), Urabe teaches, prior to forming at least one spacer for each of a plurality of gates on a substrate, applying an ion implantation and forming a lightly doped region (with first diffusion region shown in orange) within the substrate (shown in blue) in a location adjacent to each edge of each gate (shown in yellow). Pet. 65–66 (citing Ex. 1008 ¶¶ 8, 34, 52).

Patent Owner waived opposition to this challenge to claim 5. *See* Paper 20, 2.

We agree with Petitioner that teaches every limitation of claim 5 of the '089 patent and credit Dr. Neikirk's supporting testimony on that point (Ex. 1004 ¶¶ 309–354), as it is consistent with the prior art disclosures.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 5 of the '089 patent is obvious over Urabe, Yamanaka, and Mitsui.

*G. Alleged Obviousness Based Upon Spacer Art
and RTA Art*

Petitioner contends that claim 3 would have been obvious over “Spacer Art,” which is identified as Yamanaka, Mitsui, and Urabe, and “RTA Art,” which is identified as Vasudev, Hayden 2, Grim, and Rodder. Pet. 11, 17, 66–69. To support its contentions, Petitioner provided explanations as to how the prior art discloses each claim limitation. *Id.* Petitioner also relied upon the Neikirk Declaration (Ex. 1004) to support its positions.

Claim 3 recites “[t]he method of claim 2, further comprising applying a rapid thermal anneal (RTA) to cure the ion implantation.” Ex. 1001, 5:60–61. As discussed above, the Petition fails to provide sufficient evidence that Yamanaka, Mitsui, and/or Urabe teach or disclose the limitations of claim 2. By virtue of its dependency from claim 2, the challenge to dependent claim 3 is also insufficient.

Additionally, by statute, a Petition is required to identify “with particularity[] the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge.” 35 U.S.C.

§ 312(a)(3). The Petition shall also include “a full statement” with “a detailed explanation of the significance of the evidence, including material facts.” 37 C.F.R. § 42.22(a).

As we discussed in the Institution Decision, the Petition fails to identify with specificity the prior art or combination of prior art that is being relied upon in the challenge to claim 3. *See* Pet. 66–69. For instance, the Petition alleges that “one or more of the Spacer Art is modified by one or more of the RTA Art,” and the RTA Art, “alone or in combination with Mitsui, Yamanaka, and/or Urabe, disclose applying an RTA to cure the ion implantation.” *Id.* at 66, 68–69. The Petition generally alleges that “[t]he RTA Art teach using RTA to cure ion implantation,” and refers to multiple sections of the Neikirk Declaration. *Id.* at 69. Dr. Neikirk also makes general statements, for instance, that “claim 3 of the ’089 Patent . . . would have been obvious over Yamanaka and at least one of the RTA Art: Vasudev, Hayden 2, Grim, and/or Rodder.” Ex. 1004 ¶ 109.

Petitioner fails to articulate, with reasonable clarity, what specific elements from the individual Spacer Art are to be combined with the specific elements of the other Spacer Art or RTA Art to meet the limitations of claim 3. If Petitioner’s contention is that all seven of the prior art references teach the same limitation of claim 3, it is unclear why Petitioner includes all these references to the extent that they individually teach the same limitation, but the Petition nonetheless lacks requisite specificity and particularity. Pet. 66–69.

Therefore, for the reasons discussed above, Petitioner has not shown by a preponderance of the evidence that claim 3 of the ’089 patent is obvious over Spacer Art and RTA Art.

III. CONCLUSION

For the foregoing reasons, we conclude Petitioner has demonstrated, by a preponderance of the evidence, that claims 1 and 5 of the '089 patent are unpatentable based on the following grounds: (1) anticipation by Yamanaka under 35 U.S.C. § 102(b); (2) anticipation by Mitsui under 35 U.S.C. § 102(b); and (3) obviousness under 35 U.S.C. § 103(a) over Urabe, Yamanaka, and Mitsui.

IV. ORDER

Accordingly, it is

ORDERED that claims 1 and 5 of the '089 patent are determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-02124
Patent 6,046,089

PETITIONER:

Robert L. Hails
Michael J. Riesen
Theresa M. Weisenberger
BAKER HOSTETLER LLP
rhails@bakerlaw.com
mriesen@bakerlaw.com
tweisenberger@bakerlaw.com

PATENT OWNER:

Timothy P. Maloney
Nicholas T. Peters
David A. Gosse
FITCH, EVEN, TABIN & FLANNERY LLP
tim@fitcheven.com
ntpete@fitcheven.com
dgosse@fitcheven.com