

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NANYA TECHNOLOGY CORPORATION,
NANYA TECHNOLOGY CORPORATION U.S.A., and
NANYA TECHNOLOGY CORPORATION DELAWARE,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2018-00062
Patent 6,388,330 B1

Before JON B. TORNQUIST, JOHN F. HORVATH, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

Nanya Technology Corporation, Nanya Technology Corporation U.S.A., and Nanya Technology Corporation Delaware (collectively, “Petitioner”) challenges the patentability of claims 1, 2, 5–7, and 10 (“the challenged claims”) of U.S. Patent No. 6,388,330 B1 (Ex. 1001, “the ’330 patent”), assigned to Lone Star Silicon Innovations, LLC (“Patent Owner”).¹

We have jurisdiction under 35 U.S.C. § 6. This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 1, 5, 6, and 10 of the ’330 patent are unpatentable, but has not shown that claims 2 and 7 are unpatentable.

I. BACKGROUND

A. *Procedural History*

Petitioner filed a Petition seeking *inter partes* review of claims 1, 2, 5–7, and 10 of the ’330 patent. Paper 1 (“Pet.”). Patent Owner filed a Preliminary Response. Paper 5 (“Prelim. Resp.”). In our Institution Decision (Paper 7, “Dec.”), we determined Petitioner had demonstrated a reasonable likelihood of prevailing on its challenges to claims 1, 5, 6, and 10, but had not demonstrated a reasonable likelihood as to claims 2 and 7. *Id.* at 24, 28, 29. Nevertheless, we instituted *inter partes* review of all challenged claims on all grounds of unpatentability asserted in the Petition. *Id.* at 29 (citing *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348 (2018)).

Patent Owner filed a Response. Paper 12 (“PO Resp.”). Petitioner filed a Reply. Paper 15 (“Pet. Reply”).

¹ Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 21, 1.

With the Petition, Petitioner filed a declaration of Ron Maltiel. Ex. 1003. Patent Owner cross-examined Mr. Maltiel and filed a transcript of his deposition testimony as Exhibit 2013 with the Patent Owner Response.

With the Preliminary Response, Patent Owner filed a declaration of Wilmer R. Bottoms, Ph.D. Ex. 2001. With the Patent Owner Response, Patent Owner filed a second declaration of Dr. Bottoms. Ex. 2009. Petitioner cross-examined Dr. Bottoms and filed a transcript of his deposition testimony as Exhibit 1011 with the Reply.

Oral argument was held January 24, 2019, and a transcript was entered in the record. Paper 20 (“Tr.”).

B. Related Matters

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following pending federal court proceedings involving the ’330 patent: *Lone Star Silicon Innovations, LLC v. Nanya Technology Corp.*, Appeal No. 2018-1581 (Fed. Cir., filed Feb. 15, 2018) and *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (N.D. Cal., filed Mar. 16, 2018). Paper 13, 2–4. In addition, Patent Owner identifies Federal Circuit Appeal Nos. 2018-1578, 2018-1580, and 2018-1582, in which the defendant-appellees are Micron Technology, Inc., Renesas Electronics Corp., and United Microelectronics Corp., respectively. *Id.*; see also Paper 6 (Petitioner’s updated mandatory notices), 2–3.

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following *inter partes* review proceedings involving the ’330 patent: *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01566 and *Renesas Electronics Corp. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01869. Paper 13, 2; see also Paper 6, 2.

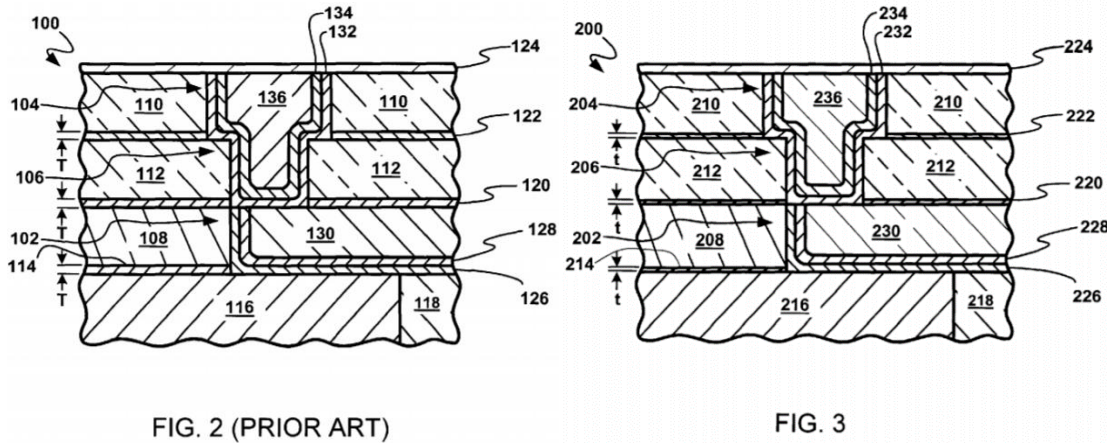
Claims 1, 2, 5–7, and 10 of the '330 patent were found unpatentable in a final written decision entered January 14, 2019, in *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01566 (Paper 24).

C. *The '330 Patent (Ex. 1001)*

The '330 patent is titled “Low Dielectric Constant Etch Stop Layers in Integrated Circuit Interconnects” and was issued May 14, 2002, from Application No. 09/776,012, filed February 1, 2001. Ex. 1001, at (21), (22), (45), (54).

The '330 patent relates to semiconductor technology and, more specifically, to etch stop layers in integrated circuits. *Id.* at 1:6–8. According to the '330 patent, semiconductor devices fabricated in and on a semiconductor substrate may be interconnected using a “damascene” technique of metallization. *Id.* at 1:11–29. A “single damascene” technique is used to form a single layer of conductive interconnects, and a “dual damascene” technique is used to form multiple layers of conductive interconnects that are separated by interlayer dielectric layers, including etch stop layers, in vertically separated planes and interconnected by vertical connections or “vias.” *Id.* at 1:30–34, 2:30–51. The '330 patent discloses that closely positioned, parallel conductive channels suffer from capacitive coupling effects, which can be reduced by reducing the dielectric constant of the silicon nitride etch stop layers between the channels. *Id.* at 3:32–42, 3:49–60. More specifically, the '330 patent represents that “currently used silicon nitride . . . has a dielectric constant in excess of 7.5” (*id.* at 3:39–41) and discloses that capacitive coupling effects are reduced by using an etch stop layer having a dielectric constant below 5.5 (*id.* at 3:53–54, 3:58–59).

Figure 2 of the '330 patent shows a “prior art” structure, and Figure 3 shows the invention. Ex. 1001, 4:14–20. Figures 2 and 3 of the '330 patent are reproduced below:



Figures 2 and 3, above, show semiconductor wafers 100, 200, including dielectric layers 108, 110, 112, 208, 210, and 212; conductor cores 130, 136, 230, 236; and etch stop layers 114, 120, 122, 124, 214, 220, 222, and 224.² *Id.* at 4:24–32, 4:42–5:4, 5:21–53. According to the '330 patent, Figure 3 is “similar” to Figure 2, except for the thickness of the etch stop layers, which is shown as “T” in Figure 2 and “t” in Figure 3. *Id.* at 4:18, 5:17–23, 5:66–6:2.

Regarding the etch stop layers, the '330 patent discloses:

In the present invention, a half thickness, high quality, etch stop layer (compared to the prior art etch stop layer) is deposited.

For example, for silicon nitride, the dielectric constant of an etch stop layer in accordance with the present invention is about 5.5 contrasted to an excess of 7.5 in the prior art.

² Structures with 100-series reference numerals are shown in Figure 2, and structures with 200-series reference numerals are shown in Figure 3.

Id. at 5:60–65. The '330 patent discloses processes that can be used to produce etch stop layers with a dielectric constant under 5.5, including successive deposition of multiple layers of silicon nitride, which “eliminates pinholes and produces a denser film.” *Id.* at 5:66–6:7.

D. Illustrative Claim

The Petition challenges claims 1, 2, 5–7, and 10 of the '330 patent, of which claims 1 and 6 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below:

1. An integrated circuit comprising:
 - a semiconductor substrate having a semiconductor device provided thereon;
 - a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;
 - a first conductor core filling the first opening and connected to the semiconductor device;
 - an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5;
 - a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core;
 - a second conductor core filling the second opening and connected to the first conductor core.

Ex. 1001, 6:54–7:2.

Claim 6 is similar to claim 1, except that it recites an additional dielectric layer (called a via dielectric layer) and an additional etch stop layer (called a channel etch stop layer), and the second conductor core fills openings in both the via and second dielectric layers. *Id.* at 7:15–8:11.

E. Instituted Grounds of Unpatentability

We instituted *inter partes* review of the challenged claims based on all grounds of unpatentability asserted in the Petition. The instituted grounds are based on 35 U.S.C. § 103(a) and are summarized below:

References	Claims
APA ³ and Tanaka ⁴	1, 5, 6, and 10
APA, Tanaka, and Watatani ⁵	2 and 7
Chooi ⁶ and Tanaka	1, 5, 6, and 10
Chooi, Tanaka, and Watatani	2 and 7

Pet. 5; Dec. 29.

II. ANALYSIS

A. Claim Construction

In this *inter partes* review, the '330 patent has not yet expired, and claim terms are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b)

³ As discussed below, Petitioner relies on certain disclosures in the '330 patent as Admitted Prior Art ("APA"). Pet. 11–18, 22–36.

⁴ M. Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47–48, Ex. 1004 ("Tanaka").

⁵ Watatani, U.S. Patent No. 6,153,511, issued November 28, 2000, filed June 25, 1999, Ex. 1006 ("Watatani").

⁶ Chooi et al., U.S. Patent No. 6,436,824 B1, issued August 20, 2002, filed July 2, 1999, Ex. 1005 ("Chooi").

(2017).⁷ Under that standard, we generally give claim terms their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Patent Owner contends that the phrase “etch stop layer of silicon nitride” should be construed as “etch stop layer characterized by the presence of silicon atoms bonded to nitrogen atoms throughout the layer.” PO Resp. 11. Petitioner opposes that construction. Pet. Reply 2.

Patent Owner concedes that “[t]he meaning of ‘etch stop layer of silicon nitride’ does not affect the analysis in this particular case.” PO Resp. 13. Relying on Patent Owner’s concession, Petitioner argues that the Board need not and should not provide an explicit construction. Pet. Reply 1.

In the Institution Decision, we determined that it was not necessary to provide an express construction for any claim term. Dec. 8. Neither party challenges that determination. Accordingly, consistent with the Institution Decision and the parties’ arguments, we determine that we do not need to provide an express construction for any claim term for purposes of resolving the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the

⁷ A recent amendment to this rule does not apply here, because the Petition was filed before November 13, 2018. *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 100(b) effective November 13, 2018).

controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Principles of Law

Petitioner bears the burden of proving unpatentability, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish the facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Petitioner’s declarant, Mr. Maltiel, testifies that a person of ordinary skill in the art (“POSITA”) would have a minimum of a bachelor’s degree in electrical engineering, chemistry, physics, material science, or a related field, and approximately five years of professional experience with semiconductor fabrication, or other relevant experience. Ex. 1003 ¶ 16. Mr. Maltiel further testifies that additional appropriate graduate education could substitute for professional experience, or significant experience in the

field could substitute for formal education. *Id.* Patent Owner’s declarant, Dr. Bottoms, testifies that a POSITA would have held at least a bachelor’s degree in electrical engineering, material science, physics, chemistry, or a closely related field and at least five years of industry experience in the fabrication of semiconductor devices. Ex. 2009 ¶ 31. Dr. Bottoms further testifies that an individual with an advanced degree in a relevant field would require less experience in semiconductor fabrication. *Id.*

We find there is little difference between the declarants’ definitions of a POSITA, and the outcome of our patentability determinations would be the same, regardless of which definition we accept. Neither declarant indicates that his opinion would change depending on the level of ordinary skill in the art. For the sake of clarity and consistent with our Institution Decision (Dec. 9), we adopt Dr. Bottoms’ definition of a POSITA. Ex. 2011 ¶ 31. We also rely on the cited prior art references as reflecting the level of ordinary skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

After reviewing the qualifications of Mr. Maltiel and Dr. Bottoms, as set forth in each witness’s declaration and curriculum vitae, we find that each of these declarants has sufficient education and experience related to the subject matter of the ’330 patent to testify regarding the perspective of a POSITA at the time of the invention. Ex. 1003 ¶¶ 2–12, Attachment A; Ex. 2002; Ex. 2009 ¶¶ 6–18. *See Trial Practice Guide Update*, 83 Fed. Reg. 39,989 (Aug. 13, 2018), available at <https://go.usa.gov/xU7GP> (“TPG Update”), 3 (“A person may not need to be a person of ordinary skill in the art in order to testify as an expert under Rule 702, but rather must be

‘qualified in the pertinent art.’” (quoting *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008))).

D. Overview of the Asserted Prior Art

1. Admitted Prior Art (“APA”) (Ex. 1001)

Figures 1 and 2 of the ’330 patent are labeled “prior art” and are reproduced below:

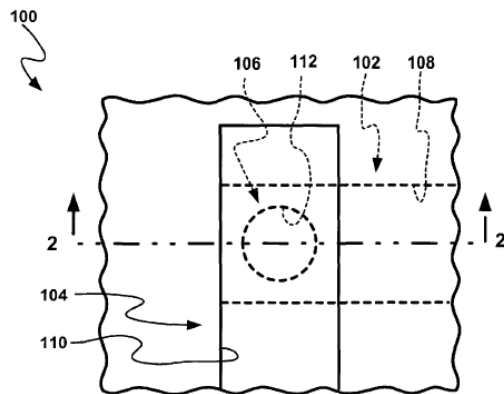


FIG. 1 (PRIOR ART)

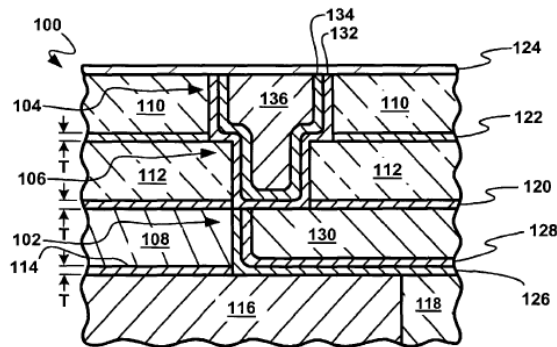


FIG. 2 (PRIOR ART)

Figure 1 of the ’330 patent shows a plan view of a semiconductor wafer, and Figure 2 is a cross-section of Figure 1 along line 2—2. Ex. 1001, 4:14–17.

Figure 1 (prior art) shows semiconductor wafer 100, first and second channels 102 and 104, via 106, first and second channel dielectric layers 108 and 110, and via dielectric layer 112. Ex. 1001, 4:24–32. First and second channels 102 and 104 serve as interconnects and are disposed in first and second channel dielectric layers 108 and 110, respectively. *Id.* at 4:28–30. Via 106 is an integral part of second channel 104 and is disposed in via dielectric layer 112. *Id.* at 4:30–32.

Figure 2 (prior art) is a cross-section of Figure 1 and shows the same structures as listed above for Figure 1. In addition, Figure 2 shows first channel stop layer 114, device dielectric layer 116, semiconductor contact

118, via stop layer 120, second channel stop layer 122, next channel stop layer 124, barrier layers 126 and 132, seed layers 128 and 134, and conductor cores 130 and 136. Ex. 1001, 4:42–5:4. Device dielectric layer 116 is formed on a silicon semiconductor substrate. *Id.* at 4:45–46. The layers above device dielectric layer 116 are sequentially: first channel stop layer 114, first channel dielectric layer 108, via stop layer 120, via dielectric layer 112, second channel stop layer 122, second channel dielectric layer 110, and next channel stop layer 124. *Id.* at 4:51–57. First channel 102 connects to an operative semiconductor device (not shown) through semiconductor contact 118, which is embedded in device dielectric layer 116. *Id.* at 4:46–51.

First channel 102 includes barrier layer 126, seed layer 128, and conductor core 130. *Id.* at 4:58–60. Second channel 104 and via 106 include barrier layer 132, seed layer 134, and conductor core 136. *Id.* at 4:61–64. Barrier layers 126 and 132 prevent diffusion of the conductor materials into the adjacent areas of the semiconductor device. *Id.* at 4:64–66. Seed layers 128 and 134 form electrodes on which the conductor material is deposited, and they become part of the respective conductor cores 130 and 136 after the deposition. *Id.* at 4:66–5:4. Copper can be used as a conductor material and seed layer. *See, e.g., id.* at 1:53–56, 2:59–62, 3:12–15, 5:5–8.

First channel stop layer 114, via stop layer 120, and second channel stop layer 122 are used as layers to stop the etching process used to form channels and via openings in first channel dielectric layer 108, via dielectric layer 112, and second channel dielectric layer 110, respectively. Ex. 1001, 5:9–14. Where the first channel dielectric layer is an oxide material, such as

silicon oxide (SiO₂), the first channel stop layer is a nitride, such as silicon nitride (SiN), so the two layers can be selectively etched. *Id.* at 1:41–45, 2:39–41, 2:43–46.

2. *Tanaka (Ex. 1004)*

Tanaka is an article titled, “Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD.”
Ex. 1004.⁸ Tanaka addresses the problem of parasitic capacitance associated with copper (Cu) interconnects formed by a conventional damascene process that uses “high-k SiN film” for the etch stopper layers. *Id.* at 47-1.⁹ To solve this problem, Tanaka discloses a “[n]ew low-k SiN film with a permittivity of 5.4 and high immunity for Cu diffusion and oxidation” *Id.* at 47-1, 47-2. The silicon nitride film is formed by an ultra low temperature thermal chemical vapor deposition (“CVD”) process using HexaChloroDisilane (HCD, Si₂Cl₆) as a silicon source. *Id.* at 47-1. Tanaka refers to the new film as “HCD-SiN” and discloses a deposition process and film properties for the new film. *Id.* at 47-1, 47-2, Figs. 2–8.

Figure 1 of Tanaka is reproduced below:

⁸ In Tanaka, the letter “k” is used to refer to permittivity or dielectric constant. Ex. 1004 (Title, Abstract). Mr. Maltiel explains that dielectric constant is sometimes referred to as permittivity or “k”. Ex. 1003 ¶ 27. Dr. Bottoms agrees that “[p]ermittivity as used in Tanaka means relative permittivity and is synonymous with dielectric constant.” Ex. 2011 ¶ 72 n.1.

⁹ We cite to Tanaka and other non-patent references using a page number of the original document followed by a hyphenated suffix (“-1” or “-2”) to indicate the first or second column.

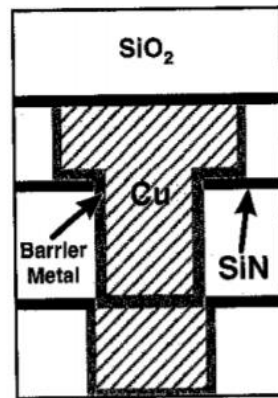


Fig.1 A schematic drawing of Cu interconnects formed by damascene process

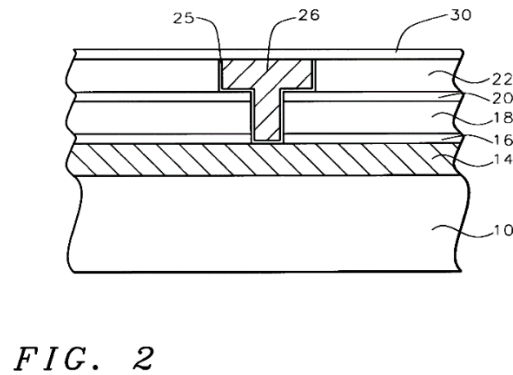
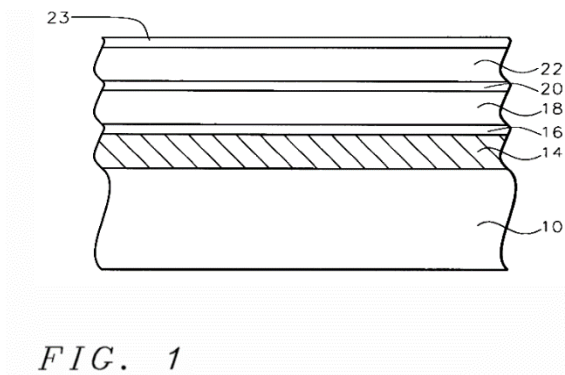
Figure 1 of Tanaka shows copper interconnects formed by a conventional damascene process, which requires “plural layers of high-k SiN film for a groove etch stopper and a barrier of Cu diffusion and oxidation.” Ex. 1004, 47-1. As explained above, Tanaka proposes improving this conventional process by using “HCD-SiN as the etch-stop and the barrier layer . . . to realize Cu damascene interconnects for high performance VLSIs.”¹⁰ *Id.*

3. Chooi (Ex. 1005)

Chooi is a U.S. patent titled, “Low dielectric constant materials for copper damascene.” Ex. 1005, at (54). Chooi discloses low dielectric constant materials for use in a dual damascene process. *Id.* at (57). More particularly, Chooi discloses two alternative low dielectric constant materials for use as a passivation or etch stop layer. *Id.* at (57), 1:49–65. Chooi also describes a process for forming passivation, dielectric, and etch stop layers for use in a dual damascene process. *Id.* at (57), 1:66–2:21.

Figures 1 and 2 of Chooi are reproduced below:

¹⁰ The acronym VLSI refers to very large scale integrated devices. See Ex. 1002, 49.



Chooi Figures 1 and 2 illustrate a dual damascene process. Ex. 1005, 2:26–28. Figure 1 depicts a partially completed integrated circuit device, including semiconductor substrate 10, interconnection line 14, passivation or barrier layer 16, first dielectric layer 18, etch stop layer 20, second dielectric layer 22, and optional capping layer 23. *Id.* at 2:42–65. With the exception of the capping layer, Figure 2 depicts the same structures as Figure 1 and additionally depicts barrier metal layer 25, copper layer 26, and final passivation layer 30. *Id.* at 2:66–3:8.

Chooi describes three embodiments of low dielectric constant materials for use in a dual damascene metallization process. *Id.* at 3:9–4:29. The materials of the first two embodiments can be used as barrier or passivation layer 16, optional capping layer 23, and final passivation layer 30. *Id.* at 3:9–4:18. The first embodiment is a carbon-doped silicon nitride film having a dielectric constant of about 3 to 6. *Id.* at 3:21–28, 4:62–66. The second embodiment is a silicon-carbide film having a dielectric constant of about 3 to 6.5. *Id.* at 4:11–18, 4:67–5:2. The third embodiment is a low dielectric constant material that can be used for dielectric layers 18 and 22 and has a dielectric constant less than 3. *Id.* at 4:19–29, 5:4–9.

4. *Watatani (Ex. 1006)*

Watatani is a U.S. Patent titled, “Semiconductor device having a multilayer interconnection structure.” Ex. 1006, at (54). Watatani discloses a multilayer interconnection structure including a lower organic interlayer insulation film, an etching stopper film on the lower interlayer insulation film, and an upper organic interlayer insulation film covering the etching stopper film, where the upper organic interlayer insulation film is covered by first and second etching stopper films of respective, different compositions. *Id.* at (57).

By way of background, Watatani discloses conventional dual damascene processes for forming multilayer interconnection structures, including a first example having a silicon oxide (SiO₂) interlayer insulation film and a second example having an organic interlayer insulation film. Ex. 1006, 1:65–67, 2:65–67, Figs. 1A–1F, 2A–2E. Watatani explains that the use of an organic interlayer insulation film alleviates the problem of stray capacitance due to the large dielectric constant of silicon oxide. *Id.* at 2:54–64. According to Watatani, a multilayer interconnection structure having an organic interlayer insulation film suffers from another problem, namely that resist pattern misalignments are difficult to correct. *Id.* at 3:51–4:41. To address the resist pattern misalignment problem, Watatani discloses a semiconductor fabrication process that includes the steps of forming a first etching stopper film on an organic interlayer insulation film and forming a second, different etching stopper film on the first etching stopper film. *Id.* at 4:48–5:25; *see also id.* at (57); *id.* at 6:4–10 (disclosing “an etching stopper structure 81, formed of a stacking of two etching stopper

layers, . . . a first etching stopper film 80 of SiN . . . and a second etching stopper film 82 of SiO₂”); Fig. 5A.

E. Petitioner’s Challenge Based on the APA and Tanaka

Petitioner contends that claims 1, 5, 6, and 10 of the ’330 patent are unpatentable as obvious in view of the APA and Tanaka. Pet. 11–18, 22–36. We address each of these claims below.

1. Claims 1 and 6

Petitioner contends that the APA teaches all elements of independent claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 11–18, 22–36. As support for that contention, Petitioner provides the following annotation of Figure 2 (prior art) of the ’330 patent:

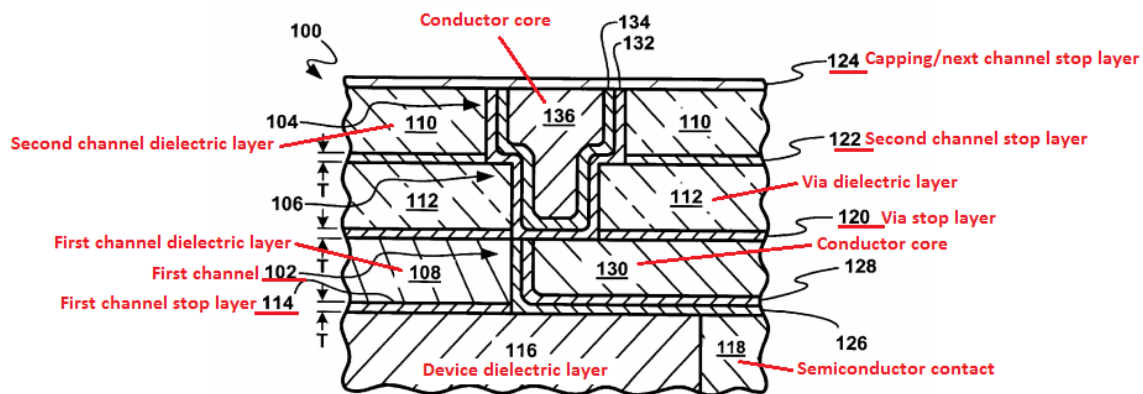


FIG. 2 (PRIOR ART)

Id. at 22; Ex. 1003 ¶ 30. Figure 2 (prior art) shows a cross-sectional view of a semiconductor wafer and is annotated by Petitioner to identify semiconductor contact 118, conductor cores 130 and 136, dielectric layers 108, 110, 112, and 116, and etch stop layers 114, 120, 122, and 124.

Ex. 1001, 4:24–32, 4:42–5:4. Petitioner provides claim charts mapping the elements of claims 1 and 6 to the APA and Tanaka. *Id.* at 22–35.

Petitioner’s claim charts rely on descriptions of the APA in the ’330 patent

for all elements of claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer, which Petitioner contends is disclosed by Tanaka. *Id.* at 25, 32, 34 (citing Ex. 1004, 47, Fig. 5).

Petitioner contends that a POSITA would have known how to make silicon nitride with a dielectric constant below 5.5 and that Tanaka discloses such a method and discloses silicon nitride with a dielectric constant of 5.4 for use as an etch stop layer. Pet. 13, 16–17 (citing Ex. 1004, 47, Fig. 5). Petitioner contends that a POSITA would have been motivated to combine Tanaka with the APA “to achieve lower parasitic capacitance in the structure disclosed in the” APA. *Id.* at 14, 16, 18. According to Petitioner, Tanaka identifies its “new low-K SiN film, with a permittivity of 5.4” for use in damascene interconnects such as the APA, and is directed to reducing “parasitic capacitance,” which is one motivation for having a low dielectric constant etch stop in the types of semiconductor devices described in the APA and Tanaka. *Id.* at 13, 16–17 (quoting Ex. 1004, 47).

Patent Owner argues that a POSITA would not have been motivated to replace the silicon nitride etch stop in the APA with Tanaka’s HCD-SiN. PO Resp. 24–27. In addition, Patent Owner argues that a POSITA would not have reasonably expected success in combining Tanaka with the APA to form etch stop layers with a dielectric constant below 5.5. *Id.* at 27–35. Under the heading “secondary considerations,” Patent Owner argues that Tanaka teaches away from substituting the silicon nitride material disclosed for the material disclosed in the APA. *Id.* at 35–37.

Patent Owner does not contest Petitioner’s reliance on the APA as prior art that can be relied upon in an *inter partes* review. Nor does Patent Owner dispute Petitioner’s contention that the APA discloses an integrated

circuit that meets all limitations of claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 11–18, 22–36; see PO Resp. 2–4 (describing prior art Figures 1 and 2 of the '330 patent); *id.* at 17–38 (Patent Owner's response to Petitioner's Ground 1). Relying on Petitioner's arguments and evidence, we find Petitioner has shown by a preponderance of the evidence that all limitations of claims 1 and 6 are disclosed by the APA, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 11–18, 22–36; Ex. 1001, Figs. 1, 2, 1:10–3:27, 4:14–17, 4:24–5:19; Ex. 1003 ¶¶ 30–36, 39–47.

Patent Owner does not dispute Petitioner's contention that Tanaka discloses a silicon nitride etch stop layer having a dielectric constant of 5.4, i.e., below 5.5, as recited in claims 1 and 6. Pet. 13, 16, 17, 25, 32, 34; see PO Resp. 18, 20–21, 36 (agreeing that Tanaka discloses HCD-SiN film having permittivity (dielectric constant) of 5.4, which can function as an etch stop layer). Relying on evidence cited by Petitioner, we find Petitioner has proven its contention by a preponderance of the evidence. Pet. 13, 16, 17, 25, 32, 34; Ex. 1003 ¶¶ 34, 43, 45; Ex. 1004, 47-1 (disclosing “[n]ew low-k SiN film, with permittivity of 5.4” as an etch stop layer for copper damascene interconnects).¹¹

After considering the parties' arguments and evidence, we find Petitioner has established that a POSITA would have been motivated to combine Tanaka's low dielectric constant silicon nitride etch stop layer with the copper damascene interconnect structure of the APA. Pet. 13, 16, 17; Ex. 1003 ¶¶ 34, 43, 45. We credit the following testimony of Mr. Maltiel:

¹¹ In Tanaka, “permittivity” and the letter “k” refer to dielectric constant. See p. 13 n.8, *supra*.

A POSITA would have been motivated to combine Tanaka with the Admitted Prior Art for at least the reason that Tanaka specifically identified its “new low-K SiN film, with a permittivity of 5.4” to be used in “damascene interconnects” such as those in described in the background art to the ’330 patent. . . . Additionally, Tanaka is directed to reducing “parasitic capacitance” which is one motivation for having a low K etch stop in the types of semiconductor devices described in the admitted prior art in the ’330 patent and describe[d] in Tanaka. Tanaka solves this problem by developing a low dielectric silicon nitride below 5.5. . . . Thus it would have been obvious to combine the specific teaching of a “new low-K SiN film” in Tanaka with prior art damascene structures to achieve lower parasitic capacitance in the structure disclosed in the ’330 patent.

Ex. 1003 ¶ 34 (citing Ex. 1004, 47; Ex. 1001, 3:35–46).

Mr. Maltiel’s testimony is supported by the express disclosures of Tanaka relied upon by Petitioner and Mr. Maltiel. Pet. 13; Ex. 1003 ¶ 34 (citing Ex. 1004, 47). As Petitioner and Mr. Maltiel correctly point out, Tanaka discloses a low dielectric constant silicon nitride etch stop film for use in the same type of structure disclosed in the APA: a conventional copper damascene interconnect structure. According to Tanaka, a “[n]ew low-k SiN film, with a permittivity of 5.4 . . . should be the solution to realize Cu damascene interconnects.” Ex. 1004, 47-1, 47-2. Tanaka teaches that the new low-k SiN can be used as the silicon nitride etch stop layer in copper interconnect structures formed by a conventional damascene process, as illustrated in Tanaka Figure 1. *Id.* at 47-1, 48, Fig. 1. Furthermore, Tanaka supports Petitioner’s contention that a desire to achieve lower parasitic capacitance would have been one motivation for a POSITA to use Tanaka’s low dielectric constant silicon nitride etch stop layer in the copper damascene interconnect structure of the APA. Tanaka identifies the high

permittivity of SiN as a cause of parasitic capacitance and proposes its low dielectric constant silicon nitride etch stop film as a solution to this problem. *Id.* at 47-1.

Patent Owner does not dispute that Tanaka's low dielectric constant silicon nitride film is disclosed for use in damascene interconnects like the APA. Ex. 1004, 47-1; *see* PO Resp. 25, 28. Patent Owner also does not dispute that a desire to reduce parasitic capacitance would have motivated a POSITA to use Tanaka's low dielectric constant silicon nitride film in a damascene process. PO Resp. 25, 28. Instead, Patent Owner argues that any motivation to use Tanaka's HCD-SiN material would have been mitigated by other factors, namely, corrosion, deposition rate, and etch selectivity. *Id.* at 25–27; Ex. 2009 ¶ 107; *see also* PO Resp. 17–24 (summary and criticism of Tanaka). We address each of these factors below in the context of addressing Patent Owner's arguments regarding motivation to combine.

First, Patent Owner argues that “Tanaka fails to provide enough information to determine the thickness of HCD-SiN that would be necessary for the material to function effectively as an etch stop layer in a given etch process.” PO Resp. 25 (citing Ex. 2009 ¶ 78). Petitioner contends that a POSITA would have known how to use Tanaka's silicon nitride material as an etch stop and presents no problems regarding etch stop thickness. Pet. Reply 3 (citing Ex. 1004, 47). After considering both parties' arguments, we find that Tanaka teaches directly toward the use of HCD-SiN material as an etch stop layer for copper damascene interconnect structures, and that Tanaka's teaching is not undermined by any lack of information regarding etch stop layer thickness. As noted by Petitioner (Pet. Reply 3), Tanaka teaches that “HCD-SiN has same RIE etching resistance as

conventional LPCVD SiN” and suggests “the possibility of SiN thickness reduction.” Ex. 1004, 47-1, 47-2. It follows logically from these statements that a POSITA would have been motivated to use Tanaka’s HCD-SiN film in place of conventional SiN etch stop layers with a reasonable expectation that it would function effectively when deposited in a thickness no greater than a conventional etch stop layer.

Second, Patent Owner argues that a POSITA would not be motivated to use Tanaka’s HCD-SiN material because it would be incompatible with copper interconnects and unreliable due to the presence of a substantial amount of chlorine, which was known to corrode copper interconnects. PO Resp. 20, 22, 26 (citing Ex. 2009 ¶¶ 74, 75, 101). Petitioner contends that Tanaka’s material is disclosed for use with copper interconnects and that its barrier ability would have been an additional motivation to apply Tanaka’s teachings to the APA. Pet. Reply 4 (citing Ex. 1004, 47). We find that Patent Owner’s argument is contradicted by the express disclosures of Tanaka. As noted by Petitioner, even the title of Tanaka teaches that the low dielectric constant silicon nitride film is “for Cu Interconnects.” Ex. 1004; Pet. Reply 4. Although Tanaka discloses that the chlorine content of HCD-SiN “is 50 times larger than conventional SiN” (Ex. 1004, 47-2), there is no suggestion of any incompatibility, unreliability, corrosion, or other problems due to the presence of chlorine. On the contrary, Tanaka states that the effect of chlorine on Tanaka’s film was investigated using thermal stability tests and further states that the film was determined to be “thermally stable.” *Id.* Patent Owner’s incompatibility argument is further contradicted by Tanaka’s disclosure that HCD-SiN has “higher barrier ability for Cu diffusion than plasma-SiN.” *Id.* at 47-1; *see also id.* at 47-2 (“HCD-SiN

kept on preventing Cu diffusion for 5000 min whereas p-SiN was broken within 20 min.”). In view of these teachings, we find Petitioner has shown that a POSITA would have understood Tanaka’s HCD-SiN to be compatible with copper interconnects and that the barrier ability of HCD-SiN provides an additional motivation to combine Tanaka’s teachings with the APA.

Third, Patent Owner argues that a POSITA would not have been motivated to use Tanaka’s HCD-SiN because “the material with the claimed dielectric constant is not necessarily compatible with practical deposition rates.” PO Resp. 19–20, 26–27 (citing Ex. 2009 ¶¶ 73, 102, 103, 106). Relying on essentially the same argument about deposition rate, Patent Owner asserts that Tanaka expressly teaches away from substituting the disclosed silicon nitride material for the material disclosed in the APA. *Id.* at 35–37. Petitioner contends that Patent Owner’s argument is speculative and not relevant to the claims, which do not require a particular deposition rate. Pet. Reply 4, 7.

After considering both parties’ arguments, we are persuaded Petitioner has established that a POSITA would have been motivated to combine Tanaka’s teachings with the APA. At most, Patent Owner shows that Tanaka’s silicon nitride film with a dielectric constant of 5.4 was deposited at a rate of 0.6 nm/min., which is slower than a “practical” rate of 1.4 nm/min. PO Resp. 18–19, 26–27; Ex. 1004, 47-1; Ex. 2009 ¶¶ 73, 103. Tanaka does not, however, suggest that the deposition rate is a disadvantage of the “[n]ew low-k SiN film.” Ex. 1004, 47-1. Instead, Tanaka states that this material has been “successfully developed,” has many advantages, including “low permittivity,” and “should be the solution to realize Cu damascene interconnects for high performance VLSIs.” *Id.* Even if

achieving a practical deposition rate would require a corresponding increase in the dielectric constant, as postulated by Patent Owner (PO Resp. 19, 27), that does not negate the advantages of Tanaka's low dielectric constant silicon nitride as motivation for combining it with the APA. Indeed, Tanaka expresses no reservations about deposition rate, nor does it state that deposition rates below the "[p]ractical high deposition rate of 1.4 nm/min" are not practical, useful, or advantageous.

Accordingly, we find Petitioner has shown by a preponderance of the evidence that a POSITA would have been motivated to use Tanaka's low dielectric constant silicon nitride film as the etch stop layer in the interconnect structure of the APA. Our finding is confirmed by Patent Owner's admission that the Petition "identifies a motivation to combine the Admitted Prior Art and the silicon nitride material disclosed in Tanaka." PO Resp. 28.

Although the Petition does not expressly discuss whether one of ordinary skill in the art would have had a reasonable expectation of success in combining Tanaka and the APA to arrive at the claimed invention, Petitioner shows a close relationship between the teachings of Tanaka and the APA. Pet. 12–13, 17–18, 53–62. As discussed above and established by Petitioner and the testimony of Mr. Maltiel, Tanaka discloses a low dielectric constant silicon nitride etch stop film for use in the same type of structure disclosed in the APA: a conventional copper damascene interconnect structure. Pet. 13; Ex. 1003 ¶ 34; Ex. 1004, 47-1, 47-2, 48, Fig. 1. Petitioner establishes a reasonable expectation of success for the combination of Tanaka and the APA by demonstrating a strong correlation between the structure disclosed by the APA—a conventional copper

damascene interconnect structure with silicon nitride etch stop layers—and the structure that is improved by Tanaka’s low dielectric constant silicon nitride film—likewise a conventional copper damascene interconnect structure with silicon nitride etch stop layers. *In re Inland Steel Co.*, 265 F.3d 1354, 1364 (Fed. Cir. 2001) (“[T]he strength of the correlation between the references gives rise to a reasonable expectation of success from combining them.”).

Patent Owner advances a series of arguments to counter Petitioner’s showing of a reasonable expectation of success. PO Resp. 28–35; *see also id.* at 17–24 (summary and criticism of Tanaka).

First, Patent Owner argues that Tanaka discloses “preliminary and incomplete information” and “prospective statements” and lacks sufficient information to prove that Tanaka’s low dielectric constant HCD-SiN material would function as an etch stop layer. PO Resp. 21, 29, 30 (citing Ex. 2009 ¶¶ 108, 109). Patent Owner identifies factors it contends are critical to the ability of a silicon nitride film to act as an etch stop, suggesting that Tanaka’s disclosure is deficient as to these factors. *Id.* at 31 (citing Ex. 2009 ¶¶ 111, 112). In addition, Patent Owner argues that Tanaka discloses etch selectivity data relative only to TEOS¹² and not to any other type of silicon oxide or insulator material. *Id.* at 20–21, 31 (citing Ex. 2009 ¶¶ 77, 112).

We agree with Petitioner that Patent Owner’s arguments are contrary to the express disclosures of Tanaka. Pet. Reply 5. Tanaka states that a new

¹² According to Patent Owner and its expert, TEOS refers to tetraethyl orthosilicate, which is a precursor used to form one type of silicon oxide film, referred to as TEOS-SiO. PO Resp. 21; Ex. 2009 ¶ 77.

low dielectric constant silicon nitride film has been “successfully developed” and can be used as an etch stop layer. Ex. 1004, 47-1 (Abstract: “HCD-SiN as the etch-stop and the barrier layer should be the solution to realize Cu damascene interconnects for high performance VLSIs.”). Tanaka backs up its prediction of success with more detailed disclosures regarding the ability of the low dielectric constant silicon nitride film to function as an etch stop. For example, Tanaka states that “HCD-SiN has same RIE etching resistance as conventional LPCVD SiN.” *Id.* at 47-1 (Abstract). In Figure 6, Tanaka compares the etching rate selectivity for HCD-SiN films to the etching rate selectivity for a DCS-SiN film.¹³ Ex. 1004, 48, Fig. 6. Based on Figure 6, Tanaka states that “selectivity of RIE etching rate showed no significant deposition temperature dependence.” *Id.* at 47-2. From this result, Tanaka concludes that HCD-SiN has “enough ability for etching stopper.” *Id.*; see Pet. Reply 5 n.2 (quoting Tanaka).

Petitioner is correct that Patent Owner’s arguments demand more from the prior art disclosure in Tanaka than is provided by the sparse disclosure of the ’330 patent. Pet. Reply 5–6. Most of the information Patent Owner argues is missing from Tanaka to establish its suitability as an etch-stop layer is not disclosed by the ’330 patent. For example, the ’330 patent does not disclose etch chemistries, etch selectivity, or the thickness of the dielectric layers being etched. *Cf.* PO Resp. 31 (listing chemistry of the etchant and relative thickness of the materials as factors affecting suitability as an etch stop); *id.* at 21 (asserting that Tanaka does not disclose etch selectivity of HCD-SiN relative to any type of silicon oxide other than

¹³ Patent Owner explains that DCS-SiN film would be understood to be a conventional SiN material. PO Resp. 32.

TEOS-SiO). Nor does the '330 patent disclose any information regarding the barrier property of silicon nitride etch stop layers. *Cf.* PO Resp. 31 (asserting that the barrier property is “critical”). Tanaka provides at least as much, if not more, information than the '330 patent regarding suitability of low dielectric constant silicon nitride as an etch stop layer. Ex. 1004, 47-2, 48, Fig. 6 (“Selectivity of RIE etching rate versus TEOS”). The '330 patent’s sparse disclosure, as compared with Tanaka’s more detailed disclosure, persuades us that Tanaka’s disclosure is sufficient to provide a reasonable expectation of success of achieving the claimed invention. *See Trustees of Columbia Univ. in City of New York v. Illumina, Inc.*, 620 F. App’x 916, 929 (Fed. Cir. 2015) (relying on disclosure of challenged patent as substantial evidence sufficient to support PTAB’s finding of a reasonable expectation of success in combining prior art references and synthesizing the claimed nucleotide).

Next, Patent Owner criticizes Tanaka for not disclosing an “actual application” and faults Petitioner for not submitting evidence that “the HCD-SiN disclosed in Tanaka was ever implemented as an etch stop layer.” PO Resp. 30. Patent Owner’s criticisms are legally irrelevant to the question of reasonable expectation of success. The prior art does not need to disclose “actual success” in making the claimed invention. *AstraZeneca LP v. Breath Ltd.*, 603 F. App’x 999, 1002 (Fed. Cir. 2015). What is required is proof that “a skilled artisan would have perceived a reasonable expectation of success in making the invention in light of the prior art.” *Id.* (quoting *Amgen Inc. v. F. Hoffman–La Roche Ltd.*, 580 F.3d 1340, 1362 (Fed. Cir. 2009)). Under that standard, there is no requirement that a POSITA have a reasonable expectation of success in developing a commercial product.

Allergan, Inc. v. Sandoz Inc., 726 F.3d 1286, 1292 (Fed. Cir. 2013). And the teachings of the prior art should not be discounted merely because a prior art device or process “was not practical and could not be used successfully commercially.” *Trojan, Inc. v. Shat-R-Shield, Inc.*, Nos. 88-1528, 88-1529, 1989 WL 12862213, *2 (Fed. Cir. Oct. 31, 1989) (unpublished).

Next, Patent Owner argues “[l]ater research identified detrimental effects . . . which likely served as a deterrent that prevented adoption” of Tanaka’s HCD-SiN material. PO Resp. 31 (citing Ex. 2009 ¶ 110; Ex. 2010,¹⁴ 2, 4, Fig. 7; Ex. 2011,¹⁵ 1). Patent Owner’s characterization of Tanaka III and Mise as “later” is accurate. Both references were published after the filing date of the ’330 patent, which means they are not relevant to the issue of reasonable expectation of success at the time of the invention. *Bristol-Myers Squibb Co. v. Teva Pharm., Inc.*, 752 F.3d 967, 976 (Fed. Cir. 2014) (“[T]he skilled artisan’s reasonable expectation of success is measured ‘as of the date of the invention.’”) (quoting *Amgen*, 580 F.3d at 1362). Moreover, neither Patent Owner nor its expert explains how the later research (Exs. 2010, 2011) relates to a reasonable expectation of success for HCD-SiN film as an etch stop layer in copper damascene interconnect structures.

¹⁴ Masayuki Tanaka et al., *Suppression of SiN-Induced Boron Penetration by Using SiH-Free Silicon Nitride Films Formed by Tetraschlorosilane and Ammonia*, 49 IEEE Transactions in Electron Devices 1526–31 (2002) (“Tanaka III”).

¹⁵ N. Mise, et al., *Suppression of Gate-Edge Metamorphoses of Metal/High-k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact on Scaled MOSFETs*, Extended Abstracts of the 2007 Int’l Conf. on Solid State Devices and Materials, Tsukuba, 724–25 (2007) (“Mise”).

Next, Patent Owner compares etch selectivity for HCD-SiN with a dielectric constant below 5.5 to etch selectivity for conventional SiN material, as disclosed in Tanaka Figure 6. PO Resp. 32 (citing Ex. 1004, Figs. 5, 6; Ex. 2009 ¶ 112). Patent Owner draws no conclusion from this comparison, which does not rebut Petitioner’s showing of a reasonable expectation of success. Patent Owner asserts that a second Tanaka article “discloses that the etch rate of HCD-SiN in HF and the chemical mechanical polish rate are substantially higher at the temperatures used to form the low-k HCD-SiN layer.” *Id.* (citing Ex. 2012¹⁶). Patent Owner provides no pinpoint citation to Tanaka II and does not explain how its assertion about HF etch rate and chemical mechanical polish rate weighs against a finding of a reasonable expectation of success for Petitioner’s combination of the APA and Tanaka.

Next, Patent Owner argues that the dielectric constant of Tanaka’s HCD-SiN material is “unpredictable,” citing disclosures in Tanaka and Tanaka II, which Patent Owner contends show that the material reacts in “opposite ways” to changes in deposition temperature. PO Resp. 32–33 (citing Ex. 1004, 2, Fig. 5; Ex. 2012, 2286, Fig. 8; Ex. 2009 ¶ 115). Patent Owner’s contention is not supported by Tanaka Figure 5 and Tanaka II Figure 8, which do not show the same temperature range. Whereas Tanaka Figure 5 shows that permittivity (dielectric constant) decreases with increasing deposition temperature in the range from 250°C to 450°C, Tanaka II Figure 8 shows that permittivity (dielectric constant) increases

¹⁶ M. Tanaka et al., *Film Properties of Low-k Silicon Nitride Films Formed by Hexachlorodisilane and Ammonia*, J. Electrochem. Soc., v. 147, pp. 2284–2289 (2000) (“Tanaka II”).

with increasing deposition temperature in the range from 450°C to 700°C. Ex. 1004, 48, Fig. 5; Ex. 2012, 2286-2, Fig. 8. Both diagrams show a permittivity below 5.5 corresponding to a deposition temperature of 450°C. *Id.*

Next, Patent Owner argues that designing an etch stop layer would require experimentation and that differences in etch selectivity would affect etch stop layer thickness, which would in turn affect “the overall capacitance of the device.” PO Resp. 33 (citing Ex. 2009 ¶ 115; Ex. 2013, 58:18–53:4¹⁷). We have considered Patent Owner’s argument, but are nevertheless persuaded that Petitioner has shown a reasonable expectation of success for the combination of the APA and Tanaka. Neither Dr. Bottoms nor Mr. Maltiel characterizes the amount of necessary experimentation as undue or extraordinary. Furthermore, “the overall capacitance of the device” (PO Resp. 33) is irrelevant because device capacitance is not recited in the challenged claims. *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) (“correct inquiry” is whether there would have been “a reasonable expectation of achieving what is claimed in the patent-at-issue”).

Next, Patent Owner argues that changes in parameters, such as deposition rate, deposition pressure, deposition temperature, and layer thickness, would “likely affect” or “might affect” the dielectric constant of Tanaka’s HCD-SiN material. PO Resp. 19, 33 (citing Ex. 1004, 48, Fig. 2; Ex. 2009 ¶¶ 73, 117, 118; Ex. 2013, 49:12–50:11). Patent Owner’s arguments are inconsistent with the legal standard for a reasonable

¹⁷ Patent Owner’s cited page range makes no sense.

expectation of success, which does not require absolute certainty of success. *In re Kubin*, 561 F.3d 1351, 1360 (Fed. Cir. 2009) (“Obviousness does not require absolute predictability of success . . . all that is required is a reasonable expectation of success.”) (citing *In re O’Farrell*, 853 F.2d 894, 903–04 (Fed. Cir. 1988)); *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (“certainty of success” is not required).

Relying on Tanaka’s disclosures regarding copper and chlorine content of the HCD-SiN film, Patent Owner argues that a POSITA would have had “reason to doubt” the film’s barrier ability and its long-term stability in view of supposed problems with copper diffusion and corrosion. PO Resp. 20, 22–24, 26, 33–35 (citing Ex. 2009 ¶¶ 74, 75, 79, 116; Ex. 1004, 47-2, 48, Figs. 4, 7, and 8). Patent Owner’s argument is not supported by Tanaka, which does not describe any problem with copper diffusion or corrosion. We find that Patent Owner’s argument is contradicted by Tanaka’s express disclosure that HCD-SiN has “higher barrier ability for Cu diffusion than plasma-SiN” and its reliance on a bias-temperature stress test to show an improvement in the film’s ability to prevent copper diffusion. Ex. 1004, 47-1, 47-2, 48 (Fig. 8). We find that Patent Owner’s argument is further contradicted by Tanaka’s discussion of thermal stability tests, which Tanaka states that chlorine “was not detected over the detection limit up to 1000 °C, and is concluded to be thermally stable.” *Id.* at 47-2. Moreover, Patent Owner’s argument is inconsistent with the legal standard for a reasonable expectation of success, which does not require certainty of success. *Kubin*, 561 F.3d at 1360; *Medichem*, 437 F.3d at 1165.

After considering the parties’ arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance

of the evidence that a POSITA would have had a reasonable expectation of success of achieving the claimed subject matter by combining Tanaka's low dielectric constant silicon nitride etch stop film with the interconnect structure of the APA.

Accordingly, we are persuaded Petitioner has established by a preponderance of the evidence that claims 1 and 6 of the '330 patent are unpatentable as obvious in view of the APA and Tanaka.

2. *Claims 5 and 10*

Claim 5 depends from claim 1 and recites "wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof." Ex. 1001, 7:11–14. Claim 10 depends from claim 6 and recites "wherein the first and second conductor cores contain materials selected from a group consisting of copper, gold, silver, a compound thereof, and a combination thereof." *Id.* at 8:20–23.

Petitioner directs us to substantial evidence that the APA discloses the limitations of claims 5 and 10 by disclosing a conductor core made from copper. Pet. 14, 18, 27–28, 36 (citing Ex. 1001, 5:1–5, 4:42–5:19). Patent Owner does not contest that evidence and submits no arguments regarding claims 5 and 10 separately from its arguments regarding claims 1 and 6. See PO Resp. 37. We determine Petitioner has demonstrated by a preponderance of the evidence that the limitations of claims 5 and 10 are taught by the APA.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a

preponderance of the evidence that claims 5 and 10 of the '330 patent are unpatentable as obvious in view of the APA and Tanaka.

F. Petitioner's Challenge Based on Chooi and Tanaka

In view of our determination that Petitioner's challenge to claims 1, 5, 6, and 10 succeeds based on the combination of the APA and Tanaka, we do not reach Petitioner's challenge to claims 1, 5, 6, and 10 based on the combination of Chooi and Tanaka.

G. Petitioner's Challenges to Claims 2 and 7

Claim 2 depends from claim 1 and recites "wherein the etch stop layer is a multilayer structure." Ex. 1001, 7:3–4. Claim 7 depends from claim 6 and recites "wherein the via and channel etch stop layers are a multilayer structure." *Id.* at 8:12–13.

The Petition asserts that claims 2 and 7 are unpatentable as obvious in view of the APA, Tanaka, and Watatani. Pet. 19–21, 27, 35–36.

Alternatively, the Petition asserts that claims 2 and 7 are unpatentable as obvious in view of Chooi, Tanaka, and Watatani. *Id.* at 43–46, 48–49, 53–54. In the subsections below, we address, first, whether Petitioner has established that the limitations of claims 2 and 7 are taught or suggested by the prior art, and second, whether Petitioner has established a reason or motivation to combine the teachings of the prior art.

1. Multilayer silicon nitride etch stop

The Petition asserts that "a POSITA would know that silicon nitride when used as an etch stop can, and often is, deposited as a multilayer structure when grown/deposited," citing Mr. Maltiel's testimony, as well as disclosures in Watatani and Tanaka. Pet. 19–21, 27, 35–36, 43–45, 48–49,

53–54. In the Institution Decision, we found that “Tanaka nowhere suggests that the foregoing deposition process results in forming a multilayer silicon nitride structure.” Dec. 23. Patent Owner challenges Petitioner’s contention that Tanaka discloses a multilayer silicon nitride etch stop, arguing that Mr. Maltiel’s deposition testimony is untimely and “strains credibility.” PO Resp. 42–45 (citing Ex. 2013, 66:16–69:5, 71:11–72:6, 72:14–73:3, 73:18–24). In the Reply, Petitioner abandons the argument that Tanaka teaches a multilayer silicon nitride etch stop, relying solely on Watatani and Dr. Bottoms’ testimony to teach the limitations of claims 2 and 7. Pet. Reply 8–10, 13. At the oral hearing, Petitioner confirmed that it is no longer pursuing the theory that Tanaka discloses multiple layers of silicon nitride. Tr. 26:2–4. Accordingly, our analysis focuses on whether Petitioner has established that Watatani discloses or suggests a multilayer silicon nitride etch stop.

The Petition’s discussion of claims 2 and 7 and Watatani is the same as Mr. Maltiel’s declaration testimony. *Compare* Pet. 19–20, 43–45, with Ex. 1003 ¶¶ 37, 48, 57, 68. As in the Institution Decision, our analysis focuses on Mr. Maltiel’s testimony. Mr. Maltiel relies on Watatani and Tanaka as support for his testimony that a POSITA would have known that a silicon nitride etch stop is often grown or deposited as a multilayer structure. Ex. 1003 ¶¶ 37, 48, 57, 68. As just discussed, Petitioner has abandoned its contention that Tanaka teaches a multilayer silicon nitride etch stop. Absent support from Watatani, as discussed below, Mr. Maltiel’s testimony is entitled to little or no weight. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Regarding Watatani, Mr. Maltiel testifies:

Watatani explains that “SiON, SiN and SiON may be used for the etching stopper film 80”. And in Watatani it provides that such an etch stopper structure can include “three or more layers of... SiN [silicon nitride].”

Ex. 1003 ¶¶ 37, 48; *see also id.* ¶¶ 57, 68 (quoting same excerpts from Watatani in reverse order).

In the Institution Decision, we made the following preliminary findings of fact based on the record before us at that time:

Mr. Maltiel’s testimony is unsupported by Watatani to the extent it implies that “etching stopper film 80” can include three or more layers of silicon nitride. Instead, Watatani describes “first and second etching stopper films of respective, different compositions.” Ex. 1006, at (57); *see also id.* at 4:64–65 (disclosing the fabrication process includes the step of “forming a second, different etching stopper film on said first etching stopper film”). More particularly, Watatani describes etching stopper structure 81, which includes first etching stopper film 80 of SiN and second etching stopper film 82 of SiO₂. Ex. 1006, 6:4–11. Watatani discloses alternative materials for each of films 80 and 82. *Id.* at 6:18–27. In each instance, first etching stopper film 80 is formed of a different material than second etching stopper film 82 to allow for selective etching. *Id.*

Watatani discloses that “etching stopper structure 81 may include three or more layers of SiO₂, SiN or SiC.” Ex. 1006, 7:54–55. However, Watatani does not suggest that etching stopper structure 81 may include three or more layers of the same material, such as silicon nitride. That would be contrary to Watatani’s disclosure that the first and second etching stopper films have “different compositions.” *Id.* at (57). And it would also be contrary to Watatani’s teaching that second etching stopper film 82 is selectively etched relative to first etching stopper film 80. *Id.* at 6:31–40, Fig. 5B; *see also id.* at 4:66–67 (disclosing the fabrication process includes the step of

“forming a first opening in said second etching stopper film so as to expose said first etching stopper film”); *see also* Ex. 2001 ¶ 84.

Neither Petitioner nor Mr. Maltiel addresses Watatani’s teaching that the first and second etching stopper films have different compositions. *Id.* at (57), 4:62–65, 6:4–11, 6:18–27. Nor do Petitioner and Mr. Maltiel address Watatani’s teaching that the second etching stopper film is selectively etched relative to the first etching stopper film. *Id.* at 4:66–67, 6:31–40, Fig. 5B. We, therefore, are not persuaded that Watatani supports Petitioner’s contention that a multilayer silicon nitride etch stop would have been known to a POSITA.

Dec. 22–23.

Patent Owner agrees with our preliminary findings regarding Watatani. PO Resp. 46; *see also id.* PO Resp. 39–40 (summarizing Watatani’s disclosure regarding a two-layer etch stop structure with etch selectivity between the layers); Ex. 2009 ¶¶ 85, 129 (Dr. Bottoms’ testimony regarding Watatani). According to Patent Owner and Dr. Bottoms, “Watatani only contemplates etching stopper structures 81 that have at least one upper layer that is selectively etched relative to the lower layers of the etching stop structure 81.” PO Resp. 46–47; Ex. 2009 ¶ 129.

Petitioner does not identify error in our preliminary findings regarding Watatani, as reproduced above from the Institution Decision. Pet. Reply 8–10, 13. Instead, Petitioner changes the thrust of its contention by asserting that “Watatani’s teaching encompasses a layer of SiO₂ on top of a layer of SiN on top of another layer of SiN.” *Id.* at 8. According to Petitioner, “including another layer of SiN underneath SiN layer 80 would not affect the etch selectivity required by Watatani.” *Id.* at 8–9. Petitioner contends that “Watatani discloses a range of etching stopper structures” and an

“etching stop layer of SiO₂/SiN/SiN is well within that disclosed range.” *Id.* at 9. Petitioner also relies on Dr. Bottoms’ deposition testimony to argue that deposition of multiple layers of the same material on top of each other was known in the art. *Id.* at 9–10 (citing Ex. 1011, 70:3–10).

After considering the parties’ arguments and evidence and the record as a whole, we are not persuaded Petitioner has established based on the evidence in this case¹⁸ that a multilayer silicon nitride etch stop would have been known to a POSITA. Petitioner relies on Watatani and the testimony of Mr. Maltiel and Dr. Bottoms. Pet. 19–20, 43–45; Pet. Reply 8–10, 13. We have addressed Mr. Maltiel’s testimony above. Regarding Watatani, we adopt the unchallenged findings reproduced above from the Institution Decision. In the Reply, Petitioner continues to rely on Watatani’s teaching that “etching stopper structure 81 may include three or more layers of SiO₂, SiN or SiC.” *Id.* at 8; Ex. 1006, 7:54–55. Petitioner contends this teaching “encompasses” a layer of SiO₂ on top of a layer of SiN on top of another layer of SiN, i.e., SiO₂/SiN/SiN. Pet. Reply 8–9.

We find that Watatani’s disclosure regarding “three or more layers” (Ex. 1006, 7:54–55) is vague, ambiguous, and not sufficient to suggest the structure posited by Petitioner. We agree with Patent Owner and Dr. Bottoms that the only specific embodiment of a three-layer etch stop disclosed by Watatani uses SiO₂, amorphous silicon, or TiN as upper etch stopper layer 82 and a stacking of SiC and SiO₂ for lower etch stopper layer 80. PO Resp. 47; Ex. 2009 ¶ 129; Ex. 1006, 6:18–30. In this embodiment, the composition of each layer is different from the composition of the

¹⁸ See page 39, *infra*, distinguishing *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01566.

adjacent layer(s). Petitioner does not direct us to any teaching or suggestion in Watatani that adjacent layers should be made of the same material, such as silicon nitride. Nor does not Petitioner offer any evidence of why such a structure would be beneficial in Watatani.

Petitioner also relies on Dr. Bottoms' deposition testimony. Pet. Reply 9–10 (citing Ex. 1011, 70:3–10, 70:20–71:3). The cited testimony is reproduced below:

Q. In the 2001 time frame, would it have been known to one of ordinary skill in the art that you could deposit multiple layers of the same material on top of each other?

A. Yeah, that was probably known in the 50s. There is nothing novel about depositing multiple layers, if there is some reason to do it.

Ex. 1011, 70:3–10.

Q. . . . Let's put it in the context of dielectric materials in semiconductor structure. Were there reasons known to one of skill in the art why you might want to put multiple layers of the same dielectric material?

A. Well, certainly, the author of the '511 patent [Watatani] knew it. . . .

Id. at 70:20–71:3. The above-quoted testimony fails to fill the gap left by Watatani and provides no reason why a POSITA would have made an etch stop layer by depositing multiple layers of silicon nitride, one on top of the other. Even if the cited testimony is read as pertaining to silicon nitride, Dr. Bottoms at most admits that silicon nitride *could* have been deposited in multiple layers, but does not admit that a POSITA *would have had a reason* to do so in the context of an etch stop layer. *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068 (Fed. Cir. 2018) (rejecting the Board's analysis where "the Board focused on what a skilled artisan would have

been *able* to do, rather than what a skilled artisan would have been *motivated* to do at the time of the invention”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”). Dr. Bottoms’ testimony that “the author of the ’511 patent [Watatani] knew it” is vague, ambiguous, and fails to provide a substantive reason for using a multilayer structure for a silicon nitride etch stop, especially in view of the limitations of Watatani’s disclosure, as discussed above.

In view of the foregoing, we find that the testimony of Mr. Maltiel and Dr. Bottoms and the disclosure of Watatani, whether considered individually or collectively, are not sufficient to meet Petitioner’s burden to show that a multilayer silicon nitride etch stop layer was known in the art.

We are aware that we previously held that the subject matter of claims 2 and 7 of the ’330 patent would have been obvious in view of Watatani and Tanaka based on the record before us in Case IPR2017-01566. The record before us now is substantially different from the record before us in Case IPR2017-01566. Most importantly, the record in Case IPR2017-01566 included substantial evidence that it was known in the art to deposit silicon nitride as a multilayer structure, including for use as an etch stop layer, in order to improve film uniformity and dielectric properties by reducing the appearance and effects of pin-holes. *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01566 (PTAB Jan. 14, 2019) (Paper 24), 37–41 (discussing the Novellus Concept One Chemical Vapor Deposition system and other evidence). Although Petitioner contends that

“a POSITA would know that silicon nitride when used as an etch stop can, and often is, deposited as a multilayer structure when grown/deposited” (*see, e.g.,* Pet. 19), Petitioner relies solely on the testimony of Mr. Maltiel and Dr. Bottoms and the disclosure of Watatani, which are insufficient to meet Petitioner’s burden of proof for the reasons discussed above.

2. *Motivation to combine*

The Petition provides the following contentions regarding motivation to combine:

Because Watatani is also in the same technological field as Tanaka and the Admitted Prior Art, a POSITA would have either known that silicon nitride could be formed in a multilayer structure, or looked to Watatani to see that it was well known before the time of the ’330 patent and would have been motivated to combine Watatani with the Admitted Prior Art and Tanaka to form a multilayer structure.

Pet. 20, 21; *see also* Ex. 1003 ¶¶ 37, 48 (same).

Because Watatani is also in the same technological field as Tanaka and Chooi, a POSITA would have either known that silicon nitride could be formed in a multilayer structure, or looked to Watatani to see that it was well known before the time of the ’330 patent and would have been motivated to combine Watatani with Chooi and Tanaka to form a multilayer structure.

Pet. 44, 45–46; *see also* Ex. 1003 ¶¶ 57, 68 (same).

Patent Owner challenges the sufficiency of Petitioner’s analysis of motivation to combine. PO Resp. 47–51, 61–62.

In the Reply, Petitioner asserts:

It is undisputed that Watatani is directed to the dual damascene process that is represented by the Admitted Prior Art. . . . In light of these admissions, it would have been obvious to apply the teachings of Watatani to the Admitted Prior Art. Likewise,

there is no evidence that Tanaka teaches away from the use of multilayered structures; thus, there is no reason why a POSITA would not use the low-k film of Tanaka in the dual damascene structure of the Admitted Prior Art with the multilayer etch stopping layer taught by Watatani.

Pet. Reply 10 (citing Ex. 1006, 4:48–54). Petitioner contends “there would have been the same motivation to use [Watatani’s multilayer etch stop] structure with Chooi as with the Admitted Prior Art.” *Id.* at 13.

Even accepting Petitioner’s contention that Watatani teaches an etch stop layer having a layer of SiO₂ on top of a layer of SiN on top of another layer of SiN, i.e., SiO₂/SiN/SiN (Pet. Reply 8–9), we agree with Patent Owner that Petitioner’s arguments and evidence are not sufficient to establish a reason or motivation for combining Watatani’s teaching with either the APA or Chooi, as modified by Tanaka. PO Resp. 48.

Petitioner’s assertion that Watatani is in the same technological field as Tanaka, the APA, and Chooi (Pet. 20, 21, 44, 45) is not sufficient to establish a reason to combine. *Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. July 14, 2017) (“[A] broad characterization of [prior art references] as both falling within the same alleged field . . . without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion.”).

Although Petitioner asserts that Watatani is directed to the dual damascene process represented by the APA (Pet. Reply 10), Watatani’s teaching of a multilayer etch stop structure relates to a **different type** of dual damascene structure—one that has an organic interlayer insulation film instead of an inorganic interlayer insulation film, as in the APA and Tanaka. *Compare* Ex. 1006, 2:54–64, 4:48–54, 7:43–50, 7:54–55 (Watatani), *with*

Ex. 1001, 1:41–44, 2:39–41 (APA) *and* Ex. 1004, 48, Fig. 1 (Tanaka). As Patent Owner and its declarant explain, Watatani’s multilayer etch stop structure solves a problem that arises only when organic insulator layers are used, not when inorganic insulators, such as silicon dioxide, are used. PO Resp. 38–39, 49; Ex. 2009 ¶¶ 81–83. Unrebutted testimony of Dr. Bottoms establishes that the purpose of Watatani’s multilayer etch stop structure is to improve the process of forming dual damascene structures using organic interlayer dielectrics. Ex. 2009 ¶¶ 85–86. Petitioner’s assertion of obviousness fails to account for this difference between Watatani, on the one hand, and the APA and Tanaka, on the other hand. Petitioner offers no reason or explanation for why a POSITA would have considered Watatani’s multilayer etch stop structure to be applicable, useful, or beneficial in a dual damascene structure that does not have organic dielectric layers. Petitioner relies on “the same motivation” for its Chooi-based combination as for the APA-based combination (Pet. Reply 13) and provides no reason or explanation for why a POSITA would have considered Watatani’s multilayer etch stop structure to be applicable, useful, or beneficial in the dual damascene structure of Chooi.

The remainder of Petitioner’s contentions regarding motivation to combine are merely conclusory and improperly seek to shift the burden to Patent Owner. For example, Petitioner asserts that a POSITA “would have been motivated to combine Watatani with the Admitted Prior Art and Tanaka to form a multilayer structure,” but provides no reasoned explanation for why that is the case. Pet. 20, 21. Similarly, Petitioner contends “it would have been obvious to apply the teachings of Watatani to the Admitted Prior Art,” but provides no reason other than its flawed assertion that

Watatani is directed to the dual damascene process represented by the APA. Pet. Reply 10. Petitioner’s conclusory assertions fall far short of the standard required to establish obviousness. *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (motivation to combine requires a “reasoned explanation”; “conclusory statements’ alone are insufficient”); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”).

Furthermore, Petitioner asserts that “there is no evidence that Tanaka teaches away from the use of multilayered structures” and “no reason why a POSITA would not use . . . the multilayer etch stopping layer taught by Watatani” with the low-k film of Tanaka in the dual damascene structure of the APA. Pet. Reply 10. These assertions are an improper attempt to shift the burden to Patent Owner to show teaching away or a reason not to combine the prior art. Petitioner’s approach is inconsistent with the burden of proof that applies in an *inter partes* review. As our reviewing court has explained:

Where, as here, the only question presented is whether due consideration of the four Graham factors renders a claim or claims obvious, no burden shifts from the patent challenger to the patentee. This is especially true where the only issues to be considered are what the prior art discloses, whether there would have been a motivation to combine the prior art, and whether that combination would render the patented claims obvious.

Magnum Tools, 829 F.3d at 1376.

3. *Conclusion regarding claims 2 and 7*

Accordingly, for all of the foregoing reasons, we are not persuaded that Petitioner has met its burden of proof to establish that claims 2 and 7 of the '330 patent are unpatentable based on either: (1) the APA, Tanaka, and Watatani, or (2) Chooi, Tanaka, and Watatani.

III. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 1, 5, 6, and 10 of the '330 patent are unpatentable. Petitioner has not shown by a preponderance of the evidence that claims 2 and 7 of the '330 patent are unpatentable.

IV. ORDER

Accordingly, in consideration of the foregoing, it is hereby:

ORDERED that, based on a preponderance of the evidence, claims 1, 5, 6, and 10 of the '330 patent are unpatentable;

FURTHER ORDERED that, on the record before us, Petitioner has not shown by a preponderance of the evidence that claims 2 and 7 of the '330 patent are unpatentable;

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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PETITIONER:

Vincent Yip
Peter J. Wied
NIXON PEABODY LLP
vyip@nixonpeabody.com
pwied@nixonpeabody.com

PATENT OWNER:

Nicholas T. Peters
Timothy P. Maloney
David Gosse
FITCH, EVEN, TABIN & FLANNERY LLP
ntpete@fitcheven.com
tim@fitcheven.com
dgosse@fitcheven.com