

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NANYA TECHNOLOGY CORPORATION,
NANYA TECHNOLOGY CORPORATION U.S.A., and
NANYA TECHNOLOGY CORPORATION DELAWARE,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2018-00065
Patent 6,103,611

Before GRACE KARAFFA OBERMANN, KRISTINA M. KALAN, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION

Finding Claims 1–5 and 8–12 Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Nanya Technology Corporation, Nanya Technology Corporation U.S.A., and Nanya Technology Corporation Delaware (collectively, “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–5, 8–12, and 15 of U.S. Patent No. 6,103,611 (Ex. 1001, “the ’611 patent”). Paper 1 (“Pet.”). Lone Star Silicon Innovations, LLC¹ (“Patent Owner”) filed a Notice Waiving Preliminary Response. Paper 5. We instituted an *inter partes* review of claims 1–5, 8–12, and 15 on all grounds of unpatentability alleged in the Petition. Paper 7 (“Institution Decision” or “Inst. Dec.”).

After institution of trial, Patent Owner filed a Patent Owner Response. Paper 12 (“PO Resp.”). Petitioner filed a Reply. Paper 15 (“Reply”). An oral hearing was held on January 24, 2019. A transcript of the hearing is included in the record. Paper 21 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has established by a preponderance of the evidence that claims 1–5 and 8–12 of the ’611 patent are unpatentable, but has failed to establish that claim 15 of the ’611 patent is unpatentable.

A. *Related Proceedings*

The parties identify a number of proceedings as related, including: *Lone Star Silicon Innovations LLC v. Nanya Technology Corp.*, Case No. 3:17-cv-04032 (N.D. Cal.) (dismissed without prejudice) and *Lone Star*

¹ Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 4, 1.

Silicon Innovations, LLC v. Nanya Technology Corp., Appeal No. 2018-1581 (Fed. Cir. Feb. 15, 2018). Paper 6, 2; Paper 20, 2.

The '611 patent was also challenged in Cases IPR2017-01563 and IPR2017-01872. In both these cases, the Board found claims 1–5, 8–12, and 15 of the '611 patent unpatentable. *Micron Tech., Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01563 (PTAB Dec. 17, 2018) (Paper 29); *Renesas Elecs. Corp. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01872 (PTAB Apr. 7, 2019) (Paper 30).

B. The '611 Patent

The '611 patent, titled “Methods and Arrangements for Improved Spacer Formation Within a Semiconductor Device,” was filed December 18, 1997, and issued August 15, 2000. Ex. 1001, at [22], [45], [54]. The '611 patent relates to increasing the process control during the formation of spacers within a semiconductor device. *Id.* at [57].

As described in the '611 patent, a problem existed in the prior art in which uneven spacing between gate conductors could lead to spacers formed adjacent thereto having inconsistent widths, which “can have a deleterious effect on the semiconductor device being fabricated.” *Id.* at 5:22–62.

Figure 2a of the '611 patent is reproduced below.

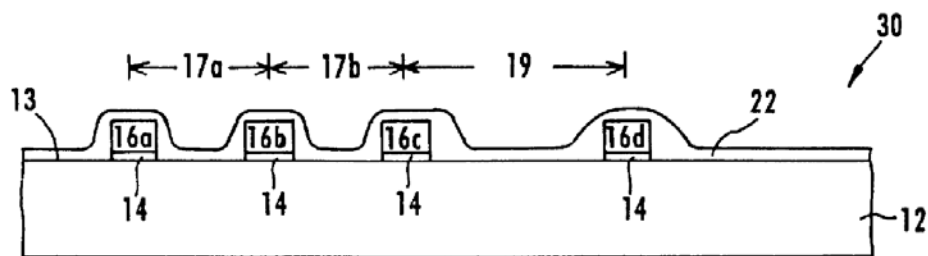


Fig. 2a (PRIOR ART)

Figure 2a, above, shows a portion of a prior-art semiconductor device. *Id.* at 3:59–62. In the device of Figure 2a, gate conductors 16a, 16b, 16c, 16d are formed on substrate 12. *Id.* at 5:23–26. Thin oxide layer 14 is formed on top surface 13 of substrate 12, and gate conductors 16a, 16b, 16c, 16d are formed on thin oxide layer 14. *Id.* at 5:8–10. Dielectric layer 22 is a “conformal dielectric layer or film that is deposited across the exposed surfaces of substrate 12 (on top surface 13) and over the exposed surfaces of gate conductors 16a–d.” *Id.* at 5:36–39. As seen in Figure 2a, the center points of gate conductors 16a and 16b are separated by space 17a; the center points of gate conductors 16b and 16c are separated by space 17b; the center points of gate conductors 16c and 16d are separated by space 19. *Id.* at 5:26–33.

Figure 2b of the '611 patent is reproduced below.

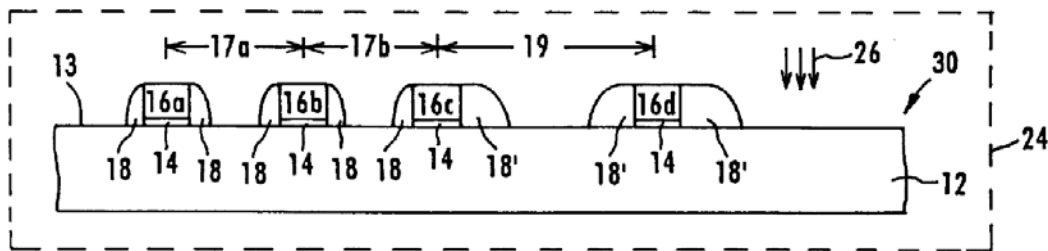


Fig. 2b (PRIOR ART)

Figure 2b, above, shows a portion of a prior-art semiconductor device following formation of spacers 18, 18'. *Id.* at 3:63–65. In the device of Figure 2b, gate conductors 16a, 16b, 16c, 16d are formed on substrate 12. *Id.* at 5:23–26. The center points of gate conductors 16a and 16b are separated by space 17a; the center points of gate conductors 16b and 16c are separated by space 17b; the center points of gate conductors 16c and 16d are separated by space 19. *Id.* at 5:26–33. As seen in Figure 2b, space 19 is

larger than spaces 17a and 17b. *Id.* at 5:31. As a result, “the spacers 18’ formed within second space 19 are differently shaped and have a wider width at their base than the spacers 18 formed, for example, in first spaces 17a and 17b.” *Id.* at 5:51–54.

In order to solve this problem, the ’611 patent teaches using non-operational transistor gate arrangements to divide the larger space into more equal smaller spaces “to provide more uniformity in the spaces/aspect ratios between gate conductors.” *Id.* at 6:9–25.

Figures 4a and 4b of the ’611 patent are reproduced below.

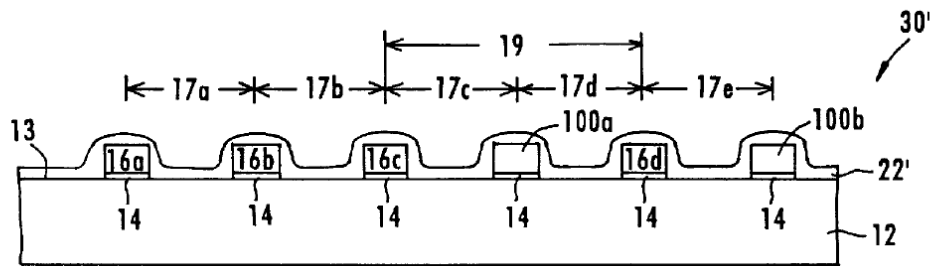


Fig. 4a

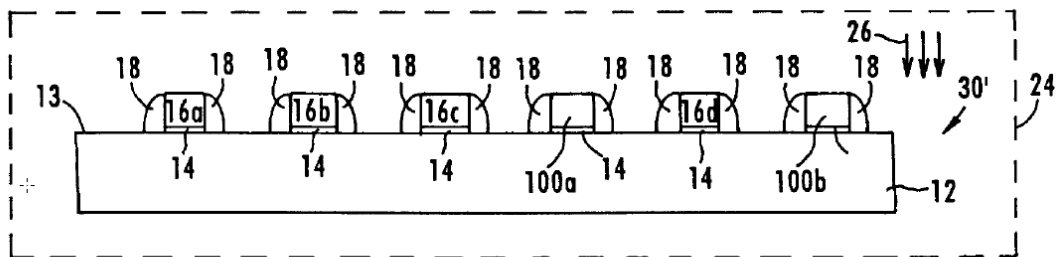


Fig. 4b

Figures 4a and 4b, above, show steps in a process for forming “substantially uniformly sized spacers” in a semiconductor device, in accordance with embodiments of the ’611 patent. *Id.* at 4:3–13. In the device of Figure 4a, gate conductors 100a, 100b are formed on substrate 12, in addition to gate conductors 16a, 16b, 16c, 16d previously described with respect to the prior

art device of Figure 2b. *Id.* at 6:9–14. The addition of gate conductor 100a, for example, “effectively divide[s] second space 19 into two first spaces 17c and 17d, which are each substantially equivalent to first spaces 17a and 17b.” *Id.* at 6:15–17. As described in the ’611 patent, “[t]he result of adding these additional non-operational transistor gate arrangements is that the topology . . . has been altered to provide more uniformity in the spaces/aspect ratios between gate conductors.” *Id.* at 6:21–25.

Shown in Figure 4a, dielectric layer 22’ is deposited over substrate 12 and gate conductors 16a, 16b, 16c, 16d, 100a, 100b, using conventional processes. *Id.* at 6:26–30. Shown in Figure 4b, dielectric layer 22’ is subjected to anisotropic etching plasma 26, resulting in the formation of spacers 18. *Id.* at 6:34–40. Due to the uniformity in the spaces/aspect ratios between gate conductors in this embodiment, spacers 18 “have substantially uniformly sized widths.” *Id.* at 6:47–49. In turn, “the source and drain regions 20a and 20b [of the semiconductor device] (not shown in FIG. 4b) will be more uniformly shaped and sized.” *Id.* at 6:49–51. Non-operational gate conductors 100a, 100b may be removed (*id.* at 6:52–63, Fig. 5a), or may remain in the complete semiconductor device (*id.* at 6:64–7:2).

C. Illustrative Claim

Of the challenged claims, claims 1, 8, and 15 are independent. Claims 2–5 depend, directly or indirectly, from claim 1, and claims 9–12 depend directly from claim 8. Independent claim 1 of the ’611 patent is illustrative of the challenged claims and is reproduced below.

1. A method for forming substantially uniformly sized spacers on transistor gate arrangements within semiconductor devices on a common substrate, the method comprising:

forming a plurality of gate arrangements on a top surface of the substrate, wherein two of the plurality of gate arrangements are positioned parallel to one another and separated by a defined space;

forming a dielectric layer over at least a portion of the two gate arrangements and at least a portion of the defined space;

removing portions of the dielectric layer to form a plurality of spacers, wherein each of the plurality of spacers physically contacts one of the two gate arrangements and the substrate, and wherein the spacers located within the defined space each have a base width that is approximately the same;

configuring one of the two gate arrangements to control an electrical current between a source region and a drain region formed in the substrate; and

configuring the remaining one of the two transistor gate arrangements to be non-operational.

Ex. 1001, 7:65–8:18.

D. References Relied Upon by Petitioner

Petitioner relies on the following references. Pet. 3–4.

Reference	Publication Date / Issue Date	Exhibit
JP Publ. No. H02-37725 (“Yonemaru”)	Feb. 7, 1990	Ex. 1004 ²
JP Publ. No. H09-64195 (“Haribuchi”)	Mar. 7, 1997	Ex. 1005 ³
U.S. Patent No. 5,410,161 (“Narita”)	Apr. 25, 1995	Ex. 1006
U.S. Patent No. 5,112,761 (“Matthews”)	May 12, 1992	Ex. 1007
U.S. Patent No. 6,130,139 (“Ukeda”)	Nov. 25, 1997	Ex. 1008

² Exhibit 1004 includes the original Japanese language document and a certified translation thereof. Citations to Yonemaru are to the translation.

³ Exhibit 1005 includes the original Japanese language document and a certified translation thereof. Citations to Haribuchi are to the translation.

Reference	Publication Date / Issue Date	Exhibit
Neil Weste & Kamran Eshraghian, Principles Of CMOS VLSI Design, A Systems Perspective (1985) (“Weste”)	1985	Ex. 1014

Petitioner relies on the Declaration of Ron Maltiel, Ph.D. (Ex. 1003) to support its positions. Patent Owner relies on the Declaration of W.R. Bottoms, Ph.D. (Ex. 2001) to support its positions.

E. Instituted Grounds of Unpatentability

We instituted an *inter partes* review of claims 1–5, 8–12, and 15 of the ’611 patent on the following grounds. Inst. Dec. 9, 24–25.

References	Basis	Claims Challenged
Admitted Prior Art ⁴ in view of Dummy Gate References ⁵	§ 103	1–5, 8–12, 15
Admitted Prior Art in view of Yonemaru	§ 103	1–5, 8–12, 15
Yonemaru in view of Haribuchi and Weste	§ 103	1–5, 8–12

⁴ Petitioner relies on Figures 2a and 2b of the ’611 patent, which are identified as prior art, and the corresponding discussion thereof. *See* Pet. 20, 23–48. Patent Owner does not contest Petitioner’s reliance on Figures 2a and 2b as prior art forming the basis of Petitioner’s Ground 1 or Ground 2 challenge. *See generally* PO Resp. Petitioner also relies on Figure 6a of the ’611 patent (*see* Pet. 48–51), but as discussed *infra* Section II.D.2.b, Petitioner has not established that Figure 6a of the ’611 patent is admitted prior art.

⁵ Petitioner characterizes Haribuchi, Yonemaru, Matthews, Ukeda, and Narita, collectively, as the “Dummy Gate References.” *See* Pet. 8–9.

II. ANALYSIS

A. Claim Construction

The parties agree that the '611 patent expired during this proceeding, and that the claim construction principles outlined in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) apply. Pet. 18; PO Resp. 7–8; *see also* Inst. Dec. 4, 9–10. We, therefore, adopt a district court-type claim construction approach. *Wasica Finance GmbH v. Continental Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017) (“The Board construes claims of an expired patent in accordance with *Phillips v. AWH Corp.*”).

Under the *Phillips* standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

In the Petition, Petitioner applies “the claim construction principles outlined in the *Phillips* case to interpret a few relevant claim terms.” Pet. 18. Patent Owner “agrees with Petitioner[] that all claim terms should be accorded their plain and ordinary meaning as understood by a person having ordinary skill in the art and as consistent with the intrinsic record.” PO Resp. 8. Patent Owner also notes Petitioner’s partial construction for the claim term “transistor gate arrangement,” but submits that a construction of this term is not needed. *Id.* (citing Pet. 18–19). After considering the parties’ arguments and evidence, we determine that it is not necessary to provide an express construction for any claim term for purposes of resolving the controversy. *See, e.g., Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d

1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art

would have had at least a Bachelor of Science degree in electrical engineering, physics, chemistry, chemical engineering, material science, or a closely related field and at least 5 years of experience in semiconductor fabrication. Additional appropriate graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education.

Pet. 17

Patent Owner asserts that a person of ordinary skill in the art

would have held a master’s degree in physics, electrical engineering or a related field and three years or more experience working with the technologies implemented in semiconductor devices and the fabrication of semiconductor devices. (*See* Ex. 2001 at ¶ 30.) Design experience is necessary with respect to changes in process and parameters in the semiconductor device and to the effects of those changes on the device as a whole. (*See, e.g., id.* at ¶¶ 30, 36.)

PO Resp. 6–7.

For the purposes of our Institution Decision, we accepted Petitioner’s contentions regarding the level of ordinary skill in the art. Inst. Dec. 11. Neither party argues that the outcome of this case would differ based on our adoption of one party’s definition over the other, and we see little difference between the parties’ definitions. PO Resp. 6–7; *see generally* Reply. In light of the record now before us and consistent with the Institution Decision, we adopt Petitioner’s definition of one of ordinary skill in the art.

The level of ordinary skill in the art is also reflected by the references themselves. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (“[T]he absence of specific findings on the level of skill in the art does not give rise to reversible error ‘where the prior art itself reflects an appropriate level and a need for testimony is not shown.’”); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (finding that the Board of Patent Appeals and Interferences did not err in concluding that the level of ordinary skill in the art was best determined by the references of record).

C. Overview of the Asserted References

Below we provide an overview of the Admitted Prior Art (“APA”), Yonemaru, and Haribuchi. An overview of the remaining references is unnecessary for purposes of this Decision.

1. Admitted Prior Art

As noted above, Petitioner relies on Figures 2a and 2b of the ’611 patent, which are expressly identified as prior art, and the corresponding discussion thereof as Admitted Prior Art. *See* Pet. 20, 23–48; Ex. 1001, 3:55–4:2, 5:2–6:2, Figs. 1, 2a, 2b, 3. The prior art described in the ’611 patent, as illustrated in Figures 2a and 2b, is discussed above. *See supra* Section I.B.

2. Yonemaru

Yonemaru relates to a manufacturing method for a semiconductor device. Ex. 1004, 121. In particular, Yonemaru describes forming a plurality of transistors, each having the same characteristics, by forming side walls (or, in other words, spacers) having the same shape at the sides of each gate electrode. *Id.* at 122. Yonemaru accomplishes this by using dummy gate electrodes between the gate electrodes. *Id.*

The manufacturing process of Yonemaru is discussed in more detail with respect to Figures 1(A)–1(E). Figure 1(A) is reproduced below.

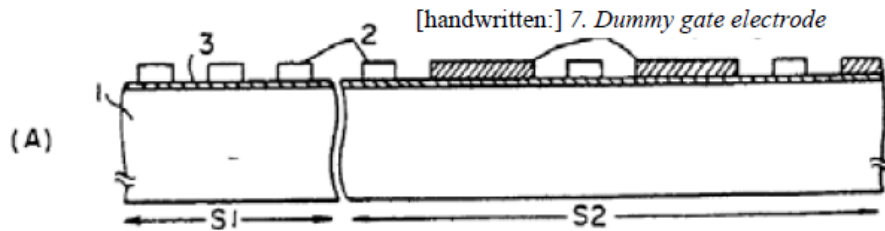


Figure 1(A), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* Gate electrodes 2 and dummy gate electrodes 7 are formed over gate oxide film 3 on semiconductor substrate 1. *Id.* As described in Yonemaru, the spacing between gate electrodes 2 may be 0.9 μm in closely spaced portion S1 and 4.5 μm in widely spaced portion S2. *Id.* Dummy gate electrode 7 is positioned in such a way as to intervene between gate electrodes 2 at widely spaced portion S2, and, furthermore, is positioned such that its distance from gate electrodes 2 is 0.9 μm , or the distance between gate electrodes 2 at closely positioned portion S1. *Id.* Yonemaru notes that dummy gate electrode 7 serves no purpose in the semiconductor integrated circuit, and is not used as wiring. *Id.* at 123.

After formation of source/drain zone 5 (*see id.* at Fig. 1(B)), a PSG (Phospho Silicate Glass) film, for example, is deposited over the entire surface (*id.* at 122–123), as seen in Figure 1(C), reproduced below.

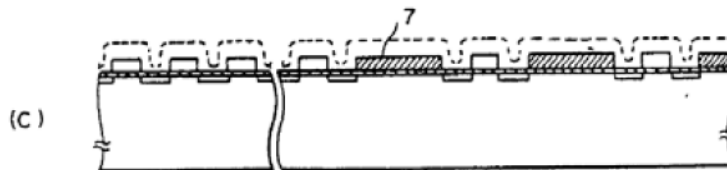


Figure 1(C), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* at 122. As seen in Figure 1(C), the “placement of a dummy gate electrode 7 causes PSG film to be deposited in the same shape at closely spaced portion S1 and widely spaced portion S2.” *Id.* at 123.

Figure 1(D) is reproduced below.

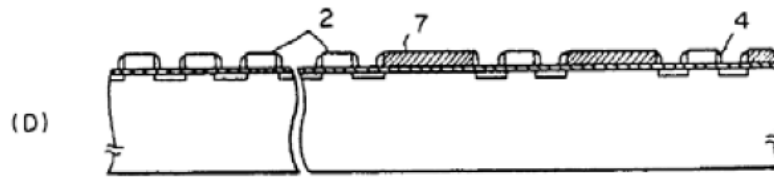


Figure 1(D), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Yonemaru. *Id.* at 122. As shown in Figure 1(D), side walls 4 are formed at the sides of gate electrodes 2 and dummy gate electrodes 7, by anisotropically etching the PSG film. *Id.* at 123. Because PSG film has already been deposited in the same shape at both the closely and widely spaced portions S1 and S2 during the above-described process, side wall 4 is also formed to the same shape. *Id.* Source/drain zone 6 (*see id.* at Figure 1(E)) is subsequently formed. *Id.*

3. Haribuchi

Haribuchi relates to a method of manufacturing a “semiconductor device having elements with uniform properties . . . irrespective of gate electrode layout.” Ex. 1005, at [57]. Haribuchi accomplishes this goal using “dummy gate electrodes that do not function as gate electrodes” in order to “mak[e] widths of side wall spacers [] of the gate electrodes [] equal . . . , irrespective of the layout density of the gate electrodes.” *Id.*; *see also id.*

¶ 29 (“With the method for manufacturing a field effect semiconductor

device as in claim 1, the width of the side wall spaces of the gate electrodes is the same in the first and second areas even if the gate electrode layout density is different in the first and second areas, making it possible to form so-called LDD layers or pocket layers, etc., that have equal channel-length widths in the first and second areas, which makes it possible to manufacture a field effect semiconductor device having elements with uniform properties in an integrated circuit, irrespective of gate electrode layout.”).

The manufacturing process of Haribuchi is discussed in more detail with respect to Figures 1(a)–1(c). Figure 1(a) is reproduced below.

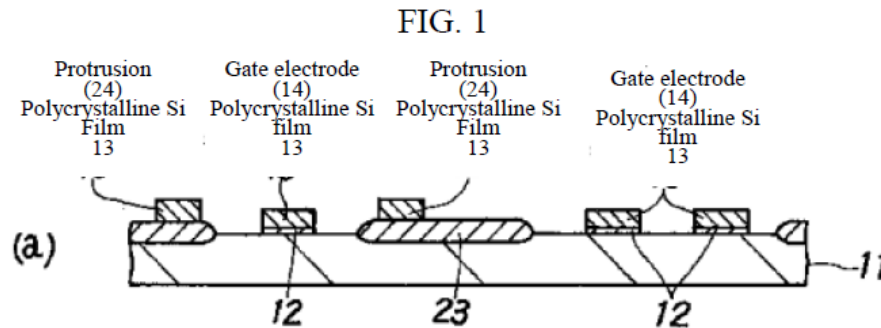


Figure 1(a), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Haribuchi. Gate electrodes 14 and protrusions 24 are formed over SiO_2 gate oxidation film 12 and SiO_2 film 23, respectively, on Si substrate 11. *Id.* ¶¶ 18–19. As described in Haribuchi, “protrusions 24 . . . serve as dummy gate electrodes that do not function as gate electrodes [and] are formed together with gate electrodes 14 . . . , resulting in a uniform overall layout density for the gate electrodes 14 and the protrusions 24 in all MOS transistor formation areas. *Id.* ¶ 19.

Thereafter, SiO_2 film 16 is deposited on the entire surface (*see id.* at Fig. 1(b)), and then the entire surface of SiO_2 film 16 is subjected to

anisotropic etching, thereby forming side wall spacers 17, as shown in Figure 1(c), reproduced below.

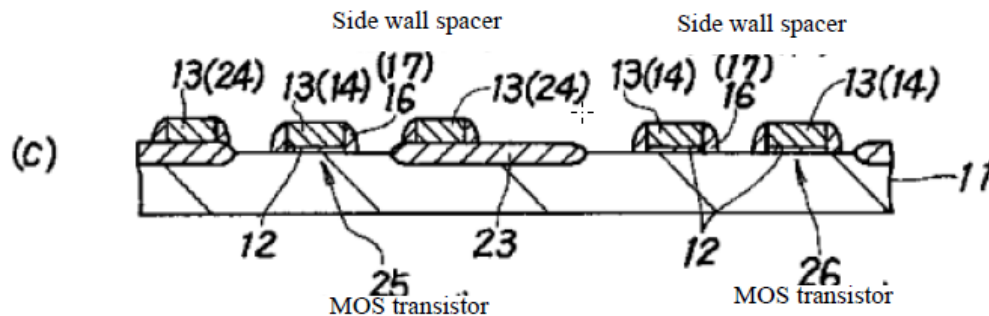


Figure 1(c), above, is a cross-section of a semiconductor device, showing a step in the manufacturing process according to Haribuchi. As described in Haribuchi, the layout density of the gate electrodes 14 is different between the MOS transistors 25 and 26, “but the overall layout density of the gate electrodes 14 and the protrusions 24 is the same where the MOS transistors 25 and 26 are formed, and therefore the width of the side wall spacers 17 is the same in the MOS transistors 25 and 26.” *Id.* ¶ 22. This uniformity of the width of side wall spacers 17 results in MOS transistors 25, 26 “having uniform properties.” *Id.* ¶ 23.

D. Analysis

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John*

Deere Co., 383 U.S. 1, 17–18 (1966). We note that, during this proceeding, the parties did not direct our attention to any objective evidence of non-obviousness.

In that regard, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007).

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Petitioner must demonstrate obviousness by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). A party that petitions the Board for a determination of obviousness must show that “a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *Procter & Gamble Co. v. Teva Pharm. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (quoting *Pfizer, Inc. v. Apotex, Inc.*, 408 F.3d 1348, 1361 (Fed. Cir. 2007)). We analyze both parties’ arguments, below, in accordance with the above-stated principles.

1. Ground 1 - Asserted Obviousness Based on the Admitted Prior Art and the Dummy Gate References

Petitioner asserts that claims 1–5, 8–12, and 15 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of the Admitted Prior Art and the Dummy Gate References. Pet. 4, 23–35.

According to Petitioner, one of ordinary skill in the art would have been motivated to modify the Admitted Prior Art in view of the Dummy Gate References because “dummy gate structure is known to improve a semiconductor device . . . in predictable ways.” *Id.* at 23–24. Petitioner asserts that such improvements include “manipulating the topology of the gate structure on the silicon substrate, controlling the number of MOSFET manufacturing steps, and/or facilitat[ing] component isolation in a substrate and to increate device operation speed.” *Id.* at 24; *see also id.* at 8–9 (listing same improvements). Petitioner cites to portions of the Dummy Gate References as support for its assertion that using dummy gates is known to provide these advantages. *See id.* at 8–9 (citing Ex. 1004, 123 (Effect of the Invention); Ex. 1005 ¶¶ 22, 25; Ex. 1006, at [57]; Ex. 1007, 11:53–61; Ex. 1008, at [57], Figs. 5, 6).

In our Institution Decision, we determined that, although the cited portions of the Dummy Gate References teach the use of dummy gates generally, they do not provide express support for the asserted advantages thereof, and Petitioner did not provide any explanation beyond bare citations to the references. Inst. Dec. 17. We also determined that Mr. Maltiel’s cited testimony did not provide further explanation. *Id.* (citing Ex. 1003 ¶¶ 38–40). Similarly, we determined that Petitioner’s claim charts, upon which it relies to show how the asserted references meet the limitations of the challenged claims, simply cite to figures of the Dummy Gate References,

with no further citation to the text of the references, and Petitioner did not provide any additional explanation as to how the cited figures teach the respective elements of the claims. *Id.* at 17–18 (citing, e.g., Pet. 28 (claim elements 1[A], 1[C]), 29 (claim element 1[E])). We also determined that Mr. Maltiel’s cited testimony in this regard did not provide further explanation. *Id.* at 18 (citing Ex. 1003 ¶ 86).

Patent Owner agrees with the Board’s Institution Decision determination, arguing that because “the Petition fails to meet mandatory statutory and regulatory requirements, there is no reason for the Board to modify its opinions regarding the deficiencies of this ground.” PO Resp. 14. Patent Owner argues that the “deficiencies in the Petition with respect to the first ground are terminal and may not be remedied in a reply.” *Id.* at 13 (citing 35 U.S.C. § 312(a)(3); 37 C.F.R. §§ 42.22(a)(2), 104(b)(3), 104(b)(4), 104 (b)(5)). Patent Owner criticizes Petitioner for (i) failing to “explain whether the alleged ground of invalidity relies on the combined teachings of the Dummy Gate References or should be based on one or more of the individual references;” (ii) failing to “specify which of the teachings from which of the references is to be relied on;” and (iii) failing to “identify how the five combined references teach more than each individual reference.” *Id.* at 14–15 (citing Pet. 8–9, 23–35). Patent Owner also criticizes Petitioner for failing to show that one of ordinary skill in the art would have been motivated to combine the references. *Id.* at 15; *see also* Tr. 14:19–22 (“Petitioner didn’t apply specific motivation for each of the different dummy references. They just combined them all and did not really provide any explanation beyond just a blanket citation to evidence. Their expert didn’t explain any further . . .”).

Petitioner replies that it properly presented this Ground 1 with respect to at least Yonemaru and Haribuchi. Reply 1. Petitioner maintains that the teachings of the Dummy Gate References on which it relies are illustrated by the figures in Petitioner’s claim charts, and that each of the Dummy Gate References is used for the same teaching. *Id.* at 3–4.

As we explained in the Institution Decision, Petitioner should not expect the Board to search the record and piece together the evidence that may support Petitioner’s arguments. 37 C.F.R. § 42.22(a)(2) (the “petition . . . must include . . . [a] full statement of the reasons for the relief requested”); *cf. DeSilva v. DiLeonardi*, 181 F.3d 865, 866–67 (7th Cir. 1999) (“A brief must make all arguments accessible to the judges, rather than ask them to play archeologist with the record.”). By statute, a petition is required to identify “with particularity[] the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge.” 35 U.S.C. § 312(a)(3). The petition shall also include a “full statement” with “a detailed explanation of the significance of the evidence, including material facts.” 37 C.F.R. § 42.22(a)(2). In that regard, our rules require a petition to include both an adequate explanation of how the claims should be construed, as well as information sufficient to show how and why the properly construed claims are unpatentable over the asserted prior art. 37 C.F.R. § 42.104(b)(3), (b)(4). A petition should also “explain why a person of ordinary skill in the art would have combined elements from specific references in the way the claimed invention does.” *ActiveVideo Networks, Inc. v. Verizon Comm’ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012).

On the full record now before us, Petitioner has failed to articulate or provide sufficient citations to evidence to support a finding that one of ordinary skill in the art would have been motivated to modify the Admitted Prior Art in view of the Dummy Gate References to arrive at the invention of the challenged claims. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.22(a). Petitioner also has failed to articulate, with reasonable clarity, how the cited references teach each element of the challenged claims. Here, we reiterate, for the same reasons expressed in the Institution Decision, that Petitioner's assertions regarding the teachings of the prior art lack the required particularity. Petitioner's Reply arguments, at this late stage in the proceeding, cannot fix the Petition's shortcomings in this regard. *See Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1370 (Fed. Cir. 2016). Petitioner argues in its Reply that the Board should consider at least this ground with respect to on the Admitted Prior Art, Yonemaru, and Haribuchi, and essentially requests that the Board modify or distill the original ground in a manner that we consider impermissible. Reply 1–4. We agree with Patent Owner that we should not allow Petitioner to reconfigure its argument to be based on the APA in view of Yonemaru or Haribuchi alone, by looking to other portions of the Petition in which Petitioner argued the combination of the APA in view of Yonemaru and Haribuchi, because doing so would be considering a ground not asserted in the Petition. Tr. 15:7–9. Thus, consistent with the Institution Decision and for the reasons expressed therein and reiterated herein, we determine that the Petition's obviousness ground is deficient under 35 U.S.C. § 312(a)(3) and 37 C.F.R. § 42.22(a). Therefore, Petitioner has not established by a preponderance of the evidence that claims 1–5, 8–12, and 15 would have

been obvious over the combination of the Admitted Prior Art and the Dummy Gate References.⁶

2. Ground 2 - Asserted Obviousness Based on the Admitted Prior Art and Yonemaru

Petitioner asserts that claims 1–5, 8–12, and 15 are unpatentable under 35 U.S.C. § 103 as obvious in view of the Admitted Prior Art and Yonemaru. Pet. 4, 35–51.

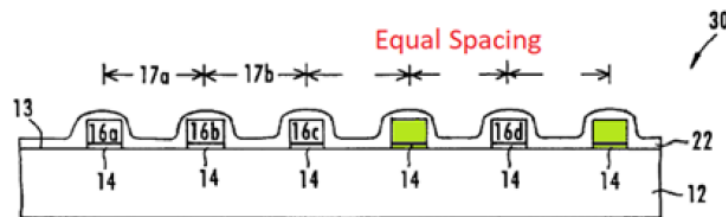
a. Claims 1–5 and 8–12

According to Petitioner, one of ordinary skill in the art would have been motivated to modify the Admitted Prior Art in view of Yonemaru in order to overcome the known problem of non-uniform gate spacers. Pet. 36; *see id.* at 11–13. Petitioner directs us to specific disclosures in Yonemaru that recognize the “need to control the width of gate spacer[s].” *Id.* at 12 (citing Ex. 1004, 122; Ex. 1003 ¶ 48); *see also* Ex. 1004, 122 (Problem to be Solved). Petitioner further asserts that Yonemaru “provides a solution to this problem” (Pet. 36), namely, using dummy gates “to compensate for the variation in gate electrode density or spacing” (*id.* at 14 (citing Ex. 1004, 123 (Effect of the Invention); Ex. 1003 ¶ 53)); *see also id.* at 37 (“Yonemaru teaches the technique of utilizing dummy gate electrodes so as to cause the

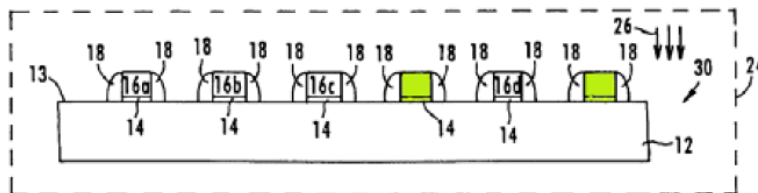
⁶ This determination with respect to Petitioner’s ground based on the combination of the Admitted Prior Art and the Dummy Gate References should not be read as inconsistent with our determination regarding Petitioner’s ground based on the combination of the Admitted Prior Art and Yonemaru, which is one of the Dummy Gate References. Petitioner addresses the ground based on the combination of the Admitted Prior Art and Yonemaru in a separate section of the Petition, providing further discussion and relying on different evidence than the evidence it relies upon with respect to the ground based on the combination of the Admitted Prior Art and the Dummy Gate References. *See* Pet. 35–51.

spacers to be uniform in shape and size. A [person of ordinary skill in the art] would recognize that this technique would improve the [Admitted Prior Art] in the same way.” (citing Ex. 1003 ¶¶ 89–90)).

Petitioner provides an illustration of the resulting structure, when the teachings of Yonemaru are applied to the Admitted Prior Art design (Pet. 37–38), reproduced below:



- Green Box: dummy gate arrangement



- Green Box: dummy gate arrangement

The figures above show a portion of the Admitted Prior Art semiconductor device as modified by Petitioner with the teachings of Yonemaru. See Pet. 37–38. In Petitioner’s combination, dummy gate arrangements (green in Petitioner’s annotated figures) are formed on substrate 12 of the Admitted Prior Art to create equal spacing, resulting in spacers 18 of uniform shape and size. *Id.*

Petitioner provides a claim chart identifying disclosures in the Admitted Prior Art, as well as in Yonemaru, for each element of claims 1–5 and 8–12. *Id.* at 38–48. Petitioner also relies on the testimony of its declarant, Mr. Maltiel. *Id.*; Ex. 1003 ¶¶ 94, 96, 98, 100, 102, 104, 106, 108, 110, 112, 114, 128. More particularly, Petitioner argues that the problem of non-uniform gate spacers, and the cause of the problem, was known in the semiconductor fabrication industry, and Yonemaru provides a solution to the problem, providing a motivation to combine Yonemaru with the APA. Pet. 36 (citing Pet. § III.C.1). Petitioner also argues that one of ordinary skill in the art would have been motivated to combine the teachings of Yonemaru with the APA, because applying Yonemaru’s technique of utilizing dummy gate electrodes so as to cause the spacers to be uniform in shape and size would improve the APA in the same way and “requires nothing other than skill sets that a POSA possesses.” *Id.* at 37 (citing Ex. 1003 ¶¶ 89–90).

Patent Owner argues that the proposed combination “fails to disclose each limitation of the challenged claims,” namely, the limitation of “removing portions of the dielectric layer to form a plurality of spacers, wherein each of the plurality of spacers physically contacts one of the two gate arrangements and the substrate, and wherein the spacers located within the defined space each have a base width that is approximately the same.” PO Resp. 21. More particularly, Patent Owner argues that “neither the APA nor Yonemaru teach[es] the required dielectric removing step that results in spacers that physically contact the substrate,” and that Yonemaru fails to disclose or suggest that non-operable gate arrangements are “freely

applicable” to gate forming processes, such as the APA, where there is no gate oxide beneath the spacers. *Id.* at 21–22 (citing Ex. 2001 ¶¶ 51–52).

Petitioner criticizes as “disingenuous” Patent Owner’s argument that the combination of the APA and Yonemaru fails to disclose each of the claimed limitations. Reply 4. Petitioner replies that it is undisputed that the APA teaches spacers that physically contact the substrate, and that Yonemaru teaches spacers that contact the non-operational gate arrangement or polysilicon line. *Id.* at 5 (citing Ex. 1001, 5:46–48; Ex. 1004, 123).

Petitioner also criticizes Patent Owner’s argument that a “specific implementation of Yonemaru would need to be modified” to achieve the claimed invention. *Id.* at 6 (citing PO Resp. 22, 31–42). Petitioner reiterates that Yonemaru teaches that “dummy gate electrodes should be formed in the same manner as functioning gate electrodes (citing Ex. 1004, 123) and that one of ordinary skill would have understood that “the dummy gate electrodes could be formed using the gate-forming process of the Admitted Prior Art,” and would not need to consider the particular process used in Yonemaru. *Id.*

We agree that Petitioner’s case is premised on the APA’s teaching of nearly every limitation of the challenged claims, but that Petitioner relies on the Yonemaru to provide uniform spacing among all gates by using dummy gates, leading to equally sized spacers. *See, e.g.*, Pet. 35–38; Reply 1, 5.

Petitioner relies on the APA to disclose

removing the dielectric layer [to] form a plurality of gate spacers. Ex 1001, '611, 5:41–45. Each gate spacer physically contacts the side of a gate electrode and the gate oxide underneath, as well as physically contacts the silicon substrate. *Id.* at 5:46–48 (“As shown, **spacers 18 and 18' each physically contact the**

sidewalls of gate conductors 16a-d (as applicable) and the top surface 13 of substrate 12.).

Pet. 40. Patent Owner does not dispute, and we find Petitioner has shown by a preponderance of the evidence, that the APA teaches all limitations of claims 1–5 and 8–12, except for the non-operable gates. *See, e.g.*, Pet. 38–41, 44–46; *see generally* PO Resp. Petitioner relies on the teachings of Yonemaru in combination with the APA, as shown in Petitioner’s modified Figures 2a and 2b, to demonstrate that the resulting combination would result in spacers each having a base width that is approximately the same (*id.* at 37–38), and on Yonemaru to demonstrate that “side wall 4 is also formed to the same shape” (*id.* at 40 (citing Ex. 1004, 123)).

We acknowledge Patent Owner’s arguments that the teachings of Yonemaru are not “freely applicable” to gate arrangements such as those disclosed in the APA (PO Resp. 22) and that the combination does not result in the claimed invention because the dummy gates of Yonemaru have oxide beneath the spacers (*id.* at 22–23). Regarding the applicability of the teachings of Yonemaru to the APA, we find that Petitioner argues persuasively that Yonemaru recognizes the problem of non-uniformly sized gate spacers in devices like the APA and solves the problem in the same manner as the ’611 patent, namely, by the use of dummy gates to create uniformity. Pet. 11–15. More particularly, Petitioner argues, the ’611 Patent “explains, within the context of describing the APA, that there exist width variations because gate electrodes are densely populated in certain areas on an IC chip, and sparsely populated in other areas.” *Id.* at 12–13 (citing Ex. 1001, Figs. 2a & 2b, 5:21–62); *see also* Ex. 1001, 5:54–56 (“Spacers 18’ are shaped differently because of the topology associated with

space 19, which is more open than space 17a and 17b, for example.”)). Petitioner also argues that Yonemaru acknowledges “the need to control the width of the gate spacer.” Pet. 12 (citing Ex. 1003 ¶ 48; Ex. 1004, 122)). Yonemaru, according to Petitioner, identifies the “same root cause” of the problem identified in the ’611 patent’s discussion of the APA, namely, the width variation problem that exists because gate electrodes are densely populated in certain areas on an IC chip, and sparsely populated in other areas. *Id.* at 13 (citing Ex. 1004, 122–123; Ex. 1003 ¶ 50). Also according to Petitioner, Yonemaru “taught the same solution to the width variation problem,” namely, “using non-operation (or dummy) gates to compensate for the variation in gate electrodes density or spacing.” *Id.* at 14 (citing Ex. 1004, 123; Ex. 1003 ¶ 53). We find that Petitioner has made its case that the “uniformity among spacers” teachings of Yonemaru are applicable to the gate formation process of the APA by showing that the APA suffers from the same non-uniformity problem identified by Yonemaru, which proposes a solution to that problem.

Regarding Patent Owner’s argument about oxide beneath the spacers of Yonemaru, we find that Petitioner relies on Yonemaru’s teachings of spacing arrangements, which Petitioner has shown are applicable to the APA’s gate formation process. We agree with Petitioner that the ’611 patent’s APA and the semiconductor fabrication industry at large identified a “need or problem known in the field or endeavor at the time of invention,” specifically, the problem of non-uniform gate spacers, which “can provide a reason for combining the elements [of the APA and Yonemaru] in the manner claimed.” Pet. 36 (quoting *KSR*, 550 U.S. at 420). We also find that Petitioner has also shown that one of ordinary skill in the art would have

been motivated to apply Yonemaru's teachings to the APA in the manner proposed by Petitioner, namely, to use Yonemaru's dummy gate electrodes to "improve the APA in '611 in the same way" so as cause the spacers of the APA to be uniform in shape and size. *Id.* at 11–14, 36–38; Ex. 1003 ¶¶ 53, 90–91, 98 (describing fabrication of dummy gates in the proposed combination); Reply 5–6. We agree with Petitioner's reply to Patent Owner's argument about the gate oxide beneath the spacers, i.e., that "it is undisputed the Admitted Prior Art teaches [spacers that physically contact the substrate]" (Reply 5 (citing Ex. 1001, 5:46–48)), and Yonemaru teaches the "limitation of spacers that contact the non-operational gate arrangement or polysilicon line." *Id.* (citing Ex. 1004, 123); *see also* Tr. 9:9–11; Pet. 36–37 (citing Ex. 1003 ¶¶ 88–90; Ex. 1001, Figs. 2a, 2b, 3; Ex. 1004, Fig. 2). Petitioner also has demonstrated that Yonemaru does not place any specific emphasis on its particular process, or on having a gate oxide layer between the spacers and the substrate, vis-à-vis solving the problem of uniformly-sized spacers. Reply 5–7 (citing Ex. 1004, 123) ("it is the process of the Admitted Prior Art that is being augmented with Yonemaru's teaching of dummy gate electrodes to obtain spacers of the same width," and one of ordinary skill in the art "would not need to consider the particular process used in Yonemaru"); Tr. 5:11–19 ("Yonemaru doesn't say that the dummy gate arrangements have to be on an oxide layer"). We further find that Petitioner demonstrates that one of ordinary skill in the art would have been motivated to solve the problem of irregular gate spacing and side wall size in the APA with the techniques taught by Yonemaru, namely, providing dummy gates as a solution to non-uniform sidewall spacing in operational transistors, and that this combination proposed by Petitioner would result in

the claimed invention. Pet. 35–38; Reply 5–7; Ex. 1003 ¶¶ 89–90. Thus, we find that Petitioner has proven by a preponderance of the evidence that Yonemaru teaches the limitations not provided by the APA, and that one of ordinary skill in the art would have been prompted to combine them with a reasonable expectation of success.

We also have reviewed Petitioner’s contentions and supporting evidence regarding claims 2–5 and 8–12. Pet. 20–21, 41–48. Other than arguments directed primarily to claim 1, which we have discussed above, Patent Owner does not present additional arguments as to these remaining claims. See PO Resp. 23. Based on the record now before us, we are persuaded that Petitioner has shown by a preponderance of the evidence that the combination of the APA and Yonemaru renders obvious claims 1–5 and 8–12.

b. Claim 15

Petitioner relies on Figure 6a of the ’611 patent as teaching several of the limitations of claim 15. Pet. 48–51. Petitioner characterizes Figure 6a of the ’611 patent as alleged Admitted Prior Art. *Id.* According to Petitioner, a person of ordinary skill in the art, “reading the ’611 description of Figure 6a in view of the overall ’611 disclosure, would understand that Fig. 6a constitutes [Admitted Prior Art].” *Id.* at 49 (citing Ex. 1003 ¶ 72); *see also id.* (citing Ex. 1001, 4:63–5:2, 7:5–11, Figs. 2a, 6a; Ex. 1002, 101–102 (Appeal Brief)). Unlike Figure 2a, however, Figure 6a of the ’611 patent is not labeled as “prior art.”

Patent Owner argues that Petitioner fails “to provide any evidence that the applicant admitted in the ’611 patent, or during the prosecution of the application that issued as the ’611 patent, that Figure 6a, or the

corresponding description thereof, is prior art.” PO Resp. 23. More particularly, Patent Owner argues that none of the evidence cited by Petitioner “rises to the level of an admission that Figure 6a or its corresponding description is prior art.” *Id.* at 24. At oral hearing, Patent Owner argued that nothing in the case law “suggests that you can derive an admission from an analogy to another figure in the patent.” Tr. 15:14–15.

Petitioner replies that the ’611 patent “uses Figure 6 to explain the invention as an improvement over the prior art.” Reply 8. Petitioner relies on the testimony of Mr. Maltiel to argue that one of ordinary skill in the art “would understand Figure 6a to be showing the same prior art problem as Figure 2.” *Id.* at 9–10 (citing Ex. 1003 ¶ 72). By way of analogy, according to Petitioner, just as Figure 4 describes portion 30’ as an “improved portion 30” of portion 30 shown in “prior art” Figure 2, one of ordinary skill in the art would “understand Figure 6 to be showing an improvement over the prior art, with Figure 6a representing the prior art and Figures 6b and 6c illustrating the improvement.” *Id.* at 8. However, at oral hearing, Petitioner stated that “6a through 6c depict 30 prime, which is the improvement” (Tr. 27:1–2) and “[t]he patent says Figure 6a through c depict the improvement” (*id.* at 27:10–11), indicating that the entirety of Figure 6 and all its subparts show an improvement, rather than prior art. To support its argument that Figure 6a is prior art, Petitioner also points to a sentence in the prosecution history characterizing “the point of novelty as being the use of the dummy gate arrangements.” Tr. 25:11–16 (citing Ex. 1002, 129 (“The point of novelty of the claimed inventive process is the formation or configuration of non-operational gate arrangements in the semiconductor

device and removing the dielectric so that spacers on the sidewalls of the operational gates have approximately the same base width.”)); Reply 2.

On this complete record, Petitioner does not satisfy its burden of demonstrating that Figure 6a was ever described in the '611 patent or during prosecution thereof as “prior art.” “While valid prior art may be created by the admissions of a party, these admissions are generally characterized by statements made during prosecution describing certain work as ‘prior art.’” *Abbott Labs. v. Baxter Pharm. Prod., Inc.*, 334 F.3d 1274, 1279 (Fed. Cir. 2003) (citing *In re Nomiya*, 509 F.2d 566 (CCPA 1975); *In re Fout*, 675 F.2d 297, 300–01 (CCPA 1982)). Petitioner’s reliance on a sentence in the prosecution history does not, in our estimation, provide sufficient foundation for Petitioner’s characterization of Figure 6a of the '611 patent as admitted prior art, as that sentence is not sufficiently clear to call out Figure 6a as prior art. Nor does Petitioner’s analogizing Figure 6a to other figures labeled “prior art” in the '611 patent succeed, because Figure 6a, along with Figures 6b and 6c, is its own figure with its own description in the specification, none of which designate Figure 6a as prior art. *See, e.g.*, Ex. 1001, Fig. 6a–6c, 4:19–26, 7:3–25. Because the applicants “intentionally labeled those figures [2a and 2b] having to do with transistor gate arrangements as being in the prior art” but in contrast, did not label Figure 6a as prior art, we are persuaded that the applicants were aware of the mechanics of designating certain figures as prior art, but chose not to do so with respect to Figure 6a. Tr. 17:3–5. Accordingly, because Petitioner has not demonstrated that Figure 6a is admitted prior art, we determine that Petitioner has not shown by a preponderance of the evidence that claim 15 would have been obvious in view of the Admitted Prior Art and Yonemaru.

3. Ground 3 - Asserted Obviousness Based on Yonemaru, Haribuchi, and Weste

Petitioner asserts that claims 1–5 and 8–12 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Yonemaru, Haribuchi, and Weste. Pet. 4, 51–63.

As discussed in Section II.D.2.a, *supra*, we conclude Petitioner has shown by a preponderance of evidence that claims 1–5 and 8–12 are unpatentable as obvious over the APA and Yonemaru. Because claim 15 is not challenged under Petitioner’s Ground 3 based on Yonemaru, Haribuchi, and Weste, our conclusion regarding the patentability of claims 1–5 and 8–12 under Petitioner’s Ground 2 is dispositive of Petitioner’s challenge to the patentability of those challenged claims. Accordingly, we decline to address whether Petitioner has further shown, by a preponderance of evidence, that claims 1–5 and 8–12 are also unpatentable as obvious over Yonemaru, Haribuchi, and Weste. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue because doing so “can not only save the parties, the [agency], and [the reviewing] court unnecessary cost and effort,” but can “greatly ease the burden on [an agency] faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits”).

III. CONCLUSION

We conclude that Petitioner has satisfied its burden of demonstrating, by a preponderance of the evidence, that the subject matter of claims 1–5 and 8–12 of the ’611 patent is unpatentable under 35 U.S.C. § 103(a) in view of the APA and Yonemaru. Petitioner, however, has not satisfied its burden

of demonstrating, by a preponderance of the evidence, that the subject matter of claim 15 of the '611 patent is unpatentable under 35 U.S.C. § 103(a).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner establishes, by a preponderance of the evidence, that claims 1–5 and 8–12 of U.S. Patent No. 6,103,611 are unpatentable; and

FURTHER ORDERED that Petitioner fails to establish, by a preponderance of the evidence, that claim 15 of U.S. Patent No. 6,103,611 is unpatentable; and

FURTHER ORDERED that this is a Final Written Decision; therefore, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2018-00065
Patent 6,103,611

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