

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

POWER INTEGRATIONS, INC.,
Petitioner,

v.

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Patent Owner.

Case IPR2018-00180
Patent 6,597,221 B2

Before BRYAN F. MOORE, JOHN F. HORVATH, and
KAMRAN JIVANI, *Administrative Patent Judges*.

JIVANI, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Power Integrations, Inc. (“Petitioner”) requested an *inter partes* review of claims 4–7 and 9–18 (the “challenged claims”) of U.S. Patent No. 6,597,221 B2 (Ex. 1001, “the ’221 patent”). Paper 2 (“Petition” or “Pet.”). Semiconductor Components Industries, LLC¹ (“Patent Owner”) did not file a Preliminary Response. Upon consideration of the Petition, we instituted an *inter partes* review of the challenged claims pursuant to 35 U.S.C. § 314. Paper 6 (“Decision on Institution” or “Dec. on Inst.”), 14–15.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 4–7, 9–16, and 18 are unpatentable. We further determine, however, that Petitioner has failed to show by a preponderance of the evidence that claim 17 is unpatentable.

II. BACKGROUND

A. *Procedural History and Asserted Grounds of Unpatentability*

Petitioner advanced the following grounds of unpatentability in the Petition (Pet. 4):

1. Claims 4–7, 9, and 15–17 as anticipated under 35 U.S.C. § 102(a) by Hwang, U.S. Patent No. 5,747,977 (“Hwang”) (Ex. 1004);

¹ Patent Owner identifies ON Semiconductor Corporation as an additional real party in interest. Paper 3, 2.

2. Claims 9–14 and 18 as obvious under 35 U.S.C. § 103 over the combined teachings of Hwang and Balakrishnan, U.S. Patent No. 5,313,381 (“Balakrishnan”) (Ex. 1005); and
3. Claims 7, 9, 15, 16, and 18 as anticipated under 35 U.S.C. § 102(b) by Harris Semiconductor Application Note No. AN9212.1, April 1994 (“Harris”) (Ex. 1006).

In our Decision on Institution, we instituted review of all challenged claims based on the grounds advanced in the Petition and enumerated above. Dec. on Inst. 14–15.

After institution, Patent Owner filed a Patent Owner Response (Paper 11, “PO Resp.”). Petitioner filed a Reply in support of its Petition (Paper 16, “Reply”). Patent Owner then filed a Sur-Reply in support of its Response (Paper 26, “Sur-Reply”).

Patent Owner moved to strike eleven exhibits and related arguments that Patent Owner contends were not present in the Petition (Paper 22, “Motion to Strike”), and Petitioner opposed this motion (Paper 30).

Patent Owner also moved to exclude four exhibits and related testimony proffered by Petitioner in support of its ground based on Harris (Paper 23, “Motion to Exclude”). Petitioner opposed this motion (Paper 29), and Patent Owner replied in support of the motion (Paper 31).

Both parties requested an oral hearing, and a hearing was held on February 7, 2019. Paper 27. A transcript of the oral hearing has been entered into the record. Paper 32 (“Tr.”).

B. Testimony

Petitioner supports its challenge with a declaration of Dr. Tamas Szepesi. Ex. 1003 (“Szepesi Declaration”). Dr. Szepesi testified by

deposition on July 25, 2018, and a transcript of his testimony has been entered into evidence. Ex. 2003. After his deposition, Dr. Szepesi further submitted a supplemental declaration in support of the Petition. Ex. 1016 (“Szepesi Supplemental Declaration”).

Patent Owner supports its Response with a declaration of Dr. Douglas Holberg. Ex. 2001 (“Holberg Declaration”). Dr. Holberg testified by deposition on November 28, 2018, and a transcript of his testimony has been entered into evidence. Ex. 1022.

C. Related Proceedings

The parties identify (Pet. 2; Paper 3, 2–3) the following consolidated district court action consisting of two underlying cases, one of which involved assertion of the ’221 patent: *Power Integrations, Inc. v. On Semiconductor Corp. et al.*, 5:16-cv-06371-BLF, 5:17-cv-03189-BLF (N.D. Cal.). Ex. 1018 (Transfer Order).

D. Overview of the ’221 patent

The ’221 patent relates to power converter integrated circuits. Ex. 1001, 1:10–11. In particular, the ’221 patent describes a “soft start” circuit for reducing the on-time of a power switch of the power supply during initial start-up. *Id.* at 2:3–6. Reduction is accomplished by limiting the duty cycle of the power switch, so that the power switch is turned off for a longer period than it is turned on, thereby preventing transformer saturation and start-up failure. *Id.* at 2:6–11. The ’221 patent further describes “a duty cycle detector circuit for reducing the power consumption of the power supply when a load at the output of the power supply draws little or no power.” *Id.* at 2:11–15. Figure 1 of the ’221 patent is reproduced below.

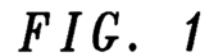


Figure 1 depicts a power supply 10 that includes full-wave bridge rectifier 12, capacitors 13 and 14, transformer 16, peak rectifiers 18 and 19, coupling circuit 21, and power converter circuit 23. *Id.* at 2:15–20. Power converter circuit 23 includes controller circuit 60, duty cycle detector circuit 61, soft start circuit 62, and power switch 63. *Id.* at 3:14–16. Controller circuit 60 controls the duty cycle of switch 63 using the FEEDBACK signal to alter the pulse width of the GATE signal to modify the inductor current in transformer 16, thereby regulating the DC output voltage. *Id.* at 4:12–23. EOUT is an error signal generated in accordance with the FEEDBACK signal and is used to adjust the duty cycle of the GATE signal. *Id.* at 4:24–26.

Figure 1 further depicts duty cycle detector circuit 61 receives as input the error signal EOUT and outputs duty cycle detect signal DETECT. *Id.* at 3:27–29. The DETECT output of comparator/duty cycle detector circuit 61 causes soft start circuit 62 to assert the MOD signal which, in turn, modifies the signal GATE. *Id.* at 5:20–24, 7:19–22, Fig. 2. When the error signal EOUT exceeds the threshold voltage of comparator 61, the DETECT output, through the MOD signal, inhibits the GATE signal output. *Id.* at 11:22–25. As a result, pulses are skipped when EOUT “is at a voltage level greater than the threshold voltage level of comparator 61.” *Id.* at 11:25–27.

E. Challenged Claims

Claims 4, 7, 9, and 15 are independent. Claims 5 and 6 depend from claim 4. Claims 10–14 depend from claim 9. Claims 16–18 depend from claim 15. Claim 4 is illustrative of the claimed subject matter, and is reproduced below.

4. A power conversion control circuit, comprising:
 - a regulator coupled for receiving a feedback signal to provide a switched drive control signal operating between a minimum and maximum on-time;
 - a detector having an input coupled for receiving the feedback signal and providing a detect signal when the feedback signal exceeds a threshold representing a predetermined duty cycle of the switched drive control signal; and
 - a control circuit having an input coupled for receiving the detect signal, wherein the control circuit disables the switched drive control signal in response to the detect signal to reduce power transfer by the power conversion control circuit.

Id. at 12:39–53.

III. ANALYSIS

A. Principles of Law

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail in its challenges, Petitioner must demonstrate by a preponderance of the evidence that the challenged claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros., Inc. v. Union Oil. Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). The elements must be arranged as recited in the challenged claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective evidence of non-obviousness, i.e., so-called secondary considerations such as commercial success, long felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). The obviousness inquiry further requires an analysis of “whether there was an apparent reason

to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)).

B. Level of Ordinary Skill in the Art

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int’l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)).

Petitioner asserts that a person of ordinary skill in the art at the time of the invention:

would have had the equivalent of a Bachelor’s degree or higher in electrical engineering with at least three years working experience in the design of electronic circuits, would be familiar with switching voltage regulator circuits, and with the operation, design and fabrication of integrated circuits related to switching voltage regulators.

Pet. 12.

Patent Owner states that a person having ordinary skill in the art “would have been someone with at least a Master’s Degree in electrical engineering or a related field, or, alternatively, a Bachelor’s Degree in electrical engineering or a related field with at least two years of work experience in power electronics.” PO Resp. 3.

Although the parties formulate slightly differently their respective assessments of the skill level, neither party disputes directly the other’s assessment nor makes any arguments related to the assessments. See *generally* Pet.; PO Resp. The ’221 patent states its disclosure “relates, in

general, to integrated circuits and, more particularly, to power converter integrated circuits.” Ex. 1001, 1:9–11. In view of the foregoing, we adopt Patent Owner’s formulation of the level of ordinary skill in the art. Further, this level of ordinary skill is reflected by the prior art of record. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of ordinary skill in the art).

C. Claim Construction

We interpret claims of an unexpired patent using the broadest reasonable interpretation in light of the specification. *See* 37 C.F.R. § 42.100(b) (2017)²; *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). Under the broadest reasonable interpretation standard, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). The claims, however, ““should always be read in light of the specification and teachings in the underlying patent,”” and “[e]ven under the broadest reasonable interpretation, the Board’s construction ‘cannot be divorced from the specification and the record evidence.’” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (citations omitted). Further, any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *See In re*

² Our recently changed version of this Rule, which requires that we interpret claims in the same manner used in a civil action under 35 U.S.C. § 282(b), does not apply here because the Petition was filed before the effective date of the new Rule, November 13, 2018. *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,344 (Oct. 11, 2018).

Paulsen, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a definition, limitations are not to be read from the specification into the claims. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

We address below the parties’ disputes regarding the related claim limitations: “wherein the control circuit disables the switched drive control signal in response to the detect signal” (claims 4–6); “wherein the gating circuit disables the drive control signal in response to the detect signal” (claims 7–8); “having an output for disabling the pulse generator” (claims 9–14); and “to terminate the step of generating in response to the error signal” (claims 15–18). Although the parties advance arguments related to construction of the limitations “developing a feedback signal from the voltage” and “routing the feedback signal” (claim 17), we determine in light of our analysis of Petitioner’s asserted ground of unpatentability against claim 17 (*see supra* Section III.E.4.) that construction of these limitations is not necessary, and, therefore, we do not construe them. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (explaining that only claim terms in controversy need to be construed, and only to the extent necessary to resolve the controversy).

After institution, Patent Owner asserts that the phrases:

- “wherein the control circuit disables the switched drive control signal in response to the detect signal,” as recited in claims 4–6, and “wherein the gating circuit disables the drive control signal in response to the detect signal,” as recited in claims 7 and 8, should be construed “to require that the switched drive control signal be disabled when the feedback signal exceeds the

threshold ***independent of other circuit conditions***”

(PO Resp. 14; Sur-Reply 4);

- “having an output for disabling the pulse generator,” as recited in claims 9–14, should be construed to mean “having an output that causes the generation of pulses to cease independent of other circuit conditions” (PO Resp. 13); and
- “to terminate the step of generating in response to the error signal,” as recited in claims 15–18, should be construed to mean “the generation of pulses cease in response to the comparison of the error signal to a reference signal ***independent of other circuit conditions***” (*id.* at 14).

Patent Owner thus urges that we should construe each of the phrases set forth above as requiring that the recited disabling or terminating occurs “independent of other circuit conditions.” PO Resp. 8–14. In support of its construction, Patent Owner cites to a single question and answer from the deposition of Petitioner’s declarant Dr. Szepesi (PO Resp. 8 (citing Ex. 2003, 44:16–45:1)) and to the declaration of its own witness, Dr. Holberg (*id.* (citing Ex. 2001 ¶ 34)). Patent Owner further asserts that the Specification supports its construction because the Specification “describes a comparator that, based on comparing an error signal with a reference signal *during normal operation*, causes pulse generation to stop regardless of the other circuit conditions.” *Id.* at 11 (citing Ex. 2001 ¶ 35) (emphasis added). According to Patent Owner, “[b]ecause they recite an ‘error signal,’ the challenged claims are limited to normal operation.”

Conversely, Petitioner urges that we reject Patent Owner's construction as overly narrow and instead apply the plain and ordinary meaning of the phrase "in response to." Reply 3. Petitioner contends,

The plain and ordinary meaning of "in response to" is permissive to include other conditions-precedent that need to be met to allow the disabling, *i.e.*, if a claim requires disabling to happen "in response to signal A," that is not the same as "in response to signal A, *independent of other circuit conditions*," nor is it the same as "in response to *only* signal A." Rather, "in response to signal A" permits the response to happen as a consequence of signal A in conjunction with other conditions.

Id. at 3. Thus, Petitioner argues that Patent Owner's asserted construction would improperly import an unrecited limitation into the claims. In support of its position, Petitioner proffers the testimony of its declarant Dr. Szepesi, distinguishing the single response Patent Owner cites. *Id.* at 2–3 (citing Ex. 1016 ¶¶ 18–21, 26–30; Ex. 2003, 43:16–45:1). Petitioner further asserts that nothing limits the claimed disabling or termination to occur only during "normal operating conditions." *Id.* at 1. Relying on the Specification, Petitioner contends that, contrary to Patent Owner's assertion, the recitation of an error signal in some of the challenged claims does not limit any of the challenged claims to "any particular mode because the disclosed embodiment of the error signal remains active during soft-start, not just normal operation." *Id.* at 5.

In determining the broadest reasonable interpretation of a claim term, we begin with the language of the claim itself. *In re Power Integrations, Inc.*, 884 F.3d 1370, 1376 (Fed. Cir. 2018) (quoting *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 457 F.3d 1293, 1301 (Fed. Cir. 2006)) ("[C]laim

construction must begin with the words of the claims themselves.”); *In re NTP, Inc.*, 654 F.3d 1279, 1288 (Fed. Cir. 2011) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc)) (“As with any claim construction analysis, we begin with the claim language.”). None of the challenged claims (nor even unchallenged claim 8) recites the claimed disabling or terminating occurs in response to the detect signal *independent of other circuit conditions* or in response *only* to the detect signal. See Ex. 1001, 12:5–14:36. For instance, independent claim 4 merely recites, “wherein the control circuit disables the switched drive control signal in response to the detect signal.” *Id.* at 12:49–51. Independent claim 7 similarly recites, “wherein the gating circuit disables the drive control signal in response to the detect signal.” *Id.* at 13:11–13. Independent claim 9 discloses only, “a first comparator . . . having an output for disabling the pulse generator.” *Id.* at 13:27–30. Finally, independent claim 15 requires, “comparing the error signal to a reference signal . . . to terminate the step of generating in response to the error signal.” *Id.* at 14:21–23. Therefore, the plain language of the challenged claims does not, standing alone, support adoption of Patent Owner’s proposed construction.

Turning to the Specification, the ’221 patent discloses a “duty cycle detector circuit” used to reduce the power consumption of the power supply when the output load draws little or no power. Ex. 1001, 2:10–14. Figure 2 of the ’221 patent is reproduced below.

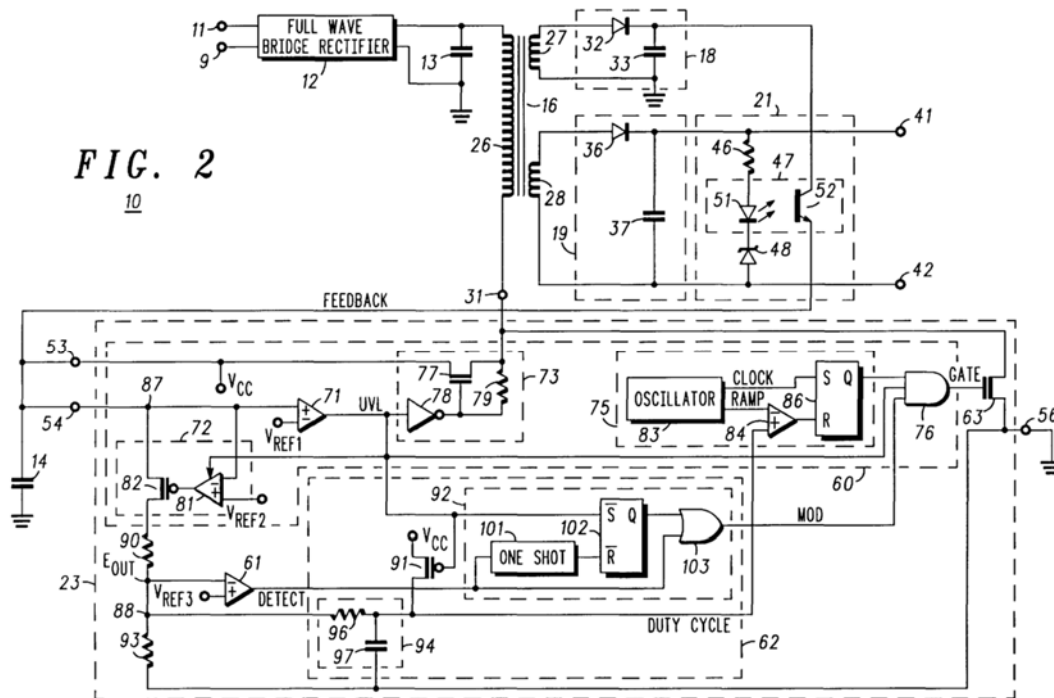


Figure 2 depicts “a more detailed schematic diagram of power supply 10 in accordance with an embodiment of the present invention.” *Id.* at 5:40–43. According to the ’221 patent, “[d]uty cycle detector circuit 61 increases the efficiency of power supply 10 by reducing the power consumption of power converter circuit 23 when a load (not shown) at the output of power supply 10 draws little or no power or is in a stand-by mode of operation.” *Id.* at 5:8–12. Duty cycle detector circuit 61 is a comparator receiving two inputs, an error signal EOUT and a reference voltage V_{REF3} , and outputting a duty cycle detect signal (“DETECT”) *Id.* at 3:27–29, 7:19–24.

The DETECT output of comparator 61 causes soft start circuit 62 to assert the MOD signal which, in turn, modifies the signal GATE. *Id.* at 5:20–24. When error signal EOUT exceeds threshold voltage V_{REF3} of comparator 61, the DETECT signal, through the MOD signal, inhibits the GATE signal output. *Id.* at 11:12–33.

The foregoing disclosure in the Specification does not support adoption of Patent Owner's proposed construction. Rather than disabling the switched drive control signal in response to the detect signal *independent of other circuit conditions* as Patent Owner contends, the disclosure above describes routing the DETECT signal through OR gate 103 and routing the output of that OR gate, i.e., the MOD signal, to control circuit 60 as "the third input of AND gate 76 for providing signal MOD." *Id.* at 7:52–60.

Patent Owner contends that, despite the disclosures discussed above, its proposed construction is consistent with the Specification because of the Specification's description of "soft-start mode." PO Resp. 9. According to Patent Owner, "[d]uring initial start-up" (i.e., soft-start mode), "the voltage EOUT (at the inverting input to comparator 61) is determined by soft-start circuit 62 in conjunction with controller circuit 60." *Id.* (citing Ex. 1001, 4:42–44). Once "[p]ower converter circuit 23 exits soft-start mode and begins normal operation . . . , soft-start circuit 62 is inactive, and EOUT is determined only by the current flow through the shunt regulator." *Id.* at 10. Relying on its declarant Dr. Holberg, Patent Owner asserts:

In normal operation, when comparator 61 detects that error signal Eout is greater than V_{REF3} , its output (the DETECT signal) is driven to a logic low voltage. Accordingly, OR gate 103 receives two logic low signals at its inputs (the output, Q, of flip-flop 102 and the DETECT signal) and provides a logic low output (the MOD signal). A logic low value of signal MOD causes AND gate 76 to stop passing pulses from the pulse width modulator 75 to gate 63.

Id. at 10–11 (citing Ex. 2001 ¶ 34). Significantly, Patent Owner contends, "[b]ecause they recite an 'error signal,' the challenged claims are limited to normal operation." *Id.* at 12.

We are not persuaded by Patent Owner's arguments. First, contrary to Patent Owner's arguments, not all challenged claims recite an "error signal." Of the challenged independent claims, only independent claims 9 and 15 recite an "error signal"; independent claims 4 and 7 do not. Second, none of the challenged claims include limitations explicitly circumscribing certain disclosed modes of operation.

Third, we agree with Petitioner that the Specification discloses the error signal remains active during soft-start, not just normal operation, because the error signal EOUT is activated through FET 82 and resistors 90 and 93. Even in soft-start, the power converter circuit is actively checking EOUT "to adjust the threshold voltage level of comparator 84 of PWM 75 which in turn controls the duty cycle of signal GATE." Reply 5 (citing Ex. 1001, 8:62–9:9). For example, during soft-start mode, signal UVL transitions from logic low to logic high when the voltage across capacitor 14 at pin 54 reaches V_{REF1} or 9V. Ex. 1001, 8:56–61. When UVL transitions to a high logic level, FET 82 is turned on, and discharges capacitor 14 through resistors 90 and 93, thereby generating signal EOUT across resistor 93. *Id.* at 8:62–9:7. EOUT adjusts the threshold of comparator 84 of PWM 75, thereby controlling the duty cycle of signal GATE. *Id.* at 9:7–9. As capacitor 14 discharges from 9V to 8.5V, the current shunted to resistor 93 decreases from a maximum to a minimum, thereby causing the duty cycle of signal GATE to increase from a minimum to a maximum. *Id.* at 9:29–36. When the voltage across capacitor 14 (pin 54) decreases to 8.5V, "power converter circuit 23 exits its soft start mode . . . and enters its normal mode." *Id.* at 9:45–48. Thus, we agree with Petitioner that signal EOUT is generated even during soft-start mode.

Finally, fourth, even if we were to accept Patent Owner's contentions that the disclosed embodiments only meet the claim limitations during "normal operation" outside the disclosed soft-start mode, it is well established that limitations not recited in the claims are not to be read into the claims from the written description, even where all disclosed embodiments include such an unclaimed limitation. *Flo Healthcare Solutions, LLC v. Kappos*, 697 F.3d 1367, 1375 (Fed. Cir. 2012) (citing *Silicon Graphics, Inc. v. ATI Techs., Inc.*, 607 F.3d 784, 792 (Fed. Cir. 2010)); *see also WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1323 (Fed. Cir.2018) (affirming the construction that "predicting positions" was not limited to a certain predictive model because the claim imposed no such requirement).

Looking beyond the Specification, both parties offer competing testimony from their respective declarants on whether one of ordinary skill in the art would understand "in response to" as requiring "independent of other circuit conditions." *Compare* Reply 2–3 (citing Ex. 1016 ¶¶ 18–21, 26–30; Ex. 2003, 43:16–45:1) *with* PO Resp. 14–15, 17 (citing Ex. 2001 ¶¶ 42, 44–45.) *and* Sur-Reply 11–12 (citing Ex. 2001 ¶ 45). Patent Owner further directs our attention to a single sentence of deposition testimony in which Petitioner's declarant Dr. Szepesi appears to agree with Patent Owner's construction by stating, in the context of claim 9, that "the output signal of this first comparator disables the output pulses driving the gate of that independent of anything else." PO Resp. 8 (citing Ex. 2003, 44:16–45:1). Petitioner rebuts Patent Owner's arguments by identifying additional deposition testimony and statements made in a second declaration offered by Dr. Szepesi opposing Patent Owner's construction. Reply 2–3 (citing

Ex. 1016 ¶¶ 18–21, 26–30; Ex. 2003, 43:16–45:1). For instance, immediately before the statement Patent Owner cites, Dr. Szepesi testified:

Q: “So is it your opinion that an output for disabling the pulse generator must disable the pulse generator regardless of the other conditions in the circuit?”

...

A: “I don't understand your question. I said disabling the pulse generator means that the output of the pulse generator which is providing the pulses to the gate of the main switch, those pulses are disabled. That's what it means in my opinion in this context.”

Ex. 2003, 43:24–44:9. And, in his supplemental declaration, Dr. Szepesi states:

As a first matter, I opined during my deposition that “an output disabling a pulse generator” means that “the output signal of this first comparator disables the output pulses driving the gate of that independent of anything else.” But, at the time of my deposition I had not done a focused claim construction analysis of the limitation “a first comparator [...] having an output for disabling the pulse generator.” This is because I hadn't anticipated there being a dispute relevant to the validity analysis in view of what I understood as the plain meaning of the language. Despite the quote that Patent Owner relied upon, I believe now that a POSITA would not understand the claim language to require the first comparator to disable the output pulses independent of anything else. This belief is consistent with my responses to the first two of three successive questions in which I was asked about “disabling the pulse generator.” *It is my opinion that the operation of the disclosed embodiment requires the presence of other conditions precedent before the first comparator can disable the drive pulses and this requirement is not excluded by the claim language.*

Ex. 1016 ¶ 18 (emphasis added).

Our reviewing court has made clear that extrinsic evidence “is generally of less significance than the intrinsic record” in matters of claim construction. *Wi-LAN, Inc. v. Apple Inc.*, 811 F.3d 455, 462 (Fed. Cir. 2016) (citation omitted). Here, beyond competing declarant testimony, neither party has entered into the record extrinsic evidence, such as dictionary definitions or contemporaneous usage in the art, addressing the scope of “in response to.” Having considered the testimony upon which Patent Owner relies and weighing it against the claim language itself, the Specification’s disclosures set forth above, and the contrary testimony of Petitioner’s declarant, we find on balance that it does not warrant departing from the plain and ordinary meaning of “in response to” as Patent Owner urges. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (holding that an inventor may define specific terms used to describe invention, but must do so “with reasonable clarity, deliberateness, and precision”) (quoting *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1387-88 (Fed. Cir. 1992)).

We note that our decision to proceed with the plain and ordinary meaning of “in response to” accords with decisions of the United States Court of Appeals for the Federal Circuit and of prior decisions of this Board. *See, e.g., Instance v. On Serts Sys., Inc.*, 108 F.3d 1392 (Fed. Cir. 1997) (finding that “operable in response to” broadly defines a causal relationship between components in a claim; and finding that, because the claim drafter did not choose either of the more limiting phrases “directly operable in response to” or “immediately operable in response to,” the limitation “adhesive applicator, which is *operable in response to* the means for detecting” does not require that the “means for detecting” *immediately* initiate operation of the adhesive applicator); *see also Ex Parte Interval*

Licensing, Appeal No. 2014-002901, 2014 WL 2387821, at *6 (PTAB May 29, 2014) (holding, under the broadest reasonable interpretation, that the limitation “generating . . . *in response to* the display of [the] first segment” requires a causal relationship between the claim elements but is not limited to the generating being automatic or without user interaction). Significantly, the parties have not identified, and we are unaware of, any evidence within the prosecution history indicating that the claim term “in response to” should be accorded a meaning more narrow than its plain and ordinary meaning. *Cf. Am. Calcar, Inc. v. Am. Honda Motor Co.*, 651 F.3d 1318, 1340 (Fed. Cir. 2011) (finding the term “in response to” requires a cause-and-effect relationship in which the second event occurs in reaction to the first event; and finding, based on prosecution history estoppel, that the limitation “identifying one of the plurality of providers *in response to* the vehicle condition” requires the identifying must occur automatically upon the occurrence of the vehicle condition because the inventors distinguished during prosecution the invention as one where the identification of service providers is in response to the vehicle condition and not a user interaction).

Accordingly, for the reasons set forth above, we decline Patent Owner’s invitation to import into these disputed limitations a requirement that the claimed disabling or terminating be performed “independent of other circuit conditions.” Instead, we apply their plain and ordinary meanings.

D. Overview of Cited References

1. Hwang

Hwang “relates to the field of minimizing the power drawn from an input source by a switching mode power converter.” Ex. 1004, 1:11–12. According to Hwang, “[a] switching mode power converter monitors the

invention of Hwang. *Id.* at 3:46–48. The switching signal VSW1 controls switch SW1, and the state of VSW1 is determined by the inputs to NOR gate 60. *Id.* at 5:18–20. During normal operation, clock signal CLK initiates a triggering pulse, turning on switch SW1 every clock period of oscillator 12. *Id.* at 3:12–17. Switch SW1 remains on until the output of PWM comparator 50 sets flip flop 58 based on the comparison between error signal VEAO and ramp signal RAMP from oscillator 12. *Id.* at 5:53–6:3.

2. Balakrishnan

Balakrishnan relates to “integrated circuit devices used in switching power supplies with minimum numbers of pinouts.” Ex. 1005, 1:8–10. Figure 3 of Balakrishnan is reproduced below.

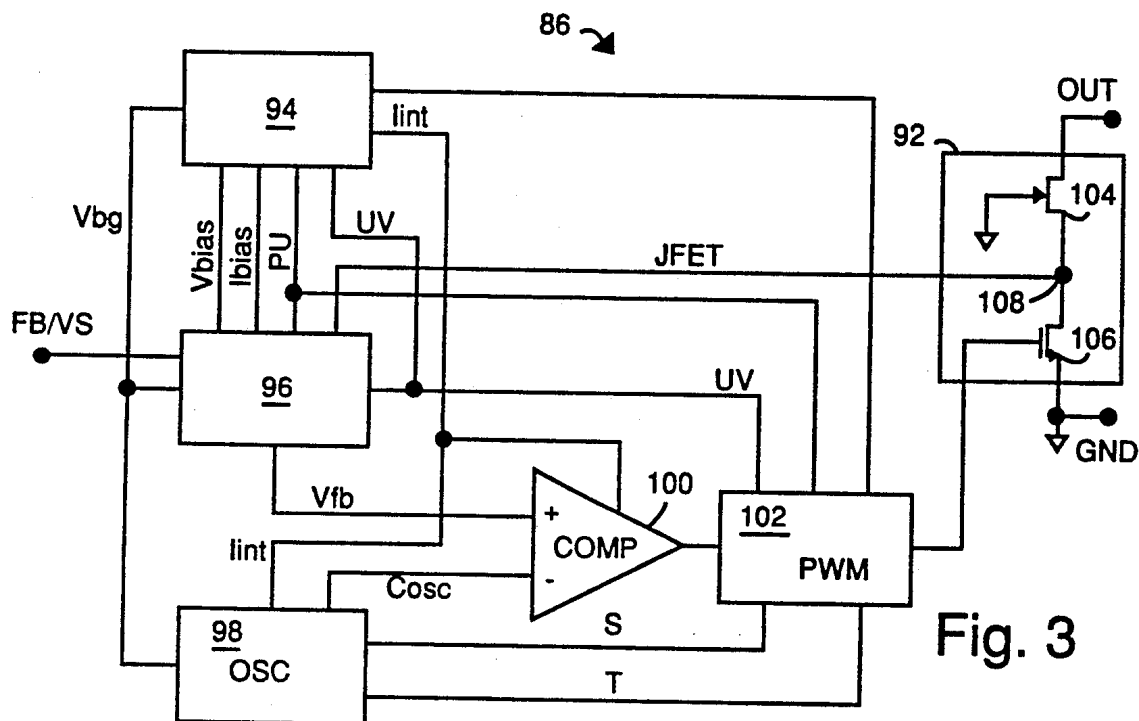


Figure 3 depicts a block diagram of a switched mode power supply chip according to the invention of Balakrishnan. *Id.* at 2:44–48. More specifically, Figure 3 shows that the disclosed integrated circuit includes

MOSFET 92, bandgap and thermal shutdown block 94, functional block 96 (including a feedback extractor, a supply voltage generator and a switching-noise filter), oscillator 98, comparator 100, and pulse width modulator 102. *Id.* at 3:47–60. Balakrishnan’s integrated circuit regulates its output voltage by comparing extracted feedback signal Vfb with a sawtooth waveform COSC from oscillator 98 to provide a pulse width modulated control signal. *Id.* at 4:14–25. While Balakrishnan’s feedback signal Vfb is within the active range of the sawtooth waveform, the pulse width sent to switch 92 will vary to regulate the output. *Id.* at 4:14–20. When extracted feedback signal Vfb is above the active range, a maximum-on pulse is sent to switch 92. *Id.* at 4:20–22. When extracted feedback signal Vfb is below the active range, the pulse width sent to MOSFET 92 will be minimum pulse or zero. *Id.* at 4:22–25.

3. *Harris*

According to Petitioner, “Harris is an application note that discloses using a HIP5060 switched mode regulator integrated circuit in a power supply application to generate a constant 5.1V output voltage.” Pet. 47 (citing Ex. 1006, 11-191). Figure 3 of Harris is reproduced below.

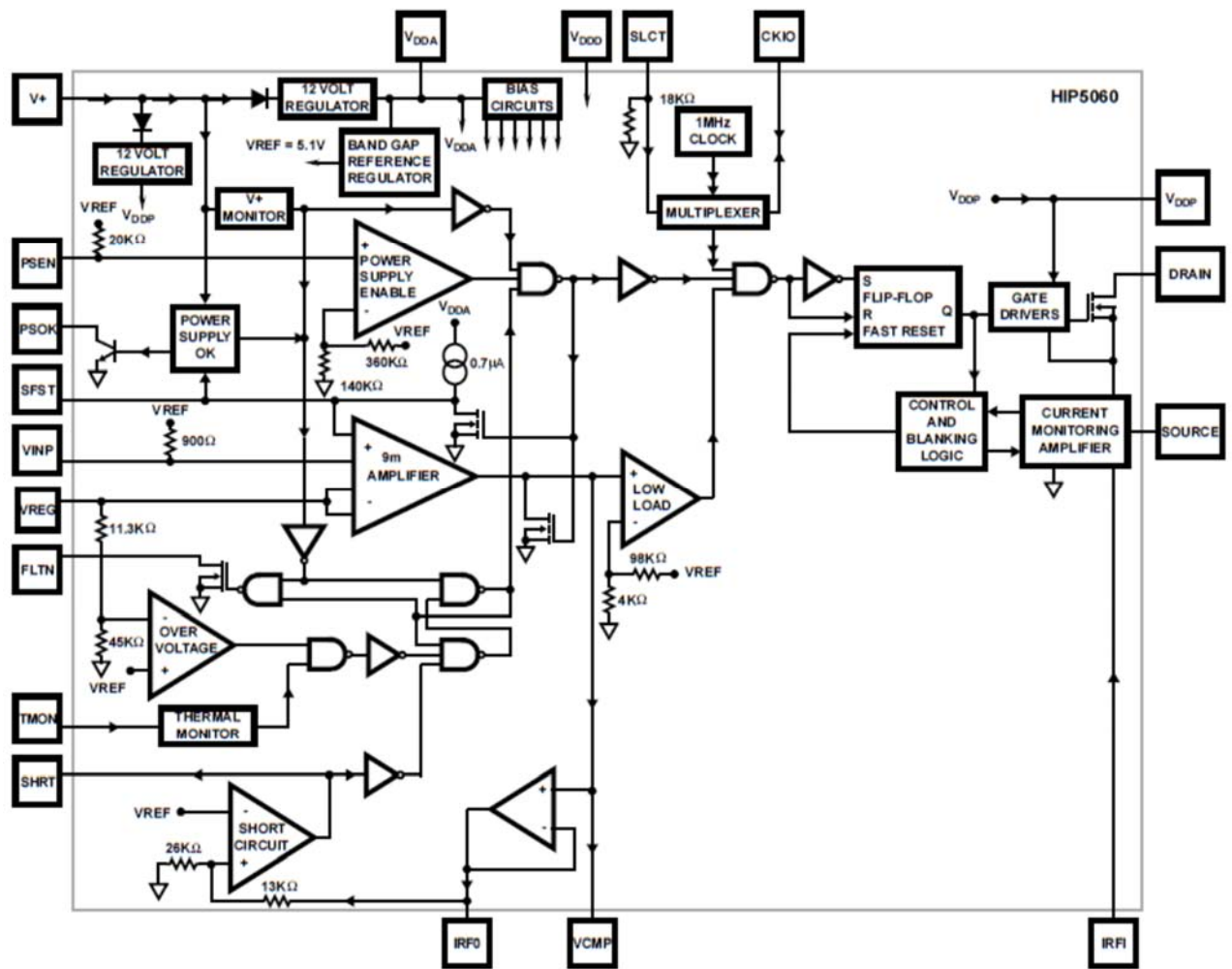


Figure 3 depicts a functional block diagram of the HIP5060, 1 MHz current controller regulator integrated circuit. Ex. 1006, 11-192. Harris describes “burst mode,” wherein cycles are skipped under light load condition. *Id.* at 11-194. Specifically, LOW LOAD comparator outputs a stop switching signal if the output voltage of error amplifier 9m AMPLIFIER drops below a low-load threshold voltage during normal operation. *Id.* at 11-193. Once the output voltage decays causing the error amplifier to increase above the threshold, switching resumes. *Id.*

E. Ground 1: Asserted Anticipation of Claims 4–7, 9, and 15–17 by Hwang

1. Claims 4–6

Petitioner and Dr. Szepesi demonstrate where each element of independent claim 4 is disclosed in Hwang. Pet. 16–21. Patent Owner does not dispute Petitioner’s contentions regarding the claimed regulator and detector. *See generally* PO Resp. Having reviewed the disclosures of Hwang upon which Petitioner and Dr. Szepesi rely, we agree with Petitioner that Hwang discloses the claimed regulator and detector. More specifically, we agree with Petitioner and Dr. Szepesi that “Hwang discloses a regulator (in Fig. 5) coupled for receiving a feedback signal (VEAO) to provide a switched drive control signal (VSW1) operating between a minimum and maximum on-time.” Pet. 17 (citing Ex. 1003 ¶¶ 97–98). We further agree that “Hwang discloses a detector (comparator 52) coupled for receiving the feedback signal (“VEAO”) and providing a detect signal (input to gate 54) when the feedback signal exceeds a threshold (“2V”) representing a predetermined duty cycle.” *Id.* at 18 (citing Ex. 1003 ¶ 99). With regard to the claimed “providing a detect signal when the feedback signal exceeds a threshold,” we agree with Petitioner and Dr. Szepesi that “[a]lthough the polarity of the detection in Hwang is such that the light load is detected when the error signal voltage becomes less than 2V (while the feedback signal is rising above a threshold in the claim)[,] both detections represent the exact same thing: the duty cycle falling below a predetermined threshold.” *Id.*

Claim 4 further recites, “a control circuit having an input coupled for receiving the detect signal, wherein the control circuit disables the switched drive control signal in response to the detect signal.” Patent Owner’s sole

contention with respect to claim 4 is that “[t]he alleged detect signal in Hwang does not satisfy this limitation” because “unlike the ’221 patent, the alleged ‘control circuit’ does not disable the switched drive control signal ‘in response to the detect signal’ ***independent of other circuit conditions.***”

PO Resp. 15–16. As discussed above, we decline to import into claim 4 a requirement that the claimed disabling must occur independent of other circuit conditions. *See supra* Section III.C.1. Because Patent Owner’s argument relies on a claim construction that we rejected above, we are not persuaded that Hwang fails to meet the limitations of claim 4. Rather, having reviewed the evidence cited by Petitioner, we agree with Petitioner that Hwang discloses the limitations of independent claim 4, arranged as recited in the claim.

Petitioner’s analysis, as supported by the Szepesi Declaration, further demonstrates where Petitioner contends each element of dependent claims 5 and 6 is disclosed in Hwang. Pet. 21–24. Patent Owner does not dispute Petitioner’s analysis beyond the argument raised with respect to claim 4. *See* PO Resp. 17. Having reviewed the evidence cited by Petitioner, we agree with Petitioner that Hwang discloses the limitations of dependent claims 5 and 6, arranged as recited in these claims, and we adopt that analysis as our own.

Accordingly, for the foregoing reasons, we find Petitioner has shown by a preponderance of the evidence that Hwang anticipates claims 4–6.

2. *Claims 7 and 9*

Petitioner’s analysis, as supported by the Szepesi Declaration, demonstrates where Petitioner contends each element of independent claims 7 and 9 is disclosed in Hwang. Pet. 24–30. Patent Owner does not dispute

Petitioner's analysis of claims 7 and 9 beyond the argument raised with respect to claim 4, namely that the disabling recited in these claims must occur independent of other circuit conditions. *See* PO Resp. 17.

Claim 7 recites, in relevant part, "wherein the gating circuit disables the drive control signal in response to the detect signal." Claim 9 recites, in relevant part, "a first comparator . . . having an output for disabling the pulse generator." Having reviewed the evidence cited by Petitioner and Dr. Szepesi, we agree with Petitioner that Hwang discloses the limitations of independent claims 7 and 9. With regard to Patent Owner's argument that the claimed disabling must occur independent of other circuit conditions, we decline to import into claims 7 and 9 such a requirement, as discussed above. *See supra* Section III.C.1. Because Patent Owner's argument relies on a claim construction that we rejected above, we are not persuaded that Hwang fails to meet the limitations of claims 7 and 9. Rather, having reviewed the evidence cited by Petitioner, we agree with Petitioner that Hwang discloses the limitations of independent claims 7 and 9, arranged as recited in these claims, and we adopt that analysis as our own.

Accordingly, for the foregoing reasons, we find Petitioner has shown by a preponderance of the evidence that Hwang anticipates claims 7 and 9.

3. *Claims 15 and 16*

Petitioner's analysis, as supported by the Szepesi Declaration, demonstrates where Petitioner contends each element of independent claim 15 and its dependent claim 16 is disclosed in Hwang. Pet. 30–33. Patent Owner's sole contention with respect to claims 15 and 16 is that the terminating recited in these claims must occur independent of other circuit conditions. PO Resp. 18.

Claim 15 recites, in relevant part, “comparing the error signal to a reference signal . . . to terminate the step of generating.” With regard to Patent Owner’s argument that the claimed terminating must occur independent of other circuit conditions, we decline to import into claim 15 and 16 such a requirement, as discussed above. *See supra* Section III.C.1. Because Patent Owner’s argument relies on a claim construction that we rejected above, we are not persuaded that Hwang fails to meet the limitations of claims 15 and 16. Rather, having reviewed the evidence cited by Petitioner, we agree with Petitioner that Hwang discloses the limitations of independent claim 15 and its dependent claim 16, arranged as recited in these claims, and we adopt that analysis as our own.

Accordingly, for the foregoing reasons, we find Petitioner has shown by a preponderance of the evidence that Hwang anticipates claims 15 and 16.

4. *Claim 17*

Claim 17 recites, in relevant part, “developing a feedback signal from the voltage; and routing the feedback signal through a resistance to develop the error signal.” Ex. 1001, 14:32–34.

In its Petition, Petitioner contends, “Hwang discloses developing a feedback signal (signal passing through PT1 to VEA) from the voltage (VOUT).” Pet. 33 (citing Ex. 1003 ¶ 88; Ex. 1004, 1:62–2:4, 4:15–17). With regard to the claimed “routing the feedback signal through a resistance to develop the error signal,” Petitioner states, “[t]he potentiometer shown in Hwang is a variable resistor through which the feedback signal is routed to develop the error signal (‘VEAO’).” *Id.* at 33–34 (citing Ex. 1003 ¶ 89; Ex. 1004, 1:29–35, 1:62–2:4, 4:15–17, Figs. 1 and 5). Petitioner thus asserts

that Hwang discloses developing a feedback signal (signal passing through PT1 to VEA) from the voltage (VOUT) and routing that feedback signal (signal routed through the potentiometer) through a resistance (the variable resistor that is the potentiometer) to develop the error signal (VEAO). *Id.*

Patent Owner argues that Petitioner fails in the Petition to account for all elements of claim 17 in the disclosure of Hwang because Hwang does not disclose routing the feedback signal (signal passing through PT1 to VEA) through potentiometer PT1 *to develop the error signal VEO*, as Petitioner contends. PO Resp. 20.

We agree with Patent Owner. Hwang describes, “[b]ecause of its parallel connection to the output of the circuit, the voltage across the capacitor C1 is equivalent to the output voltage VOUT and the voltage across the potentiometer PT1.” Ex. 1004, 1:62–67. Thus, Hwang describes that a voltage equivalent to VOUT is routed across the potentiometer PT1. *Id.* Hwang continues, “A predetermined fraction of that voltage is measured from the potentiometer PT1 forming the voltage VEA.” *Id.* Hwang thus describes routing a voltage equivalent to VOUT (i.e., “the voltage”) through potentiometer PT1 *to develop the voltage VEA* (i.e., “a feedback signal”). *Id.* Petitioner, however, contends that the alleged feedback signal is routed through potentiometer PT1 “to develop the error signal (‘VEAO’).” Pet. 33.

Contrary to Petitioner’s contentions, Hwang does not disclose routing the feedback signal (signal passing through PT1 to VEA) through potentiometer PT1 to develop the error signal VEO. Rather, Hwang discloses routing *a voltage equivalent to VOUT* through potentiometer PT1 *to develop the alleged feedback signal (signal passing through PT1 to VEA)*. Ex. 1004, 1:62–67. The error signal Petitioner identifies, VEO, is the

output of the voltage error amplifier 10 and, therefore, is developed through error amplifier 10, not potentiometer PT1. Ex. 1001, 4:55–61 (“A potentiometer PT1 is coupled across the load RL and as a *negative input into to a voltage error amplifier 10*. A reference voltage REF is coupled to a positive input of the error amplifier 10. An output VEAO of the voltage error amplifier 10 is coupled as a negative input to the comparators 50 and 52.”) (emphasis added); see also *id.* at 1:66–2:2 (“A predetermined fraction of that voltage is measured from the potentiometer PT1 forming the voltage VEA which is input into the negative terminal of the voltage error amplifier 10 and is compared to the reference voltage REF.”) (emphasis added). Accordingly, Petitioner fails in the Petition to properly account for the claimed “routing the feedback signal through a resistance to develop the error signal.”

In its Reply, Petitioner contends that “in Hwang, the resistance through which the feedback signal is routed to develop the error signal is at least the resistive components forming the potentiometer PT1 *and/or the connection from PT1 to the inverting input of error amplifier EA 10*, which SCI’s expert concedes has a non-zero resistance.” Reply 16–17 (emphasis added) (citing Ex. 1016 ¶¶ 72–82; Ex. 1022, 71:6–16). According to Petitioner, one of ordinary skill “would know that a connection has some resistance.” *Id.* at 16. Thus, the “resistance of the components that form the potentiometer PT1, *coupled with the connection from PT1 to the inverting input of error amplifier EA 10*, satisfies the claim 17 limitation of ‘routing the feedback signal through a resistance to develop an error signal.’” *Id.* (emphasis added) (citing Ex. 1016 ¶¶ 80–82). We are not persuaded by Petitioner’s arguments for two reasons.

First, Petitioner's identification in its Reply of "the connection from PT1 to the inverting input of error amplifier EA 10" as meeting the claimed resistance is not set forth in the Petition. *Compare* Pet. 33–34, with Reply 16–17. Petitioner's theory as set forth in the Reply, therefore, constitutes a new theory of unpatentability. Such a new theory is impermissible because the scope of this trial is limited by the prior art and arguments articulated in the Petition and set forth in our Decision on Institution. *See SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) ("in an *inter partes* review the petitioner is master of its complaint"); *see also* 37 C.F.R. 42.104(b)(4) (requiring that "the petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon"). Therefore, we do not consider Petitioner's identification in its Reply of "the connection from PT1 to the inverting input of error amplifier EA 10" as meeting the resistance recited in claim 17.

Second, even if we were to consider Petitioner's identification of the resistance in PT1 or the wire connecting PT1 to the inverting input of error amplifier EA 10, the error signal identified by Petitioner (VEAO) is not developed by routing the feedback signal (signal passing through PT1 to VEA) through that resistance. Rather, as explained above, the alleged feedback signal is developed by routing a voltage equivalent to VOUT through the resistance in PT1 and the wire connecting PT1 to the inverting input of error amplifier EA 10. *See* Ex. 1004, 1:62–67. The error signal VEO is developed within EA 10 based on the difference between VEA and reference voltage REF, and the gain of error amplifier EA 10. *See id.* at 4:54–61, 5:35–41.

Accordingly, for the foregoing reasons, we find Petitioner has failed to show by a preponderance of the evidence that Hwang anticipates claim 17 because Petitioner failed to identify in its Petition disclosure in Hwang of the claimed “routing the feedback signal through a resistance to develop the error signal.”

F. Ground 2: Asserted Obviousness of Claims 9–14 and 18 over Balakrishnan and Hwang

Petitioner’s analysis, as supported by the Szepesi Declaration, demonstrates where Petitioner contends each of the limitations of claims 9–14 and 18 is taught or suggested by Balakrishnan and Hwang. Pet. 41–46. Patent Owner does not dispute Petitioner’s mapping of the claims to the teachings of Balakrishnan and Hwang and, having reviewed the cited teachings, we agree with Petitioner that Balakrishnan and Hwang teach or suggest all of the limitations of claims 9–14 and 18. A determination of obviousness, however, requires more in that Petitioner must also demonstrate that “there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)).

Petitioner asserts that an artisan of ordinary skill would have combined the cited teachings and suggestions of Balakrishnan and Hwang “to provide a 3-pin switch mode power supply integrated circuit that exhibits improved efficiency at very light loads utilizing pulse skipping, whereby pulse skipping is initiated below a well-defined threshold duty cycle, thereby mitigating the disadvantages of Balakrishnan’s implementation of pulse skipping.” Pet. 38–39. According to Petitioner, “the disadvantages of

Balakrishnan's implementation of pulse skipping" include "reduced efficiency at very light load because it corresponds to the power switching transistor not being fully on, and thus operating in an inefficient state." *Id.* at 38. Moreover, one of ordinary skill would have recognized that Balakrishnan's switch mode power supply controller implemented as an integrated circuit in a 3-pin package "represented the lowest pin count in the category at the time. As such, the 3-pin implementation of Balakrishnan provided cost savings compared to prior art solutions." *Id.*

Petitioner further states that "[i]mplementing the combination would have involved adding Hwang's light load threshold comparator (52), light threshold reference (2V in Figure 5 of Hwang) and AND gate (54) to Balakrishnan's block diagram of the switched mode power supply chip shown in Figure 3." *Id.* at 39. Such an implementation "would have been well within the grasp of a POSITA [at] the time of the earliest priority date of the '221 patent and would have been obvious to implement for a POSITA." *Id.*

Patent Owner contends that one of ordinary skill in the art would not have been motivated to combine the teachings of Balakrishnan and Hwang as Petitioner asserts. PO Resp. 25–27. According to Patent Owner, "Balakrishnan expressly prioritizes stability over efficiency." *Id.* at 27 (citing Ex. 2003, 74:14–21). Patent Owner argues that the proposed combination, however, would create instability in the circuit. *Id.* at 29 (citing Ex. 2001 ¶ 62). Patent Owner elaborates:

the Balakrishnan circuit, in order to achieve its goals of a three-pin regulator, is designed around the assumption that the supply current is constant. If, as Petitioner proposes, cycle skipping is initiated, no current would be consumed

by the chip to charge the gate of the switching transistor during the cycles that are skipped.

Id. Therefore, Patent Owner contends, “Petitioner’s proposed modifications to Balakrishnan make the [instability] problem even worse by even further reducing the supply current consumption due to cycle skipping.” *Id.* at 29–30.

We are not persuaded by Patent Owner’s arguments. Petitioner identifies at least two motivations for the proposed combinations: (i) cost savings because utilizing the 3-pin implementation of Balakrishnan would provide the lowest pin count in the category at the time and (ii) improved efficiency operating at very light loads utilizing pulse skipping. Pet. 38. Patent Owner’s arguments do not dispute that the proposed modification would result in cost savings. See PO Resp. 25–30; Sur-Reply 15–19. Moreover, we do not agree with Patent Owner that “Balakrishnan expressly prioritizes stability over efficiency.” PO Resp. 27. Patent Owner fails to identify any such statement in Balakrishnan. See *id.* Even assuming *arguendo* that Balakrishnan suggests prioritizing stability over efficiency and that the proposed modification would, in fact, introduce some amount of instability, such a suggestion is insufficient to defeat the proffered motivation. “[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.” *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006). Finally, as Petitioner correctly points out, Hwang explicitly identifies the motivation to improve efficiency, stating, “[e]fficient use of power is a desirable characteristic for all electronic systems. Minimizing the power drawn from a line voltage source by a switching mode power converter will

allow a user to realize significant savings in the cost of power consumption.”
Reply 18 (citing Ex. 1004, 2:63–67).

Accordingly, for the foregoing reasons, we find Petitioner has shown by a preponderance of the evidence that Balakrishnan and Hwang together render obvious claims 9–14 and 18.

G. Ground 3: Asserted Anticipation of Claim 7, 9, 15, 16, and 18 by Harris

In this ground, Petitioner asserts that Harris anticipates each of claims 7, 9, 15, 16, and 18. Pet. 49–56. We determined above that claims 7, 9, 15, and 16 are anticipated by Hwang and that claims 9 and 18 are rendered obvious over the combined teachings of Hwang and Balakrishnan. See *supra* Sections III.E.1–3 and F. Accordingly, having determined all claims challenged under this ground have been shown to be invalid under other grounds addressed above, we decline to reach this cumulative ground.

IV. MOTION TO STRIKE

Patent Owner moves to strike arguments and related evidence from Petitioner’s Reply on the following topics:

- (i) whether, under Ground 3, Harris inherently meets the limitations of claims 7, 9, and 15 (Paper 22, 2–4);
- (ii) the construction of the limitation “developing a feedback signal from the voltage,” as recited in claim 17 (*id.* at 4–5);
- (iii) whether the resistance recited in claim 17 is met by Hwang’s “connection from PT1 to the inverting input of error amplifier EA 10” (*id.* at 5); and

- (iv) the use of two textbooks to show that one of ordinary skill in the art would have been motivated to combine Balakrishnan and Hwang (*id.* at 5).

Patent Owner's motion is moot in light of our determinations above. Specifically, regarding Patent Owner's first topic, we declined to address Petitioner's third asserted ground, which asserts anticipation based on Harris, because we found that Petitioner has shown by a preponderance of the evidence that claims 7, 9, and 15 were anticipated or rendered obvious as alleged in Grounds 1 and 2. Regarding Patent Owner's second topic, we did not construe the limitation "developing a feedback signal from the voltage," as recited in claim 17, because construction of this limitation would not alter our determination above that Petitioner failed to show in the Petition that Hwang discloses the resistance recited in claim 17. Regarding Patent Owner's third topic, we declined to consider, based on *SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018), Petitioner's late identification of components allegedly meeting the resistance recited in claim 17. Finally, regarding Patent Owner's fourth topic, even without relying on these textbooks, we determined above that Petitioner had shown by a preponderance of the evidence that one of ordinary skill in the art would have been motivated to combine Balakrishnan and Hwang. Accordingly, we dismiss as moot Patent Owner's motion.

V. MOTION TO EXCLUDE

Patent Owner moves to exclude Exhibits 1020, 1023, 1025, 1032 and portions of Dr. Szepesi's Supplemental Declaration (Ex. 1016) relying thereon. Paper 23, 8. Petitioner offered these exhibits and testimony in support of its Ground 3 asserting anticipation based on Harris. As discussed

above, we declined to address Petitioner's Ground 3 asserting anticipation based on Harris because we found that Petitioner has shown a preponderance of the evidence that all claims challenged under Ground 3 were anticipated or rendered obvious as alleged in Grounds 1 and 2. Accordingly, we dismiss as moot Patent Owner's motion.

VI. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 4–7, 9–16, and 18 are anticipated or rendered obvious. Petitioner, however, has failed to carry its burden on its challenge to claim 17.

VII. ORDER

It is, therefore,

ORDERED that claims 4–7, 9–16, and 18 of the '221 patent are unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Strike is *dismissed as moot*;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *dismissed as moot*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2018-00180
Patent 6,597,221 B2

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