

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.,  
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,  
Patent Owner.

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IPR2018-00989  
Patent 5,943,274

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Before MICHELLE N. WORMMEESTER, GARTH D. BAER, and  
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining Some Challenged Claims Unpatentable  
35 U.S.C. § 318(a)

## I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–12, 14–16, and 20–23 of U.S. Patent No. 5,943,274 (Ex. 1001, “the ’274 patent”). Under 37 C.F.R. § 42.107(b), North Star Innovations, Inc. (“Patent Owner”) waived its Preliminary Response (Paper 8).

In our Institution Decision (Paper 10, “Inst. Dec.”), we instituted review based on all the grounds set forth in the Petition. We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that claims 1, 3–9, 11, 12, 14–16, and 20–23 of the ’274 patent are unpatentable but has not shown by a preponderance of the evidence that claims 2 and 10 are unpatentable. *See* 35 U.S.C. § 316(e).

## II. BACKGROUND

### A. *Procedural History*

After we instituted review, Patent Owner filed a Response (Paper 17, “Resp.”), Petitioner filed a Reply (Paper 24, “Reply”), and Patent Owner filed a Sur-reply (Paper 26, “Sur-reply”). On July 18, 2019, we held an oral hearing. *See* Paper 30 (“Tr.”).

On July 19, 2019, we issued an order authorizing the parties to file opening and responsive briefs addressing the following issues:

- (1) The construction of the term “clock signal” in the ’274 patent claims and the effect of any construction identified by a party on the anticipation issues.

(2) Whether Tachibana anticipates '274 patent claim 2 if the term “clock delay circuit” in claim 2 means “a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version.”

Paper 29, 1. Then, Patent Owner filed an opening brief (Paper 31), Petitioner filed an opening brief (Paper 32), Patent Owner filed a responsive brief (Paper 33), and Petitioner filed a responsive brief (Paper 34).

### *B. Related Proceedings*

Petitioner and Patent Owner identify the following district-court cases where Patent Owner has asserted the '274 patent: *North Star Innovations, Inc. v. Micron Technology, Inc.*, No. 17-cv-506-LPS-CJB (D. Del. filed May 3, 2017), and *North Star Innovations, Inc. v. Kingston Technology Co.*, No. 8:17-cv-1833 (C.D. Cal. filed Oct. 19, 2017). Pet. 10–11; Paper 5, 1.

### *C. The '274 Patent (Ex. 1001)*

The '274 patent discloses a semiconductor memory with an output stage including a differential amplifier, a level converter, a timing circuit, a clock-free latch, an impedance-control circuit, and an output driver. Ex. 1001, code (57), 2:50–4:13, Fig. 2; see Pet. 13. Figure 2 of the '274 patent is reproduced below:

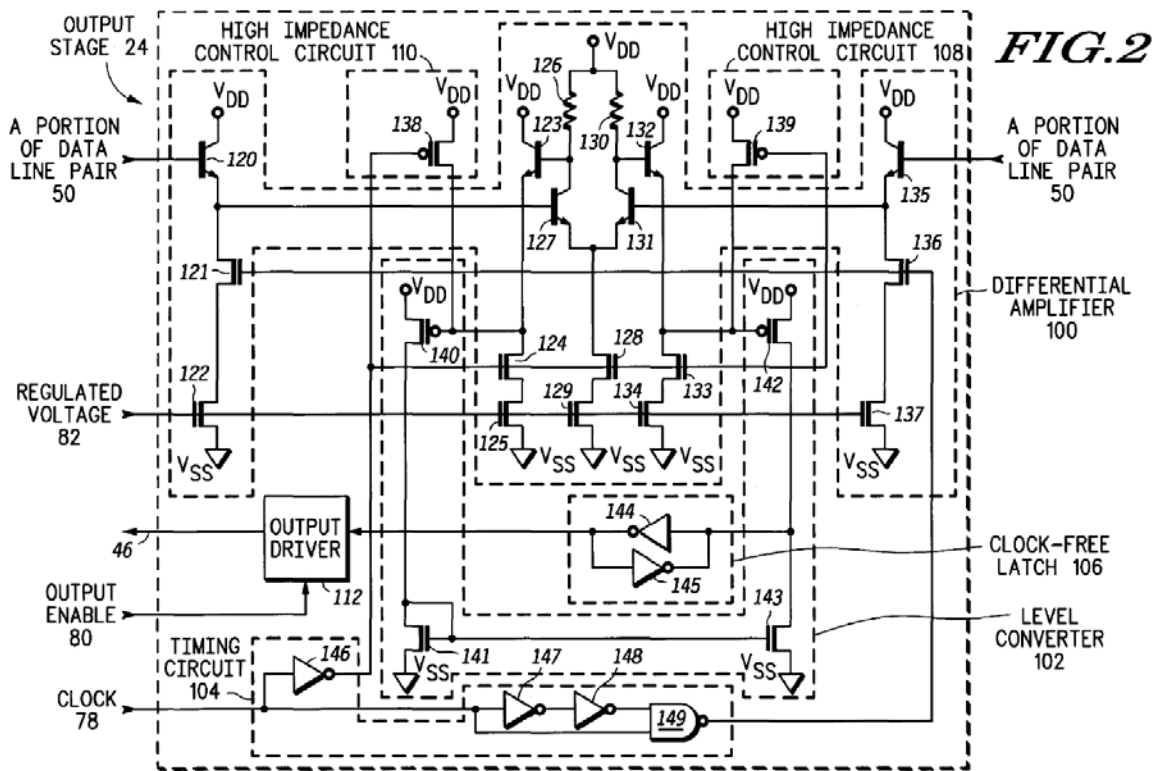


Figure 2 “illustrates in partial block diagram form and partial schematic diagram form” an output stage for a semiconductor memory “in accordance with one embodiment” of the invention. Ex. 1001, 1:51–53.

In Figure 2, the output stage includes the following circuit elements: differential amplifier 100, level converter 102, timing circuit 104, clock-free latch 106, impedance-control circuits 108 and 110, and output driver 112. *Id.* at 2:50–57, Fig. 2. Timing circuit 104 receives clock signal 78 as an input. *Id.* at 3:63–4:1, Fig. 2. The ’274 patent explains that “alternate embodiments of the present invention may use different circuit elements than those illustrated in” Figure 2. *Id.* at 3:11–13; *see id.* at 4:48–51.

The ’274 patent instructs that semiconductor memories commonly use a differential amplifier and latch as follows. A differential amplifier located “between the bit cell array and the data output signals” detects “a small voltage difference and amplifies that small voltage difference into a larger

voltage difference.” *Id.* at 1:23–29. A latch located “between the differential amplifier and the data I/O pad” latches the data output signals “to provide a consistent logic level one or logic level zero at the data I/O pad while the differential amplifier is detecting the next data value.” *Id.* at 1:29–33.

The ’274 patent explains that prior-art circuits “use[d] two clock signals,” i.e., “one clock signal to clock the differential amplifier portion, and one clock signal to clock the latch portion of the memory output stage.” *Id.* at 1:33–37. The patent also explains that using “two clock signals” caused problems because “the timing relationship between the two clocks cannot be consistently controlled due to manufacturing process variations, temperature variations, power supply voltage variations, etc.” *Id.* at 1:37–40. The patent purports to solve those problems by providing an output stage “that does not require two or more clocks, and thus does not require that a precise timing relationship between two or more clocks be maintained.” *Id.* at 1:40–44.

In particular, the ’274 patent instructs that “clock 78 and timing circuit 104” may in “one embodiment” provide “two versions of clock signal 78” to differential amplifier 100. *Id.* at code (57), 5:20–23, 5:26–29. The two versions selectively enable and disable differential amplifier 100 “to reduce power [consumption] and to increase speed.” *Id.* at 5:23–25; *see id.* at code (57), 5:18–20. The two versions “are not separate clock signal[s] as used by the prior art, but are merely different versions of the same clock.” *Id.* at 5:34–36.

In addition, the ’274 patent explains that the two versions “have approximately simultaneous rising [or enabling] edges” and “a delay

between their [falling or] disabling edges,” i.e., “purposely skewed” disabling edges. *Id.* at code (57), 5:26–37. The patent describes the two versions as “slightly different versions” of the input clock signal. *Id.* at 5:43–44.

But the ’274 patent also explains that “[t]he present invention merely requires a single clock signal” and that “some embodiments of the present invention may use clock 78 directly as the only clock, without using timing circuit 104 to create two slightly different versions.” *Id.* at 5:25–26, 5:41–44; *see id.* at code (57).

#### *D. The Challenged Claims*

Petitioner challenges independent claims 1, 14, 20, and 21 and dependent claims 2–12, 15, 16, 22, and 23. Pet. 12. Independent claims 1, 14, and 21 exemplify the challenged claims and read as follows:

1. An apparatus for use as an output stage of a memory device, the apparatus comprising:
  - a timing circuit;
  - a differential amplifier responsive to the timing circuit;
  - an impedance control circuit;
  - a level converter responsive to the differential amplifier and the impedance control circuit; and
  - a clock-free latch responsive to the level converter.
14. A method of amplifying a signal to produce a latched digital signal, the method comprising the steps of:
  - amplifying a differential input to produce a differential output in response to a clock signal;
  - level converting the differential output to produce a level converted signal;

detecting a change in impedance at an input of a clock-free latch and latching the level converted signal at the clock-free latch to produce the latched digital signal; and

outputting the latched digital signal.

21. A memory device comprising:

[a] bit cell array;

an amplifier module responsive to the bit cell array; and

an output stage responsive to the amplifier module, the output stage comprising:

a differential amplifier responsive to a clock signal;

a high impedance control circuit;

a level converter responsive to the differential amplifier and responsive to the high impedance control circuit; and

a clock-free latch responsive to the level converter.

Ex. 1001, 6:62–7:3, 7:56–8:9, 8:37–47.

#### *E. References*

For its challenges, Petitioner relies on the following prior-art references:

1. Japanese Patent Application Publication No. H4-170816 to Tachibana et al., titled “Semiconductor Integrated Circuit,” and published June 18, 1992 (Ex. 1005, “Tachibana”).

2. U.S. Patent No. 4,891,792 to Hanamura et al., titled “Static Type Semiconductor Memory with Multi-Stage Sense Amplifier,” and issued January 2, 1990 (Ex. 1006, “Hanamura”).

#### *F. Testimonial Evidence*

To support its challenges, Petitioner relies on two declarations of R. Jacob Baker, Ph.D. (Ex. 1003, “Baker Decl.”; Ex. 1028, “Baker Reply

Decl.”). Patent Owner relies on the declaration of Sunil P. Khatri, Ph.D. (Ex. 2001, “Khatri Decl.”). The record includes a transcript of Dr. Khatri’s deposition (Ex. 1029, “Khatri Dep.”).

### *G. Asserted Grounds of Unpatentability*

We instituted an *inter partes* review of claims 1–12, 14–16, and 20–23 on the following grounds:

| Claims Challenged        | 35 U.S.C. §         | Reference(s)/Basis                                             |
|--------------------------|---------------------|----------------------------------------------------------------|
| 1–3, 8–12, 14–16, 20, 21 | 102(b) <sup>1</sup> | Tachibana                                                      |
| 4–7                      | 103(a)              | Tachibana in view of an ordinarily skilled artisan’s knowledge |
| 22, 23                   | 103(a)              | Tachibana and Hanamura                                         |

Inst. Dec. 28.

## III. PATENTABILITY ANALYSIS

### *A. Applicable Legal Principles*

#### 1. BURDEN

Petitioner bears “the burden of proving . . . unpatentability by a preponderance of the evidence.” 35 U.S.C. § 316(e); *see* 37 C.F.R. § 42.1(d). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

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<sup>1</sup> On September 16, 2012, the Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), took effect and amended 35 U.S.C. §§ 102 and 103. Because the ’274 patent’s filing date predates the AIA’s amendments to §§ 102 and 103, this decision refers to the pre-AIA versions of §§ 102 and 103.

## 2. CLAIM CONSTRUCTION

The '274 patent has expired. *See* Ex. 1001, code (22); Pet. 20; Resp. 23. Because the '274 patent has expired, we construe disputed claim terms according to the principles articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See Black & Decker, Inc. v. Positec USA, Inc.*, 646 F. App'x 1019, 1024 (Fed. Cir. 2016) (employing a *Phillips*-type claim construction for a patent that expired approximately three months before the Board's final written decision); *In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) (explaining that "the Board's review of the claims of an expired patent is similar to that of a district court's review"). Further, the parties agree that we should construe disputed claim terms according to *Phillips*. *See* Pet. 20; Resp. 23.

According to *Phillips*, claim terms "are generally given their ordinary and customary meaning" as understood by "a person of ordinary skill in the art." *Phillips*, 415 F.3d at 1312–13. "[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent," including the other claims ("both asserted and unasserted") and the written description. *Id.* at 1313–14, 1321. Further, "the prosecution history can often inform the meaning of the claim language by demonstrating how" an inventor or an examiner understood the claim language. *Id.* at 1317. Thus, the meaning of a disputed claim term may be determined by "look[ing] principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

To the extent that the parties raise patentability issues requiring claim construction, we address claim construction in the following sections when considering the patentability issues. We do so to provide better context to explain the dispute about claim construction and our resolution of the dispute.

*B. Anticipation by Tachibana:  
Claims 1–3, 8–12, 14–16, 20, and 21*

1. ANTICIPATION UNDER 35 U.S.C. § 102

“[T]o demonstrate anticipation, the proponent must show ‘that the four corners of a single, prior art document describe every element of the claimed invention.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Xerox Corp. v. 3Com Corp.*, 458 F.3d 1310, 1322 (Fed. Cir. 2006)). The prior-art document “must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Hence, a patent challenger cannot rely on portions from different embodiments in a prior-art document to demonstrate anticipation. *See id.* at 1369, 1371. We analyze the anticipation issues accordingly.

2. OVERVIEW OF TACHIBANA (EX. 1005)

Tachibana describes several embodiments of an output buffer circuit for a semiconductor memory. Ex. 1005<sup>2</sup>, 110–20, Figs. 1, 10, 15, 17; *see*

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<sup>2</sup> For this publication and other publications, a page number in the citation references a page number in the publication itself rather than a page number added by Petitioner, e.g., 1005 p. 1, 1005 p. 2, 1005 p. 3, etc.



to emitter-coupled logic, and the acronym MOS refers to metal-oxide semiconductor. *IEEE 100 The Authoritative Dictionary of IEEE Standards Terms* 351, 708 (7th ed. 2000) (“*IEEE 7th*”); *see* Pet. 21.

In the Figure 1 embodiment, various circuit elements connect to terminals 19, 21, 26, and 27 that receive control signals from a timing circuit. Ex. 1005, 110–11, 116–17, 124, Figs. 8–9; Ex. 1003 ¶¶ 58, 72, A3–A5, A29–A31. Although Tachibana calls those terminals “clock signal terminals,” the timing circuit generates control signals for those terminals from an address signal. Ex. 1005, 111, 116–17, Figs. 8–9; *see* Ex. 1003 ¶ 80, B1. Tachibana explains, however, that “if there is a standard clock, for instance in the case of STRAM [self-timed random-access memory], it goes without saying that a control signal can easily be generated from the standard clock.” Ex. 1005, 117; *see* Ex. 1003 ¶¶ 70, 75, B1.

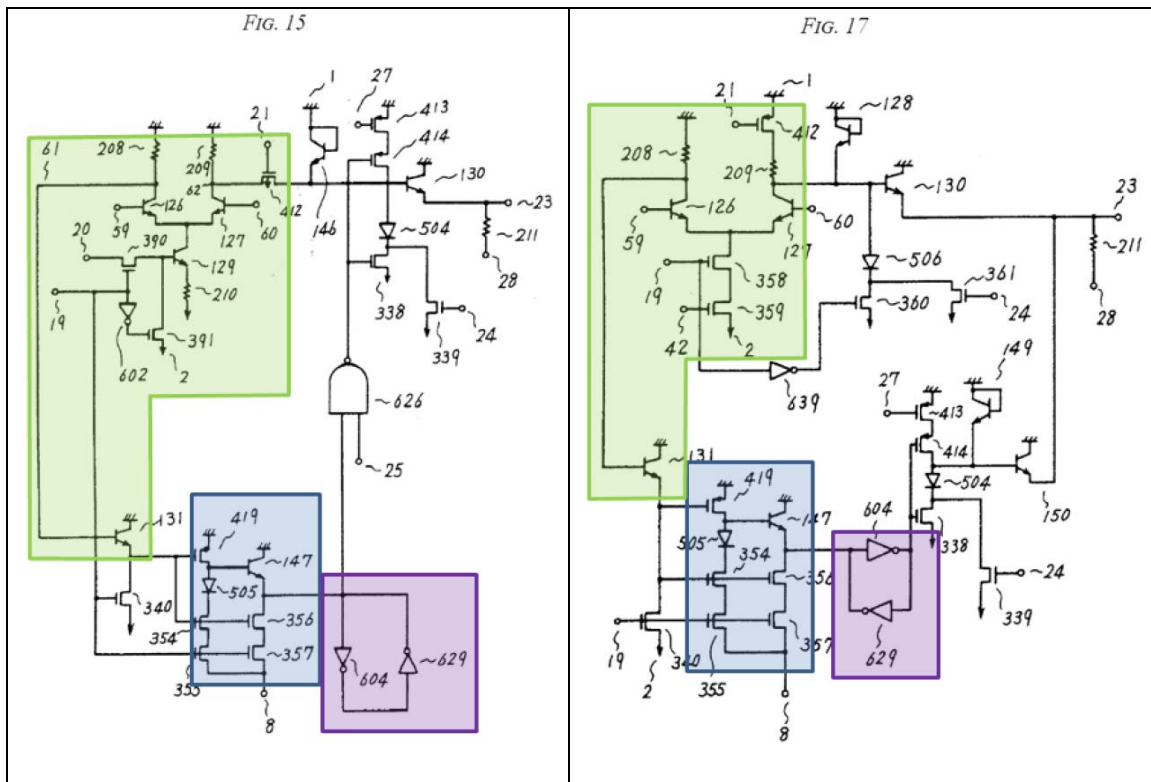
In the Figure 1 embodiment, the differential amplifier’s first stage receives signals at input terminals 17 and 18 and produces amplified signals at terminals 59 and 60 for the differential amplifier’s second stage. Ex. 1005, 110–13, Fig. 1. The second stage receives the amplified signals at terminals 59 and 60 and produces further amplified signals at output terminals 61 and 62. *Id.* at 112–14, Fig. 1. The ECL-MOS level-conversion circuit receives the signals from terminals 61 and 62 and produces a level-converted signal at terminal 63 for the latch circuit. *Id.* at 112–14, Fig. 1; Ex. 1003 ¶ 53. Depending on the control signals at terminals 19, 21, 26, and 27, the latch circuit may latch the signal at terminal 63. Ex. 1005, 112–16, Figs. 1–2; Ex. 1003 ¶¶ 55–57. Figure 1’s output buffer circuit provides an output signal at output terminal 23. Ex. 1005, 110–12, 115–16, Figs. 1, 10; *see* Ex. 1003 ¶ 79, A1–A3.

Tachibana's Figures 15 and 17 illustrate related but somewhat simplified embodiments of an output buffer circuit for a semiconductor memory. Ex. 1005, 119–20, Figs. 15, 17; *see* Ex. 1003 ¶¶ 58–61; Ex. 2001 ¶¶ 78–86. For example, each embodiment employs a single-stage differential amplifier and a latch circuit formed by only two inverters. Ex. 1005, 119–20, Figs. 15, 17; *see* Ex. 1003 ¶¶ 58–61; Ex. 2001 ¶¶ 81, 85.

Tachibana states that the Figure 15 embodiment “achieves the same operation” as the Figure 1 embodiment. Ex. 1005, 119; *see* Ex. 2001 ¶¶ 62, 79. Similarly, Tachibana states that the Figure 17 embodiment “realizes the same operations” as the Figure 1 and 15 embodiments. Ex. 1005, 120; *see* Ex. 2001 ¶¶ 62, 83. Further, Tachibana describes the operation of all three embodiments as “essentially the same.” Ex. 1005, 119–20; *see* Ex. 2001 ¶¶ 62, 78–79, 83. Tachibana explains that elements or terminals in Figures 1, 15, and 17 with the same number correspond to the same element or terminal. Ex. 1005, 119–20; *see* Ex. 1003, A3; Ex. 2001 ¶¶ 62, 79, 82–83, 86, 88.

### 3. INDEPENDENT CLAIM 1

Petitioner contends that Tachibana describes two embodiments of an output buffer circuit that each anticipate claim 1: the Figure 15 embodiment and the Figure 17 embodiment. Pet. 29–54. To support its contention, Petitioner presents the following annotated versions of Figures 15 and 17:



Pet. 24–27; Ex. 1003 ¶¶ 58, 60. According to Petitioner, these annotated versions of Figures 15 and 17 each show a differential amplifier highlighted in green, an ECL-MOS level-conversion circuit highlighted in blue, and a latch circuit highlighted in purple. Pet. 25–26; Ex. 1003 ¶¶ 58–61.

(a) Preamble

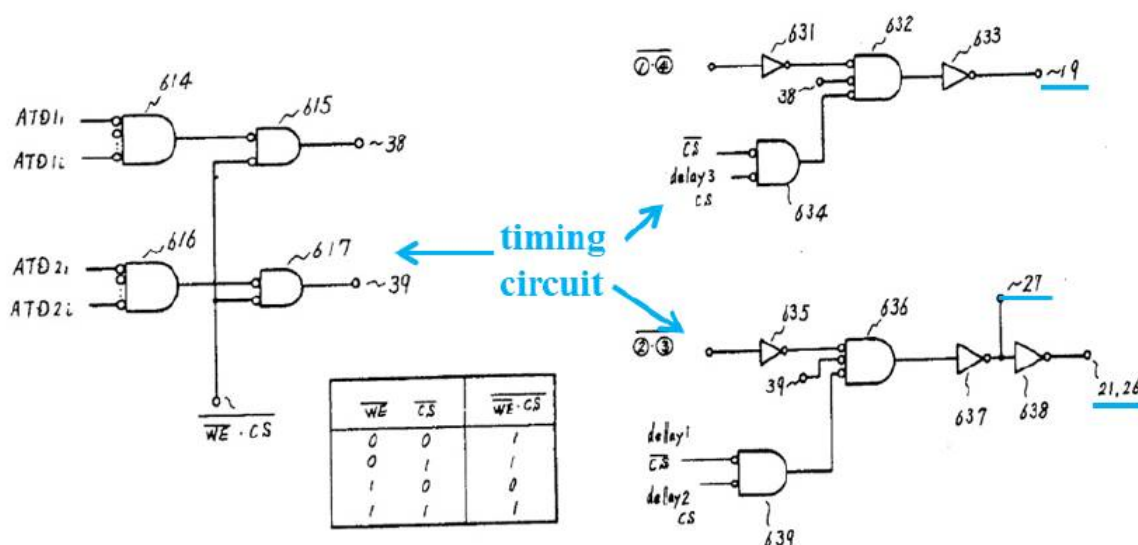
Claim 1’s preamble recites “[a]n apparatus for use as an output stage of a memory device.” Ex. 1001, 6:63–64. Petitioner contends that Tachibana “discloses a BiCMOS memory” that “is a memory device.” Pet. 29 (citing Ex. 1005, 117, Fig. 10); see Ex. 1003, A1–A3. Petitioner also contends that Tachibana’s “BiCMOS memory includes an output buffer circuit” that “is an output stage of the BiCMOS memory.” Pet. 29; see Ex. 1003, A1–A3. In addition, Petitioner identifies “the circuits in Figures 15 and 17” as “output stages for a BiCMOS memory.” Pet. 29; see Ex. 1003, A1–A3.

Patent Owner does not make any arguments specific to claim 1's preamble. *See, e.g.*, Resp. 28–42.

As discussed above, Tachibana describes several embodiments of an output buffer circuit for a semiconductor memory, e.g., the Figure 15 and 17 embodiments. Ex. 1005, 110–20, Figs. 1, 10, 15, 17; *see* Ex. 1003 ¶¶ 51–52, 58–61. Thus, we agree with Petitioner that the Figure 15 and 17 embodiments each correspond to “[a]n apparatus for use as an output stage of a memory device” according to claim 1's preamble. Ex. 1005, 117, 119–20, Figs. 10, 15, 17; *see* Ex. 1003 ¶¶ 58–61, A1–A3.

(b) Timing Circuit

Claim 1 recites “a timing circuit.” Ex. 1001, 6:65. To show the claimed “timing circuit,” Petitioner directs us to Tachibana's Figures 8 and 9. Pet. 31–32; *see* Ex. 1003, A3–A4. Petitioner provides the following annotated excerpts from Figures 8 and 9 to illustrate the claimed “timing circuit”:



Pet. 32; *see* Ex. 1003, A4. These annotated excerpts depict the NAND gates, NOR gates, and inverters comprising a timing circuit that generates

control signals at terminals 19, 21, 26, and 27 for the output buffer circuits in Figures 1, 15, and 17. Ex. 1005, 116–17, 119–20, Figs. 1, 8–9, 15, 17; see Ex. 1003, A3–A7; Ex. 2001 ¶¶ 98–99.

Tachibana states that Figures 8 and 9 show “how to generate a control signal,” i.e., “how to generate a signal for terminals 19, 21, 26, 27” in an output buffer circuit. Ex. 1005, 116–17, 124; see Ex. 1003, A3–A4, A29–A30. Tachibana explains that the NAND gates, NOR gates, and inverters in Figures 8 and 9 “creat[e] several delay signals from an address signal.” Ex. 1005, 116–17; see Ex. 1003 ¶ 80, B1. For the Figure 15 and 17 embodiments, Tachibana identifies terminals 19, 21, and 27 as “control terminals.” Ex. 1005, 119–20; see *id.* at 124. Consistent with Tachibana’s disclosure, Dr. Baker states that Figures 8 and 9 depict “a circuit for generating control signals that are received at terminals 19, 21, 26 and 27” in Figures 15 and 17. Ex. 1003, A3; see *id.* at A29.

For the reasons discussed above, Tachibana discloses “a timing circuit” according to claim 1 for each of the Figure 15 and 17 embodiments.

In a post-hearing brief, Patent Owner asserts for the first time that Tachibana does not anticipate claim 1 because “Tachibana does not disclose” that the output buffer circuits in Figures 15 and 17 receive signals from the timing circuit in Figures 8 and 9. Paper 31, 11. Patent Owner contends that “it is only the output buffer circuit” in Figure 1 that receives signals from that timing circuit. *Id.* Patent Owner waived that argument by not making it earlier. See *Hannon v. Dep’t of Justice*, 234 F.3d 674, 680 (Fed. Cir. 2000); Paper 11, 5 (“Patent Owner is cautioned that any arguments for patentability not raised in the response may be deemed waived.”).

In any event, Patent Owner’s belated argument lacks merit. Tachibana explains that the output buffer circuits in Figures 15 and 17 operate “essentially the same” as the output buffer circuit in Figure 1. Ex. 1005, 119–20; *see* Ex. 2001 ¶¶ 62, 78–79, 83. Tachibana also explains that terminals in Figures 1, 15, and 17 with the same number correspond to the same terminal. Ex. 1005, 119–20; *see* Ex. 1003, A3; Ex. 2001 ¶¶ 62, 79, 82–83, 86, 88.

As Patent Owner concedes, the output buffer circuits in Figures 15 and 17 each receive control signals at terminals 19, 21, and 27. Ex. 1005, 116–17, 119–20, Figs. 15, 17; *see* Paper 31, 11. Tachibana discloses only one circuit that generates control signals at terminals 19, 21, and 27, i.e., the timing circuit in Figures 8 and 9. Ex. 1005, 116–17, Figs. 8–9. Thus, that timing circuit generates control signals for the output buffer circuits in Figures 15 and 17 just as it generates control signals for the output buffer circuit in Figure 1. Ex. 1003, A3–A7; Ex. 2001 ¶¶ 98–99. Further, when discussing differences between the output buffer circuits in Figures 1, 15, and 17, Tachibana does not identify any differences in the control signals at terminals 19, 21, and 27 or how those signals function to enable or disable any circuit elements. Ex. 1005, 119–20.

In addition, Dr. Khatri admits that Tachibana’s timing circuit generates control signals for the output buffer circuits in Figures 15 and 17. Ex. 2001 ¶¶ 98–99. He states that Tachibana “discloses, in FIGS. 8 and 9, a circuit . . . that generates the signals for terminals 19, 21, and 27” and that “terminals 19, 21, and 27 are inputs to the output buffer circuits of the embodiments of FIGS. 15 and 17.” *Id.* ¶¶ 98–99.

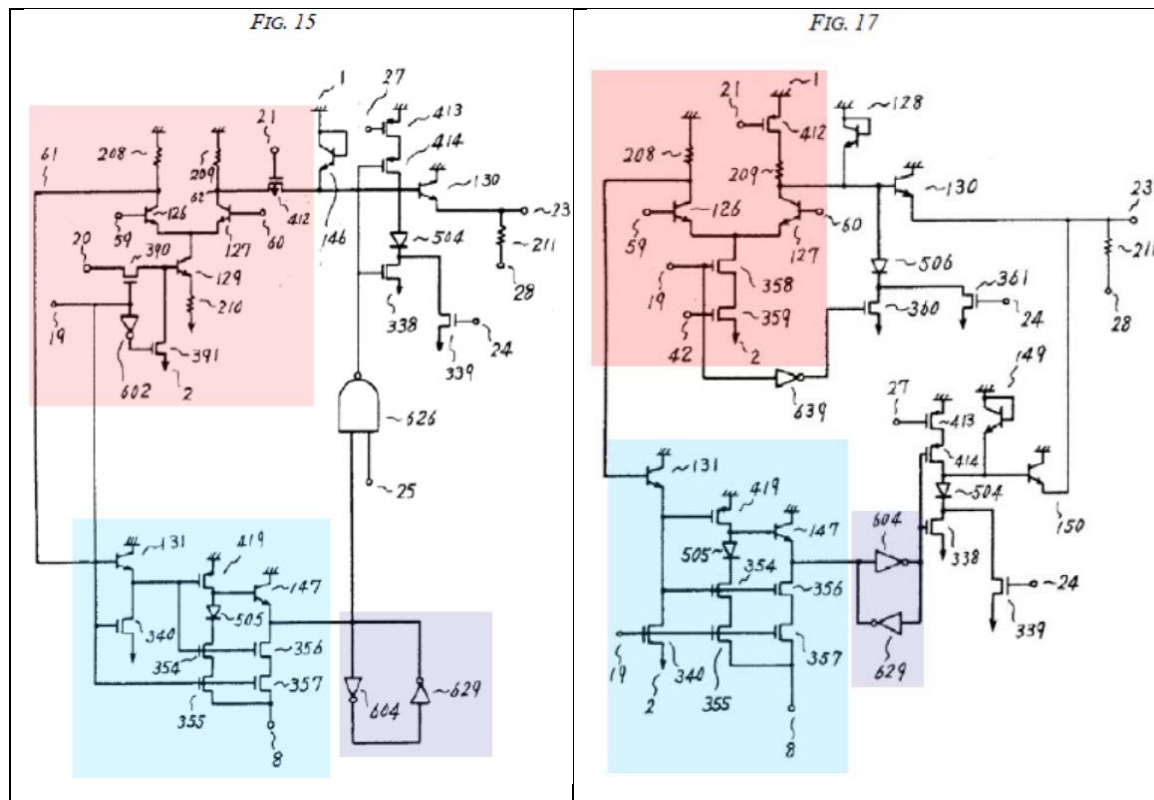
(c) Differential Amplifier

Claim 1 recites “a differential amplifier responsive to the timing circuit.” Ex. 1001, 6:66. For the claimed “differential amplifier” in Figure 15, Petitioner identifies the following components: “resistors 208 and 209, bipolar transistors 126 and 127, PMOS transistor 412, bipolar transistor 129, resistor 210, NMOS transistors 390 and 391, inverter circuit 602, and bipolar transistor 131.” Pet. 33–34; *see* Ex. 1003, A7–A9, A11–A13. For the claimed “differential amplifier” in Figure 17, Petitioner identifies the following components: “resistors 208 and 209, bipolar transistors 126 and 127, NMOS transistors 358 and 359, and PMOS transistor 412.” Pet. 35–36; *see* Ex. 1003, A7–A11. Although Petitioner’s component listing for Figure 17 lacks bipolar transistor 131, Petitioner’s annotated version of Figure 17 shows bipolar transistor 131 included in the differential amplifier. Pet. 35–36.

Patent Owner does not dispute that each embodiment includes a differential amplifier. Resp. 20–22; *see* Ex. 2001 ¶¶ 63–64. Instead, Patent Owner disputes that each differential amplifier includes bipolar transistor 131. Resp. 20–22; *see* Ex. 2001 ¶¶ 63–64. As discussed in detail below, whether each differential amplifier includes bipolar transistor 131 relates to claim 10’s requirement that “the differential amplifier has an output driven by at least one of an emitter and a source of a transistor.” *See* Resp. 47–50; Sur-reply 20–21; Ex. 1001, 7:27–29; Ex. 2001 ¶¶ 102–105.

Responding to Petitioner’s argument for claim 1, Patent Owner asserts that Tachibana “makes clear that bipolar transistor 131” is part of the level converter in each of Figures 15 and 17. Resp. 40; *see id.* at 34–39, 50;

Ex. 2001 ¶¶ 82, 86. To support its assertion, Patent Owner presents the following annotated versions of Tachibana’s Figures 15 and 17:



Resp. 21–22; Ex. 2001 ¶¶ 63–64, 80, 84. According to Patent Owner, these annotated versions of Figures 15 and 17 each show a differential amplifier highlighted in red, a level converter highlighted in blue, and a latch circuit highlighted in purple. Resp. 20–22; *see* Ex. 2001 ¶¶ 63–64.

We agree with Patent Owner that the differential amplifiers in Figures 15 and 17 do not include bipolar transistor 131. For Figure 1, Tachibana describes bipolar transistor 131 as part of ECL-MOS level-conversion circuit 623. Ex. 1005, 111, Fig. 1; *see* Ex. 1003 ¶¶ 52–53; Ex. 2001 ¶¶ 76–77. When discussing differences between the ECL-MOS level-conversion circuits in Figures 1, 15, and 17, Tachibana does not identify any difference for bipolar transistor 131. Ex. 1005, 119–20; *see* Ex. 2001 ¶¶ 82, 86. In addition, Dr. Khatri explains that the ECL-MOS

level-conversion circuits in Figures 15 and 17 each include bipolar transistor 131. Ex. 2001 ¶¶ 80, 82, 84, 86.

Next, we consider whether the Figure 15 and 17 embodiments each include “a differential amplifier responsive to the timing circuit” as required by claim 1. For each embodiment, Petitioner asserts that the differential amplifier is “responsive” to the timing circuit in Figures 8 and 9 because “the level of the signal on terminal 19, which is generated by the circuit in Figures 8 and 9, affects the level of” the differential amplifier’s output signals. Pet. 37; *see* Ex. 1003, A13–A14.

For each embodiment, we agree with Petitioner that the differential amplifier is “responsive” to the timing circuit in Figures 8 and 9. For Figure 1, Tachibana explains that the signal at terminal 19 received from the timing circuit affects the differential amplifier’s output signals at output terminals 61 and 62. Ex. 1005, 111–16, Fig. 5; *see* Ex. 1003, A7–A10, A13–A14. For instance, if “terminal 19 is at low-level potential, . . . current does not flow to the differential amplifier comprised of bipolar transistors 126, 127, resistors 208, 209, and PMOS transistor 412,” and “the potential of [output] terminal 61 attains the GND terminal’s potential of 0 V.” Ex. 1005, 111; *see id.* at 116. Depending on the control signals at terminals 21, 26, and 27 during a memory-read operation, when the potential at terminal 19 transitions to a high level, the “potential of [output] terminals 61, 62 is determined by the resistance and current flow of resistors 208, 209 and PMOS transistor 412.” *Id.* at 112–13. For example, if “the potential of [input] terminal 60 is . . . higher than the potential of [input] terminal 59, current flows through bipolar transistor 127, causing the potential of [output] terminal 62 to attain the low level and the potential of [output] terminal 61 to

attain the high level.” *Id.* at 113. Thus, in the Figure 1 embodiment, the differential amplifier is “responsive” to the timing circuit.

As discussed above, Tachibana explains that the Figure 15 and 17 embodiments operate “essentially the same” as the Figure 1 embodiment. Ex. 1005, 119–20; *see* Ex. 2001 ¶¶ 62, 78–79, 83. For example, Figures 15 and 17 each depict terminals 19, 21, and 27 for receiving control signals from the timing circuit. Ex. 1005, 116–17, 119–20, Figs. 15, 17. Further, Figures 15 and 17 each show a single-stage differential amplifier similar to the differential amplifier’s second stage in Figure 1. Ex. 1003 ¶¶ 58–60, A10–A12; Ex. 1005, 111, 119–20, Figs. 1, 15, 17; Ex. 2001 ¶¶ 80–81, 84–85. In addition, the differential amplifiers in Figures 15 and 17 each include resistors 208 and 209, bipolar transistors 126 and 127, and PMOS transistor 412 just like the differential amplifier’s second stage in Figure 1. Ex. 1003 ¶¶ 58–60, A10–A12; Ex. 1005, 111, 119–20, Figs. 1, 15, 17; Ex. 2001 ¶¶ 80, 84.

For the reasons discussed above, the Figure 15 and 17 embodiments each satisfy claim 1’s requirement for “a differential amplifier responsive to the timing circuit.”

(d) Impedance Control Circuit

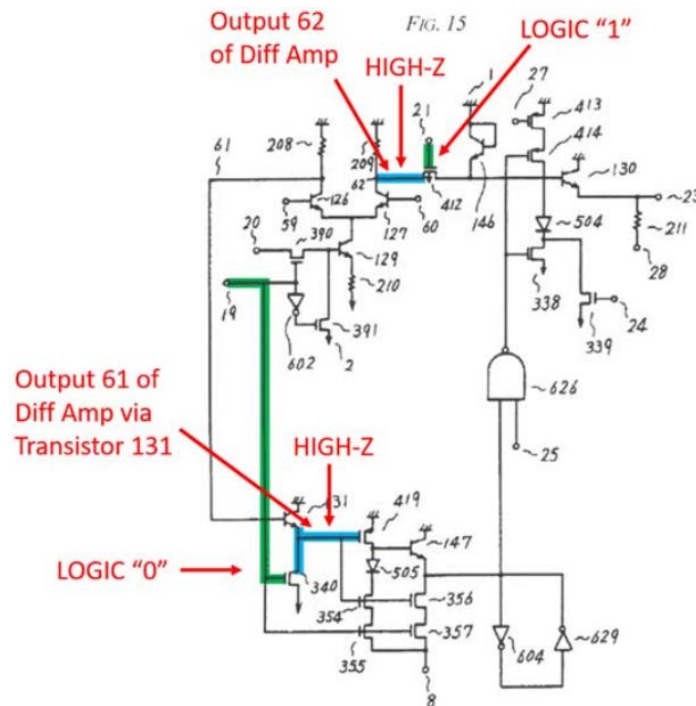
Claim 1 recites “an impedance control circuit.” Ex. 1001, 6:67. For the claimed “impedance control circuit” in Figures 15 and 17, Petitioner identifies the following components in each figure: PMOS transistor 412 and NMOS transistor 340. Pet. 38–40 & n.6; *see* Ex. 1003, A14–A19 & n.1. Specifically, Petitioner asserts that PMOS transistor 412 and NMOS transistor 340 “function to control the impedance of the differential amplifier (at its output) and level converter (at its input) and thus correspond to” the

claimed “impedance control circuit.” Reply 4–5; *see* Ex. 1028 ¶¶ 11–12, 14–15, 17.

Dr. Baker articulates three reasons why PMOS transistor 412 in each embodiment functions to control impedance: First, “Tachibana discloses that PMOS transistor 412 in FIG. 1 is an impedance control circuit to control the output impedance of the differential amplifier 622.” Ex. 1003, A14–A15 (citing Ex. 1005, 110, 112–14); *see* Ex. 1028 ¶¶ 11–12, 17. Second, Figures 15 and 17 “both include the transistor 412.” Ex. 1003, A15. Third, because Tachibana explains that elements in Figures 1, 15, and 17 with the same number correspond to the same element, “the transistor 412 functions as an impedance control circuit for the output buffer circuits” in Figures 15 and 17. *Id.*; *see* Ex. 1028 ¶ 12.

In addition, Dr. Baker explains that NMOS transistor 340 in each embodiment “is also an impedance control circuit, because it directly controls the impedance of” the ECL-MOS level-conversion circuit in each embodiment. Ex. 1003, A15 n.1, A23 n.2, A25 n.3; *see* Ex. 1028 ¶ 11.

To show how PMOS transistor 412 and NMOS transistor 340 function to control impedance, Dr. Baker provides the following annotated version of Tachibana’s Figure 15:



Dr. Baker explains that this version of Figure 15 shows a high level (logic “1”) at terminal 21 and PMOS transistor 412 “turned off,” thus “caus[ing] the transistor’s drain, connected to output [terminal] 62 of the differential amplifier, to be placed in a high impedance state.” Ex. 1028 ¶ 17; see Reply 5–6. He also explains that this version of Figure 15 shows a low level (logic “0”) at terminal 19 and NMOS transistor 340 “turned off,” thus “caus[ing] its drain, connected to the emitter of [bipolar transistor] 131, and the gate/base of [PMOS] transistor 419 to be placed in a high impedance state.” *Id.* In addition, Dr. Baker states that when the signals at terminals 19 and 21 transition to their respective opposite logic levels, “PMOS transistor 412 and NMOS transistor 340 are turned on,” thus “caus[ing] the transistors’ drains to be placed in a low-impedance state, which in turn causes the outputs of [the] differential amplifier” to pass to other circuit elements. *Id.*

Dr. Khatri agrees that (1) with a low level (logic “0”) at terminal 19, the impedance “looking into” NMOS transistor 340 from its drain “would be high” and (2) with a high level (logic “1”) at terminal 19, the impedance looking into NMOS transistor 340 from its drain “would be low.” Ex. 1029, 44:15–45:16.

Patent Owner argues that the Figure 15 and 17 embodiments do not include the claimed “impedance control circuit” for four reasons. *See* Resp. 28–42; Sur-reply 1–10. First, when a patent claim lists elements separately, “‘the clear implication of the claim language’ is that those elements are ‘distinct component[s]’ of the patented invention.” Resp. 29 (alteration in original) (quoting *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010)); Sur-reply 1. Second, claim 1 “separately and distinctly enumerates (i) a timing circuit, (ii) a differential amplifier, (iii) an impedance control circuit, (iv) a level converter, and (v) a clock-free latch.” Resp. 29. Third, claim 1 “require[s] an impedance control circuit that is separate and distinct from the differential amplifier and the level converter.” *Id.* at 32; *see id.* at 41. Fourth, “Tachibana does not disclose an impedance control circuit that is separate and distinct from the differential amplifier and the level converter” because “PMOS transistor 412 is an integral part of” the differential amplifier and “NMOS transistor 340 is an integral part of” the level converter. *Id.* at 32–34, 41–42; Sur-reply 3–4.

In response, Petitioner argues that Patent Owner wrongly asserts that “an apparatus claim that lists a number of elements only covers apparatuses with entirely separate and distinct structures corresponding to each element.”

Reply 3 (emphasis omitted). According to Petitioner, “the structures corresponding to the claim elements” may overlap. *Id.*

Petitioner also argues that PMOS transistor 412 and NMOS transistor 340 in each embodiment constitute “separate and distinct” components that “function to control the impedance of” the differential amplifier and the level converter. Reply 4–5. In particular, Petitioner contends that PMOS transistor 412 “controls the impedance of [the differential amplifier’s] output element 62.” *Id.* at 2–3. Petitioner also contends that NMOS transistor 340 “controls the impedance of [the differential amplifier’s] output element 61” connected to the ECL-MOS level-conversion circuit. *Id.* at 3. Further, Petitioner asserts that PMOS transistor 412 and NMOS transistor 340 “serve a function other than amplification and level conversion,” respectively, and that other circuitry in Figures 15 and 17 “corresponds to the claimed ‘differential amplifier’ and ‘level converter.’” *Id.* at 5.

Under the circumstances here, we agree with Petitioner that overlapping circuitry may satisfy separate claim limitations. In *Linear Technology Corp. v. International Trade Commission*, 566 F.3d 1049 (Fed. Cir. 2009), the Federal Circuit addressed overlapping circuitry. There, certain claims required a “first circuit” for generating a “first feedback signal,” a “second circuit” for generating a “first control signal,” and a “third circuit” for generating a “second control signal.” *Id.* at 1052–53. An Administrative Law Judge construed the “second circuit” and the “third circuit” as “precluding shared use of the same circuitry,” i.e., “that every element in the second circuit [must] be completely distinct from every element in the third circuit.” *Id.* at 1055. The Commission disagreed. *Id.*

The Commission determined that “even a difference such as having an additional [component] can cause the circuits to be different and distinct in their topology and their operation.” *Id.* (alteration in original). The Federal Circuit agreed with the Commission that the “second circuit” and the “third circuit” did not “require entirely separate and distinct circuits.” *Id.*

Here, for the Figure 15 and 17 embodiments, Dr. Baker states that (1) PMOS transistor 412 “controls the output impedance of the differential amplifier” and (2) NMOS transistor 340 “controls the impedance of the ECL-MOS level conversion circuit.” Ex. 1028 ¶ 11. He also states that “PMOS transistor 412 and NMOS transistor 340 are designed only to engage in circuit impedance control.” *Id.* ¶ 12. He adds that neither component “engages in either differential amplification or level conversion.” *Id.* In addition, Dr. Baker explains that “different circuit elements besides PMOS transistor 412 . . . perform differential amplification” and that “different circuit elements besides NMOS transistor 340 . . . perform level conversion.” *Id.* ¶ 14; *see id.* ¶ 15.

Further, using Figure 15 as an example, Dr. Baker identifies the following components that perform differential amplification: bipolar transistors 126, 127, and 129, resistors 208, 209, and 210, NMOS transistors 390 and 391, and inverter 602. Ex. 1028 ¶ 12; *see* Ex. 1003 ¶¶ 36–37. In addition, he identifies the following components that perform level conversion: bipolar transistor 147, NMOS transistors 354, 355, 356, and 357, PMOS transistor 419, and diode 505. Ex. 1028 ¶ 12.

For the Figure 15 and 17 embodiments, Dr. Khatri states that (1) PMOS transistor 412 “is an integral part of” the differential amplifier and (2) NMOS transistor 340 “is an integral part of” the level converter.

Ex. 2001 ¶ 91; *see* Resp. 42 (citing Ex. 2001 ¶ 91). He explains that “integral means it’s a part of the circuit.” Ex. 1029, 41:10–42:12, 43:25–44:4. Dr. Khatri also states that “neither the PMOS transistor 412 nor the [NMOS] transistor 340 are separate and distinct from the differential amplifier and the level converter.” Ex. 2001 ¶ 91.

Dr. Khatri’s statement that PMOS transistor 412 “is an integral part of” the differential amplifier does not contradict Dr. Baker’s statements that PMOS transistor 412 “controls the output impedance of the differential amplifier” and “different circuit elements besides PMOS transistor 412 . . . perform differential amplification.” *See* Ex. 1028 ¶¶ 11, 14. Moreover, Patent Owner admitted that with PMOS transistor 412 removed from the differential amplifier, other components still amplify signals received at the differential amplifier’s input terminals. Tr. 24:15–21. In addition, Dr. Khatri’s statement that NMOS transistor 340 “is an integral part of” the level converter does not contradict Dr. Baker’s statements that NMOS transistor 340 “controls the impedance of the ECL-MOS level conversion circuit” and “different circuit elements besides NMOS transistor 340 . . . perform level conversion.” *See* Ex. 1028 ¶¶ 11, 14.

Tachibana’s description of PMOS transistor 412 as part of the differential amplifier and NMOS transistor 340 as part of the ECL-MOS level-conversion circuit does not override circuit operation. Uncontradicted evidence demonstrates that PMOS transistor 412 “controls the output impedance of the differential amplifier” and that other components perform differential amplification. Ex. 1028 ¶¶ 11–12, 14, 17; *see* Ex. 1003, A14–A19. Uncontradicted evidence demonstrates that NMOS transistor 340 “controls the impedance of the ECL-MOS level conversion circuit” and that

other components perform level conversion. Ex. 1028 ¶¶ 11–12, 14, 17; *see* Ex. 1003, A15 n.1, A23 n.2, A25 n.3; Ex. 1029, 44:15–45:16.

In the Figure 15 and 17 embodiments, separate and distinct components perform differential amplification, separate and distinct components perform level conversion, and separate and distinct components perform impedance control, i.e., PMOS transistor 412 and NMOS transistor 340 for impedance control. Ex. 1028 ¶¶ 11–12, 14–15, 17; *see* Ex. 1003, A14–A19 & n.1, A23 n.2, A25 n.3, A39–A40; Ex. 1005, 110–13, 119–20, Figs. 1, 15, 17; Ex. 1029, 44:15–45:16; Tr. 24:15–21.

For the reasons discussed above, the Figure 15 and 17 embodiments each satisfy claim 1’s requirement for “an impedance control circuit.”

Patent Owner asserts that Petitioner improperly relies on new evidence and arguments in the Reply. Sur-reply 10–11, 15. In particular, Patent Owner objects to Petitioner’s evidence and arguments that Figures 15 and 17 “include separate differential amplification, impedance control, and level converter circuit elements.” *Id.* at 10–11. But Petitioner’s evidence and arguments properly respond to Patent Owner’s evidence and arguments. *See Genzyme Therapeutic Prods. Ltd. P’ship v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1366–69 (Fed. Cir. 2016). Specifically, Petitioner’s evidence and arguments about separate and distinct components performing different functions properly respond to Patent Owner’s evidence and arguments that “Tachibana does not disclose an impedance control circuit that is separate and distinct from the differential amplifier and the level converter” because “PMOS transistor 412 is an integral part of” the differential amplifier and “NMOS transistor 340 is an integral part of” the

level converter. *See* 37 C.F.R. § 42.23(b); Resp. 32–34, 41–42; Ex. 2001 ¶ 91.

(e) Level Converter

Claim 1 recites “a level converter responsive to the differential amplifier and the impedance control circuit.” Ex. 1001, 7:1–2. For the claimed “level converter” in Figures 15 and 17, Petitioner identifies the following components in each figure: “bipolar transistor 147, diode 505, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357.” Pet. 40–44; *see* Ex. 1003, A19–A25.

Patent Owner does not dispute that each embodiment includes a level converter with those components. Resp. 20–22; *see* Ex. 2001 ¶¶ 63–64. Instead, Patent Owner disputes that each level converter includes only those components. Resp. 20–21, 33–42; *see* Ex. 2001 ¶¶ 63–64. Specifically, Patent Owner asserts that each level converter additionally includes bipolar transistor 131 and NMOS transistor 340. Resp. 20–21; Sur-reply 3–4, 16, 23–24; *see* Ex. 2001 ¶¶ 63–64.

We agree with Patent Owner that the level converters in Figures 15 and 17 each include bipolar transistor 131 and NMOS transistor 340. For Figure 1, Tachibana describes bipolar transistor 131 and NMOS transistor 340 as part of ECL-MOS level-conversion circuit 623. Ex. 1005, 111; *see* Ex. 1003 ¶¶ 52–53; Ex. 2001 ¶¶ 76–77. When discussing differences between the ECL-MOS level-conversion circuits in Figures 1, 15, and 17, Tachibana does not identify any difference for bipolar transistor 131 or NMOS transistor 340. Ex. 1005, 119–20; *see* Ex. 2001 ¶¶ 82, 86. In addition, Dr. Khatri explains that the ECL-MOS level-

conversion circuits in Figures 15 and 17 each include bipolar transistor 131 and NMOS transistor 340. Ex. 2001 ¶¶ 80, 82, 84, 86.

Next, we consider whether the Figure 15 and 17 embodiments each include “a level converter responsive to the differential amplifier and the impedance control circuit” as required by claim 1. Petitioner contends that each embodiment does so for two reasons. First, Petitioner asserts that the ECL-MOS level-conversion circuit is “responsive” to the differential amplifier and PMOS transistor 412 because “one of the outputs of the differential amplifier (reference numeral 61 in Figure 15; unnumbered output of bipolar transistor 126 in Figure 17) is an input to” the ECL-MOS level-conversion circuit. Pet. 45; Ex. 1003, A22–A23, A25. According to Petitioner, changing the state of PMOS transistor 412 changes current flow through the differential amplifier and that in turn changes the differential amplifier’s output that “is an input to the ECL-MOS level conversion circuit.” Pet. 47–48; Ex. 1003, A22–A23, A25. Second, Petitioner asserts that the ECL-MOS level-conversion circuit is “responsive” to NMOS transistor 340 “because it controls the impedance of” the level-conversion circuit. Pet. 48 n.7; see Ex. 1003, A15 n.1, A23 n.2, A25 n.3; Ex. 1028 ¶¶ 11, 17.

For each embodiment, we agree with Petitioner that the ECL-MOS level-conversion circuit is “responsive” to the differential amplifier and PMOS transistor 412. With a high level (logic “1”) at terminal 21, PMOS transistor 412 does not conduct, thus setting the differential amplifier’s output impedance “to high impedance.” Ex. 1003, A14–A17; Ex. 1005, 110–12, 119–20, Figs. 15, 17; Ex. 1028 ¶ 17. Changing to a low level (logic “0”) at terminal 21 causes PMOS transistor 412 to conduct, and the

differential amplifier's output impedance then changes "from the high impedance state to the low impedance state." Ex. 1003, A14–A15; Ex. 1005, 113–14, 119–20, Figs. 15, 17; Ex. 1028 ¶ 17. In "the low impedance state," the differential amplifier's two output signals pass to other circuit elements, e.g., the ECL-MOS level-conversion circuit. Ex. 1003, A14–A15; Ex. 1005, 113–14, 119–20, Figs. 15, 17; Ex. 1028 ¶ 17.

In particular, the ECL-MOS level-conversion circuit receives as an input signal one of the differential amplifier's two output signals. Ex. 1003, A19–A25; Ex. 1005, 119–20, Figs. 15, 17; Ex. 2001 ¶¶ 80–81, 84–85, 103–104. Changing the state of PMOS transistor 412 changes the differential amplifier's output impedance, and that changes the differential amplifier's two output signals, thus changing the input signal to the ECL-MOS level-conversion circuit. Ex. 1003, A19–A25; Ex. 1005, 119–20, Figs. 15, 17; Ex. 1028 ¶¶ 11, 17. Hence, the ECL-MOS level-conversion circuit is "responsive" to the differential amplifier and PMOS transistor 412.

For each embodiment, we also agree with Petitioner that the ECL-MOS level-conversion circuit is "responsive" to NMOS transistor 340. Dr. Baker describes NMOS transistor 340 as "directly" controlling the impedance of the ECL-MOS level-conversion circuit. Ex. 1003, A15 n.1, A23 n.2, A25 n.3; Ex. 1028 ¶ 11. He explains that with a low level (logic "0") at terminal 19, "NMOS transistor 340 is turned off," thus presenting "a high impedance state" to other components in the ECL-MOS level-conversion circuit. Ex. 1028 ¶ 17.

Dr. Baker's explanation comports with Tachibana's disclosure. For Figure 1, Tachibana explains that if "the potential of terminal 19 is at low-level potential, NMOS transistors 340, 341 are in the non-conducting state

and current does not flow” to other components in the ECL-MOS level-conversion circuit, thus deactivating it. Ex. 1005, 111–12; *see* Ex. 1003 ¶ 54, A39–A40. But if “the potential of terminal 19 is at the high level, NMOS transistors 340, 341 attain the conducting state, causing current to flow” to other components in the ECL-MOS level-conversion circuit, and it “attain[s] the active state.” Ex. 1005, 113; *see* Ex. 1003, A40. As discussed above, Tachibana explains that the Figure 15 and 17 embodiments operate “essentially the same” as the Figure 1 embodiment. Ex. 1005, 119–20; *see* Ex. 2001 ¶¶ 62, 78–79, 83.

For the reasons discussed above, the Figure 15 and 17 embodiments each satisfy claim 1’s requirement for “a level converter responsive to the differential amplifier and the impedance control circuit.”

(f) Clock-Free Latch

Claim 1 recites “a clock-free latch responsive to the level converter.” Ex. 1001, 7:3. For the claimed “clock-free latch” in Figures 15 and 17, Petitioner identifies the following components in each figure: inverters 604 and 629. Pet. 48–50; *see* Ex. 1003 ¶¶ 58–61, A25–A29. Patent Owner does not dispute that each embodiment includes a clock-free latch formed by inverters 604 and 629. Resp. 17–18, 20–22, 34; *see* Ex. 2001 ¶¶ 60, 63–64, 78.

For each embodiment, Petitioner asserts that the clock-free latch is “responsive” to the level converter because the clock-free latch receives as an input the output of the ECL-MOS level-conversion circuit. Pet. 53; *see* Ex. 1003 ¶¶ 59, 61, A25, A27.

For each embodiment, we agree with Petitioner that the clock-free latch is “responsive” to the level converter. For Figure 15, Tachibana states

that “inverter circuits 604, 629 were used” instead of latch circuit 650 in Figure 1. Ex. 1005, 119; *see* Ex. 1003, A26–A27. For Figure 17, Tachibana states that “[i]nverter circuits 604, 629 are latch circuits that serve the same purpose as inverter circuits 604, 629” in Figure 15. Ex. 1005, 120; *see* Ex. 1003, A28–A29. Further, the clock-free latch in each embodiment receives as an input the output of the ECL-MOS level-conversion circuit, i.e., where the emitter of bipolar transistor 147 and the drain of NMOS transistor 356 connect to the input of inverter 604. Ex. 1005, Figs. 15, 17. Because the clock-free latch receives as an input the output of the ECL-MOS level-conversion circuit, the clock-free latch is “responsive” to the level converter.

For the reasons discussed above, the Figure 15 and 17 embodiments each satisfy claim 1’s requirement for “a clock-free latch responsive to the level converter.”

(g) Whether Tachibana Anticipates Claim 1

As explained above, Petitioner has shown by a preponderance of the evidence that the Figure 15 and 17 embodiments each include every element of claim 1 arranged as required by the claim. Hence, Petitioner has shown by a preponderance of the evidence that claim 1 is unpatentable under § 102(b) as anticipated by Tachibana.

4. DEPENDENT CLAIM 2

Claim 2 depends from claim 1 and specifies that “the timing circuit is a clock delay circuit.” Ex. 1001, 7:4–5. The parties dispute the meaning of “clock delay circuit.” *See* Resp. 42–45; Reply 10–12; Sur-reply 16–20.

For the reasons explained below, we construe “clock delay circuit” to mean “a circuit that receives a clock signal as an input and provides different

versions of the input clock signal, with one version delayed compared to the other version.” Because our construction of “clock delay circuit” references a “clock signal,” we initially address the construction of “clock signal” and then address the construction of “clock delay circuit.” After addressing claim construction, we consider whether Tachibana anticipates claim 2.

(a) Construction of “Clock Signal”

Petitioner contends that in the context of the ’274 patent “clock signal” means “a signal that enables or disables a differential amplifier.” Paper 32, 9, 14. Petitioner also contends that in the context of the ’274 patent “clock signals” and “clocks” are “merely timing signals,” including “aperiodic timing signals” that “control circuitry in the memory.” Paper 34, 4–5. To support its proposed construction, Petitioner cites various parts of the ’274 patent, i.e., certain language in claims 14, 20, and 21 and certain statements in the written description. See Paper 32, 2–9 & n.1.

Patent Owner criticizes Petitioner’s proposed construction for ignoring the language in claim 20 that requires “amplifying and level converting a differential input to produce a level converted signal in response to a clock signal.” See Paper 33, 1. According to Patent Owner, claim 20 “makes clear that the clock signal synchronizes the operations of the differential amplifier and level converter.” *Id.* at 3. Patent Owner contends that Petitioner’s proposed construction “would read out an express limitation of the claim language.” *Id.* at 2. Patent Owner also contends that “many different kinds of signals” may “enable and disable circuit elements” and that “a clock signal is a type of control signal.” *Id.* at 1–2.

Further, Patent Owner asserts that an ordinarily skilled artisan “would have construed ‘clock signal’ in accordance with its plain and ordinary

meaning: ‘a periodic digital signal that synchronizes circuit operations in a digital computer system.’” Paper 31, 2 (emphasis omitted); see Paper 33, 6. To support its proposed construction, Patent Owner cites “various prior art references submitted by Petitioner and its expert.” Paper 31, 1–2 (citing Exs. 1015–1018).

Petitioner criticizes Patent Owner’s proposed construction for ignoring the intrinsic evidence and “**only** citing extrinsic evidence as support.” Paper 34, 1–2. Petitioner asserts that Patent Owner fails to cite “anything showing how its proposed construction” comports with the ’274 patent’s usage of “clock signal.” *Id.* at 2. Petitioner contends that “nothing in the intrinsic record suggests that the claimed ‘clock signal’ is (or must be) periodic.” *Id.*

In light of the intrinsic evidence and the parties’ respective arguments, and for the reasons explained below, we construe “clock signal” to mean “a control signal that enables or disables a circuit element in an output stage, such as a differential amplifier or a level converter.”

Claim construction “begins with the claim language itself.” *Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 955 (Fed. Cir. 2000). Here, the claim language requires a “response” to a “clock signal” by a circuit element in an output stage, such as a differential amplifier or a level converter.

In particular, claim 1 recites “an output stage of a memory device.” Ex. 1001, 6:62–63. Claim 6 depends indirectly from claim 1 and specifies that a “level converter produces [a] modified impedance output in response to the clock signal.” *Id.* at 7:13–15. Further, claim 14 recites “amplifying a differential input to produce a differential output in response to a clock

signal.” *Id.* at 8:1–2. Similarly, claim 20 recites “amplifying and level converting a differential input to produce a level converted signal in response to a clock signal.” *Id.* at 8:29–31. The phrase “in response to” connotes a cause-and-effect relationship. *Am. Calcar, Inc. v. Am. Honda Motor Co.*, 651 F.3d 1318, 1340 (Fed. Cir. 2011). Thus, the claim language indicates that a “clock signal” causes a “response” by a circuit element in an output stage, such as a differential amplifier or a level converter.

The ’274 patent’s written description demonstrates that the “response” to the “clock signal” involves enabling or disabling a circuit element. Figure 2 illustrates an output stage including, among other things, differential amplifier 100, level converter 102, timing circuit 104, and impedance-control circuits 108 and 110. *Id.* at 2:50–57, Fig. 2. Timing circuit 104 receives clock signal 78 as an input. *Id.* at 3:63–4:1, Fig. 2. The patent instructs that “clock 78 and timing circuit 104” may in “one embodiment” provide “two versions of clock signal 78,” i.e., a delayed disablement clock and a non-delayed disablement clock, for “selective enablement and disablement” of circuit elements. *Id.* at 5:18–29, 5:45–53.

As Dr. Khatri explains, the delayed disablement clock and the non-delayed disablement clock selectively enable and disable differential amplifier 100, level converter 102, and impedance-control circuits 110 and 108 when the clocks transition between logic levels. Ex. 2001 ¶¶ 51–59; see Ex. 1001, 5:18–29, 5:45–53, 5:67–6:42. For example, level converter 102 “is re-enabled” when the non-delayed disablement clock transitions to “a logic level high.” Ex. 1001, 6:15–19, 6:38–40.

For the reasons explained above, the evidence establishes that a “clock signal” enables or disables a circuit element in an output stage, such

as a differential amplifier or a level converter. Thus, we decline to adopt Petitioner’s proposed construction because, as Patent Owner points out, that construction does not encompass enabling or disabling a circuit element other than a differential amplifier, e.g., a level converter. *See* Paper 32, 2–9; Paper 33, 1–3.

We decline to adopt Patent Owner’s proposed construction because, as Petitioner points out, that construction does not comport with the ’274 patent’s usage of “clock signal.” *See* Paper 31, 1–3; Paper 34, 1–2. The Federal Circuit has described a patent’s specification as “highly relevant” to claim construction and “the single best guide to the meaning of a disputed term.” *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

Here, the ’274 patent’s written description shows that “clock signal” encompasses not only “periodic digital signals,” as Patent Owner contends, but also “aperiodic timing signals,” as Petitioner contends. For example, when discussing the prior art in the Background of the Invention, the patent uses “clock” as a verb meaning “trigger” or “enable” and uses “clock signal” generically to encompass periodic and aperiodic signals. *See* Ex. 1001, 1:33–44.

In particular, the ’274 patent explains that prior-art circuits “use[d] two clock signals,” i.e., “one clock signal to clock the differential amplifier portion, and one clock signal to clock the latch portion of the memory output stage.” *Id.* at 1:33–37. The patent also explains that using “two clock signals” caused problems because “the timing relationship between the two clocks cannot be consistently controlled due to manufacturing process variations, temperature variations, power supply voltage variations, etc.” *Id.*

at 1:37–40. The patent purports to solve those problems by providing an output stage “that does not require two or more clocks, and thus does not require that a precise timing relationship between two or more clocks be maintained.” *Id.* at 1:40–44.

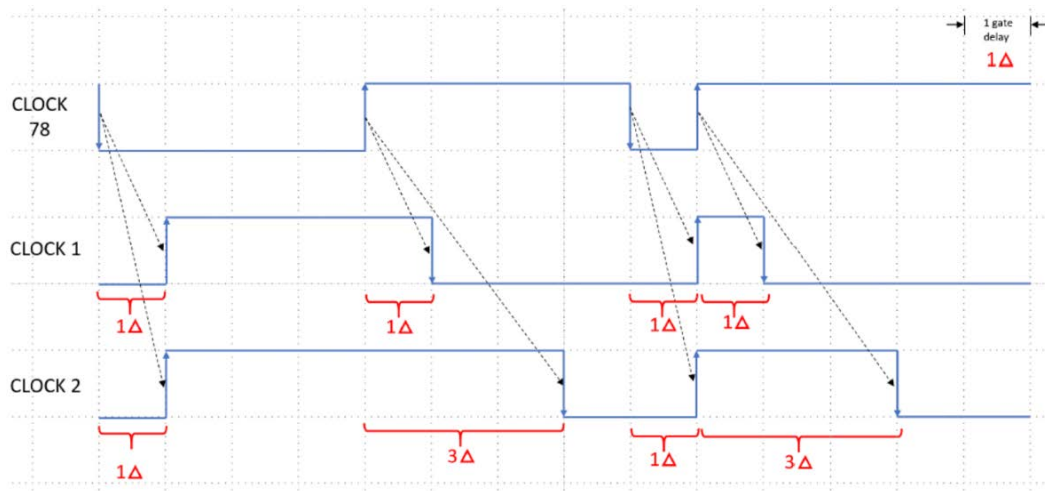
In the Detailed Description, the ’274 patent uses “clock signal” generically to encompass periodic and aperiodic signals. For example, the patent explains that “[t]he present invention merely requires a single clock signal” and that “two clock signals are not required . . . but are merely used to reduce power [consumption] and to increase speed.” *Id.* at 5:23–25; see *id.* at code (57), 5:18–20. The patent also explains that “some embodiments of the present invention may use clock 78 directly as the only clock, without using timing circuit 104 to create two slightly different versions.” *Id.* at 5:41–44. Nothing in that explanation limits “clock” or “clock signal” to periodic signals.

Further, Figure 1 illustrates memory 10 and its various components, including output stages 24 and 28. Ex. 1001, code (57), 1:48–49, 2:20–25, Fig. 1. Figure 1 does not depict a “clock” producing “periodic digital signals” for output stages 24 and 28. Instead, Figure 1 shows output stages 24 and 28 receiving clock signal 78 from control logic 32. *Id.* at 2:44–46, Fig. 1. The patent explains that “[c]ontrol logic 32 provides the control signals necessary to operate memory 10.” *Id.* at 4:33–34. More specifically, the patent states that “[c]ontrol logic 32 provides” the following signals: “a read/write (R/W) signal 74,” “an enable signal 76,” “a clock signal 78,” and “an output enable signal 80.” *Id.* at 2:42–47. Thus, the patent identifies clock signal 78 as one of “the control signals necessary to operate memory 10.” *Id.* at 2:42–47, 4:33–34.

In addition, claim 13 depends from claim 1 and specifies that “the timing circuit includes a first inverter to produce a first clock signal . . . and a NAND gate to produce a second clock signal.” *Id.* at 7:35–38. The “first clock signal” corresponds to the non-delayed disablement clock. *See id.* at 3:4–5, 5:48–53, 5:67–6:3, Fig. 2 (output of inverter 146). The “second clock signal” corresponds to the delayed disablement clock. *See id.* at 3:4–5, 5:45–48, Fig. 2 (output of NAND gate 149). Those clocks are not periodic signals. Limiting “clock signal” to periodic signals would prevent (1) the “first clock signal” from covering the non-delayed disablement clock and (2) the “second clock signal” from covering the delayed disablement clock. A construction excluding a preferred embodiment is “rarely, if ever correct.” *PPC Broadband, Inc. v. Corning Optical Commc’ns RF, LLC*, 815 F.3d 747, 755 (Fed. Cir. 2016).

For the reasons explained above, the ’274 patent lacks support for Patent Owner’s contention that “clock signal” encompasses only “periodic digital signals.”

Moreover, Dr. Khatri admits that “clock signal” encompasses “aperiodic timing signals,” as Petitioner contends. In particular, Dr. Khatri provides the following “timing diagram generated based on the disclosure of the ’274 patent” to show the relationship between clock signal 78 received by timing circuit 104 and the non-delayed disablement clock and the delayed disablement clock produced by timing circuit 104.



This timing diagram depicts three signals: clock signal 78, the non-delayed disablement clock identified as “clock 1,” and the delayed disablement clock identified as “clock 2.” Ex. 2001 ¶¶ 53, 58, 95; see Resp. 11–12, 15–16, 43–44. This timing diagram shows clock signal 78 as an aperiodic signal. See Paper 32, 9; Paper 34, 3.

Patent Owner asserts that this timing diagram “was not intended to show a continuous clock signal 78 that is aperiodic” but instead intended “to show two different examples of how the falling edge of one version of clock 78 provided by timing circuit 104 is delayed compared to the falling edge of the other version.” Paper 33, 4–5 n.1. But Dr. Khatri could have illustrated a delay between the falling edges of clock 1 and clock 2 just as easily by showing clock signal 78 as a periodic signal rather than an aperiodic signal.

In addition, the prior art indicates that “clock signal” encompasses “aperiodic timing signals,” as Petitioner contends. See Paper 34, 4–5 (citing Ex. 1019, 213, 218, 394, 401). For instance, a 1997 handbook about semiconductor memories describes an address-transition-detection circuit that provides “activation pulses.” Ex. 1019, 394. That handbook explains

that an activation pulse “acts as an original clock for subsequent internal clocks which control the timing for various internal operations,” e.g., to “selectively turn on particular” circuit elements. *Id.*; *see id.* at 401.

For the reasons explained above, we decline to impose a periodicity requirement on “clock signal,” and we construe that term to mean “a control signal that enables or disables a circuit element in an output stage, such as a differential amplifier or a level converter.”

(b) Construction of “Clock Delay Circuit”

Petitioner contends that “‘clock delay circuit’ simply refers to circuitry that generates a delayed clock signal.” Reply 11 (citing Ex. 1003, A30–A31). Dr. Baker states that “clock delay circuit” means “a circuit that is designed to delay a clock signal in some manner.” Ex. 1028 ¶ 22.

Patent Owner contends that “clock delay circuit” means “a circuit that receives a clock signal as an input and creates an output with a particular type of delay.” Resp. 44. Patent Owner asserts that the circuit would create that particular type of delay as follows:

by outputting at least two versions of the clock signal, wherein the two versions of the clock signal have rising or enabling edges that are approximately simultaneous, and wherein one version of the clock signal being output has a disabling or falling edge that is purposely delayed or skewed as compared [to] the other version of the clock signal being output.

*Id.* at 44–45 (citing Ex. 2001 ¶¶ 96–97); *see id.* at 43. Dr. Khatri offers the same definition as Patent Owner. Ex. 2001 ¶¶ 95–97.

Petitioner criticizes Patent Owner’s proposed construction as too narrow. *See* Reply 11–12. Patent Owner criticizes Petitioner’s proposed construction as too broad. *See* Sur-reply 16–19.

We agree with each criticism. We decline to adopt Petitioner’s proposed construction as too broad. We decline to adopt Patent Owner’s proposed construction as too narrow. For the reasons explained below, we construe “clock delay circuit” to mean “a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version.”

First, the parties and their respective experts agree that a “clock delay circuit” receives a clock signal as an input. Resp. 43–44; Reply 11; Paper 31, 2; Ex. 1003, A30–A31; Ex. 1028 ¶ 22; Ex. 2001 ¶ 96; Tr. 7:17–8:15.

Second, the parties and their respective experts agree that a “clock delay circuit” produces a delayed signal. Resp. 43–45; Reply 11; Ex. 1003, A30–A31; Ex. 1028 ¶ 22; Ex. 2001 ¶¶ 95–96.

Third, patent applicants typically present “a set of claims, each differing in scope, one from the other, and usually running from the broadest permissible definition of the invention to a very specific definition of the invention.” *Westwood Chem., Inc. v. United States*, 525 F.2d 1367, 1371–72 (Ct. Cl. 1975). Hence, “[d]ifferences among claims can also be a useful guide in understanding the meaning of particular claim terms.” *Phillips*, 415 F.3d at 1314.

Here, claim 1 recites “a timing circuit.” Ex. 1001, 6:65. Claims 2 and 13 each depend from claim 1, and they each further define claim 1’s “timing circuit.” But they do so in different ways using different language. Claim 2 recites a circuit and specifies that “the timing circuit is a clock delay circuit.” *Id.* at 7:4–5. Claim 13 recites circuit components and specifies that “the timing circuit includes a first inverter to produce a first clock signal, a

second inverter, a third inverter, and a NAND gate to produce a second clock signal.” *Id.* at 7:36–38.

The circuit components in claim 13’s “timing circuit” correspond to the circuit components in Figure 2’s timing circuit 104, i.e., “a first inverter [146] to produce a first clock signal, a second inverter [147], a third inverter [148], and a NAND gate [149] to produce a second clock signal.” *Id.* at 3:4–5, 3:63–4:1, 5:18–23, 5:26–37, 7:36–38, Fig. 2; *see* Ex. 2001 ¶¶ 51–59. Consistent with claim 13, the ’274 patent states, “In one embodiment, timing circuit 104 includes inverters 146, 147, and 148 as well as NAND gate 149.” Ex. 1001, 3:4–5.

The circuit components in claim 13’s “timing circuit” and Figure 2’s timing circuit 104 provide different versions of the input clock signal that “have approximately simultaneous rising [or enabling] edges” and “a delay between their [falling or] disabling edges,” i.e., “purposely skewed” disabling edges. *Id.* at code (57), 5:26–37; Ex. 2001 ¶¶ 51–59, 94–95. Thus, claim 13’s “timing circuit” produces the particular relationship between the rising and falling edges of the different versions that Patent Owner attributes to claim 2’s “clock delay circuit.” *See* Resp. 43–45; Ex. 2001 ¶¶ 93–97.

As noted above, claims 2 and 13 further define claim 1’s “timing circuit” in different ways using different language. That different claims use different language in parallel settings supports the conclusion that the different language differs in scope. *See Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1349 (Fed. Cir. 2012). Because claims 2 and 13 further define claim 1’s “timing circuit” in different ways using

different language, claim 2's "clock delay circuit" should differ in scope from claim 13's "timing circuit."

The '274 patent's written description supports this conclusion by describing different embodiments of a "timing circuit." Ex. 1001, code (57), 3:4–5, 5:18–44; *see id.* at 4:48–51. For instance, it states that "some embodiments . . . may use clock 78 directly as the only clock, without using timing circuit 104 to create two slightly different versions," and that "[a]lternate embodiments may skew the disabling edge of the clock to improve the speed characteristics of [the] output stage." *Id.* at code (57), 5:41–44. By describing different embodiments, the '274 patent indicates that some claims have a scope not "strictly coextensive" with Figure 2's illustrative embodiment. *See id.* at 1:51–53, 2:50–52, 4:48–51; *see also Phillips*, 415 F.3d at 1323.

The '274 patent's prosecution history sheds no light on the meaning of claim 2's "clock delay circuit." In the first Office action, the Examiner issued a Notice of Allowability and made minor amendments to application claims 7, 10, and 19 that have no bearing on the patentability issues here. Ex. 1002, 30–34; *see Pet.* 19; Ex. 1002, 17–20. In the Notice of Allowability, the Examiner included the following statement of reasons for allowance:

The prior art of record fails to show an apparatus and a method for use as an output stage of a memory device, utilizing a timing circuit, a differential amplifier responsive to the timing circuit, an impedance control circuit, a level converter responsive to the differential amplifier and the impedance control circuit, and a clock-free latch responsive to a level converter, as represented in claims 1, 14, 20, and 21.

Ex. 1002, 31. Application claims 1–24 then issued as patent claims 1–24 without further commentary from the Examiner or the Applicants. *See, e.g., id.* at 135.

Nevertheless, claim 13 shows that the Applicants knew how to claim a “timing circuit” that produces the particular relationship between the rising and falling edges of the different versions that Patent Owner attributes to claim 2’s “clock delay circuit.”

The Federal Circuit “has often acknowledged the fine line between reading a claim in light of the specification and importing a limitation from the specification into the claim.” *Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 632 F.3d 1246, 1255 (Fed. Cir. 2011). Here, we believe that Patent Owner’s proposed construction of “clock delay circuit” crosses the line and improperly imports a limitation into the claim. *See* Resp. 43–45; Ex. 2001 ¶¶ 93–97. Hence, we decline to adopt Patent Owner’s proposed construction.

We also decline to adopt Petitioner’s proposed construction. That construction of “clock delay circuit” permits the circuit to just “generate[] a delayed clock signal” without providing different versions of the input clock signal. *See* Reply 11 (citing Ex. 1003, A30–A31); Ex. 1028 ¶ 22. Petitioner does not explain why “generat[ing] a delayed clock signal” provides any advantage or avoids the timing-relationship problem with “separate clock signal[s] as used by the prior art.” *See* Reply 11–12; Ex. 1028 ¶¶ 22–24; Tr. 7:17–8:15, 41:16–42:15; *see also* Ex. 1001, 1:33–44, 5:34–35 (discussing the timing-relationship problem).

Further, the ’274 patent instructs that “it is advantageous for the memory output stage to be as fast as possible.” Ex. 1001, 1:44–45. “Faster

memories decrease the system access time” and “improve[] bandwidth.” Ex. 1019, 84. Consistent with this, Dr. Baker describes “[f]aster access times” as “a benefit for memory systems.” Ex. 1003 ¶ 77. Just “generat[ing] a delayed clock signal” introduces a delay for no apparent reason, and thus appears to conflict with the objective that an output stage “be as fast as possible.” See Ex. 1001, 1:44–45.

In addition, Petitioner’s proposed construction of “clock delay circuit” disregards the ’274 patent’s stated reason for providing different versions of the input clock signal. In particular, with one version delayed compared to the other version, the different versions selectively enable and disable the differential amplifier because doing so “reduce[s] power consumption” and “increase[s] speed.” Ex. 1001, code (57), 5:18–25. A claim construction should comport “with the purposes of the invention.” See *OSRAM GmbH v. Int’l Trade Comm’n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007). Construing “clock delay circuit” to provide different versions of the input clock signal, with one version delayed compared to the other version, comports with the purposes of the invention.

We note that claim 4 depends from claim 1 and specifies that claim 1’s “timing circuit” receives a “clock signal.” Ex. 1001, 7:8–9. Under our construction, claim 2’s “clock delay circuit” also receives a “clock signal.” Our construction does not render claim 4 superfluous, however, because claim 4 does not require different versions of the input clock signal, with one version delayed compared to the other version.

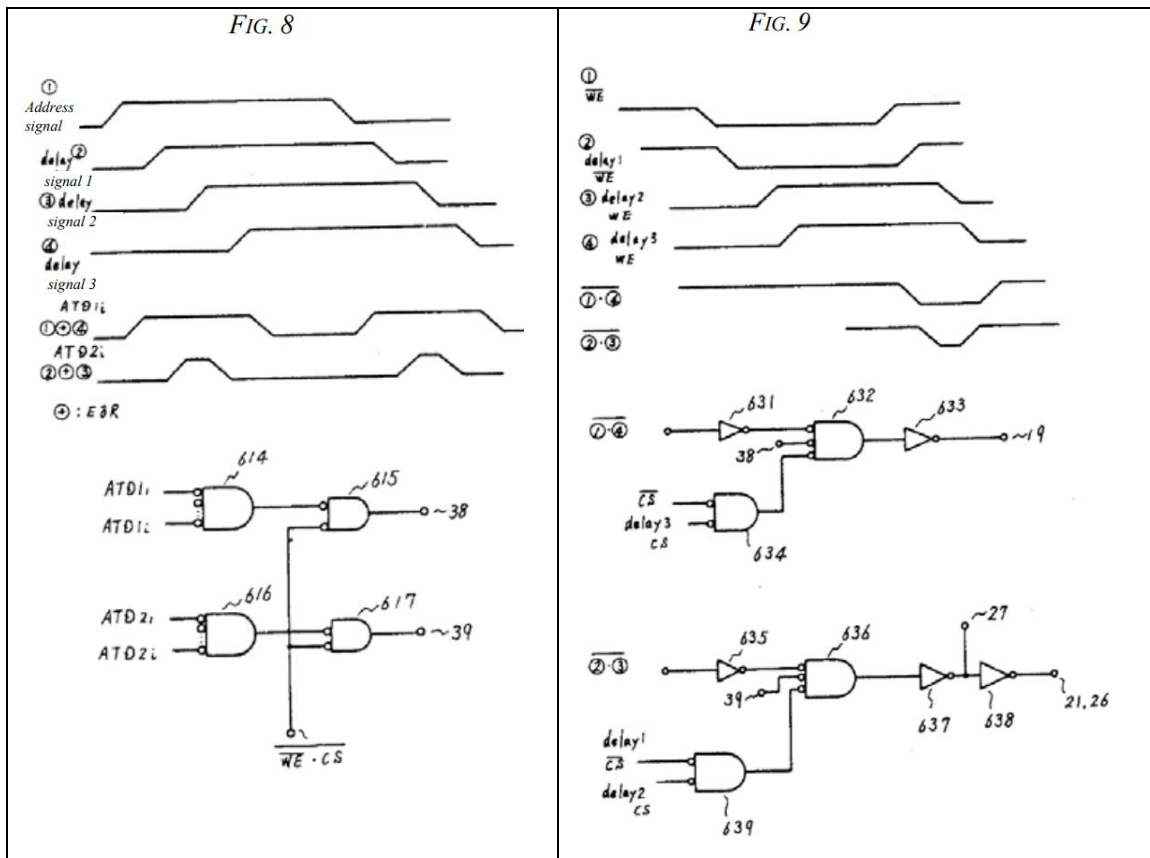
(c) Whether Tachibana Anticipates Claim 2

Petitioner contends that Tachibana anticipates claim 2 because Tachibana’s timing circuit, i.e., the circuit in Figures 8 and 9, is a “clock

delay circuit,” i.e., “a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version.” See Paper 32, 12–15; Paper 34, 7–8. Specifically, Petitioner asserts that Tachibana’s timing circuit “applies delays to differential amplifier enabling/disabling signals” supplied as inputs and generates as outputs “signals 19 and 21 . . . with [signal] 19 delayed relative to [signal] 21 for its disabling transition from high to low.” Paper 32, 13–14 (citing Ex. 1005, 111–13, 116–17, 119, Figs. 2, 5).

Patent Owner contends that Tachibana does not anticipate claim 2 for two reasons. First, Patent Owner asserts that the input signals to Tachibana’s timing circuit “are not signals that enable and disable the differential amplifier.” Paper 33, 6; see Paper 31, 3–10, 12–13. Patent Owner argues that these input signals “‘*start the process of signal generation that will eventually enable/disable Tachibana’s differential amplifier,*’ and these input signals ‘*are used*’ to generate the signals provided to terminals 19 and 21.” Paper 33, 6 (quoting Paper 32, 14) (emphasis added by Patent Owner). Second, Patent Owner asserts that the signals at terminals 19 and 21 are each “a *new logic signal* generated from” the timing circuit’s logic circuitry “based on several input logic signals.” Paper 31, 13–14; see Paper 33, 7–8. Patent Owner also asserts that the signals at terminals 19 and 21 are not different versions of any input signal. Paper 31, 13–14; see Paper 33, 7–8.

We agree with Patent Owner that Tachibana does not anticipate claim 2 for the reasons Patent Owner articulates. Tachibana’s Figures 8 and 9 are reproduced below.



Ex. 1005, Figs. 8–9. Figures 8 and 9 depict the NAND gates, NOR gates, and inverters comprising a timing circuit that generates control signals at terminals 19, 21, 26, and 27. Ex. 1005, 116–17, Figs. 8–9; see Ex. 1003, A3–A7. Figures 8 and 9 also depict the waveforms for certain signals used to create the input signals to that timing circuit and the waveforms for certain input signals to that timing circuit. Ex. 1005, 116–17, Figs. 8–9.

As Figures 8 and 9 show, the input signals to Tachibana’s timing circuit result from various combinations of the following signals: an address signal, three delayed versions of the address signal with three different delays, a write-enable signal (“WE”), an inverted version of the write-enable signal (“ $\overline{WE}$ ”), a chip-select signal (“CS”), an inverted version of the chip-select signal (“ $\overline{CS}$ ”), and delayed versions of the write-enable, inverted-

write-enable, chip-select, and inverted-chip-select signals.<sup>3</sup> Ex. 1005, 116–17, Figs. 8–9; *see* Ex. 1003, A29–A30 & n.4; Paper 31, 3–10; Paper 32, 13.

No input signal to Tachibana’s timing circuit corresponds to a “clock signal,” i.e., “a control signal that enables or disables a circuit element in an output stage, such as a differential amplifier or a level converter.” Although Tachibana’s timing circuit receives some input signals derived from the write-enable signal and the chip-select signal, Petitioner makes no attempt to show that the write-enable signal or the chip-select signal (or a delayed or inverted version of either signal) enables or disables a differential amplifier or any other circuit element in an output stage. *See* Paper 32, 12–15; Paper 34, 7–8.

As the parties state, the input signals to Tachibana’s timing circuit “start the process of signal generation that will eventually enable/disable Tachibana’s differential amplifier.” Paper 32, 14; Paper 33, 6 (emphasis omitted). Specifically, Figure 8’s logic circuitry receives logic signals ATD1<sub>1</sub> to ATD1<sub>i</sub> and ATD2<sub>1</sub> to ATD2<sub>i</sub> (derived from an address signal) as logic input signals, combines those logic input signals with another logic input signal (derived from  $\overline{WE}$  and CS), and then provides logic signals at terminals 38 and 39 for Figure 9’s logic circuitry. Ex. 1005, 116–17, Figs. 8–9; *see* Ex. 1003, A29–A30 & n.4; Paper 31, 4–6, 13–14; Paper 32, 13. Further, Figure 9’s logic circuitry receives logic signals at terminals 38

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<sup>3</sup> In its figures, Tachibana uses a bar over a signal identifier to denote an inverted version of the signal. In its text, Tachibana adds a “B” to the signal identifier to denote an inverted version of the signal, e.g., “WEB” for an inverted version of the write-enable signal and “CSB” for an inverted version of the chip-select signal. *See* Ex. 1005, 116.

and 39, combines those logic input signals with other logic input signals (derived from WE,  $\overline{\text{WE}}$ , CS, and  $\overline{\text{CS}}$ ), and then provides control signals at terminals 19 and 21, e.g., for enabling or disabling a differential amplifier. Ex. 1005, 116–17, 119–20, Figs. 8–9, 15, 17; *see* Ex. 1003, A29–A30; Paper 31, 4–7, 13–14; Paper 32, 13–14; Paper 34, 7–8.

While Tachibana’s timing circuit produces a “clock signal” as an output, it does not receive a “clock signal” as an input. Because that timing circuit does not receive a “clock signal” as an input, it does not correspond to claim 2’s “clock delay circuit,” i.e., “a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version.”

In addition, Tachibana’s timing circuit does not correspond to claim 2’s “clock delay circuit” because it does not provide different versions of an input signal, with one version delayed compared to the other version. The signals at terminals 19 and 21 are not different versions of any input signal. *See* Ex. 1005, 111–17, Figs. 2, 5, 8–9. Instead, the logic circuitry in Figures 8 and 9 manipulates the input signals in various ways to create new output signals, e.g., the signals at terminals 19 and 21. *See id.* at 116–17, Figs. 8–9.

As Petitioner notes, the signals at terminals 19 and 21 transition between logic levels at different times, with one signal delayed relative to the other signal. *See id.* at 111–15, Figs. 2, 5; Paper 32, 13–14. But different transition timing does not mean that those signals are different versions of each other. Rather, the signals at terminals 19 and 21 result from different logic circuitry operating on different logic input signals. Ex. 1005, 116–17, Figs. 8–9; *see* Paper 31, 3–7. Specifically, the signal at terminal 19

results from logic operations performed by NOR gate 614 and NAND gate 615 in Figure 8 and by inverter 631, NOR gate 632, inverter 633, and NOR gate 634 in Figure 9. Ex. 1005, 116–17, Figs. 8–9. The signal at terminal 21 results from logic operations performed by NOR gate 616 and NAND gate 617 in Figure 8 and by inverter 635, NOR gate 636, inverter 637, inverter 638, and NOR gate 639 in Figure 9. *Id.* at 116–17, Figs. 8–9. Additionally, the logic input signals to Figure 8’s logic circuitry differ from the logic input signals to Figure 9’s logic circuitry. Ex. 1005, 116–17, Figs. 8–9; see Ex. 1003, A29–A30 & n.4; Paper 31, 4–6, 13–14; Paper 32, 13. Due to different logic circuitry operating on different logic input signals, the signals at terminals 19 and 21 are not different versions of each other or different versions of any input signal.

For the reasons discussed above, Tachibana’s timing circuit does not correspond to claim 2’s “clock delay circuit.” Hence, Petitioner has not shown by a preponderance of the evidence that claim 2 is unpatentable under § 102(b) as anticipated by Tachibana.

#### 5. DEPENDENT CLAIM 3

Claim 3 depends from claim 1 and specifies that “the clock-free latch includes a first inverter and a second inverter.” Ex. 1001, 7:6–7. Petitioner contends that the Figure 15 and 17 embodiments each include a “clock-free latch” according to claim 3 for the same reasons they include a “clock-free latch” according to claim 1. Pet. 57; see Ex. 1003, A31–A32. Further, Petitioner asserts that “Tachibana discloses that a first inverter 604 and a second inverter 629 comprise the clock-free latch” in each embodiment. Pet. 57; see Ex. 1003, A31–A32.

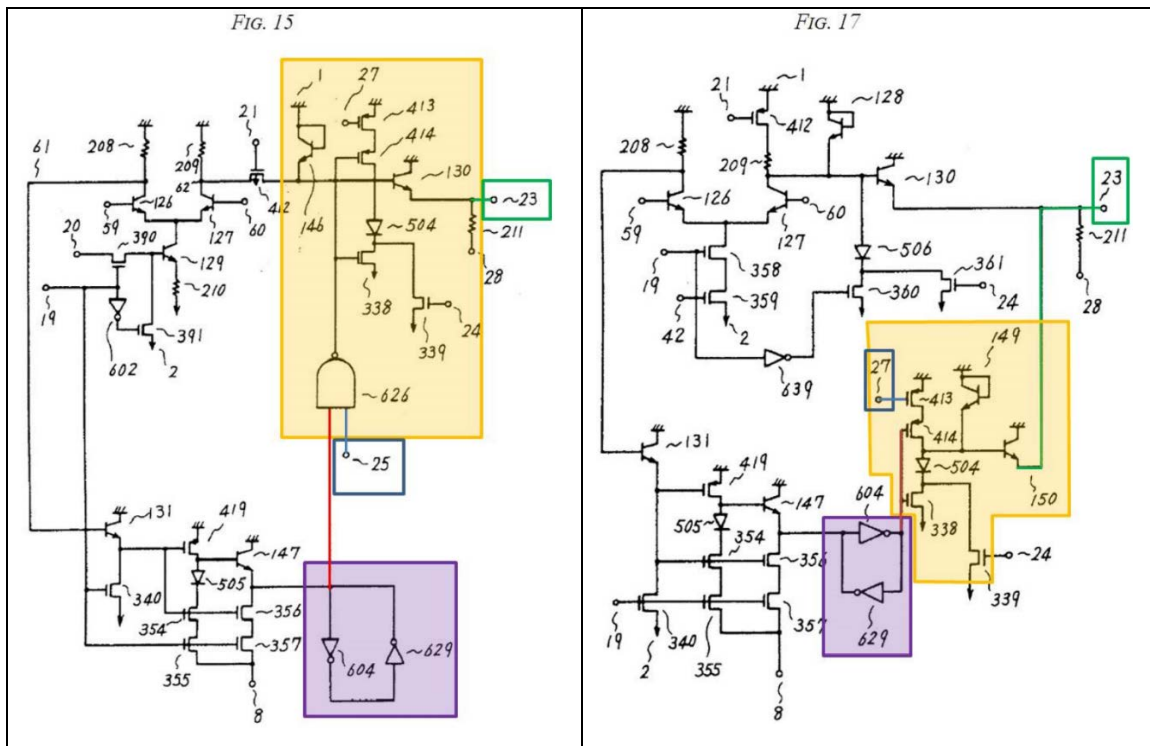
Patent Owner does not make any arguments specific to claim 3. *See, e.g.*, Resp. 28–42.

As discussed above for claim 1, the Figure 15 and 17 embodiments each include a clock-free latch formed by inverters 604 and 629, i.e., “a first inverter and a second inverter” as required by claim 3. Ex. 1003 ¶¶ 59, 61, A25–A29, A31–A32; Ex. 1005, 119–20, Figs. 15, 17; Ex. 2001 ¶¶ 60, 63–64, 78. Hence, Petitioner has shown by a preponderance of the evidence that claim 3 is unpatentable under § 102(b) as anticipated by Tachibana.

#### 6. DEPENDENT CLAIM 8

Claim 8 depends from claim 1 and further requires “a driver module responsive to the clock-free latch, the driver module receiving an output enable signal and producing an output signal.” Ex. 1001, 7:21–24. For the claimed “driver module” in Figure 15, Petitioner identifies the following components: bipolar transistors 130 and 146, resistor 211, NMOS transistors 338 and 339, PMOS transistors 413 and 414, diode 504, and NAND gate 626. Pet. 58–59; *see* Ex. 1003, A32–A36. For the claimed “driver module” in Figure 17, Petitioner identifies the following components: bipolar transistors 149 and 150, NMOS transistors 338 and 339, PMOS transistors 413 and 414, and diode 504. Pet. 59–60; *see* Ex. 1003, A32–A36.

Petitioner provides the following annotated versions of Tachibana’s Figures 15 and 17 to illustrate the claimed “driver module”:



Pet. 58, 60; see Ex. 1003, A33, A36; Ex. 1005, 119–20, Figs. 15, 17.

According to Petitioner, these annotated versions of Figures 15 and 17 each show a latch circuit highlighted in purple, a driver module highlighted in yellow, a terminal for a control signal outlined in blue, and a terminal for an output signal outlined in green. See Pet. 58–61; Ex. 1003, A32–A36.

Dr. Baker explains that the Figure 15 embodiment includes a “driver module” according to claim 8 for four reasons: First, “[t]he driver module receives an input from the clock-free latch (i.e., inverters 604, 629),” and thus the driver module “is responsive to the clock-free latch.” Ex. 1003, A32. Second, “[t]he drive[r] module produces a signal at a terminal 23,” and “the terminal 23 is an output terminal” in the Figure 1 embodiment. *Id.* at A32–A34 (citing Ex. 1005, 111, Figs. 1, 15). Third, the Figure 15 embodiment “achieves the same operation” as the Figure 1 embodiment, and terminals with the same number correspond to the same terminal. *Id.* at A35

(citing Ex. 1005, 119–20). Fourth, “[t]he driver module also receives a control signal at a terminal 25” for “enabling the write operation,” and thus the driver module receives “an output enable signal.” *Id.* at A32–A35 (citing Ex. 1005, 111–13, 116, 119–20, Figs. 6, 15).

Additionally, Dr. Baker explains that the Figure 17 embodiment includes a “driver module” according to claim 8 because that embodiment “includes a similar module that receives the output of the clock-free latch and a control signal 27, and produces an[] output signal at terminal 23.” *Id.* at A36 (citing Ex. 1005, Fig. 17).

Patent Owner does not make any arguments specific to claim 8. *See, e.g.*, Resp. 28–42.

For the reasons explained by Dr. Baker, the Figure 15 and 17 embodiments each include a “driver module” according to claim 8. Hence, Petitioner has shown by a preponderance of the evidence that claim 8 is unpatentable under § 102(b) as anticipated by Tachibana.

#### 7. DEPENDENT CLAIM 9

Claim 9 depends from claim 1 and specifies that “the level converter includes a plurality of transistors.” Ex. 1001, 7:25–26. Petitioner contends that the Figure 15 and 17 embodiments each include a “level converter” according to claim 9 for the same reasons they include a “level converter” according to claim 1. Pet. 61; *see* Ex. 1003, A37. Further, Petitioner asserts that Tachibana discloses that the ECL-MOS level-conversion circuit in each embodiment includes “a plurality of transistors comprised of at least bipolar transistor 147, PMOS transistor 419, and NMOS transistors 354, 355, 356, and 357.” Pet. 61; *see* Ex. 1003, A37.

Patent Owner does not make any arguments specific to claim 9. *See, e.g.*, Resp. 28–42.

As discussed above for claim 1, the ECL-MOS level-conversion circuit in each embodiment includes bipolar transistors 131 and 147, NMOS transistors 340, 354, 355, 356, and 357, PMOS transistor 419, and diode 505. Ex. 2001 ¶¶ 82, 86; *see* Ex. 1003 ¶¶ 52–53; Ex. 1005, 111–13, 119–20, Figs. 1, 15, 17; Ex. 2001 ¶¶ 76–77. Thus, each embodiment includes a “level converter” with “a plurality of transistors” as required by claim 9. Hence, Petitioner has shown by a preponderance of the evidence that claim 9 is unpatentable under § 102(b) as anticipated by Tachibana.

#### 8. DEPENDENT CLAIM 10

Claim 10 depends from claim 1 and specifies that “the differential amplifier has an output driven by at least one of an emitter and a source of a transistor.” Ex. 1001, 7:27–29. Petitioner contends that the Figure 15 and 17 embodiments each include a differential amplifier with bipolar transistor 131 and that the emitter of bipolar transistor 131 “drives the output of the differential amplifier to the ECL-MOS level conversion circuit.” Pet. 61–63; Ex. 1003, A37–A40.

Our Institution Decision explained that “Petitioner’s contention for claim 10 that the differential amplifiers in Figures 15 and 17 include bipolar transistor 131 conflicts with its contentions for claim 1 that those differential amplifiers provide an output at the collector of bipolar transistor 126 that serves as an input to the ECL-MOS level conversion circuits.” Inst. Dec. 21 (citing Pet. 37, 45, 47–48; Ex. 1003, A13–A14, A22–A23, A25). Our Institution Decision also explained that “Petitioner repeatedly describes the differential amplifiers in Figures 15 and 17 as having an output on

terminal 61” and that “[t]erminal 61 corresponds to the collector of bipolar transistor 126, not the emitter of bipolar transistor 131.” *Id.* (citing Pet. 71, 73–75, 86, 95–96; Ex. 1003, A12–A14, A22–A23, A44–A45, B10–B11; Ex. 1005, Figs. 1, 15, 17).

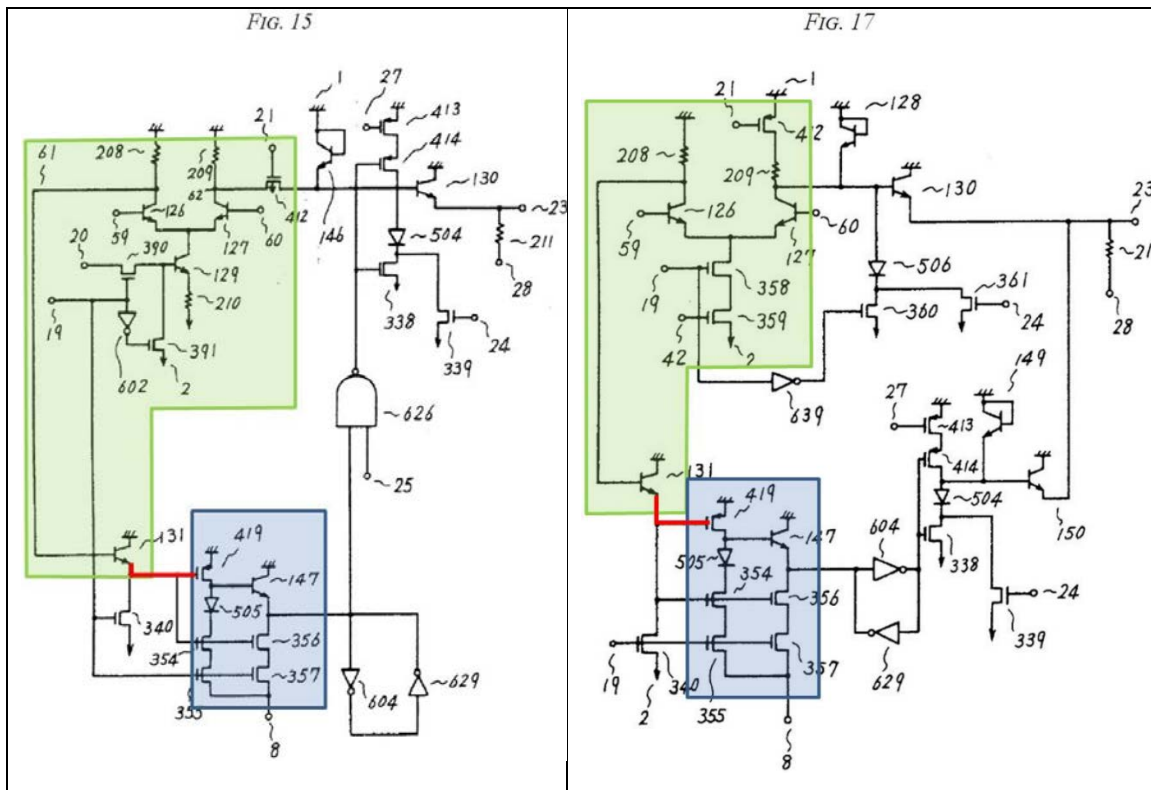
In the Reply, Petitioner asserts that “claim 10 does not require that the output of the differential amplifier be driven by a transistor located in a specific circuit.” Reply 14. Petitioner also asserts that claim 10 does not specify “where the claimed transistor is located in the overall apparatus.” *Id.* According to Petitioner, “the transistor can be part of the ‘differential amplifier,’ part of the ‘level converter,’ or located apart from these circuit elements.” *Id.* But Petitioner cites no part of the ’274 patent to support its assertions. *Id.* Instead, Petitioner cites Dr. Baker’s Reply Declaration. *Id.* (citing Ex. 1028 ¶¶ 25–27). In that declaration, Dr. Baker states that “one of ordinary skill . . . would not interpret claim 10 to require the output driving transistor to be located within the confines of any particular circuit.” Ex. 1028 ¶ 27. But Dr. Baker cites no part of the ’274 patent to support his statement. *Id.* ¶¶ 25–27.

In the Reply, Petitioner further asserts that “Tachibana and the ’274 patent employ a nearly identical circuit path to convey the output of their respective differential amplifiers to their level converters.” Reply 15. Specifically, for Tachibana’s Figure 15, Petitioner contends that a “differential output 61 proceeds out of the collector of [bipolar transistor] 126 (part of a differential pair) and towards the base/emitter of [bipolar transistor] 131 before being provided to the level conversion circuitry.” *Id.* (citing Ex. 1005, Fig. 15; Ex. 1029, 49:20–50:4). Similarly, for ’274 patent Figure 2, Petitioner contends that a “differential output proceeds out of the

collector of [bipolar transistor] 127 (part of a differential pair) and then on to the base/emitter of [bipolar transistor] 123 before being provided to the level conversion circuitry.” *Id.* at 15–16 (citing Ex. 1001, Fig. 2; Ex. 1029, 30:13–20).

In response, Patent Owner argues that the differential amplifiers in Figures 15 and 17 have outputs “generated by the collector of bipolar transistor 126” and, therefore, “the output of Tachibana’s differential amplifier is ‘driven by’ the collector of bipolar transistor 126, not the emitter of bipolar transistor 131.” Sur-reply 21; *see* Resp. 47–48; *see* Ex. 2001 ¶¶ 103–104. Patent Owner asserts that “Tachibana makes clear that bipolar transistor 131 is part of the level converter in” each embodiment. Resp. 50; *see id.* at 20–22, 34–38; Ex. 2001 ¶¶ 79–80, 82–84, 86, 88. Patent Owner quotes Tachibana’s disclosure that “bipolar transistors 131, 132 . . . are elements comprising the ECL-MOS level conversion circuit” in Figure 1. Resp. 33 (emphasis omitted) (quoting Ex. 1005, 111); *see* Ex. 2001 ¶ 77.

In addition, Patent Owner notes that the Petition includes the following annotated versions of Figures 15 and 17 showing bipolar transistor 131 as “part of the differential amplifier”:



Resp. 50; see Pet. 62–63; Ex. 1003, A37–40; Ex. 2001 ¶ 106. According to Petitioner, these annotated versions of Figures 15 and 17 each show a differential amplifier highlighted in green, an ECL-MOS level-conversion circuit highlighted in blue, and “the emitter of bipolar transistor 131 (indicated by the arrow pointing away from the base of the transistor) driv[ing] the output of the differential amplifier to” the ECL-MOS level-conversion circuit. Pet. 63; see *id.* at 24–27; Ex. 1003 ¶¶ 58–61.

For these annotated versions of Figures 15 and 17, Patent Owner argues that Petitioner failed to follow “the express language of Tachibana” in the Petition and instead wrongly redrew “the boundaries of the circuits in Tachibana.” Resp. 50–51. Patent Owner asserts that Petitioner “redrew the boundaries of the differential amplifier to include bipolar transistor 131” because Petitioner understood “that in order for a transistor to drive the output of the differential amplifier, that transistor must be part of the

differential amplifier.” Sur-reply 20. Patent Owner also asserts that in redrawing “the boundaries from what is disclosed by Tachibana,” Petitioner “implicitly acknowledged that bipolar transistor 131 cannot be said to drive the output of the differential amplifier if it is part of the level conversion circuit as Tachibana discloses.” *Id.*

We agree with Patent Owner that if a circuit element, such as a differential amplifier, has an output “driven by” a component, the circuit element includes the component doing the driving. Although the ’274 patent’s written description does not use the term “driven by,” it discusses one circuit element’s output driving another circuit element’s input. *See* Ex. 1001, 4:4, 6:31–34, 6:46–49. As an example, the patent explains that “[o]utput driver 112 provides an output signal 46” and that output driver 112 “may include a variety of buffers” and “any other type of circuit that may be used to drive [output] signal 46 to I/O pad 26.” *Id.* at 4:4, 6:46–49; *see id.* at 2:26–28, Figs. 1–2. Hence, output driver 112 includes the components that drive its output such that output driver 112 has an output “driven by” those components.

Focusing on a differential amplifier as recited in claim 10, the ’274 patent states that “differential amplifier 100 includes” transistors 123 and 132. Ex. 1001, 2:58–67. The patent also states that “[t]ransistors 123 and 132 . . . provide the output of differential amplifier 100” to “the input of level converter 102.” *Id.* at 5:5–6, 5:13–17, 6:16–19; *see* Ex. 1028 ¶ 31 (citing Ex. 1001, 5:5–17). In particular, the emitters of transistors 123 and 132 provide the output of differential amplifier 100 to the control electrodes of transistors 140 and 142, respectively, in level converter 102. Ex. 1001, 3:1–4, 3:28–32, 3:39–42, 5:13–17, 5:63–64, 6:16–19, Fig. 2.

Hence, differential amplifier 100 includes the components, i.e., transistors 123 and 132, that drive its outputs such that differential amplifier 100 has its outputs “driven by” those components. Specifically, differential amplifier 100 has its outputs “driven by” the emitters of transistors 123 and 132. *Id.* at 5:5–6, 5:13–17, 6:16–19, Fig. 2. Thus, differential amplifier 100 exemplifies an arrangement according to claim 10, e.g., a differential amplifier having an output “driven by” an emitter of a transistor.

For these reasons, the '274 patent indicates that if a circuit element, such as a differential amplifier, has an output “driven by” a component, the circuit element includes the component doing the driving.

As discussed above for claim 1, the differential amplifiers in Figures 15 and 17 do not include bipolar transistor 131. Ex. 2001 ¶¶ 80–81, 84–85; *see* Ex. 1003 ¶¶ 52–53; Ex. 1005, 111–13, 119–20, Figs. 1, 15, 17; Ex. 2001 ¶¶ 76–77. Instead, the ECL-MOS level-conversion circuit in each embodiment includes bipolar transistor 131. Ex. 2001 ¶¶ 82, 86; *see* Ex. 1003 ¶¶ 52–53; Ex. 1005, 111–13, 119–20, Figs. 1, 15, 17; Ex. 2001 ¶¶ 76–77. Because the differential amplifier in each embodiment does not include bipolar transistor 131, the differential amplifier does not have an output driven by the emitter of bipolar transistor 131.

Hence, Petitioner has not shown by a preponderance of the evidence that claim 10 is unpatentable under § 102(b) as anticipated by Tachibana.

#### 9. DEPENDENT CLAIM 11

Claim 11 depends from claim 1 and specifies that “the impedance control circuit is a switching element connected to a power source.” Ex. 1001, 7:30–32. Petitioner contends that the Figure 15 and 17

embodiments each include an “impedance control circuit” according to claim 11 for two reasons: First, PMOS transistor 412 is a “switching element.” Pet. 64; *see* Ex. 1003, A40–A41. Second, Figures 15 and 17 each show PMOS transistor 412 connected to a ground terminal, and “ground terminals are power sources.” Pet. 64–65; *see* Ex. 1003, A40–A41.

Dr. Baker explains that PMOS transistor 412 “is a switching element because it switches between a ‘non-conducting state’ and a ‘conducting state.’” Ex. 1003, A41 (citing Ex. 1005, 112–13). He also explains that “[g]round terminals are power sources because they supply power at ground voltage level.” *Id.* at A40. In addition, Dr. Baker states that Figure 15 “shows that the impedance control circuit (*i.e.*, transistor 412) is a switching element connected to a power source (*i.e.*, a GND terminal) via a resistor 209.” *Id.* He also states that Figure 17 “shows that the impedance control circuit (*i.e.*, transistor 412) is a switching element directly connected to a power source (*i.e.*, a GND terminal 1).” *Id.*

Patent Owner does not make any arguments specific to claim 11. *See, e.g.*, Resp. 28–42.

For the reasons explained by Dr. Baker, the Figure 15 and 17 embodiments each include an “impedance control circuit” according to claim 11. Hence, Petitioner has shown by a preponderance of the evidence that claim 11 is unpatentable under § 102(b) as anticipated by Tachibana.

#### 10. DEPENDENT CLAIM 12

Claim 12 depends from claim 1 and specifies that “the differential amplifier receives a regulated voltage signal.” Ex. 1001, 7:33–34. For the claimed “regulated voltage signal” in Figure 15, Petitioner identifies the “constant voltage” the differential amplifier receives “from terminal 20.”

Pet. 66; *see* Ex. 1003, A42. For the claimed “regulated voltage signal” in Figure 17, Petitioner identifies the “constant voltage” the differential amplifier receives “from terminal 42.” Pet. 66–67; *see* Ex. 1003, A43. Based on the received “constant voltage,” Petitioner contends that the Figure 15 and 17 embodiments each include a “differential amplifier” that “receives a regulated voltage signal” as required by claim 12. Pet. 66–68.

For Figure 15, Tachibana describes terminal 20 as “a constant voltage terminal.” Ex. 1005, 119; *see id.* at 124; Ex. 1003, A43. In Figure 15, terminal 20 connects to NMOS transistor 390 in the differential amplifier. Ex. 1005, Fig. 15; *see* Ex. 1003, A42. For Figure 17, Tachibana describes terminal 42 as “a constant voltage terminal.” Ex. 1005, 120; *see id.* at 124; Ex. 1003, A43–A44. In Figure 17, terminal 42 connects to NMOS transistor 359 in the differential amplifier. Ex. 1005, Fig. 17; *see* Ex. 1003, A43. In addition, Dr. Baker explains that a “constant voltage terminal provides a regulated voltage signal because the voltage supplied from these terminals is constant.” Ex. 1003, A44.

Patent Owner does not make any arguments specific to claim 12. *See, e.g.*, Resp. 28–42.

Based on Tachibana’s disclosure and Dr. Baker’s explanation, we agree with Petitioner that the Figure 15 and 17 embodiments each include a “differential amplifier” that “receives a regulated voltage signal” as required by claim 12. Hence, Petitioner has shown by a preponderance of the evidence that claim 12 is unpatentable under § 102(b) as anticipated by Tachibana.

## 11. INDEPENDENT CLAIM 14

### (a) Preamble

Claim 14’s preamble recites “[a] method of amplifying a signal to produce a latched digital signal.” Ex. 1001, 7:56–57. Petitioner asserts that Tachibana satisfies claim 14’s preamble for the same reasons that Tachibana discloses “a differential amplifier,” “a level converter,” and “a clock-free latch” according to claim 1. Pet. 68–72; *see* Ex. 1003, A44. Patent Owner does not make any arguments specific to claim 14’s preamble. *See, e.g.*, Resp. 28–54.

We agree with Petitioner that Tachibana satisfies claim 14’s preamble for the same reasons that Tachibana discloses “a differential amplifier,” “a level converter,” and “a clock-free latch” according to claim 1. *See supra* §§ III.B.3(c), (e), (f); Ex. 1003, A7–A14, A19–A29, A44; Ex. 1005, 119–20, Figs. 15, 17.

### (b) Amplifying

Claim 14 recites “amplifying a differential input to produce a differential output in response to a clock signal.” Ex. 1001, 8:1–2. For Figures 15 and 17, Petitioner contends that the differential amplifier in each embodiment “amplif[ies] the difference between” the signals at its two input terminals and then outputs “the result as differential outputs” at its two output terminals. Pet. 73; *see* Ex. 1003, A7–A14, A44–A45. For the differential amplifier in each embodiment, Petitioner asserts that each of the amplifier’s two output terminals provides a “differential output” because the signal at each output terminal “reflect[s] the amplified difference between” the signals at the amplifier’s two input terminals. Pet. 73; *see* Ex. 1003,

A44–A45 (citing Ex. 1026, code (57), 2:36–39, Fig. 1; Ex. 1027, code (57), 2:19–25, 3:17–19, Fig. 1).

We agree with Petitioner that the differential amplifier in each embodiment amplifies the signals at its two input terminals to produce amplified signals at its two output terminals. Ex. 1003, A7–A14, A44–A45; Ex. 1005, 119–20, Figs. 15, 17. A differential amplifier “accepts two inputs and amplifies the voltage difference between the two inputs.” Ex. 1003 ¶ 36, A44; *see* Ex. 1001, 1:25–29; Ex. 1007, 273; Ex. 1008, 579.

In addition, Petitioner contends that the differential amplifier in each embodiment amplifies the signals at its two input terminals to produce amplified signals at its two output terminals “in response to a clock signal.” Pet. 74–75; *see* Ex. 1003, A44–A45. Specifically, Petitioner asserts that the differential amplifier in each embodiment “produce[s] a differential output” in response to a clock signal “received on clock signal terminal 19.” Pet. 75; *see* Ex. 1003, A45.

Patent Owner asserts that Petitioner has not shouldered its burden to show that the differential amplifiers in Figures 15 and 17 “amplify a differential input in response to a clock signal.” Resp. 53–54.

Based on the entire record, including the evidence introduced during the trial, we disagree with Patent Owner. For the reasons explained above, we construe “clock signal” to mean “a control signal that enables or disables a circuit element in an output stage, such as a differential amplifier or a level converter.” Under our construction, Tachibana’s timing circuit produces “clock signals” because the control signals that it produces enable or disable circuit elements in the Figure 15 and 17 embodiments. Ex. 1003, A3–A15, A44–A45; Ex. 1005, 111–17, 119–20, Figs. 2, 5, 8–9, 15, 17.

For instance, Tachibana’s timing circuit produces control signals at terminals 19 and 21 that enable or disable the differential amplifier in each embodiment. Ex. 1003, A9, A14–A15, A45; Ex. 1005, 111–16, 119–20, Figs. 15, 17; Ex. 1028 ¶ 17; *see* Ex. 1003 ¶ 54; Ex. 2001 ¶¶ 98–99. Hence, the differential amplifier in each embodiment amplifies the signals at its two input terminals to produce amplified signals at its two output terminals “in response to a clock signal.”

For the reasons discussed above, the Figure 15 and 17 embodiments each “amplify[] a differential input to produce a differential output in response to a clock signal” as required by claim 14.

(c) Level Converting

Claim 14 recites “level converting the differential output to produce a level converted signal.” Ex. 1001, 8:3–4. For Figures 15 and 17, Petitioner asserts that the ECL-MOS level-conversion circuit in each embodiment “level convert[s] the output 61 of the differential amplifier to MOS transistor levels.” Pet. 75; *see* Ex. 1003, A19–A25, A45.

Patent Owner asserts that the ECL-MOS level-conversion circuit in each embodiment does not level convert “**the** differential output” because that circuit receives as an input signal only one of the differential amplifier’s two output signals and the two output signals together constitute “**the** differential output.” *See* Resp. 51–53; Sur-reply 24–26.

The dispute concerning “level converting the differential output to produce a level converted signal” centers on the meaning of “differential output.” Thus, we address the construction of “differential output” and then consider whether the Figure 15 and 17 embodiments each “level convert[]

the differential output to produce a level converted signal” as required by claim 14.

(i) Construction of “Differential Output”

Petitioner asserts that an ordinarily skilled artisan “would understand ‘differential output’ to simply refer to [an] output of a differential amplifier indicating the difference in voltage between inputs.” Reply 21; *see id.* at 20. Petitioner contends that a differential amplifier “is a common, well-known electrical component that receives two inputs and produces amplified output proportional to the difference between” the two inputs. *Id.* at 19 (citing Ex. 1007, 273); *see* Ex. 1003 ¶ 36. Petitioner also contends that a differential amplifier “does not require any particular number” of output terminals. Reply 19; *see* Ex. 1003 ¶ 36; Ex. 1028 ¶ 34.

Further, Petitioner argues that the prior art includes differential amplifiers with one output terminal and differential amplifiers with two output terminals. Reply 19 (citing Ex. 1007, 274; Ex. 1009, 195); *see* Ex. 1003 ¶¶ 36–37 (citing Ex. 1009, 195); Ex. 1028 ¶ 34 (citing Ex. 1030, 245). For differential amplifiers with two output terminals, Petitioner contends that the two output signals “are inverted with respect to each other” but “have identical magnitudes and thus provide the same indication of the difference in input voltages.” Reply 19; *see* Ex. 1003 ¶ 37.

Patent Owner asserts that an ordinarily skilled artisan “would have understood a differential output to be an output provided on two wires.” Resp. 52; *see* Ex. 2001 ¶ 110. Patent Owner also asserts that “differential output” can “mean different things depending on the specific differential amplifier” and that an ordinarily skilled artisan’s understanding of the term “must be informed by” the context of the ’274 patent. Sur-reply 24–25. To

support its assertions, Patent Owner cites the '274 patent's description of differential amplifier 100 and level converter 102 in Figure 2. Resp. 51–52 (citing Ex. 1001, 5:63–67); *see* Ex. 2001 ¶¶ 109–110.

In particular, Patent Owner contends that differential amplifier 100 produces “a differential output on the drain terminals of transistors 124 and 133.” Resp. 51; *see* Ex. 2001 ¶ 109. The drain terminals of transistors 124 and 133 connect to the emitters of transistors 123 and 132, respectively, that provide “the output of differential amplifier 100” to “the input of level converter 102.” Ex. 1001, 3:28–32, 3:39–42, 5:5–6, 5:13–17, 5:63–64, 6:16–19, Fig. 2. The drain terminals of transistors 124 and 133 also connect to the control electrodes of transistors 140 and 142, respectively, at the input of level converter 102. *Id.* at 3:28–32, 3:39–42, 5:13–17, Fig. 2; *see* Ex. 2001 ¶ 109.

According to Patent Owner, “the drain terminals of transistors 124 and 133” with the “differential output” are “two separate wires,” and those “two separate wires” are “connected to the control electrodes of transistors 140 and 142” at the input of level converter 102. Resp. 51; *see* Ex. 2001 ¶ 109. Patent Owner asserts that as a result of this arrangement “the level converter 102 converts the differential output of the differential amplifier 100.” Resp. 51; *see* Ex. 2001 ¶ 109.

In response, Petitioner argues that Patent Owner improperly attempts to limit claim scope “to the particular embodiment shown in Figure 2.” Reply 20. Petitioner also argues that “it is axiomatic that claims are not to be limited to specific embodiments in [the] specification.” *Id.* at 21 (citing *Phillips*, 415 F.3d at 1313).

We agree with Petitioner that Patent Owner improperly attempts to limit claim scope to the particular embodiment shown in Figure 2. Federal Circuit case law “counsels against incorporating a feature of a preferred embodiment into the claims.” *Arthrex, Inc. v. Smith & Nephew, Inc.*, 935 F.3d 1319, 1330 (Fed. Cir. 2019).

Here, the '274 patent describes Figure 2 as depicting “one embodiment” of an output stage. Ex. 1001, 1:51–53, 2:50–52, 4:48–51, 6:51–56. The patent expressly states that “alternate embodiments of the present invention may use different circuit elements than those illustrated” in Figure 2. *Id.* at 3:11–13. The patent describes the components comprising differential amplifier 100 in Figure 2 as “one embodiment” of a differential amplifier. *Id.* at 2:58–67. The patent describes the components comprising level converter 102 in Figure 2 as “one embodiment” of a level converter. *Id.* at 3:1–4. Thus, the patent contemplates other embodiments of an output stage, a differential amplifier, and a level converter.

Patent Owner quotes the following statement in the '274 patent: “[T]he output of differential amplifier 100 (*i.e.*, the emitters of transistors 123 and 132) provides the amplified differential voltage to the gates of transistors 140 and 142.” Sur-reply 25 (quoting Ex. 1001, 6:16–19) (emphasis added by Patent Owner). Patent Owner then contends that “[t]he use of ‘*i.e.*’ defines what is meant by ‘differential output,’ specifically, that the differential output of the differential amplifier is provided to the level converter on the two wires corresponding to the emitters of two separate transistors.” *Id.*

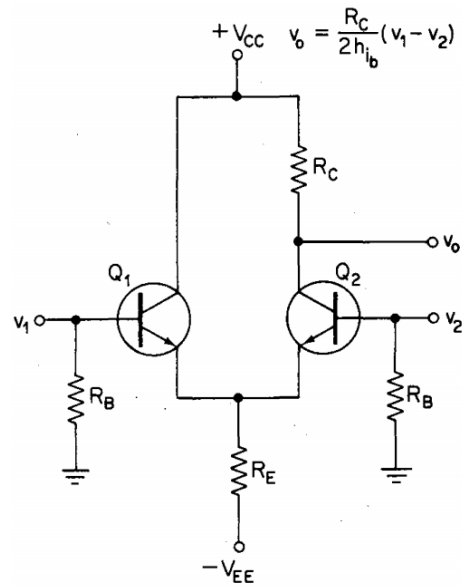
We disagree. The '274 patent does not use “*i.e.*” to define “differential output.” That term appears nowhere in the written description.

Ex. 1001, 1:5–6:60. Rather, the '274 patent uses “i.e.” to define “the output of differential amplifier 100” as “the emitters of transistors 123 and 132.” *Id.* at 6:16–19.

“As a general rule, the ordinary and customary meaning controls unless ‘a patentee sets out a definition and acts as his own lexicographer, or . . . the patentee disavows the full scope of a claim term either in the specification or during prosecution.’” *Sumitomo Dainippon Pharma Co. v. Emcure Pharm. Ltd.*, 887 F.3d 1153, 1157 (Fed. Cir. 2018) (quoting *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)). For “differential output,” we see no reason to depart from that general rule.

For the reasons explained below, the evidence establishes that the ordinary and customary meaning of “differential output” encompasses a signal at an output terminal of a differential amplifier. *See* Ex. 1003 ¶¶ 36–37, A44–A45 (citing Ex. 1026, code (57), 2:36–39, Fig. 1; Ex. 1027, code (57), 2:19–25, 3:17–19, Fig. 1); Ex. 1009, 194–95; Ex. 1026, code (57), 2:36–39, 2:47–56, Fig. 1; Ex. 1027, code (57), 2:19–25, 3:17–19, Fig. 1; Ex. 1028 ¶¶ 34–35, 38–39; Ex. 1029, 50:5–9, 51:12–17; Ex. 1030, 241–48.

First, the prior art includes differential amplifiers with one output terminal and differential amplifiers with two output terminals. Ex. 1007, 273–80; Ex. 1009, 194–95; Ex. 1030, 241–48; *see* Ex. 1003 ¶¶ 36–37; Ex. 1028 ¶¶ 34–35. As an example of a prior-art differential amplifier with one output terminal, the figure below shows a differential amplifier producing one output signal identified as signal  $V_o$ :



(b) Single-ended output differential amplifier.

Ex. 1030, 245. In the figure above, the differential amplifier “has two input terminals and a *single-ended* output.” *Id.* at 246 (emphasis in original).

Dr. Baker discusses a similar differential amplifier with two input terminals and a single-ended output. Ex. 1028 ¶¶ 34–35 (citing Ex. 1030, 245–46); *see* Ex. 1030, 245–46.

As an example of a prior-art differential amplifier with two output terminals, the figure below shows a differential amplifier producing two output signals identified as signals  $V_{o1}$  and  $V_{o2}$ :

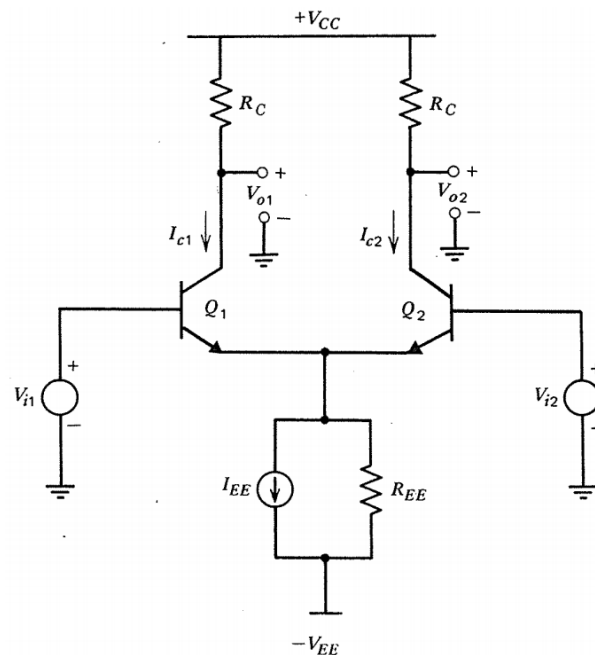


Figure 3.26 Emitter-coupled pair circuit diagram.

Ex. 1009, 195; *see* Ex. 1003 ¶ 36. In the figure above, “bipolar transistors  $Q_1$  and  $Q_2$  form a transistor pair that amplifies the difference between the input voltages  $V_{i1}$  and  $V_{i2}$ ,” and “differential outputs  $V_{o1}$  and  $V_{o2}$  are inverted with respect to one another (*i.e.*, equal and opposite).” Ex. 1003 ¶ 37.

Second, the prior art describes differential amplifiers with two output terminals as having two “differential outputs,” *i.e.*, a “differential output” at each output terminal. *See* Ex. 1003, A44–A45 (citing Ex. 1026, code (57), 2:36–39, Fig. 1; Ex. 1027, code (57), 2:19–25, 3:17–19, Fig. 1). As an example, U.S. Patent No. 4,720,686 (issued in 1988) discloses a “fully differential amplifier” with two output terminals that provide a “positive output” and a “negative output.” Ex. 1026, code (57), 2:36–39, 2:47–56, Fig. 1. That patent also discloses a circuit that “converts [the] differential outputs of” the “fully differential amplifier” to “a single output using a buffer amplifier.” *Id.* at code (57), Fig. 1; *see id.* at 2:36–39. As another

example, European Patent Application 0345621 (published in 1989) discloses a two-stage differential amplifier where “[t]he differential outputs of the first stage are applied to the inputs of” the second stage. Ex. 1027, code (57), 2:19–25, 3:17–19, Fig. 1. Patent Owner does not address this prior art. *See, e.g.*, Resp. 51–53; Sur-reply 24–26.

Third, Dr. Baker and Dr. Khatri agree that the differential amplifier in Tachibana’s Figure 15 has two “differential outputs,” i.e., a “differential output” at output terminal 61 and a “differential output” at output terminal 62. Ex. 1003, A44–A45; Ex. 1028 ¶ 38; Ex. 1029, 50:5–9, 51:12–17.

Fourth, consistent with the prior art, claim 7 recites a “differential amplifier” with two outputs, i.e., “first and second outputs.” Ex. 1001, 7:16–18.

Based on the evidence, the ordinary and customary meaning of “differential output” encompasses a signal at an output terminal of a differential amplifier. Specifically, a differential amplifier with one output terminal provides a “differential output” at the output terminal. *See* Ex. 1028 ¶¶ 34–35. Similarly, a differential amplifier with two output terminals provides a “differential output” at each output terminal, with the two outputs “inverted with respect to one another (*i.e.*, equal and opposite).” *See* Ex. 1003 ¶¶ 36–37, A44–A45; Ex. 1026, code (57), 2:36–39, 2:47–56, Fig. 1; Ex. 1027, code (57), 2:19–25, 3:17–19, Fig. 1; Ex. 1028 ¶¶ 38–39.

To support its assertions about the meaning of “differential output,” Patent Owner offers the following dictionary definition of “differential signal”: “A signal that is conveyed between two separate conductors, instead of one active conductor and signal ground. The magnitude of the differential signal is the difference between the two signals, rather than the

voltages between the two individual signals and ground.” Resp. 52 (quoting Ex. 2003 (*IEEE 7th*), 304); *see* Ex. 2001 ¶ 111.

In response, Petitioner argues that the dictionary definition of “differential signal” is irrelevant because claim 14 “does not use the term ‘differential signal’ . . . [and] refers only to a ‘differential output.’” Reply 21–22.

The dictionary definition of “differential signal” provides some support for Patent Owner’s position. Reasoning by analogy, if a “differential signal” is “conveyed between two separate conductors,” then a “differential output” is also “conveyed between two separate conductors.” But that dictionary definition does not outweigh the other evidence to narrow the ordinary and customary meaning of “differential output.” As the Federal Circuit explained in *Phillips*, dictionary definitions “do not necessarily reflect the inventor’s goal of distinctly setting forth” the invention, and “[t]here is no guarantee” that a dictionary uses a term “in the same way” as a patent. *Phillips*, 415 F.3d at 1322.

For the reasons discussed above, we conclude that “differential output” encompasses a signal at an output terminal of a differential amplifier.

(ii) Level Converting the Differential Output

Next, we consider whether the Figure 15 and 17 embodiments each “level convert[] the differential output to produce a level converted signal” as required by claim 14. As discussed above, the differential amplifier in each embodiment amplifies the signals at its two input terminals to produce amplified signals at its two output terminals. Ex. 1003, A10–A14, A44–A45; Ex. 1005, 119–20, Figs. 15, 17; *see* Ex. 1007, 273; Ex. 1008,

579. As also discussed above, a differential amplifier with two output terminals provides a “differential output” at each output terminal.

Further, the ECL-MOS level-conversion circuit in each embodiment receives as an input signal one of the differential amplifier’s two output signals, i.e., a “differential output.” Ex. 1003, A19–A25, A45; Ex. 1005, 119–20, Figs. 15, 17; Ex. 2001 ¶¶ 80–81, 84–85, 103–104. The ECL-MOS level-conversion circuit then level converts the input signal, i.e., the “differential output,” to MOS transistor levels. Ex. 1003, A19–A25, A45; Ex. 1005, 119–20, Figs. 15, 17.

For the reasons discussed above, the Figure 15 and 17 embodiments each “level convert[] the differential output to produce a level converted signal” as required by claim 14.

(d) Detecting and Latching

Claim 14 recites “detecting a change in impedance at an input of a clock-free latch and latching the level converted signal at the clock-free latch to produce the latched digital signal.” Ex. 1001, 8:5–7. For Figures 15 and 17, Petitioner contends that changing the signal at terminal 19 in each embodiment changes the impedance detected by a clock-free latch formed by inverters 604 and 629. Pet. 78; *see* Ex. 1003, A45.

Specifically, Petitioner asserts that a low level (logic “0”) at terminal 19 places the ECL-MOS level-conversion circuit in “a high impedance state” and the clock-free latch “continue[s] to latch the level converted signal value” received from the level-conversion circuit. Pet. 78; *see* Ex. 1003, A45, B2–B6; Ex. 1005, 110–14, 119–20. Petitioner also asserts that transitioning to a high level (logic “1”) at terminal 19 switches the ECL-MOS level-conversion circuit to “a low impedance state” and “provides a

new level converted signal to” the clock-free latch, and the latch then latches the new level-converted signal. Pet. 78; *see* Ex. 1003, A45, B2–B6; Ex. 1005, 110–14, 119–20.

Patent Owner does not make any arguments specific to this limitation. *See, e.g.*, Resp. 28–54.

For the reasons stated by Petitioner, the clock-free latch formed by inverters 604 and 629 detects a change in impedance at its input when the ECL-MOS level-conversion circuit switches from “a high impedance state” to “a low impedance state,” and the latch then latches the new level-converted signal from the level-conversion circuit. *See* Ex. 1003, A25–A29, A45, B2–B6; Ex. 1005, 110–14, 119–20, Figs. 15, 17. Thus, the Figure 15 and 17 embodiments each “detect[] a change in impedance at an input of a clock-free latch and latch[] the level converted signal at the clock-free latch to produce the latched digital signal” as required by claim 14.

(e) Outputting

Claim 14 also recites “outputting the latched digital signal.” Ex. 1001, 8:9. For Figures 15 and 17, Petitioner contends that a “module” in each embodiment receives an input from the clock-free latch and then provides an output signal at output terminal 23. Pet. 78; *see* Ex. 1003, A32–A36, A45–A46. Petitioner identifies that “module” as the “driver module” discussed above for claim 8. Pet. 78–80; *see id.* at 57–61.

Patent Owner does not make any arguments specific to this limitation. *See, e.g.*, Resp. 28–54.

For the reasons explained by Dr. Baker for claim 8, the Figure 15 and 17 embodiments each include a “driver module” that receives an input from the clock-free latch and then provides an output signal at output

terminal 23. *See* Ex. 1003, A32–A36, A45–A46; Ex. 1005, 110–13, 116, 119–20, Figs. 15, 17. Thus, the Figure 15 and 17 embodiments each “output[] the latched digital signal” as required by claim 14.

(f) Whether Tachibana Anticipates Claim 14

As explained above, Petitioner has shown by a preponderance of the evidence that the Figure 15 and 17 embodiments each include every element of claim 14 arranged as required by the claim. Hence, Petitioner has shown by a preponderance of the evidence that claim 14 is unpatentable under § 102(b) as anticipated by Tachibana.

12. DEPENDENT CLAIM 15

Claim 15 depends from claim 14 and further requires “providing the level converted signal to the clock-free latch.” Ex. 1001, 8:10–12. For Figures 15 and 17, Petitioner asserts that the ECL-MOS level-conversion circuit in each embodiment provides an output signal to the clock-free latch. Pet. 81; *see* Ex. 1003, A25–A29, A46. Patent Owner does not make any arguments specific to claim 15. *See, e.g.*, Resp. 28–54.

The Figure 15 and 17 embodiments each “provid[e] the level converted signal to the clock-free latch” as required by claim 15 for the same reasons they include “a clock-free latch responsive to the level converter” as required by claim 1. *See supra* § III.B.3(f); Ex. 1003 ¶¶ 58–61, A25–A29, A46; Ex. 1005, 119–20, Figs. 15, 17. Hence, Petitioner has shown by a preponderance of the evidence that claim 15 is unpatentable under § 102(b) as anticipated by Tachibana.

13. DEPENDENT CLAIM 16

Claim 16 depends from claim 14 and further requires “buffering the latched digital signal to produce an output signal.” Ex. 1001, 8:13–15.

Petitioner contends that “Tachibana discloses that the circuits shown in Figures 15 and 17 act as the output buffer circuit 608 in Figure 10.” Pet. 82–83; *see* Ex. 1003, A1–A3, A46. Petitioner also contends that “the latch comprised of inverters 604 and 629 itself buffers the signal.” Pet. 83; *see* Ex. 1003, A46.

Dr. Baker explains that “a latch is ‘[a]lso called a buffer.’” Ex. 1003, A46 (alteration in original) (quoting Ex. 1011, 328). He also explains that “in a latch, ‘the value on the input wires is buffered upon occurrence of some event, such as a clock pulse or ri[s]ing edge of a separate latch signal.’” *Id.* (quoting Ex. 1012, 361–62).

Patent Owner does not make any arguments specific to claim 16. *See, e.g.*, Resp. 28–54.

For the reasons explained by Dr. Baker, the Figure 15 and 17 embodiments each “buffer[] the latched digital signal to produce an output signal” as required by claim 16. Hence, Petitioner has shown by a preponderance of the evidence that claim 16 is unpatentable under § 102(b) as anticipated by Tachibana.

#### 14. INDEPENDENT CLAIM 20

##### (a) Preamble

Claim 20’s preamble recites “[a] method of amplifying a signal to produce a latched digital signal.” Ex. 1001, 8:27–29. Petitioner asserts that Tachibana satisfies claim 20’s preamble for the same reasons that Tachibana satisfies claim 14’s preamble. Pet. 83; *see* Ex. 1003, A47. Patent Owner does not make any arguments specific to claim 20’s preamble. *See, e.g.*, Resp. 28–54.

We agree with Petitioner that Tachibana satisfies claim 20's preamble for the same reasons that Tachibana satisfies claim 14's preamble. *See supra* § III.B.11(a); Ex. 1003, A7–A14, A19–A29, A44, A47; Ex. 1005, 119–20, Figs. 15, 17.

(b) Amplifying and Level Converting

Claim 20 recites “amplifying and level converting a differential input to produce a level converted signal in response to a clock signal.” Ex. 1001, 8:29–31. Petitioner asserts that this limitation “is merely the union of” claim 14's first two limitations and that the Figure 15 and 17 embodiments each satisfy this limitation for the same reasons they satisfy claim 14's corresponding limitations. Pet. 83.

As discussed above for claim 14, Patent Owner asserts that Petitioner has not shouldered its burden to show that the differential amplifiers in Figures 15 and 17 “amplify a differential input in response to a clock signal.” Resp. 53–54.

We disagree with Patent Owner for the reasons discussed above for claim 14. In addition, we agree with Petitioner that the Figure 15 and 17 embodiments each satisfy this limitation for the same reasons they satisfy claim 14's corresponding limitations. *See supra* §§ III.B.11(b)–(c); Ex. 1003, A10–A14, A19–A25, A44–A45; Ex. 1005, 119–20, Figs. 15, 17.

(c) Detecting and Latching

Claim 20 recites “detecting a change in impedance at an input of a clock-free latch and latching the level converted signal at the clock-free latch to produce the latched digital signal.” Ex. 1001, 8:32–34. Petitioner asserts that this limitation “is identical to” claim 14's third limitation and that the Figure 15 and 17 embodiments each satisfy this limitation for the same

reasons they satisfy claim 14's corresponding limitation. Pet. 84. Patent Owner does not make any arguments specific to this limitation distinct from claim 14. *See, e.g.*, Resp. 28–54.

We agree with Petitioner that the Figure 15 and 17 embodiments each satisfy this limitation for the same reasons they satisfy claim 14's corresponding limitation. *See supra* § III.B.11(d); Ex. 1003, A25–A29, A45, B2–B6; Ex. 1005, 110–14, 119–20, Figs. 1, 15, 17.

(d) Outputting

Claim 20 also recites “outputting the latched digital signal.” Ex. 1001, 8:36. Petitioner asserts that this limitation “is identical to” claim 14's fourth limitation and that the Figure 15 and 17 embodiments each satisfy this limitation for the same reasons they satisfy claim 14's corresponding limitation. Pet. 84. Patent Owner does not make any arguments specific to this limitation. *See, e.g.*, Resp. 28–54.

We agree with Petitioner that the Figure 15 and 17 embodiments each satisfy this limitation for the same reasons they satisfy claim 14's corresponding limitation. *See supra* § III.B.11(e); Ex. 1003, A32–A36, A45–A46; Ex. 1005, 110–13, 116, 119–20, Figs. 1, 15, 17.

(e) Whether Tachibana Anticipates Claim 20

As explained above, Petitioner has shown by a preponderance of the evidence that the Figure 15 and 17 embodiments each include every element of claim 20 arranged as required by the claim. Hence, Petitioner has shown by a preponderance of the evidence that claim 20 is unpatentable under § 102(b) as anticipated by Tachibana.

15. INDEPENDENT CLAIM 21

(a) Preamble

Claim 21's preamble recites "[a] memory device." Ex. 1001, 8:37. Petitioner contends that Tachibana "discloses a BiCMOS memory" that "is a memory device." Pet. 84 (citing Ex. 1005, 117, Fig. 10); *see* Ex. 1003, A1–A3, A47. Patent Owner does not make any arguments specific to claim 21's preamble. *See, e.g.*, Resp. 28–54.

Based on Tachibana's disclosure, we agree with Petitioner that Tachibana's BiCMOS memory corresponds to "[a] memory device" according to claim 21's preamble. Ex. 1005, 117, Fig. 10; *see* Ex. 1003 ¶ 79, A1–A3, A47.

(b) Bit Cell Array

Claim 21 recites a "bit cell array." Ex. 1001, 8:38. For the claimed "bit cell array," Petitioner identifies memory cell array 606 in Tachibana's Figure 10. Pet. 84; *see* Ex. 1003, A47. Patent Owner does not make any arguments specific to this limitation. *See, e.g.*, Resp. 28–54.

Tachibana's Figure 10 illustrates "the overall configuration of a BiCMOS memory" that includes, among other circuit elements, memory cell array 606, sense amp 607, and output buffer circuit 608 providing an output signal at output terminal 23. Ex. 1005, 117, Fig. 10; *see* Ex. 1003 ¶ 79, A1–A3, A47–A48.

Based on Tachibana's disclosure, we agree with Petitioner that Tachibana satisfies claim 21's requirement for a "bit cell array." Ex. 1005, 117, Fig. 10; *see* Ex. 1003 ¶ 79, A1–A3, A47.

(c) Amplifier Module

Claim 21 recites “an amplifier module responsive to the bit cell array.” Ex. 1001, 8:39. For the claimed “amplifier module,” Petitioner identifies sense amp 607 in Figure 10. Pet. 84–85; *see* Ex. 1003, A47–A48. Patent Owner does not make any arguments specific to this limitation. *See, e.g.*, Resp. 28–54.

As discussed above, Tachibana discloses that the BiCMOS memory includes sense amp 607. Ex. 1005, 117, Fig. 10; *see* Ex. 1003, A47–48. Dr. Baker explains that “a sense amplifier senses the signals from the bit lines of a memory array and amplifies them to recognizable logic levels.” Ex. 1003, A48 (citing Ex. 1025, 413). He also explains that sense amp 607 “receives input from the memory cell array 606 (*i.e.*, bit cell array)” and “is an amplifier module responsive to the bit cell array.” *Id.*

Based on Tachibana’s disclosure and Dr. Baker’s explanation, we agree with Petitioner that Tachibana satisfies claim 21’s requirement for “an amplifier module responsive to the bit cell array.” Ex. 1005, 117, Fig. 10; *see* Ex. 1003 ¶ 79, A1–A3, A47–A48.

(d) Output Stage

Claim 21 recites “an output stage responsive to the amplifier module.” Ex. 1001, 8:40. For the claimed “output stage,” Petitioner identifies output buffer circuit 608 in Figure 10. Pet. 85; *see* Ex. 1003, A48. Petitioner asserts that “Tachibana discloses that output buffer circuit 608 is the output buffer circuit of Figure 1” and that “Tachibana also discloses that Figures 15 and 17 are circuits that provide ‘the same operation as’ the circuit in Figure 1.” Pet. 85 (quoting Ex. 1005, 119–20); *see* Ex. 1003, A48. Patent

Owner does not make any arguments specific to this limitation. *See, e.g.,* Resp. 28–54.

As discussed above, Tachibana discloses that the BiCMOS memory includes output buffer circuit 608. Ex. 1005, 117, Fig. 10; *see* Ex. 1003, A47–48. Dr. Baker explains that output buffer circuit 608 “receives input from the sense amp 607 (*i.e.*, amplifier module)” and “is an output stage responsive to the amplifier module.” Ex. 1003, A48.

In addition, Tachibana discloses that output buffer circuit 608 in Figure 10 uses the Figure 1 embodiment of an output buffer circuit. Ex. 1005, A117; *see* Ex. 1003, A47. Tachibana states that the Figure 15 embodiment “achieves the same operation” as the Figure 1 embodiment. Ex. 1005, 119; *see* Ex. 2001 ¶¶ 62, 79. Similarly, Tachibana states that the Figure 17 embodiment “realizes the same operations” as the Figure 1 and 15 embodiments. Ex. 1005, 120; *see* Ex. 2001 ¶¶ 62, 83.

Based on Tachibana’s disclosure and Dr. Baker’s explanation, we agree with Petitioner that Tachibana satisfies claim 21’s requirement for “an output stage responsive to the amplifier module.” Ex. 1005, 117, 119–20, Fig. 10; *see* Ex. 1003 ¶ 79, A1–A3, A48.

(i) Output Stage Comprising a Differential Amplifier

Claim 21 requires an “output stage” comprising “a differential amplifier responsive to a clock signal.” Ex. 1001, 8:40–42. Petitioner asserts that Tachibana discloses a “differential amplifier” according to claim 21 for the same reasons that Tachibana discloses a “differential amplifier” according to claim 1. Pet. 86; *see* Ex. 1003, A7–A14, A48. Further, for each of Figures 15 and 17, Petitioner asserts that “the level of

the signal on terminal 19 affects the level of” the differential amplifier’s two output signals. Pet. 86; *see* Ex. 1003, A7–A14, A48.

As discussed above for claim 14, Patent Owner asserts that Petitioner has not shouldered its burden to show that the differential amplifiers in Figures 15 and 17 “amplify a differential input in response to a clock signal.” Resp. 53–54.

We disagree with Patent Owner for the reasons discussed above for claim 14. Further, for the reasons discussed above for claims 1 and 14, we agree with Petitioner that the Figure 15 and 17 embodiments each include “a differential amplifier responsive to a clock signal” as required by claim 21. *See supra* §§ III.B.3(c), III.B.11(b); Ex. 1003, A7–A14, A44–A45, A48; Ex. 1005, 119–20, Figs. 15, 17; *see also supra* § III.B.4(a) (construction of “clock signal”).

(ii) Output Stage Comprising a High Impedance Control Circuit

Claim 21 requires an “output stage” comprising “a high impedance control circuit.” Ex. 1001, 8:43. Petitioner asserts that Tachibana discloses a “high impedance control circuit” according to claim 21 for the same reasons that Tachibana discloses an “impedance control circuit” according to claim 1. Pet. 86–87 & n.9; *see* Ex. 1003, A14–A19 & n.1, A48. Petitioner contends that “[t]his impedance control circuit is a *high* impedance control circuit because Tachibana discloses that” PMOS transistor 412 “serves to set the impedance of” the differential amplifier’s output terminal 62 “to high impedance in the data held state.” Pet. 87 (citing Ex. 1005, 112). Patent Owner does not make any arguments distinguishing between a “high impedance control circuit” according to claim 21 and an “impedance control circuit” according to claim 1. *See, e.g.*, Resp. 28–54.

For the reasons discussed above for claim 1, we agree with Petitioner that the Figure 15 and 17 embodiments each include “a high impedance control circuit” as required by claim 21. *See supra* § III.B.3(d); Ex. 1003, A14–A19 & n.1, A48; Ex. 1005, 119–20, Figs. 15, 17.

(iii) Output Stage Comprising a Level Converter

Claim 21 requires an “output stage” comprising “a level converter responsive to the differential amplifier and responsive to the high impedance control circuit.” Ex. 1001, 8:44–45. Petitioner asserts that Tachibana discloses a “level converter” according to claim 21 for the same reasons that Tachibana discloses a “level converter” according to claim 1. Pet. 87; *see* Ex. 1003, A19–A25 & nn.2–3, A48–A49. Patent Owner does not make any arguments specific to this limitation. *See, e.g.*, Resp. 28–42.

For the reasons discussed above for claim 1, we agree with Petitioner that the Figure 15 and 17 embodiments each include “a level converter responsive to the differential amplifier and responsive to the high impedance control circuit” as required by claim 21. *See supra* § III.B.3(e); Ex. 1003, A19–A25 & nn.2–3, A48–A49; Ex. 1005, 119–20, Figs. 15, 17.

(iv) Output Stage Comprising a Clock-Free Latch

Claim 21 requires an “output stage” comprising “a clock-free latch responsive to the level converter.” Ex. 1001, 8:47. Petitioner asserts that Tachibana discloses a “clock-free latch” according to claim 21 for the same reasons that Tachibana discloses a “clock-free latch” according to claim 1. Pet. 87; *see* Ex. 1003, A25–A29, A49. Patent Owner does not make any arguments specific to this limitation. *See, e.g.*, Resp. 28–54.

For the reasons discussed above for claim 1, we agree with Petitioner that the Figure 15 and 17 embodiments each include “a clock-free latch

responsive to the level converter” as required by claim 21. *See supra* § III.B.3(f); Ex. 1003 ¶¶ 59, 61, A25–A29, A49; Ex. 1005, 119–20, Figs. 15, 17.

(e) Whether Tachibana Anticipates Claim 21

As explained above, Petitioner has shown by a preponderance of the evidence that Tachibana discloses every element of claim 21 arranged as required by the claim. Hence, Petitioner has shown by a preponderance of the evidence that claim 21 is unpatentable under § 102(b) as anticipated by Tachibana.

*C. Obviousness over Tachibana in View of an  
Ordinarily Skilled Artisan’s Knowledge: Claims 4–7*

1. OBVIOUSNESS UNDER 35 U.S.C. § 103

A patent may not be obtained “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). An obviousness analysis involves underlying factual inquiries including (1) the scope and content of the prior art; (2) differences between the claimed invention and the prior art; (3) the level of ordinary skill in the art; and (4) where in evidence, objective evidence of nonobviousness, such as commercial success, long-felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 35–36 (1966); *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1047–48 (Fed. Cir. 2016) (en banc). We analyze the obviousness issues accordingly.

## 2. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner asserts that a person of ordinary skill in the art would have had “at least a Bachelor of Science degree in electrical engineering or a closely related field, along with at least 4-5 years of experience in the design of integrated circuits.” Pet. 21 (citing Ex. 1003 ¶¶ 26–30); *see* Ex. 1003 ¶ 28. Petitioner also asserts that an “individual with an advanced degree in a relevant field would require less experience in the design of integrated circuits.” Pet. 21; *see* Ex. 1003 ¶ 28. Patent Owner states that “[f]or purposes of this proceeding,” it “is not challenging Petitioner’s proposed definition of” a person of ordinary skill in the art. Resp. 27; *see* Ex. 2001 ¶ 26. Thus, we adopt Petitioner’s proposed definition as consistent with the ’274 patent and the asserted prior art.

## 3. DEPENDENT CLAIM 4

Claim 4 depends from claim 1 and specifies that “the timing circuit receives a clock signal.” Ex. 1001, 7:8–9. Petitioner contends that it would have been obvious to an ordinarily skilled artisan “to adapt Tachibana’s timing circuit to receive a clock signal” according to claim 4. Pet. 88–90, 96–97; *see* Ex. 1003 ¶¶ 69–75, B1–B2. Patent Owner does not make any arguments specific to claim 4. *See, e.g.*, Resp. 28–54.

Dr. Baker explains that prior-art memory devices included synchronous devices, e.g., a self-timed random-access memory (“STRAM”), and asynchronous devices, e.g., as disclosed in Tachibana. Ex. 1003 ¶¶ 70–71, 73–74, 80 (citing Ex. 1015, 4:9–28, 6:59–7:66, Figs. 4–5, 8–11; Ex. 1016, 1:61–2:20, 4:12–49, 5:31–6:44, Figs. 1, 3–11; Ex. 1017, code (57), 3:36–5:15, Figs. 1–6; Ex. 1018, Figs. 1–2, 23, 25, 32, 34, 36, 40–44, 48–50, 53–60, 65, 67–74, 77–79, 81–93). In synchronous devices, “a clock

signal used as a synchronizing signal” controls the “input and output of signals.” Ex. 1003 ¶ 70 (quoting Ex. 1014, 2:60–64); *see* Ex. 1014, 2:54–64. In Tachibana’s asynchronous device, “internal signals are generated based on the line address signal,” a write-enable signal, and a chip-select signal. Ex. 1003 ¶ 80, A29–A30 & n.4; *see* Ex. 1005, 116–17, Figs. 6–10.

Dr. Baker identifies speed as an advantage that synchronous devices had over asynchronous devices. Ex. 1003 ¶ 71. In particular, he explains that “synchronous devices time all of their control signals to the edges of the system clock, whereas asynchronous devices could experience internal timing delays as the various internal signals and inputs are established.” *Id.* In addition, he quotes Tachibana’s explanation that “if there is a standard clock, for instance in the case of STRAM [self-timed random-access memory], it goes without saying that a control signal can easily be generated from the standard clock.” *Id.* ¶¶ 70, 75, B1 (quoting Ex. 1005, 117); *see* Ex. 1005, 117.

Dr. Baker describes Tachibana’s explanation about using a standard clock as an “express teaching, suggestion, or motivation” to use a standard clock with Tachibana’s timing circuit, i.e., the circuit in Figures 8 and 9. Ex. 1003 ¶ 72. Based on Tachibana’s explanation about using a standard clock, he states that an ordinarily skilled artisan “would have been motivated to adapt Tachibana’s output buffer circuit for use with” a synchronous device “by having the timing circuit accept a clock signal” from a standard clock “to attain the speed benefits” available with synchronous devices. *Id.*; *see id.* ¶ 69.

Thus, Petitioner identifies a reason that would have prompted an ordinarily skilled artisan to modify Tachibana’s timing circuit to receive

a clock signal from a standard clock. See Pet. 88–90, 96–98 (citing Ex. 1003 ¶¶ 70–75, B1–B2; Ex. 1005, 116–17, Figs. 8–10). By modifying Tachibana’s timing circuit to receive a clock signal from a standard clock, an ordinarily skilled artisan would have produced an apparatus according to claim 4. Thus, claim 4’s subject matter would have been obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 4 is unpatentable under § 103(a) as obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge.

#### 4. DEPENDENT CLAIM 5

Claim 5 depends from claim 4 and specifies that “the clock-free latch performs a latching function in response to the level converter providing a modified impedance output.” Ex. 1001, 7:10–12. Petitioner contends that “the latch in Figures 15 and 17 . . . performs its latching function solely in response to the output of” the ECL-MOS level-conversion circuit. Pet. 91; see Ex. 1003, B2. Petitioner also contends that the latch preserves a previously read value until the ECL-MOS level-conversion circuit becomes operational and passes a “new output value from the differential amplifier to” the latch. Pet. 91–94; see Ex. 1003, B2–B6; Ex. 1005, 110–14, 119–20. Patent Owner does not make any arguments specific to claim 5. See, e.g., Resp. 28–54.

Dr. Baker explains that the latch in Figures 15 and 17 “is only responsive to the output of the” the ECL-MOS level-conversion circuit. Ex. 1003, B2; see *id.* at A25–A29. He also explains that the signal at terminal 19 “controls current flow to” the ECL-MOS level-conversion circuit. *Id.* at B2–B4. In particular, a high level (logic “1”) at terminal 19

activates the ECL-MOS level-conversion circuit and causes it to pass a “new output value from the differential amplifier to” the latch. *Id.* at B5; *see* Ex. 1005, 113. Transitioning to a low level (logic “0”) at terminal 19 deactivates the ECL-MOS level-conversion circuit and places it in “a high impedance state.” Ex. 1003, B5; *see* Ex. 1005, 111–12. As a result, the ECL-MOS level-conversion circuit provides “a modified impedance output.” Ex. 1003, B5. In “a high impedance state,” the ECL-MOS level-conversion circuit “does not output a new value into the latch,” and the latch “continues to preserve the previously read value (*i.e.*, perform[s] the latching function).” *Id.*; *see id.* ¶¶ 56–57.

For the reasons explained by Dr. Baker, in Figures 15 and 17 “the clock-free latch performs a latching function in response to the level converter providing a modified impedance output” as required by claim 5. *See* Ex. 1003, A25–A29, B2–B6; Ex. 1005, 119–20, Figs. 15, 17. Thus, claim 5’s subject matter would have been obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 5 is unpatentable under § 103(a) as obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge.

#### 5. DEPENDENT CLAIM 6

Claim 6 depends from claim 5 and specifies that “the level converter produces the modified impedance output in response to the clock signal.” Ex. 1001, 7:13–15. Petitioner asserts that the ECL-MOS level-conversion circuits in Figures 15 and 17 produce a modified impedance output in response to the signal at terminal 19. Pet. 91–94; *see* Ex. 1003, B2–B9. In addition, Petitioner contends that Tachibana’s timing circuit generates the

signal at terminal 19. Pet. 94–95; *see* Ex. 1003, B1, B8–B9. Petitioner also contends that an ordinarily skilled artisan would have been motivated to modify Tachibana’s timing circuit to receive a clock signal from a standard clock. Pet. 94; *see* Ex. 1003 ¶¶ 70–72, B1–B2. Patent Owner does not make any arguments specific to claim 6. *See, e.g.*, Resp. 28–54.

Dr. Baker explains that the ECL-MOS level-conversion circuits in Figures 15 and 17 “are controlled by, thus responsive to,” the signal at terminal 19 generated by Tachibana’s timing circuit. Ex. 1003, B6–B9. As discussed above for claim 4, he also explains that an ordinarily skilled artisan would have been motivated to modify Tachibana’s timing circuit to receive a clock signal from a standard clock. *See id.* ¶¶ 69–72, B1–B2.

For the reasons explained by Dr. Baker, claim 6’s subject matter would have been obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge. Hence, Petitioner has shown by a preponderance of the evidence that claim 6 is unpatentable under § 103(a) as obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge.

#### 6. DEPENDENT CLAIM 7

Claim 7 depends from claim 6 and specifies that “the level converter produces the modified impedance output when first and second outputs of the differential amplifier have substantially the same voltage level indicating a modified impedance condition.” Ex. 1001, 7:16–20. Petitioner asserts that the ECL-MOS level-conversion circuits in Figures 15 and 17 enter “the high impedance state” with a low level (logic “0”) at terminal 19 and, as a result, the related differential amplifier’s two output signals “both have the ground voltage level.” Pet. 95–96; *see* Ex. 1003, B9–B12. Patent Owner does not make any arguments specific to claim 7. *See, e.g.*, Resp. 28–54.

Dr. Baker explains how a low level (logic “0”) at terminal 19 affects the ECL-MOS level-conversion circuits and differential amplifiers in Figures 15 and 17. Ex. 1003, B9–B12. Specifically, with a low level (logic “0”) at terminal 19, the ECL-MOS level-conversion circuit enters “a high impedance state.” *Id.* at B9. In addition, “the differential amplifier is deactivated,” and it “outputs a high impedance.” *Id.* at B9, B12. When deactivated, the differential amplifier’s two outputs “have substantially the same voltage level (*i.e.*, the ground level).” *Id.* at B9.

For the reasons explained by Dr. Baker, in Figures 15 and 17 “the level converter produces the modified impedance output when first and second outputs of the differential amplifier have substantially the same voltage level indicating a modified impedance condition” as required by claim 7. *See* Ex. 1003, B9–B12; Ex. 1005, 119–20, Figs. 15, 17. Thus, claim 7’s subject matter would have been obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge.

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 7 is unpatentable under § 103(a) as obvious over Tachibana in view of an ordinarily skilled artisan’s knowledge.

*D. Obviousness over Tachibana and Hanamura: Claims 22 and 23*

1. OBVIOUSNESS: COMBINING REFERENCES

When evaluating a combination of references, an obviousness analysis should address “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Further, “mere conclusory statements” do not suffice for an apparent reason to combine. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Instead, an obviousness challenge

resting on a combination of references requires “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *Kahn*, 441 F.3d at 988). We analyze the obviousness issues accordingly.

## 2. OVERVIEW OF HANAMURA (Ex. 1006)

Hanamura describes a semiconductor memory with a plurality of output buffer circuits providing a plurality of output signals at a plurality of output terminals. Ex. 1006, 3:46–48, 4:1–9, 5:25–45, Fig. 1; Ex. 1003 ¶ 63. Hanamura’s Figure 1 is reproduced below:

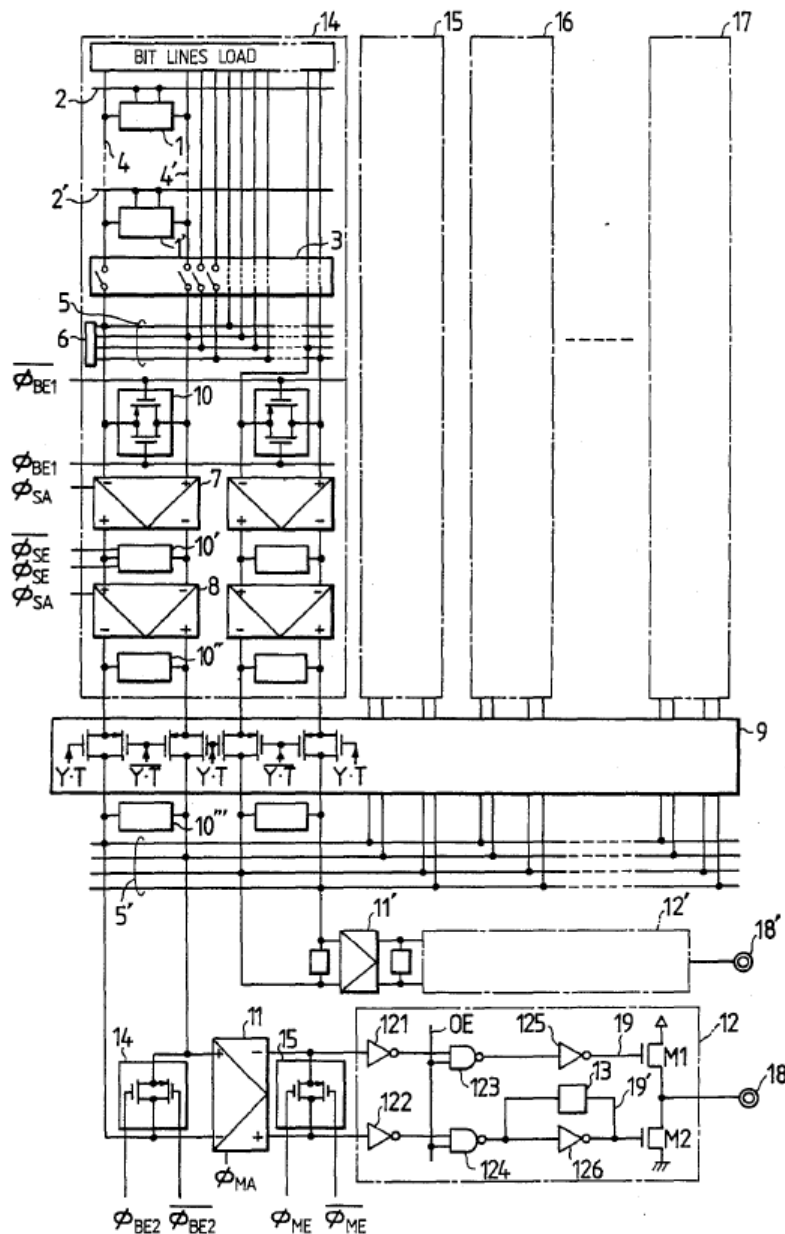


Figure 1 illustrates adjacent memory arrays 14, 15, 16, and 17 in a semiconductor memory. Ex. 1006, 4:1–9; Ex. 1003 ¶ 63.

Each memory array includes memory cells 1 and 1' that supply signals through column switch 3 and to sense amplifiers 7 and 8. Ex. 1006, 4:1–32, Fig. 1. Sense amplifiers 7 and 8 supply signals to main amplifiers 11 and 11'. *Id.* at 4:48–5:18, Fig. 1. Main amplifiers 11 and 11' supply signals to output buffer circuits 12 and 12', respectively. *Id.* at 5:15–34, Fig. 1.

Output buffer circuits 12 and 12' supply output signals to output terminals 18 and 18', respectively. *Id.* at 5:25–45, 7:35–41, 7:60–63, Fig. 1; Ex. 1003

¶ 63. The output signals at output terminals 18 and 18' change “between a level which is approximate to a power supply voltage and a level which is approximate to a ground voltage.” Ex. 1006, 5:25–32. Although output buffer circuits 12 and 12' amplify voltage, “the main amplification function . . . is current amplification.” *Id.* at 5:32–34.

Each memory array also includes equalizing circuits, such as circuits 10 and 10', arranged at the inputs of the amplifiers located between memory cells 1 and 1' and output terminals 18 and 18'. *Id.* at code (57), 4:53–5:64, Fig. 1. A “parallel connection of a P-channel MOSFET and an N-channel MOSFET” serves as an equalizing circuit. *Id.* at 4:55–63.

The memory cells store “digital information,” i.e., a “1” (high logic level) or a “0” (low logic level). *Id.* at 2:58–62. The equalizing circuits set the inputs of the amplifiers to “an intermediate level between” the levels “1” and “0” so memory-read operations can occur “at high speed.” *Id.* at 2:62–3:6.

### 3. DEPENDENT CLAIM 22

Claim 22 depends from claim 21 and further requires “a plurality of output stages and a plurality of data outputs.” Ex. 1001, 8:48–49. Petitioner asserts that Hanamura “discloses a plurality of output stages and a plurality of data outputs.” Pet. 98; *see* Ex. 1003 ¶ 63, C1–C3. Patent Owner does not make any arguments specific to claim 22. *See, e.g.*, Resp. 28–54.

For Hanamura’s memory device, Dr. Baker explains that output buffer circuits 12 and 12' correspond to two output stages and that output terminals 18 and 18' correspond to two data outputs. Ex. 1003 ¶¶ 63, 79, C1–C3

(citing Ex. 1006, 5:25–40, Fig. 1); *see* Ex. 1006, 5:25–45, 7:35–41, 7:60–63, Fig. 1.

Further, as discussed above for claim 21, Tachibana’s Figure 10 illustrates “the overall configuration of a BiCMOS memory” with one output stage and one data output, i.e., at output terminal 23. Ex. 1005, 117, 124, Fig. 10; *see* Ex. 1003, A47–A48. Petitioner asserts that an ordinarily skilled artisan would have combined Hanamura’s teachings about multiple output stages and multiple data outputs with Tachibana’s teachings because the “combination would allow faster memory accesses, which was generally recognized as a benefit for memory systems.” Pet. 102 (citing Ex. 1019, 84); *see* Ex. 1003 ¶¶ 76–78; Ex. 1019, 84. In particular, Petitioner contends that with multiple output stages, some output stages “could continue to latch the most recently read data value from” some memory cells, while other output stages “actively read[] out data stored in” other memory cells. *See* Pet. 102; Ex. 1003 ¶¶ 77–78.

Dr. Baker describes “[f]aster access times” as “a benefit for memory systems.” Ex. 1003 ¶ 77. He states that “having two output stages and two data outputs increases access speed relative to the same device with only one output stage and one data output by keeping twice as many latched values available for readout.” *Id.* ¶ 78. Referencing Hanamura’s Figure 1, he explains that output stage 12 “could continue to latch the most recently read data value from” one memory cell, while output stage 12’ “actively read[s] out data stored in” another memory cell. *Id.* He also explains that “[a]s a result, the data latched in output stage 12 remains available for immediate output on data output 18, without the need for a new read from” the associated memory cell. *Id.*

Thus, Petitioner identifies a reason that would have prompted an ordinarily skilled artisan to combine Hanamura's teachings with Tachibana's teachings to achieve claim 22's subject matter. *See* Pet. 102–04 (citing Ex. 1003 ¶¶ 77–83; Ex. 1005, Fig. 10; Ex. 1006, Fig. 1; Ex. 1019, 84; Ex. 1020, Figs. 1–3; Ex. 1021, Fig. 25).

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 22 is unpatentable under § 103(a) as obvious over Tachibana and Hanamura.

#### 4. DEPENDENT CLAIM 23

Claim 23 depends from claim 22 and further requires “a bit line load array coupling the bit cell array and the amplifier module.” Ex. 1001, 8:50–52. For the claimed “bit line load array,” Petitioner identifies data line load MOS transistor 618 in Tachibana's Figure 10. Pet. 100; *see* Ex. 1003, C3–C5. Petitioner contends that Figure 10 depicts MOS transistor 618 coupled to memory cell array 606 in the BiCMOS memory. Pet. 100; *see* Ex. 1003, C3–C5; Ex. 1005, 117, Fig. 10. Petitioner asserts that “it would have been obvious” to an ordinarily skilled artisan to couple MOS transistor 618 between memory cell array 606 and sense amp 607 based on Hanamura's teachings. Pet. 101, 104–06; *see* Ex. 1003 ¶¶ 84–90, C5–C6. Patent Owner does not make any arguments specific to claim 23. *See, e.g.*, Resp. 28–54.

Dr. Baker discusses the “widespread and commonplace” practice of precharging, i.e., “setting the potential of the bit lines to a predetermined, intermediate level between the high and low logic levels.” Ex. 1003 ¶¶ 85–86, 89 (citing Ex. 1019, 172, 174, 215, 219, 221, 223, 233, 248, 249, 259, 269, 285, 340, 394, 397, 401, 405, 413, 415, 446, 466, 519, 549;

Ex. 1022, code (57), 1:5–40; Ex. 1023, 1:48–59; Ex. 1024, code (57), 5:35–62, 7:48–54, Fig. 6). He explains that precharging “speeds up memory accesses by avoiding the need to change the potential of the bit lines by a large amount when reading a logic ‘1’ immediately after reading a logic ‘0’ or vice versa.” *Id.* ¶ 85. He states that an ordinarily skilled artisan would have understood that Tachibana’s data line load MOS transistor 618 corresponds to structure “enabl[ing] precharging of the bit lines.” *Id.* ¶¶ 85, 90.

In addition, Dr. Baker identifies in Hanamura’s Figure 1 precharging structures coupling memory cells 1 and 1’ to sense amplifiers 7 and 8. *Id.* ¶¶ 64, 84, 86, 88–90, C5–C6; *see* Ex. 1006, Fig. 1. He states that an ordinarily skilled artisan “would have been motivated by the speed and efficiency benefits of precharging to couple the memory array and the sense amplifiers” with precharging structures arranged as in Hanamura. Ex. 1003 ¶ 87.

Thus, Petitioner identifies a reason that would have prompted an ordinarily skilled artisan to combine Hanamura’s teachings with Tachibana’s teachings to achieve claim 23’s subject matter. *See* Pet. 104–06 (citing Ex. 1003 ¶¶ 85–90; Ex. 1019, 172, 174, 215, 219, 221, 223, 233, 248, 249, 259, 269, 285, 340, 394, 397, 401, 405, 413, 415, 446, 466, 519, 549; Ex. 1022, code (57), 1:5–40; Ex. 1023, 1:48–59; Ex. 1024, code (57), 5:35–62, 7:48–54, Fig. 6).

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claim 23 is unpatentable under § 103(a) as obvious over Tachibana and Hanamura.

#### IV. CONCLUSION

Based on the evidence presented with the Petition, the evidence introduced during the trial, and the parties' respective arguments, Petitioner has shown by a preponderance of the evidence that (1) claims 1, 3, 8, 9, 11, 12, 14–16, 20, and 21 are unpatentable under § 102(b) as anticipated by Tachibana; (2) claims 4–7 are unpatentable under § 103(a) as obvious over Tachibana in view of an ordinarily skilled artisan's knowledge; and (3) claims 22 and 23 are unpatentable under § 103(a) as obvious over Tachibana and Hanamura.<sup>4</sup> But Petitioner has not shown by a preponderance of the evidence that claims 2 and 10 are unpatentable under § 102(b) as anticipated by Tachibana.

In summary:

| <b>Claims</b>                  | <b>35 U.S.C. §</b> | <b>Reference(s)/<br/>Basis</b> | <b>Claims<br/>Shown<br/>Unpatentable</b> | <b>Claims Not<br/>Shown<br/>Unpatentable</b> |
|--------------------------------|--------------------|--------------------------------|------------------------------------------|----------------------------------------------|
| 1–3, 8–12,<br>14–16,<br>20, 21 | 102(b)             | Tachibana                      | 1, 3, 8, 9, 11,<br>12, 14–16,<br>20, 21  | 2, 10                                        |
| 4–7                            | 103(a)             | Tachibana                      | 4–7                                      |                                              |
| 22, 23                         | 103(a)             | Tachibana,<br>Hanamura         | 22, 23                                   |                                              |

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<sup>4</sup> Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding after the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

| <b>Claims</b>              | <b>35 U.S.C. §</b> | <b>Reference(s)/<br/>Basis</b> | <b>Claims<br/>Shown<br/>Unpatentable</b> | <b>Claims Not<br/>Shown<br/>Unpatentable</b> |
|----------------------------|--------------------|--------------------------------|------------------------------------------|----------------------------------------------|
| <b>Overall<br/>Outcome</b> |                    |                                | 1, 3–9, 11,<br>12, 14–16,<br>20–23       | 2, 10                                        |

#### V. ORDER

Accordingly, it is

ORDERED that claims 1, 3–9, 11, 12, 14–16, and 20–23 of the '274 patent are determined to be unpatentable;

ORDERED that claims 2 and 10 of the '274 patent are not determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 5,943,274

PETITIONER:

Jeremy Jason Lang  
Jared Bobrow  
Christopher J. Siebens  
K. Patrick Herman  
ORRICK, HERRINGTON & SUTCLIFFE LLP  
PTABDocketJJL2@orrick.com  
PTABDocketJ3B3@orrick.com  
29CPTABDocket@orrick.com  
P52PTABDocket@orrick.com

PATENT OWNER:

Philip E. Levy  
Edward C. Flynn  
Robert W. Morris  
ECKERT SEAMANS CHERIN & MELLOTT, LLC  
plevy@eckertseamans.com  
eflynn@eckertseamans.com  
rwmorris@eckertseamans.com