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Paper 32
Date: February 4, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

Case IPR2018-01035
Patent 7,268,588 B2

Before ROBERT J. WEINSCHENK, MINN CHUNG, and KIMBERLY McGRAW, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Intel Corporation ("Petitioner") challenges the patentability of claims 1, 2, 4, and 17 (the "challenged claims") of U.S. Patent No. 7,268,588 B2 (Ex. 1001, "the '588 patent"), owned by VLSI Technology LLC ("Patent Owner"). This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1, 2, 4, and 17 of the '588 patent are unpatentable.

II. BACKGROUND

A. Procedural History

On June 4, 2018, Petitioner filed a Petition (Paper 3, "Pet.") requesting *inter partes* review of claims 1, 2, 4, and 17 of the '588 patent. Patent Owner filed a Preliminary Response (Paper 7, "Prelim. Resp."). On February 5, 2019, we instituted an *inter partes* review of all challenged claims of the '588 patent based on all the grounds presented in the Petition. Paper 6 ("Dec. on Inst."), 40.

After institution, Patent Owner filed a Patent Owner Response (Paper 16, "PO Resp."), Petitioner filed a Reply to Patent Owner Response (Paper 18, "Reply"), and Patent Owner filed a Sur-reply (Paper 22, "Sur-reply"). An oral hearing was held on October 30, 2019, and a copy of the hearing transcript has been entered into the record. Paper 31 ("Tr.").

B. Related Matters

According to the parties, the '588 patent is the subject of the following district court litigation: *VLSI Technology LLC v. Intel*

Corporation, No. 5:17-cv-05671 (N.D. Cal. Oct. 2, 2017). Pet. 1–2; Paper 5, 2.

C. The '588 Patent

The '588 patent describes a level shifter circuit comprising a first circuit, a second circuit, and a protection layer. Ex. 1001, code (57). The '588 patent describes that the first circuit, upon receiving an input signal, switches first and second nodes to opposite states within a first voltage range. *Id.* In response to the switching of the first and second nodes, the second circuit switches third and fourth nodes to opposite states within a second voltage range. *Id.* The protection layer couples the first circuit to the second circuit via isolation paths, which keep the voltages at the first and second nodes within the first voltage range and the voltages at the third and fourth nodes within the second voltage range. *Id.* According to the '588 patent, such isolation allows using thin gate-oxide devices for speed in a circuit while extending the voltage range of the circuit beyond the maximum voltage permissible for any individual thin gate-oxide device used in the circuit. *Id.*

Figure 1 of the '588 patent is reproduced below.

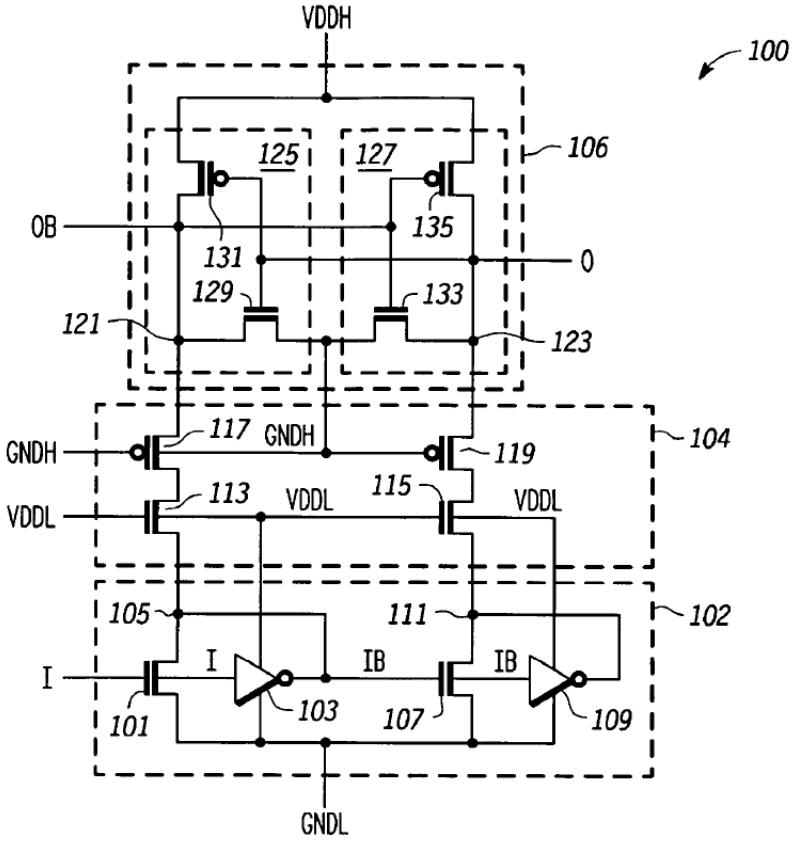


FIG. 1

Figure 1 is a schematic diagram of an exemplary up-shift circuit. *Id.* at 2:51–53.

As shown in Figure 1, up-shift circuit 100 comprises lower input circuit 102 coupled to protection layer 104, which, in turn, is coupled to upper output circuit 106. *Id.* at 2:53–55. As also shown in Figure 1, lower input circuit 102 comprises N-channel transistors 101 and 107 and inverters 103 and 109. *Id.* at 2:56–63, Fig. 1. The output of inverter 103 is coupled to node 105, which is, in turn, coupled to the drain of N-channel transistor 101. *Id.* at 2:60–61. Similarly, the output of inverter 109 is coupled to node 111, which, in turn, is coupled to the drain of N-channel transistor 107. *Id.* at

3:2–3. The output of inverter 103 is also coupled to the gate of N-channel transistor 107 and the input of inverter 109. *Id.* at 2:60–63.

As depicted in Figure 1, protection layer 104 comprises N-channel transistors 113 and 115 and P-channel transistors 117 and 119. *Id.* at 3:4–10, Fig. 1. The '588 patent describes that N-channel transistors 113 and 115 are coupled to P-channel transistors 117 and 119, respectively, such that the drain of each N-channel transistor (i.e., transistor 113 or 115) is tied to the drain of its paired P-channel transistor (i.e., transistor 117 or 119, respectively). *Id.* at 3:8–10. The sources of P-channel transistors 117 and 119 are coupled to nodes 121 and 123, respectively, of upper circuit 106. *Id.* at 3:10–13.

According to the '588 patent, because a voltage of VDDL is applied to the gates of N-channel transistors 113 and 115, protection layer 104 prevents the voltage of lower circuit 102 (e.g., the voltages at nodes 105 and 111) from exceeding VDDL. *Id.* at 4:36–38. P-channel transistors 117 and 119, on the other hand, receive a voltage of GNDH at their gates, which prevents the voltage of upper circuit 106 (e.g., the voltages at nodes 121 and 123) from falling below GNDH. *Id.* at 4:38–41.

The '588 patent describes that upper circuit 106 includes a pair of crossed-coupled inverters 125 and 127 such that the output of one inverter is coupled or tied to the input of the other inverter in the pair and vice versa. *Id.* at 3:21–34. The outputs of inverters 125 and 127 are coupled to nodes 121 and 123, respectively. *Id.* at 3:22–27.

Regarding the operation of up-shift circuit 100, the '588 patent describes that an input signal I is provided to the gate of N-channel transistor 101 and to the input of inverter 103 at lower input circuit 102. *Id.* at 2:56–

58, Fig. 1. According to the '588 patent, the output signal O of up-shift circuit 100 is the signal (or the voltage) at node 123 of upper output circuit 106. *Id.* at 3:28–31, Fig. 1.

The '588 patent describes that, in operation of up-shift circuit 100, the input signal I switches between GNDL and a voltage level at or near VDDL. *Id.* at 3:39–41. When the input signal I is low (i.e., at the voltage level of GNDL), the '588 patent describes that transistors 101 and 107 and inverters 103 and 109 operate such that node 105 is pulled high (i.e., at the voltage level of VDDL) and node 111 is pulled low (i.e., at the voltage level of GNDL). *Id.* at 3:42–46. According to the '588 patent, this in turn causes the transistors in protection layer 104 (with VDDL applied to the gates of transistors 113 and 115 and GNDH applied to the gates of transistors 117 and 119) and the transistors in upper output circuit 106 (with the sources of transistors 129 and 133 coupled together at GNDH and the sources of transistors 131 and 135 coupled together at VDDH) to operate in such a way that node 121 is high at VDDH and node 123 is low at GNDH. *Id.* at 3:54–65. Thus, when the input signal I is low at GNDL, the output signal O (at node 123) is low at the voltage level of GNDH. *Id.* at 3:64–66.

When the input signal I is high at VDDL, the '588 patent describes that node 105 is pulled low at GNDL and node 111 is pulled high at VDDL, which causes node 121 pulled low at GNDH and node 123 (and the output signal O) pulled high at VDDH. *Id.* at 4:1–20. Thus, when the input signal I switches from GNDL to VDDL, the output signal O is switched from GNDH to VDDH. *Id.* at 4:15–20.

In summary, the '588 patent describes that up-shift circuit 100 operates responsive to the input signal I to switch nodes 105 and 111 to

opposite states within the lower voltage range of GNDL to VDDL, which causes nodes 121 and 123, responsive to the switching of nodes 105 and 111, to switch to opposite states within the upper voltage range of GNDH to VDDH. *Id.* at 4:20–26.

In an embodiment, all of the transistors and the inverters of up-shift circuit 100 are or made of smaller thin-gate devices. *Id.* at 4:27–46. As used in the context of the '588 patent, the term "thin-gate" refers to thin gate-oxide devices that are suitable for lower voltage ranges but are likely to break down if exposed to higher voltage levels. *Id.* at 1:33–35. According to the '588 patent, thin-gate devices (such as 90-nm CMOS devices) are relatively fast but unable to withstand higher voltage levels, such as a range greater than 1.5 volts. *Id.* at 4:29–31, 1:19–26.

In an embodiment, the voltage difference or range of GNDL to VDDL is sufficiently large to enable the switching of the thin-gate devices but sufficiently small to protect each thin-gate device of lower circuit 102 from being exposed to excessive voltage levels. *Id.* at 4:31–35. Similarly, the voltage range of GNDH to VDDH in upper circuit 106 is sufficiently large to enable the switching of the thin-gate devices but sufficiently small to protect each thin-gate device of upper circuit 106 from being exposed to excessive voltage levels. *Id.* at 4:41–46.

As discussed above, protection layer 104 prevents the voltage of lower circuit 102 from exceeding VDDL and the voltage of upper circuit 106 from falling below GNDH, thereby keeping the voltage of lower circuit 102 within the voltage range of GNDL to VDDL and the voltage of upper circuit 106 within the voltage range of GNDH to VDDH. *Id.* at 4:36–41. In an embodiment, VDDH is greater than VDDL and GNDH is greater than

GDDL such that the voltage level across the entire up-shift circuit 100, i.e., GNDL to VDDH, can exceed the allowable maximum voltage of any individual thin-gate device in the circuit because none of the thin-gate devices are exposed to the entire voltage range. *Id.* at 4:46–53. In this manner, the overall switching is relatively fast while the voltage range of the entire up-shift circuit 100 is extended beyond the maximum permissible for any individual thin-gate of the up-shift circuit. *Id.* at 4:56–60, code (57).

D. Illustrative Claim

Of the challenged claims, claims 1 and 17 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below.

> 1. A level shifter circuit, comprising:
>
> a first circuit, responsive to an input signal, that switches first and second nodes to opposite states within a first voltage range between first and second supply voltages;
>
> a protection layer which couples said first and second nodes to third and fourth nodes via first and second isolation paths, respectively, wherein said first and second isolation paths keep said first and second nodes within said first voltage range and keep said third and fourth nodes within a second voltage range; and
>
> a second circuit that switches said third and fourth nodes to opposite states within said second voltage range between third and fourth supply voltages in response to switching of said first and second nodes, said second circuit comprising:
>
> a first inverter having an input coupled to said fourth node, an output coupled to said third node and supply inputs coupled between said third and fourth supply voltages; and
>
> a second inverter having an input coupled to said third node, an output coupled to said fourth node and supply inputs coupled between said third and fourth supply voltages.

Ex. 1001, 16:56–17:11.

E. Applied References and Declarations

Petitioner relies upon the following references in its challenges to patentability.

Reference and Date	Designation	Exhibit No.
U.S. Patent No. 5,440,249 (issued Aug. 8, 1995)	Schucker	1002
U.S. Patent No. 5,969,542 (issued Oct. 19, 1999)	Maley	1003

Petitioner also relies on two declarations from Patrick Chapman, Ph.D. in support of its Petition and Reply. Ex. 1004 ("the Chapman Declaration"); Ex. 1013 ("the Chapman Reply Declaration"). Patent Owner relies on the Declaration of Engin Ipek, Ph.D. (Ex. 2002, "the Ipek Declaration") in support of its Patent Owner Response.

F. Instituted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1, 2, 4, and 17 of the '588 patent on the following grounds (Pet. 3, 25–74):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 4, 17	102[1]	Schucker
2	103(a)	Schucker and Maley
2	103(a)	Schucker and the knowledge of a person of ordinary skill in the art

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the '588 patent has an effective filing date prior to the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of §§ 102 and 103.

III. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner proposes that a person of ordinary skill in the art at the time of the invention would have had at least an M.S. degree in electrical engineering and three years of experience with CMOS technology. Pet. 24. Neither Patent Owner, in its Response, nor Dr. Ipek, in his declaration, proposes a level of ordinary skill in the art. Dr. Ipek, however, states "[f]or the purposes of the subject IPR proceedings, I have been asked to employ [Petitioner's proposed] standard of a person of ordinary skill, but I do not offer the opinion that it is the correct standard." Ex. 2002 ¶ 19.

Based on the complete record, we find Petitioner's proposal consistent with the level of ordinary skill in the art reflected by the prior art of record, *see Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978), and adopt Petitioner's unopposed position as to the level of ordinary skill in the art.

B. Claim Construction

In an *inter partes* review based on a petition filed prior to November 13, 2018, claim terms in an unexpired patent are construed according to their broadest reasonable interpretation in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b) (2017);[2] *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016).

[2] A recent amendment to this rule does not apply here because the Petition was filed before November 13, 2018. *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before

Under the broadest reasonable interpretation (BRI) standard, and absent any special definitions, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art, in view of the specification. *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Petitioner does not propose express constructions for any claim terms in the Petition and asserts that the challenged claims are unpatentable under the plain meaning interpretation of the claims. Pet. 24. In its Response, Patent Owner proposes constructions for three terms—namely, "couples" recited in claim 1, "coupling" recited in claim 17, and "thin-gate oxide devices" recited in claim 2. PO Resp. 19–34.

Patent Owner asserts that the claim term "couples" recited in claim 1 should be construed to require the recited "protection layer" electrically connect the nodes of the lower circuit to the nodes of the upper circuit via both of the isolation paths, "in a push/pull function." *Id.* at 20. Patent Owner contends that to "couple," as recited in the claim, the "protection layer" must (1) conduct electricity, (2) in both isolation paths, (3) in opposite directions, and (4) at the same time. *Id.* at 3, 13, 20–25, 35–36, 42, 48; Sur-reply 5–7. Patent Owner makes similar claim construction arguments regarding the claim term "coupling" recited in claim 17. PO Resp. 27–29.

Patent Owner argues that because Schucker's protection layer "can only pull" in one isolation path while the other isolation path is "non-conductive," Schucker does not anticipate the claims. *Id.* at 20.

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the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective Nov. 13, 2018) (now codified at 37 C.F.R. pt. 42 (2019)).

Although Patent Owner's arguments raise an issue of claim construction, Patent Owner's arguments are closely related to and interspersed with Patent Owner's arguments that Schucker does not anticipate claims 1 and 17. Thus, for efficiency and completeness, we address this issue in the context of the patentability discussion below.

Turning next to the claim term "thin-gate oxide devices" recited in claim 2, in its Response, Patent Owner asserts that the claim term "thin-gate oxide devices" should be interpreted to exclude "Schucker's 3.3V-range devices" because the '588 patent defines such devices as "thick-gate" devices. PO Resp. 29. Again, although Patent Owner's argument raises an issue of claim construction, Patent Owner's argument is closely related to and interspersed with Patent Owner's arguments that Schucker in combination with Maley does not render claim 2 unpatentable. Thus, for efficiency and completeness, we also address this issue in the context of the patentability discussion below.

No other claim terms need to be construed expressly for this Final Written Decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that only terms that are in controversy need to be construed, and "only to the extent necessary to resolve the controversy"); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

C. Anticipation by Schucker

Petitioner contends that claims 1, 4, and 17 are unpatentable as anticipated by Schucker. Pet. 25–60; Reply 2–20. Petitioner provides

detailed explanations and specific citations to Schucker indicating where in the reference the claimed features are disclosed. Pet. 25–60. In addition, Petitioner relies upon the Chapman Declaration (Ex. 1004) and the Chapman Reply Declaration (Ex. 1013) to support its positions. Pet. 25–60; Reply 2–20. Patent Owner's opposition is directed to one specific claimed feature only—namely, Patent Owner asserts that Schucker does not disclose the feature of coupling by isolation paths recited in independent claims 1 and 17. PO Resp. 19–29, 35–54; Sur-reply 5–24. Patent Owner relies on the Ipek Declaration (Ex. 2002) to support its positions. *Id.* The parties also cite the deposition testimony of Dr. Chapman (Exs. 2005, 2009) and the deposition testimony of Dr. Ipek (Ex. 1012) in support of the parties' respective arguments. *See* PO Resp.; Reply; Sur-reply. Upon review of all of the parties' papers and after considering the evidence of record presented during this proceeding, for the reasons explained below, we are persuaded that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1, 4, and 17 are unpatentable under 35 U.S.C. § 102 as anticipated by Schucker.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 102 only if a single prior art reference expressly or inherently describes each and every limitation set forth in the claim. *See Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005); *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987). Further, a reference cannot anticipate "unless [it] discloses within the four corners of the document not only all of the limitations claimed[,] but also all of the limitations arranged or combined in the same way as recited in the claim." *Net MoneyIN, Inc. v. VeriSign, Inc.*,

545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged in the same way as in the claim, "the reference need not satisfy an *ipsissimis verbis* test," i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). Moreover, the prior art reference is read from the perspective of one with ordinary skill in the art. *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) ("A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention." (citation and quotation marks omitted)); *In re Preda*, 401 F.2d 825, 826 (CCPA 1968) ("[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom."). We analyze this asserted ground based on anticipation with the principles identified above in mind.

2. Overview of Schucker (Ex. 1002)

Schucker describes a voltage level translator circuit that converts an input signal ranging between first and second operating potentials to an output signal ranging between second and third operating potentials. Ex. 1002, code (57). As background, Schucker describes that voltage level translator circuits are commonly used to convert a data signal from one voltage level to another voltage level that represents the same logic state. *Id.* at 1:9–11. According to Schucker, such voltage level shifting is necessary when interfacing sub-micron MOS devices to larger or higher-micron MOS devices, which operate at higher voltage levels. *Id.* at 1:12–20.

Schucker describes that a problem occurs in such level shifting MOS transistors when they are subject to the full higher voltage across their gate oxide layer, because the submicron MOS gate oxide devices cannot handle the higher voltage stresses. *Id.* at 1:25–29. According to Schucker, a need therefore exists to translate voltage levels in submicron MOS devices without overstressing the gate oxide layers. *Id.* at 1:30–32.

Figure 1 of Schucker is reproduced below.

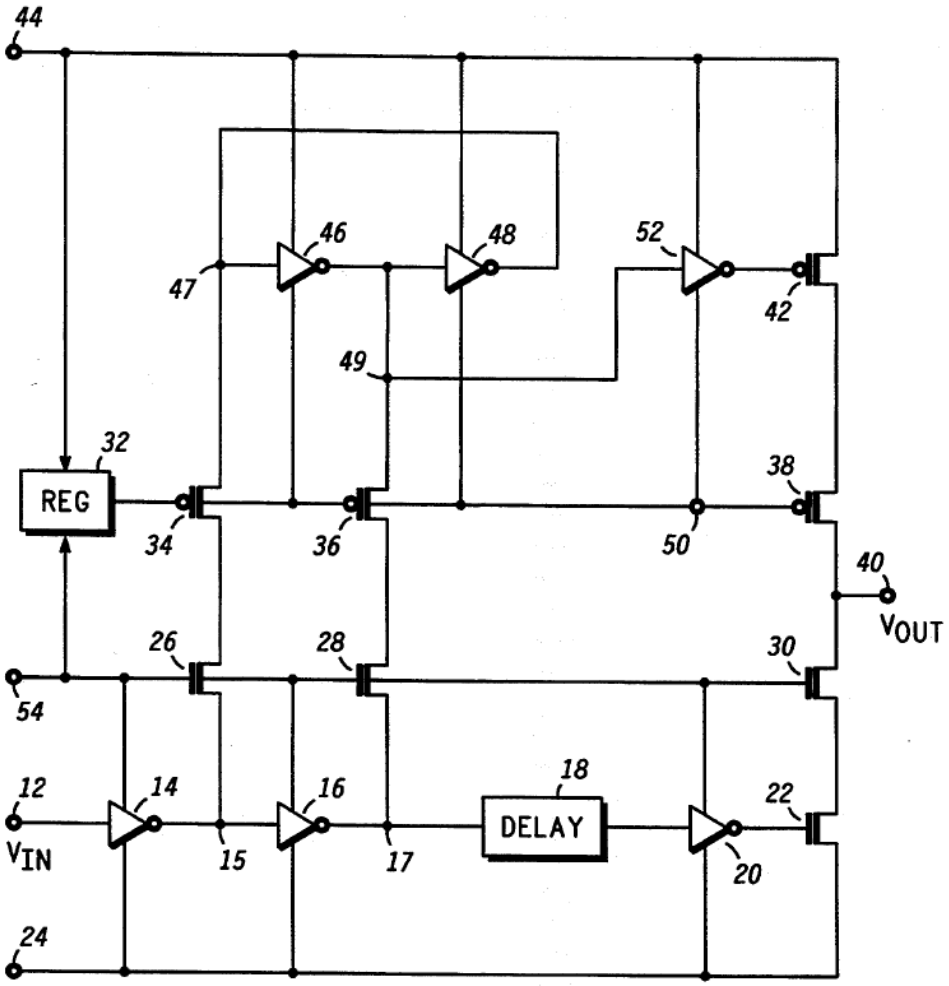


FIG. 1

Figure 1 is a schematic and block diagram illustrating a voltage level translator circuit. *Id.* at 1:35–36.

Referencing Figure 1, Schucker describes that voltage level translator circuit 10 can be used to transition from 0.5 submicron MOS technology, where a logic one (or high) is 3.3 volts, to higher micron MOS technology, where a logic one is 5.0 volts. *Id.* at 1:49–53. Starting with the input signal to voltage level translator circuit 10, Schucker describes that an input signal V_{IN} operating between 0.0 volts (for logic zero) and 3.3 volts (for logic one) is applied to the input of inverter 14. *Id.* at 1:54–56. The output of inverter 14 is coupled to node 15 and to the input to inverter 16. *Id.* at 1:56–57. The output of inverter 16 is coupled to node 17. *Id.* at 1:57–59.

As depicted in Figure 1 and described in the accompanying text, the source of N-channel transistor 26 is coupled to node 15, and the source of N-channel transistor 28 is coupled to node 17. *Id.* at 1:65–2:2. N-channel transistors 26 and 28 each have a gate commonly coupled to terminal 54 to receive a power supply potential of 3.3 volts. *Id.* at 1:65–67. A ground potential (i.e., 0.0 volts) is provided at terminal 24. *Id.* at 1:64–65.

As shown in Figure 1, P-channel transistors 34 and 36 each receive an operating potential at their gates from the output of regulator circuit 32. *Id.* at 2:9–11. According to Schucker, the output of regulator circuit 32 is at 1.7 volts, which is 3.3 volts lower than 5 volts, the power supply voltage at terminal 44. *Id.* at 2:9–16. Referencing Figure 1, Schucker describes that the drain of P-channel transistor 34 is coupled to the drain of N-channel transistor 26, and the drain of P-channel transistor 36 is coupled to the drain of N-channel transistor 28. *Id.* at 2:32–34.

According to Schucker, in this arrangement of transistors, inverters, and supply voltages, the maximum voltages for all transistors in circuit 10 (i.e., the voltages across gate to source, gate to drain, and drain to source) is limited to 3.3 volts. *Id.* at 2:17–18. That is, no transistor junction or gate oxide layer in the circuit is exposed to more than 3.3 volts. *Id.* at 2:19–22. Schucker describes that the voltage level translation process of circuit 10, therefore, does not cause any of the 0.5 submicron MOS transistors to exceed their maximum voltage rating of 3.3 volts. *Id.* at 2:26–29.

Regarding the operation of voltage level translator circuit 10, Schucker describes that when the input signal V_{IN} is at logic zero (i.e., 0.0 volts), node 15 goes to logic one (i.e., 3.3 volts) and node 17 goes to logic zero (i.e., 0.0 volts). *Id.* at 2:56–59. Schucker describes that node 15 being set to logic one turns off transistors 26 and 34, which in turn sets node 47 to logic one. *Id.* at 2:60–65, 3:6–7. On the other hand, node 17 being set to logic zero turns transistors 28 and 36 on, causing them to pull node 49 to logic zero. *Id.* at 2:66–3:3, 3:5–6.

According to Schucker, node 49 being at logic zero sets the output of inverter 52 to logic one, which turns off transistor 42 and makes transistor 38 non-conductive. *Id.* at 3:14–17. Schucker describes that while the logic zero input signal V_{IN} turns off transistors 38 and 42, the logic zero at node 17 propagates through delay circuit 18 and causes the output of inverter 20 to go to logic one approximately two nanoseconds later. *Id.* at 3:18–20, 25–28. This turns on transistor 22, which allows conduction from output terminal 40, through transistors 30 and 22, to terminal 24. *Id.* at 3:29–32. Schucker describes that the output signal V_{OUT} at terminal 40,

therefore, is pulled low to logic zero, i.e., the ground voltage 0.0 volts at terminal 24. *Id.* at 3:31–32.

When the input signal V_{IN} switches to logic one (i.e., 3.3 volts), Schucker describes that node 15 goes to logic zero (i.e., 0.0 volts) and node 17 goes to logic one (3.3 volts). *Id.* at 3:33–35. This turns off transistors 28 and 36, and turns transistor 26 on and makes transistor 34 conduct. *Id.* at 3:35–43. According to Schucker, as the result, node 47 goes to logic zero and node 49 goes to logic one. *Id.* at 3:8–9, 45–47. The logic one at node 49 causes the output of inverter 52 to go to logic zero, which turns on transistor 42 and makes transistor 38 conduct. *Id.* at 3:47–48. Consequently, the conduction path from terminal 44 and output 40 is completed, pulling the output signal V_{OUT} at terminal 40 high to logic one at the operating potential of terminal 44, i.e., 5 volts. *Id.* at 3:48–51.

Thus, voltage level translator circuit 10 converts the input signal V_{IN} operating between 0.0 volts (for logic zero) and 3.3 volts (for logic one) to the output signal V_{OUT} between 0.0 volts (for logic zero) and 5 volts (for logic one) without causing any of the 0.5 submicron MOS transistors of the circuit to exceed their maximum allowable voltage of 3.3 volts. *Id.* at 1:54–56, 2:17–29, 2:56–3:51.

3. Discussion — Claim 1

Petitioner contends that Schucker's "voltage level translator circuit," as illustrated in Schucker's Figure 1 and described in the related text, discloses every limitation of claim 1. Pet. 25–46. As noted above, Patent Owner's counter arguments are directed to one particular claim limitation only—that is, Patent Owner asserts that Schucker does not disclose "a protection layer which couples said first and second nodes to third and

fourth nodes via first and second isolation paths, respectively," as recited in claim 1, under Patent Owner's proposed construction of the term "couples." *See, e.g.*, PO Resp. 19–27, 35–36. In what follows, we first discuss Petitioner's contentions on how Schucker discloses each limitation recited in claim 1. We then address Patent Owner's arguments, including its claim construction arguments, and Petitioner's responses.

a. Petitioner's Contentions

(i) Preamble[3]

The preamble of claim 1 recites a "level shifter circuit." Petitioner contends that "[t]o the extent the preamble is limiting," Schucker's "voltage level translator circuit" discloses a level shifter circuit because it "converts an input signal referenced between first and second operating potentials to an output signal referenced between second and third operating potentials." Pet. 25 (citing Ex. 1002, code (57)). Petitioner asserts that, in Schucker, the input signal is "*level shifted* through cascoded transistors and latched by series inverters to drive upper cascoded transistors in the output stage." *Id.* (citing Ex. 1002, code (57), Fig. 1; Ex. 1004 ¶ 58).

Patent Owner does not specifically dispute Schucker discloses the preamble of claim 1. *See* PO Resp. 35–52.

[3] We take no position on whether the preamble of claim 1 is limiting as the parties have not raised that issue before us.

Based on the complete record and for the reasons explained by Petitioner, we are persuaded that Petitioner has demonstrated sufficiently that Schucker discloses the preamble of claim 1.[4]

(ii) Claim element 1[a]

Petitioner designates as claim element 1[a] the limitation that recites "a first circuit, responsive to an input signal, that switches first and second nodes to opposite states within a first voltage range between first and second supply voltages." Pet. 26. Referencing an annotated version of Figure 1 of Schucker, Petitioner contends that Schucker discloses all recitations of claim element 1[a]. *Id.* at 26–28 (citing Ex. 1002, 1:3–5, 1:55–2:9, 2:58–60, 3:33–35, 6:3–5, Fig. 1; Ex. 1004 ¶¶ 59–61).

[4] We also find that Patent Owner has waived any argument directed to the preamble of claim 1. *See* Paper 9 (Scheduling Order), 5 ("Patent Owner is cautioned that any arguments for patentability not raised in the response may be deemed waived" (emphasis omitted)).

Figure 1 of Schucker, as annotated by Petitioner, is reproduced below.

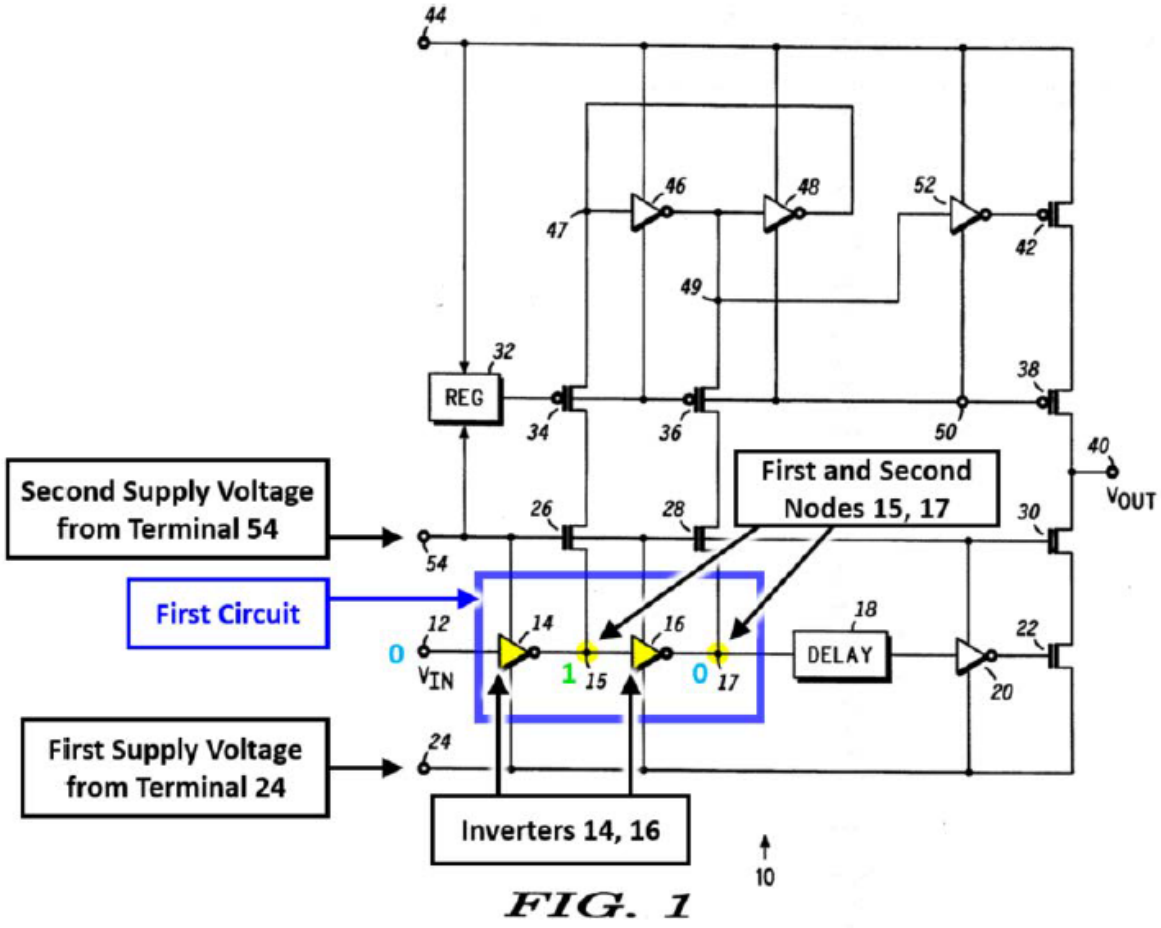


FIG. 1

Id. at 27. Annotated Figure 1 above shows Petitioner's identification of the recitations of claim element 1[a] allegedly present in Schucker.

Referencing Figure 1, Petitioner asserts that the circuit Petitioner identified in Figure 1 of Schucker, including inverters 14 and 16 and nodes 15 and 17, discloses the "first circuit" recited in claim 1. *Id.* at 26–27 (citing Ex. 1002, 1:55–2:5, 2:58–60, 3:33–35, Fig. 1; Ex. 1004 ¶ 59). Petitioner also maps nodes 15 and 17 of Schucker to the recited "first node" and "second node," respectively. *Id.* at 27. Petitioner argues that these elements of Schucker identified by Petitioner comprise a circuit because they provide a path for current flow from a supply voltage of 3.3 volts at

terminal 54 (the recited "second supply voltage") to a ground voltage of 0.0 volts at terminal 24 (the recited "first supply voltage"). *Id.* at 26 (citing Ex. 1002, 1:55–2:5), 27 (citing Ex. 1002, 1:64–66, 2:6–9, Fig. 1).

Petitioner further contends that Schucker's circuit identified by Petitioner as the claimed "first circuit" is "responsive to an input signal" and "switches first and second nodes to opposite states within a first voltage range between first and second supply voltages," as recited in claim 1, because Schucker describes that when the input signal V_{IN} (the recited "input signal") is at logic zero of 0.0 volts (i.e., the recited "first supply voltage"), node 15 goes to logic one (3.3 volts) and node 17 goes to logic zero (0.0 volts), and that when the input signal V_{IN} is at logic one of 3.3 volts (i.e., the recited "second supply voltage"), node 15 goes to logic zero and node 17 goes to logic one (i.e., "switch[ing] to opposite states," as recited in the claim). *Id.* at 26–27 (citing Ex. 1002, 1:64–66, 2:6–9, 2:58–60, 3:33–35, Fig. 1; Ex. 1004 ¶ 59). Petitioner argues that Schucker's voltage range of 0.0 volts (provided at terminal 24) to 3.3 volts (provided at terminal 54) discloses "a first voltage range between first and second supply voltages," as recited in claim 1. *Id.* at 27–28 (citing Ex. 1002, 1:3–5, 1:55–57, 1:64–68, 2:3–9, 6:3–5, Fig. 1; Ex. 1004 ¶ 60).

Patent Owner does not contest Petitioner's argument that Schucker discloses the recitations of claim element 1[a]. *See* PO Resp. 35–52.

Based on the complete record and for the reasons explained by Petitioner, we are persuaded that Petitioner has demonstrated sufficiently that Schucker discloses "a first circuit, responsive to an input signal, that

switches first and second nodes to opposite states within a first voltage range between first and second supply voltages," as recited in claim 1.[5]

(iii) Claim element 1[b]

Petitioner designates as claim element 1[b] the limitation that recites "a protection layer which couples said first and second nodes to third and fourth nodes via first and second isolation paths, respectively." Pet. 28. Referencing another annotated version of Figure 1 of Schucker, Petitioner contends that Schucker discloses all recitations of claim element 1[b]. *Id.* at 28–31 (citing Ex. 1002, 1:66–2:29, 2:32–42, 3:3–6, 4:35–41, 5:49–60, Fig. 1; Ex. 1004 ¶¶ 62–66).

[5] We also find that Patent Owner has waived any argument directed to this claim limitation. *See* Paper 9, 5.

Figure 1 of Schucker, as annotated by Petitioner, is reproduced below.

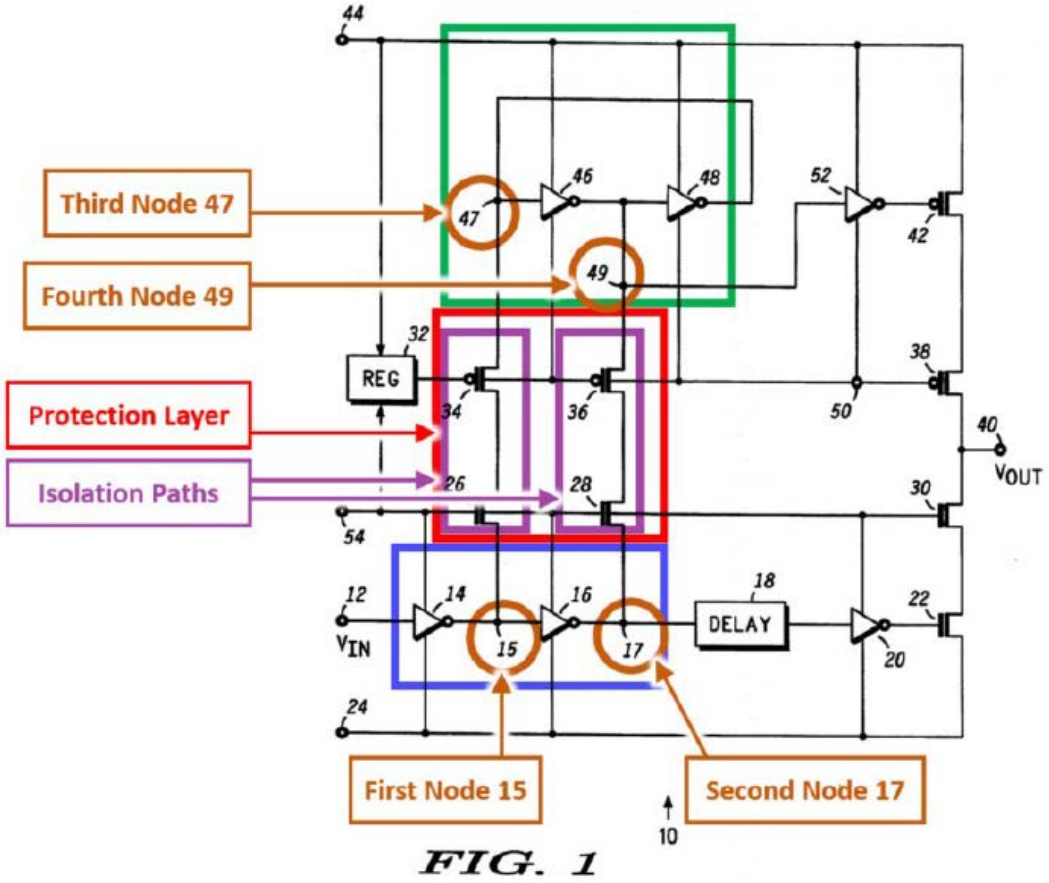


FIG. 1

Id. at 29. Figure 1 above, as annotated by Petitioner, shows Petitioner's identification of the recitations of claim element 1[b] allegedly present in Schucker, including "a protection layer," "first and second nodes," "third and fourth nodes," and "first and second isolation paths." *Id.*

Referencing Figure 1, Petitioner asserts that the circuit Petitioner identified in Schucker's Figure 1, including transistors 26, 28, 34, and 36, discloses "a protection layer," as recited in claim 1. *Id.* at 28–29 (citing Ex. 1002, 5:49–60, Fig. 1). Petitioner also maps nodes 47 and 49 depicted in Figure 1 of Schucker to the recited "third and fourth nodes," respectively. *Id.* (citing Ex. 1002, 1:66–2:29, 2:32–42, 3:3–6, 5:49–60, Fig. 1; Ex. 1004

¶ 62). Petitioner contends that Schucker's cascoded transistors 26 and 34 [6] disclose the recited "first isolation path" that couples node 15 (the recited "first node") to node 47 (the recited "third node") and that the cascoded transistors 28 and 36 disclose the recited "second isolation path" that couples node 17 (the recited "second node") to node 49 (the recited "fourth node"). *Id.* (citing Ex. 1002, 1:66–2:29, 2:32–42, 3:3–6, 5:49–60, Fig. 1; Ex. 1004 ¶ 62).

Petitioner asserts that Schucker's circuit (including transistors 26, 28, 34, and 36) identified by Petitioner as the claimed "protection layer" provides "electrical stress protection." *Id.* at 28 (citing Ex. 1002, 5:49–60). Petitioner also contends that, for the reasons discussed in its analysis of claim element 1[c], Schucker's configuration of transistors 26, 28, 34 and 36 (a) protects Schucker's first circuit (discussed above) from being subject to a high voltage used for Schucker's second circuit (also discussed above) and (b) protects transistors in Schucker's second circuit from being subject to the

[6] The word "cascoded" appears to be a term of art in the field of electronic circuits. Schucker uses the phrase "cascoded" transistors to refer to "stacked" transistors, such as transistors 26 and 34 or transistors 28 and 36 depicted in Figure 1 of Schucker. *See* Ex. 1002, code (57) ("Additional *cascoded* transistors may be *stacked* to extend the range of voltage translation." (emphases added)), 1:66–2:23 (describing the configuration of stacked transistors 26, 34 and stacked transistors 28, 36 depicted in Figure 1 as "cascoded arrangement"), Fig. 1. This usage appears to be consistent with the definition or description of the term "cascode" found in general electronics literature. *See, e.g.*, Ex. 3001 ("The Illustrated Dictionary of Electronics," 8th ed., 2001), 103 (defining "cascode" as a "high-gain, low-noise, high-input impedance amplifier circuit, consisting of a grounded-emitter or grounded-source input stage coupled directly to a grounded-base or grounded-gate output stage" and describing two stacked FETs as "cascode (field-effect transistor arrangement).")

ground voltage of 0 volts used for Schucker's first circuit. *Id.* at 29 (citing *id.* § IX.A.1.d.; Ex. 1004 ¶ 63); *see also id.* at 31–40 (describing in detail the operation of transistors 26, 28, 34, and 36 to keep inverters 14 and 16 and nodes 15 and 17 within the voltage range of 0 volts to 3.3 volts and to keep inverters 46 and 48 and nodes 47 and 49 within the voltage range of 1.7 volts to 5 volts (citing Ex. 1002, 1:55–57, 1:64–66, 2:6–36, 2:58–3:1, 3:3–12, 3:33–35, 3:38–67, 4:9–12, 4:40–42, Figs. 1, 2; Ex. 1004 ¶¶ 67–76)).

Petitioner further asserts that Schucker's configuration of transistors 26, 28, 34, and 36 discloses the same "protection layer" as disclosed in the '588 patent because Schucker's transistors 26, 28, 34, and 36, arranged as shown in Figure 1, operate the same way as the "protection layer" described in the '588 patent. *Id.* at 29–31 (citing Ex. 1002, 1:66–68, 2:9–11; Ex. 1001, 4:35–41; Ex. 1004 ¶¶ 63–66). Petitioner contends that the '588 patent discloses

> [t]he transistors 113, 115, 117 and 119 of the protection layer 104 are also thin gate devices. The *transistors 113 and 115 receive VDDL at their gates* thereby preventing the voltage of the lower circuit 102 from exceeding VDDL. The *transistors 117 and 119 receive GNDH at their gates* thereby preventing the voltage of the upper circuit 106 from falling below GNDH.

Id. at 29–30 (citing Ex. 1001, 4:35–41; Ex. 1004 ¶ 64). Petitioner asserts that Schucker similarly discloses "the transistors 26, 28 receive the second supply voltage of 3.3 volts at their gates, and the transistors 34, 36 receive the third supply voltage of 1.7 volts at their gates." *Id.* at 30 (citing Ex. 1002, 1:66–68, 2:9–11; Ex. 1004 ¶ 65). Petitioner illustrates the alleged similarities with a side-by-side comparison (not reproduced herein) of Figure 1 of the '588 patent and Figure 1 of Schucker, with annotations showing Petitioner's mapping of the elements of Schucker and the matching

elements of the '588 patent allegedly corresponding to the same recitations of claim 1. *Id.* (comparing Ex. 1001, Fig. 1, with Ex. 1002, Fig. 1). Petitioner contends that Schucker therefore discloses "a protection layer which couples said first and second nodes to third and fourth nodes via first and second isolation paths, respectively," as recited in claim 1. *Id.* at 31 (citing Ex. 1004 ¶ 66).

Patent Owner appears not to dispute Petitioner's contention that Schucker discloses the "a protection layer," "first and second nodes," "third and fourth nodes," and "first and second isolation paths," arranged as recited in the claim. *See, e.g.*, PO Resp. 15 ("There is considerable *similarity in topology* between Schucker's Figure 1 circuit and the Patent's Figure 1 circuit." (emphasis added)). Instead, Patent Owner argues that "Schucker's topologically similar circuit" *operates differently* than the circuit described and claimed by the '588 patent. *See id.* at 37 ("The Petition . . . fails to show that *Schucker's topologically similar circuit* operates in the manner described in and claimed by the Patent. In fact, Schucker explicitly teaches that it *does not work in the same manner*." (emphases added)), 49 ("[A]lthough *Schucker and the Patent have similar topology*, they can and do *operate in a different manner*." (emphases added)). We discuss Patent Owner's arguments on the purported operational differences and Petitioner's responses to those arguments in Section III.C.3.b. below.

Based on the complete record and the foregoing discussion of the evidence and arguments presented by Petitioner and Patent Owner, we are persuaded that Petitioner has demonstrated sufficiently that Schucker discloses "a protection layer," "first and second nodes," "third and fourth

nodes," and "first and second isolation paths," arranged as recited in the claim.

(iv) Claim element 1[c]

Petitioner designates as claim element 1[c] the wherein clause that modifies claim element 1[b], i.e., the limitation that recites "wherein said first and second isolation paths keep said first and second nodes within said first voltage range and keep said third and fourth nodes within a second voltage range." Pet. 31. Petitioner contends that Schucker discloses the recitations of claim element 1[c]. *Id.* at 31–40 (citing Ex. 1002, 1:55–57, 1:64–66, 2:6–36, 2:58–3:1, 3:3–12, 3:33–35, 3:38–67, 4:9–12, 4:40–42, Figs. 1, 2; Ex. 1004 ¶¶ 67–76).

As discussed above regarding Petitioner's contentions on claim element 1[a], Petitioner asserts that Schucker's voltage range between 0.0 volts provided at terminal 24 (the recited "first supply voltage") and 3.3 volts provided at terminal 54 (the recited "second supply voltage") discloses "a first voltage range between first and second supply voltages," as recited in claim 1. *Id.* at 27–28 (citing Ex. 1002, 1:3–5, 1:55–57, 1:64–68, 2:3–9, 6:3–5, Fig. 1; Ex. 1004 ¶ 60), 31 (citing Ex. 1002, 1:64–66, 2:6–9, Fig. 1; Ex. 1004 ¶ 67). Petitioner also contends that Schucker's voltage range of 1.7 volts (provided by voltage regulator circuit 32) to 5 volts (provided at terminal 44) discloses "a second voltage range" recited in claim 1. *Id.* at 32–33 (citing Ex. 1002, 2:6–17, Fig. 1; Ex. 1004 ¶ 68).

In addition, as discussed above in the context of claim element 1[b], Petitioner asserts that Schucker's cascoded N-channel transistor 26 and P-channel transistor 34 disclose the recited "first isolation path" that couples node 15 (the recited "first node") to node 47 (the recited "third node") and

that Schucker's cascoded N-channel transistor 28 and P-channel transistor 36 disclose the recited "second isolation path" that couples node 17 (the recited "second node") to node 49 (the recited "fourth node"). *Id.* at 28–29 (citing Ex. 1002, 1:66–2:29, 2:32–42, 3:3–6, 5:49–60, Fig. 1; Ex. 1004 ¶ 62).

Petitioner asserts that Schucker's circuit elements Petitioner identifies as the recited "first and second isolation paths" (i.e., the cascoded transistors 26, 34 and 28, 36) perform the function recited in element 1[c] (i.e., to "keep" the recited "first and second nodes" and "third and fourth nodes" within the "first voltage range" and the "second voltage range," respectively), using the same arrangement of N-channel transistors and P-channel transistors described in the Specification of the '588 patent. *Id.* at 31–40 (citing Ex. 1002, 1:55–57, 1:64–66, 2:6–36, 2:58–3:1, 3:3–12, 3:33–35, 3:38–67, 4:9–12, 4:40–42, Figs. 1, 2; Ex. 1001, Fig. 1; Ex. 1004 ¶¶ 67–76). Petitioner contends, therefore, that Schucker's isolation paths are identical to the isolation paths disclosed in the '588 patent. *Id.* at 39 (citing Ex. 1004 ¶ 75).

Turning first to Petitioner's contentions on the identity or similarity of arrangement between the "first and second isolation paths" allegedly present in Schucker and the "first and second isolation paths" described in the '588 patent, Petitioner provides annotated versions of Schucker's Figure 1 (not reproduced herein), illustrating the arrangement of Schucker's N-channel transistors 26 and 28 and P-channel transistors 34 and 36, with the drains of the N-channel transistors tied to the drains of the respectively cascoded P-channel transistors and the sources of the N-channel transistors and the P-channel transistors connected to nodes 15 and 17 and nodes 47 and 49,

respectively. *Id.* at 34, 37. Petitioner also provides a side-by-side comparison (not reproduced herein) of Figure 1 of Schucker and Figure 1 of the '588 patent, with annotations showing Petitioner's mapping of the elements of Schucker to the allegedly matching elements of the '588 patent (*id.* at 39), and asserts that Schucker's isolation paths are identical to the isolation paths disclosed in the '588 patent (*id.* (citing Ex. 1004 ¶ 75)).

As discussed above, Patent Owner acknowledges that circuit elements in Schucker's Figure 1 Petitioner identifies as the recited "first and second isolation paths" are "topologically similar" to the allegedly matching circuit elements in Figure 1 of the '588 patent. *See* PO Resp. 37; *see also id.* at 15 ("There is considerable *similarity in topology* between Schucker's Figure 1 circuit and the Patent's Figure 1 circuit." (emphasis added)), 49 ("[A]lthough *Schucker and the Patent have similar topology,* they can and do operate in a different manner." (emphasis added)).

Upon review of the complete record and considering the arguments and evidence presented by Petitioner and Patent Owner, we agree with Petitioner that the arrangement of N-channel transistors 26 and 28, P-channel transistors 34 and 36, nodes 15 and 17, and nodes 47 and 49 of Schucker described in Schucker's Figure 1 discloses the arrangement of N-channel transistors 113 and 115, P-channel transistors 117 and 119, nodes 105 and 111, and nodes 121 and 123 of the '588 patent, as described in Figure 1 of the '588 patent. *Compare* Ex. 1001, Fig. 1, 3:4–13 (The '588 patent describing the arrangement of N-channel transistors 113 and 115 and P-channel transistors 117 and 119, with the drains of the N-channel transistors coupled to the drains of the corresponding P-channel transistors, the sources of the N-channel transistors coupled to nodes 105 and 111, and

the sources of the P-channel transistors coupled to nodes 121 and 123.), 5:16–19 ("The transistors 113 and 117 form a first isolation path between nodes 105 and 121 and the transistors 115 and 119 form a second isolation path between nodes 111 and 123."), *with* Ex. 1002, 1:64–2:5, 2:33–35, Fig. 1 (Schucker describing the arrangement of N-channel transistors 26 and 28 and P-channel transistors 34 and 36, with the drains of the N-channel transistors coupled to the drains of the respectively cascoded P-channel transistors, the sources of the N-channel transistors coupled to nodes 15 and 17, and the sources of the P-channel transistors coupled to nodes 47 and 49). In other words, we agree with Petitioner that the arrangement of Schucker's circuit elements Petitioner identifies as the recited "first and second isolation paths" discloses the "first and second isolation paths" described in the '588 patent.

Turning to the functional or operational aspects of Schucker's circuit elements Petitioner identifies as the recited "first and second isolation paths," Petitioner contends that Schucker's cascoded transistors 26 and 34 and cascoded transistors 28 and 36 (the recited "first and second isolation paths") keep nodes 15 and 27 (the recited "first and second nodes") within the voltage range of the ground voltage of 0.0 volts provided at terminal 24 (the recited "first supply voltage") and 3.3 volts provided at terminal 54 (the recited "second supply voltage"), i.e., within the recited "first voltage range," and also keep nodes 47 and 49 (the recited "third and fourth nodes") within the voltage range of 1.7 volts provided by voltage regulator circuit 32 and 5 volts provided at terminal 44, i.e., within the recited "second voltage range." Pet. 33–34 (citing Ex. 1002, 1:66–68, 2:9–29; Ex. 1004 ¶ 70). Petitioner provides detailed explanations and specific citations to Schucker,

describing in detail the operation of transistors 26, 28, 34, and 36 based on their cascoded arrangement to keep nodes 15 and 17 within the voltage range of 0.0 volts to 3.3 volts and to keep and nodes 47 and 49 within the voltage range of 1.7 volts to 5 volts. *Id.* at 31–40 (citing Ex. 1002, 1:55–57, 1:64–66, 2:6–36, 2:58–3:1, 3:3–12, 3:33–35, 3:38–67, 4:9–12, 4:40–42, Figs. 1, 2; Ex. 1004 ¶¶ 67–76).

In particular, Petitioner explains, citing the testimony of Dr. Chapman, the "protection" function (to "keep" the nodes within the first and second voltage ranges) provided by Schucker's isolation paths results from the operation of the cascoded transistors forming the isolation paths in the arrangement discussed above, where certain transistors in the isolation paths are turned on or off due to the cascode arrangement of the drains and sources of the transistors, as well as certain voltage conditions produced when the input signal V_{IN} switches between 0.0 volts and 3.3 volts. *Id.* at 33–40 (citing Ex. 1002, Fig. 1, 1:55–57, 1:66–68, 2:9–29, 2:58–3:12, 3:1–3, 3:5–6, 3:10–12, 3:33–35, 3:38–47; Ex. 1004 ¶¶ 70–76). Petitioner also explains, citing the testimony of Dr. Chapman, the arrangement of the '588 patent's transistors 113, 115, 117, and 119 forming the first and second isolation paths operates to keep nodes 105 and 111 within the voltage range of GNDL and VDDL and keep nodes 121 and 123 within the voltage range of GNDH and VDDH. *See id.* at 9–13 (citing Ex. 1001, Fig. 1, 2:58–60, 3:11–15, 3:40–67, 4:53–56, 4:1–26, 4:35–41, 5:23–25, 10:28–29; Ex. 1004 ¶¶ 37–41).

Patent Owner does not specifically dispute Schucker discloses the recitations of claim element 1[c]. *See* PO Resp. 35–52.

Upon review of the complete record and considering the arguments and evidence presented by Petitioner, we agree with Petitioner that the cascode arrangement of Schucker's transistors 26, 28, 34, and 36 (the recited "first and second isolation paths") operates to keep nodes 15 and 17 (the recited "first and second nodes") within the voltage range of 0.0 volts to 3.3 volts (the recited "first voltage range') and keep nodes 47 and 49 (the recited "third and fourth nodes") within the voltage range of 1.7 volts to 5 volts (the recited "second voltage range"), in the same way the arrangement of the '588 patent's transistors 113, 115, 117, and 119 forming the first and second isolation paths operates to keep nodes 105 and 111 within the voltage range of GNDL and VDDL and keep nodes 121 and 123 within the voltage range of GNDH and VDDH.

Based on the complete record and for the reasons explained by Petitioner, we are persuaded that Petitioner has demonstrated sufficiently that Schucker discloses "wherein said first and second isolation paths keep said first and second nodes within said first voltage range and keep said third and fourth nodes within a second voltage range," as recited in claim 1.[7]

(v) Claim element 1[d]

Petitioner designates as claim element 1[d] the limitation that recites "a second circuit that switches said third and fourth nodes to opposite states within said second voltage range between third and fourth supply voltages in response to switching of said first and second nodes." Pet. 40. Petitioner asserts that Schucker discloses all recitations of claim element 1[d]. *Id.* at

[7] We also find that Patent Owner has waived any argument directed to this claim limitation. *See* Paper 9, 5.

40–42 (citing 2:6–9, 2:29–31, 2:37–42, 2:58–66, 3:1–3, 3:6–8, 3:33–35, 3:42–47, Fig. 1; Ex. 1004 ¶¶ 77–81).

First, referencing Figure 1 of Schucker, Petitioner identifies Schucker's circuit including cross-coupled inverters 46 and 48 and nodes 47 and 49 as the claimed "second circuit" present in Schucker. *Id.* at 40–41 (citing Ex. 1002, 2:6–9, 2:29–31, Fig. 1; Ex. 1004 ¶¶ 77–78).

Next, Petitioner asserts that nodes 47 and 49 (the recited "third and fourth nodes") are switched to opposite states within the second voltage range between 1.7 volts (the recited "third supply voltage") provided by voltage regulator circuit 32 and 5.0 volts (the recited "fourth supply voltage") provided by terminal 44. *Id.* at 41 (citing Ex. 1002, 2:6–9; Ex. 1004 ¶ 78). Petitioner contends that node 47 (the recited "third node") is at 5 volts when node 15 (the recited "first node") is at logical one, and within a threshold voltage above 1.7 volts when node 15 is at logical zero. *Id.* at 41–42 (citing Ex. 1002, 2:58–66, 3:6–8, 3:33–35, 3:45–47). Petitioner further asserts that node 49 (the recited "fourth node") is within a threshold voltage above 1.7 volts when node 17 (the recited "second node") is at logical zero, and is at 5 volts when node 17 is at logical one. *Id.* at 42 (citing Ex. 1002, 2:58–60, 3:1–3, 3:33–35, 3:42–44; Ex. 1004 ¶ 79). Thus, Petitioner argues that the second circuit of Schucker switches nodes 47 and 49 (the recited "third and fourth nodes") to opposite states between 1.7 volts and 5 volts (the recited "second voltage range between third and fourth supply voltages") in response to the switching of nodes 15 and 17 (the recited "first and second nodes"). *Id.* (citing Ex. 1004 ¶ 80).

Patent Owner does not specifically dispute Schucker discloses the recitations of claim element 1[d]. *See* PO Resp. 35–52.

Based on the complete record and for the reasons explained by Petitioner, we are persuaded that Petitioner has demonstrated sufficiently that Schucker discloses "a second circuit that switches said third and fourth nodes to opposite states within said second voltage range between third and fourth supply voltages in response to switching of said first and second nodes," as recited in claim 1.[8]

(vi) Claim elements 1[e] and 1[f]

Petitioner designates as claim element 1[e] the limitation that recites "a first inverter having an input coupled to said fourth node, an output coupled to said third node and supply inputs coupled between said third and fourth supply voltages" and as claim element 1[f] the limitation reciting "a second inverter having an input coupled to said third node, an output coupled to said fourth node and supply inputs coupled between said third and fourth supply voltages." Pet. 42, 44. Petitioner contends that Schucker discloses all recitations of claim elements 1[e] and 1[f]. *Id.* at 42–46 (citing Ex. 1002, Fig. 1, 2:12–16, 2:29–40, 2:42–43, 2:51–53; Ex. 1004 ¶¶ 82–88).

Referencing Figure 1 of Schucker, Petitioner identifies Schucker's cross-coupled inverters 48 and 46 as the recited "first inverter" and "second inverter," respectively, present in Schucker. *Id.* at 42–43 (citing Ex. 1002, 2:38–39, Fig. 1), 44–45 (citing Ex. 1002, 2:29–31, Fig. 1).

Petitioner asserts that, as shown in Figure 1, inverter 48 of Schucker has an input coupled to node 49 (the recited "fourth node") and an output coupled to node 47 (the recited "third node"). *Id.* at 42–43 (citing Ex. 1002,

[8] We also find that Patent Owner has waived any argument directed to this claim limitation. *See* Paper 9, 5.

2:38–39, 2:42–43, Fig. 1; Ex. 1004 ¶ 82). Petitioner contends that Figure 1 also shows that inverter 48 has supply inputs of 1.7 volts from voltage regulator circuit 32 (the recited "third supply voltage") and 5.0 volts from terminal 44 (the recited "fourth supply voltage"). *Id.* at 43–44 (citing Ex. 1002, 2:12–16, 2:29–31; Ex. 1004 ¶¶ 83, 84).

Similarly, Petitioner asserts that, as shown in Figure 1, inverter 46 of Schucker has an input coupled to node 47 (the recited "third node") and an output coupled to node 49 (the recited "fourth node"). *Id.* at 44–45 (citing Ex. 1002, 2:37–39, Fig. 1; Ex. 1004 ¶ 86). Petitioner also argues that Figure 1 shows that inverter 46 has supply inputs of 1.7 volts from voltage regulator circuit 32 (the recited "third supply voltage") and 5.0 volts from terminal 44 (the recited "fourth supply voltage"). *Id.* at 45–46 (citing Ex. 1002, 2:12–16, 2:29–31, 2:51–53, Fig. 1; Ex. 1004 ¶ 87).

Patent Owner does not contest Petitioner's argument that Schucker discloses the recitations of claim elements 1[e] and 1[f]. *See* PO Resp. 35–52.

Based on the complete record and for the reasons explained by Petitioner, we are persuaded that Petitioner has demonstrated sufficiently that Schucker discloses "a first inverter having an input coupled to said fourth node, an output coupled to said third node and supply inputs coupled between said third and fourth supply voltages" and "a second inverter having an input coupled to said third node, an output coupled to said fourth node and supply inputs coupled between said third and fourth supply voltages," as recited in claim 1.[9]

[9] We also find that Patent Owner has waived any argument directed to these claim limitations. *See* Paper 9, 5.

b. Patent Owner's Arguments and Petitioner's Responses

The parties dispute whether Schucker discloses the limitation reciting "a protection layer which couples said first and second nodes to third and fourth nodes via first and second isolation paths, respectively" (i.e., the limitation Petitioner identifies as claim element 1[b]). As discussed below, the disputed issue turns on whether the claim term "couples" recited in claim element 1[b] requires the isolation paths to operate in a "push/pull" configuration.

Patent Owner asserts that the disputed term "couples" must describe (a) making an electrical connection during circuit operation (b) in response to an input signal. PO Resp. 3, 22–24. Specifically, Patent Owner contends that to "couple," as recited in the claim, the "protection layer" must (1) conduct electricity (i.e., pass electrical current), (2) in both isolation paths, (3) in opposite directions, and (4) at the same time. *Id.* at 3, 13, 20–25, 27–28, 35–36, 42, 48; Sur-reply 5–7. Patent Owner's proposed claim construction is predicated on Patent Owner's contention that the challenged claims require the recited "isolation paths" operate in a "'push/pull' configuration," where "*both* isolation paths" conduct electricity in opposite directions, "one pulling, the other pushing" (PO Resp. 35–36), i.e., "one path pulling current down as the other pushes current up" (Sur-reply 17). According to Patent Owner, this "push/pull" function is "critical to a core purpose of '588 embodiments: noise immunity" (PO Resp. 36) and is "a key aspect to the invention" of the '588 patent (*id.* at 51).

Patent Owner asserts that Schucker does not disclose the recited feature of coupling by isolation paths under its proposed claim construction, and, therefore, does not anticipate claim 1, because Schucker's isolation

paths can "only pull" in one isolation path (*id.* at 3) while the other isolation path is "non-conductive" (*id.* at 20, 36).

Petitioner disagrees with Patent Owner's proposed construction of the claim term "couples" requiring the alleged "push/pull" operation and asserts that the disputed limitation should be construed to encompass isolation paths that conduct electricity some of the time, without requiring current flow on both isolation paths in opposite directions at the same time. Reply 1–19.

In what follows, we first consider the plain meaning of the disputed term based on the claim language of claim 1, including Petitioner's plain meaning interpretation indicated in the Petition. We then consider the parties' arguments regarding the embodiments described in the Specification. Next, we consider the parties' arguments on whether the alleged "push/pull" feature argued by Patent Owner restricts the scope of the challenged claims to require "pushing current up" in one isolation path while "pulling current down" in the other isolation path. For the reasons explained below, we determine it does not. Lastly, we consider Patent Owner's claim construction and patentability arguments based on the alleged purpose of the '588 patent to improve noise immunity.

(i) Claim Language

In determining the broadest reasonable construction of a claim limitation, we begin with the language of the claim itself. *In re Power Integrations, Inc.*, 884 F.3d 1370, 1376 (Fed. Cir. 2018) ("[C]laim construction must begin with the words of the claims themselves." (quoting *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 457 F.3d 1293, 1301 (Fed. Cir. 2006))); *In re NTP, Inc.*, 654 F.3d 1279, 1288 (Fed. Cir. 2011) ("As with

any claim construction analysis, we begin with the claim language." (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc))).

"Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016) (citing *Straight Path IP Grp., Inc. v. Sipnet EU S.R.O.*, 806 F.3d 1356, 1362 (Fed. Cir. 2015)).

As discussed above in Section III.B. (Claim Construction), Petitioner does not propose express constructions for any claim terms in the Petition and asserts that the challenged claims are unpatentable under the plain meaning interpretation of the claims. Pet. 24. As discussed above in the context of claim elements 1[b] and 1[c], Petitioner's application of Schucker to claim 1 appears to indicate that Petitioner's plain meaning interpretation of the claim term "couples" encompasses isolation paths that conduct electricity some of the time. *See* Pet. 28–31, 33–39. For example, in the context of claim element 1[b], Petitioner points to the cascode arrangement of transistors 26, 28, 34, and 36 depicted in Schucker's Figure 1 and argues that Schucker discloses "a first isolation path that *couples* the first node 15 to third node 47 via cascoded transistors 26 and 34, and a second isolation path that *couples* the second node 17 to fourth node 49 via cascoded transistors 28 and 36, as shown below in Fig. 1." *Id.* at 28 (emphases added) (citing Ex. 1002, 1:66–2:29, 2:32–42, 3:3–6, 5:49–60). In the context of claim element 1[c], Petitioner argues, citing the testimony of Dr. Chapman, that the "protection" function (to keep the first and second nodes within the first voltage range and keep the third and fourth nodes within the second voltage range) provided by Schucker's isolation paths results from the operation of

the N-channel and P-channel transistors forming the isolation paths in the cascode arrangement between the upper and lower nodes, where certain transistors in the isolation paths are turned on or off (i.e., conducting electricity through the isolation paths between the nodes under certain voltage conditions) when the input signal V_{IN} switches between 0.0 volts and 3.3 volts. *Id.* at 33–40 (citing Ex. 1002, Fig. 1, 1:55–57, 1:66–68, 2:9–29, 2:58–3:12, 3:1–3, 3:5–6, 3:10–12, 3:33–35, 3:38–47; Ex. 1004 ¶¶ 70–76). Thus, Petitioner's contentions presented in the Petition indicate that Petitioner's plain meaning interpretation of the claim term "couples" encompasses isolation paths that conduct electricity some of the time, e.g., potentially conductive paths that can conduct electricity under certain conditions.

In its Response, Patent Owner asserts that Petitioner's "implicit[]" plain meaning construction (PO Resp. 20) is erroneous because the term "couples" recited in claim element 1[b] does not "encompass both non-conductive and conductive paths." *Id.* at 24. In support of its proposed construction, Patent Owner points to the present tense of the verb "couples" and asserts that the only other present tense verbs recited in claim 1 are the verb "switches" recited in claim elements 1[a] and 1[d]—i.e., "the first circuit, '<u>responsive to an input signal</u> . . . *switches* first and second nodes to opposite states' and the second circuit '*switches* said third and fourth nodes to opposite states . . . <u>in response to</u> switching of said first and second nodes.'" *Id.* at 23 (underlined emphases added). Patent Owner argues that because the phrases "responsive to an input signal" and "in response to switching of said first and second nodes" modify the present tense verb "switches" recited in claim elements 1[a] and 1[d], the present tense verb

"couples" recited in claim element 1[b] should similarly be interpreted to describe "an action in operation" "responsive to the input signal" carried out by the recited "protection layer." *Id.* at 24.

Patent Owner overlooks the fact that claim elements 1[a] and 1[d] expressly recite the phrases "responsive to an input signal" and "in response to switching of said first and second nodes," respectively, that modify the verb "switches," whereas claim element 1[b] recites no such adverbial phrase that restricts the verb "couples." This claim language shows that the patentee knew how to modify the recitation "switches" with "responsive to an input signal" and "in response to switching of said first and second nodes," respectively. If the patentee had intended to similarly restrict the verb "couples" recited in claim element 1[b], it could have done so using the same or similar language, but did not. *See Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1358–59 (Fed. Cir. 2016).

More importantly, even if we were to read in the phrase "responsive to an input signal" from claim element 1[a] to modify the term "couples" recited in claim element 1[b], Patent Owner does not explain adequately how such modified claim language (i.e., the present tense verb "couples" modified by the phrase "responsive to an input signal") requires current flow on both isolation paths so as to exclude electrical conduction in only one isolation path during operation.

In its Reply, Petitioner argues that claim 1 "simply recites that the protection layer couple the first circuit to the second circuit via isolation paths" and "does not impose any requirement that those isolation paths conduct current in opposite directions or that one isolation path 'push' current up while the other path 'pulls' current down." Reply 11.

We agree with Petitioner. At least based on the plain language of the claim, the claim term "couples" does not require current flow on both isolation paths at the same time, much less "pushing current up" in one isolation path while "pulling current down" in the other isolation path.

(ii) Embodiments Described in the Specification

Turning to the Specification, Patent Owner cites the following portions of the '588 patent as disclosing the alleged "push/pull" function.

> The complementary switching of the lower nodes 105 and 111 of the lower circuit 102 between opposite voltage levels within the limits of the lower voltage range VDDL/GNDL results in a *push/pull function* of the corresponding nodes 121 and 123 of the upper circuit 106.

Ex. 1001, 4:64–5:1 (emphasis added). "Each isolation path enables each of the nodes 105 and 111 to operate in a *push/pull configuration* to pull one of the nodes 121 and 123 towards GNDH and to *push the other node higher*." *Id.* at 5:19–23 (emphases added).

> When I goes high towards VDDL, the transistor 101 is turned on and the inverter 103 pulls its output low driving node 105 to GNDL. Node 105 going low turns off transistor 107 and causes inverter 109 to drive its output at node 111 high to VDDL. Node 105 going low tends to pull node 121 low whereas *driving node 111 high pushes node 123* to a higher voltage level. Node 121 is pulled low towards GNDH turning on transistor 135 and turning off transistor 133, so that the inverter 127 pulls node 123 high to VDDH.

Id. at 4:1–9 (emphasis added). PO Resp. 24–25 (citing Ex. 1001, 5:19–23, Fig. 1), 28–29 (citing Ex. 1001, 4:1–7), 43 (citing Ex. 1001, 5:22–23, 4:64–5:10).

Citing the testimony of Dr. Ipek, Patent Owner asserts that a person of ordinary skill in the art would recognize that "the only way for an 'isolation path' to 'enable' a node to affect another node's voltage level . . . is for the isolation path to 'couple' the nodes, i.e., electrically connect the nodes so that *current can flow* from one node to the other." PO Resp. 25 (emphasis added) (quoting Ex. 2002 ¶ 68). Thus, Patent Owner argues that in order to pull and push voltages in the '588 patent's push/pull operation (*id.* at 35–36; Sur-reply 5), the recited "isolation paths" must pass current up and down, "one path pulling current down as the other pushes current up" (Sur-reply 17).

In its Reply, Petitioner asserts that Patent Owner disregards the disclosure in the portions of the Specification reproduced above which describes that "node 123 *is pulled high* because node 121 was pulled low by the opposite isolation path, which through the action of the cross-coupled inverters drives node 123 high." Reply 15 (citing Ex. 1001, 4:7–9; Ex. 1013 ¶ 13). In the cited paragraph of his Reply Declaration, Dr. Chapman explains

> In reality, the third and fourth nodes are actually "pulled" to logic high by the cross-coupled inverters. The '588 patent explains that "[n]ode 121 is pulled low towards GNDH turning on transistor 135 and turning off transistor 133, so that the inverter 127 pulls node 123 high to VDDH." Node 123 is *pulled high* because node 121 was pulled low by the opposite isolation path, which through the action of the cross-coupled inverters drives node 123 high. Specifically, when node 121 is pulled low, the gates of PMOS transistor 135 and NMOS transistor 133 in inverter 127 are pulled low. The low value at the gate of PMOS transistor 135 means transistor 135 is on, while the low value at the gate of NMOS transistor 133 means transistor 133 is off.

> Because transistor 135 is on, the output of inverter 127 at node 123 is pulled high to VDDH.

Ex. 1013 ¶ 13 (underlined emphasis added) (citing Ex. 1001, 4:7–9). In other words, Dr. Chapman opines that the '588 patent describes, when the input to the level shifter circuit (depicted in Figure 1) goes high toward VDDL, node 123 is *pulled high* by inverter 127, *not pushed up* by node 111 via transistors 115 and 119, as Patent Owner contends (*see, e.g.*, PO Resp. 23–24 (citing Ex. 1001, 4:5–8)).

Nonetheless, the portion of the Specification cited by Patent Owner also states "[n]ode 105 going low tends to pull node 121 low whereas driving node 111 high *pushes node 123 to a higher voltage level*." Ex. 1001, 4:5–8. We note that the '588 patent describes up-shift circuit 100 depicted in Figure 1 as an "exemplary embodiment." *Id.* at 2:51–53. Thus, the '588 patent appears to disclose alternative embodiments to drive the third or fourth nodes (nodes 121 or 123 depicted in Figure 1) high to VDDH: push high by nodes 105 or 111, or pull high by cross-coupled inverters 125 or 127. In other words, the "push up" feature argued by Patent Owner appears to be a feature of an alternative embodiment described in the '588 patent.

In addition, during the trial hearing, Patent Owner acknowledged that the '588 patent describes an embodiment where the alleged "push/pull" operation is not possible because no "pushing up" can take place. *See* Tr. 78:12–19, 79:21–80:9. The relevant portion of the Specification of the '588 patent describing the operation of up-shift circuit 100 depicted in Figure 1 is set forth below:

> The transistors 113 and 115 receive VDDL at their gates thereby *preventing the voltage of the lower circuit 102 from exceeding VDDL*. The transistors 117 and 119 receive GNDH at their gates

> thereby *preventing the voltage of the upper circuit 106 from falling below GNDH*. . . . The voltage level across the entire up-shift circuit 100, or VDDH to GNDL, can exceed the allowable maximum voltage of any given thin-gate device since none of the devices are exposed to the entire voltage range. And although GNDH may have a smaller magnitude than VDDL, GNDH can be the same voltage as VDDL or even a little higher to maximize the voltage differential between VDDH and GNDL. In this manner, the overall switching is relatively fast since smaller thin-gate devices are used and yet the voltage range is extended by operation of the protection layer 104 separating the lower and upper circuits 102 and 106.

Ex. 1001, 4:36–60 (italicized and underlined emphases added). As shown in the portion of the Specification reproduced above, the '588 patent describes an embodiment where protection layer 104 prevents the voltage of lower circuit 102 from exceeding VDDL and prevents the voltage of upper circuit 106 from falling below GNDH. In other words, in this embodiment, the highest possible voltage for lower circuit 102, including nodes 105 and 111 (*see id.*, Fig. 1), is VDDL, and the lowest possible voltage for upper circuit 106, including nodes 121 and 123, is GNDH. As also shown above with underlined emphasis, the '588 patent describes an embodiment where GNDH, the lowest possible voltage for nodes 121 and 123 (the recited "third and fourth nodes"), is *higher* than VDDL, the highest possible voltage for nodes 105 and 111 (the recited "first and second nodes"). *Id.* at 4:54–56. The '588 patent describes that this embodiment "maximize[s] the voltage differential between VDDH and GNDL" so that "the overall switching is relatively fast." *Id.* at 4:55–57.

Because current can only flow from a higher voltage to a lower voltage (*see, e.g.*, Reply 13 (citing Ex. 1012, 110:13–111:5); Tr. 14:10–11, 44:7–11), in this embodiment it is not possible for current to flow up in

either isolation path (i.e., from node 111 to node 123 or from node 105 to node 121) to push the voltages at node 121 or node 123 up to a higher voltage. Indeed, during the oral hearing, counsel for Patent Owner admitted that the alleged "push/pull" operation is not possible in this embodiment.

> JUDGE WEINSCHENK: -- is that portion, Column 4, Lines 54 to 56 that talks about the comparison, is -- does Claim 1 cover all the different options?
>
> MR. WEATHERWAX: No.
>
> JUDGE WEINSCHENK: And how do we know that?
>
> MR. WEATHERWAX: Because -- well, under our construction, it doesn't because *not all of those can possibly do push/pull*.

Tr. 78:12–19 (emphasis added).

> JUDGE WEINSCHENK: So in that portion of the spec, it says GNDH can be the same or even a little higher than VDDL; you're saying that that portion of the spec is not covered by Claim 1?
>
> MR. WEATHERWAX: Well, part of it is, but not that statement. Not where -- I just want to make sure I'm talking about the correct line here.
>
> JUDGE WEINSCHENK: Sure.
>
> MR. WEATHERWAX: We're talking about Line 54 of Column 4?
>
> JUDGE WEINSCHENK: Correct.
>
> MR. WEATHERWAX: Yes. That sentence, GNDH can be even a little higher to maximize the voltage differential between VDDH and GNDL? *Yes. That would not allow push/pull*.

Tr. 79:21–80:9 (emphases added). Thus, the evidence of record shows that the '588 patent describes embodiments that do not include the "push/pull" feature argued by Patent Owner.

In general, "a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (citation omitted). As discussed above in the context of the plain meaning of the disputed limitation, claim 1 does not state, explicitly or by necessary implication, that the recited "isolation paths" must perform a "push/pull" operation. And, as also discussed above, not all the embodiments described in the Specification require a "push/pull" operation. Thus, unless one of the established exceptions, such as lexicography or disavowal, applies, claim 1 is not restricted to require a "push/pull" operation described in the embodiments.

(iii) Petitioner's Additional Responses

In its Reply, Petitioner presents additional arguments to show that claim 1 does not require a "push/pull" operation—one based on dependent claim 4, another based on a preferred embodiment described in the Specification. We discuss each in turn.

Claim 4 depends from claim 1 and further recites

> wherein said protection layer comprises:
>
> a first N-channel device having a gate receiving said second supply voltage, a source coupled to said first node and a drain;
>
> a first P-channel device having a gate receiving said third supply voltage, a source coupled to said third node and a drain coupled to said drain of said first N-channel device;
>
> a second N-channel device having a gate receiving said second

> supply voltage, a source coupled to said second node and a drain; and
>
> a second P-channel device having a gate receiving said third supply voltage, a source coupled to said fourth node and a drain coupled to said drain of said second N-channel device.

Ex. 1001, 17:34–49.

Pointing to the additionally recited limitations of claim 4, Petitioner asserts that claim 4 shows "the level shifter in claim 1 does not require a 'push/pull configuration.'" Reply 16. Petitioner argues that dependent claim 4 "recites the specific configuration of the transistors in the protection layer," namely, "the sources of the NMOS transistors are connected to the first and second nodes, . . . the sources of the PMOS transistors are connected to the third and fourth nodes, and the drains of the NMOS transistors are tied to the drains of the PMOS transistors." *Id.* To illustrate its argument, Petitioner presents an annotated version of Figure 1 of the '588 patent. Figure 1, as annotated by Dr. Chapman in different colors, is reproduced below.

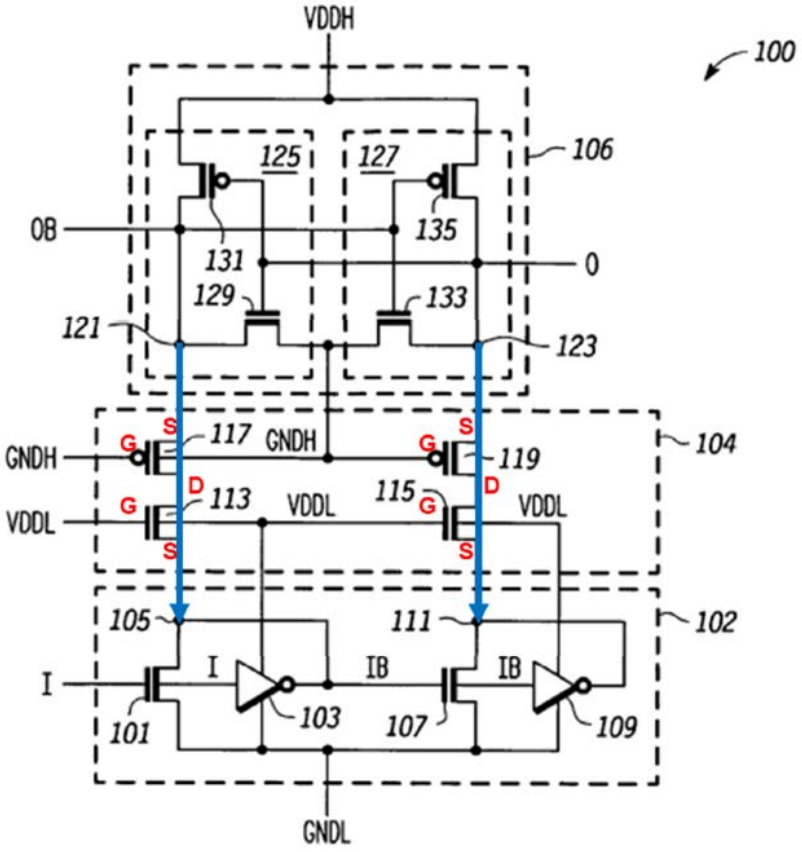


FIG. 1

Id. at 17; Ex. 1013 ¶ 15. Annotated Figure 1 reproduced above shows Dr. Chapman's illustration of the arrangement of N-channel devices and P-channel devices in the protection layer of the '588 patent, as recited in claim 4, with the sources (labeled S in red) of the N-channel devices coupled to the first and second nodes, the sources of the P-channel devices coupled to the third and fourth nodes, and the drains (labeled D in red) of the N-channel devices coupled to the drains of the P-channel devices. Ex. 1013 ¶ 15; Reply 16–17.

The parties' declarants agree that in P-channel transistors the current flows from the source to the drain and in N-channel transistors the current flows from the drain to the source. Ex. 1013 ¶ 15; Ex. 1012, 7:12–19.

Noting this fact, Dr. Chapman testifies that, as illustrated in the Annotated Figure 1 reproduced above, when the transistors in the isolation paths are arranged as recited in claim 4, current in the isolation paths (depicted with blue arrows) "will only flow from the third and fourth nodes to the first and second nodes." Ex. 1013 ¶ 15; Reply 16.

Petitioner asserts, therefore, claim 4 requires the isolation paths to conduct in the same direction—pulling current from the second circuit to the first circuit when an isolation path is conducting—and *not* in opposite directions as Patent Owner contends. Reply 17. That is, the protection layer recited in claim 4 can only "pull" current down (and not necessarily at the same time)[10] and, therefore, does not perform the "push/pull" function argued by Patent Owner. Petitioner argues, because claim 4 depends from claim 1, claim 1 cannot be construed to conflict with the requirements of claim 4. *Id.* at 17–18.

Patent Owner disputes Petitioner's argument that the isolation paths of claim 4 must only "pull" and not "push." Sur-reply 22. Patent Owner argues, citing the deposition testimony of Dr. Chapman, "[i]t is *undisputed* that, for each symmetrical CMOS transistor *in each isolation path*, the electrode that is the 'source' and the electrode that is the 'drain' are *not fixed*, and *can switch back and forth* depending on which electrode is at a

[10] Dr. Chapman testifies that in the '588 patent the switching of nodes 121 and 123 to opposite states takes place by pulling one node low in one isolation path, which causes the cross-coupled inverters to pull the other node high in the opposite isolation path. *See* Ex. 1013 ¶ 13; *see also* Reply 15 (presenting the same argument) (citing Ex. 1013 ¶ 13).

higher voltage potential." *Id.* (emphases added) (citing Ex. 2009,[11] 19:20–21:3; Exs. 2011, 2012).

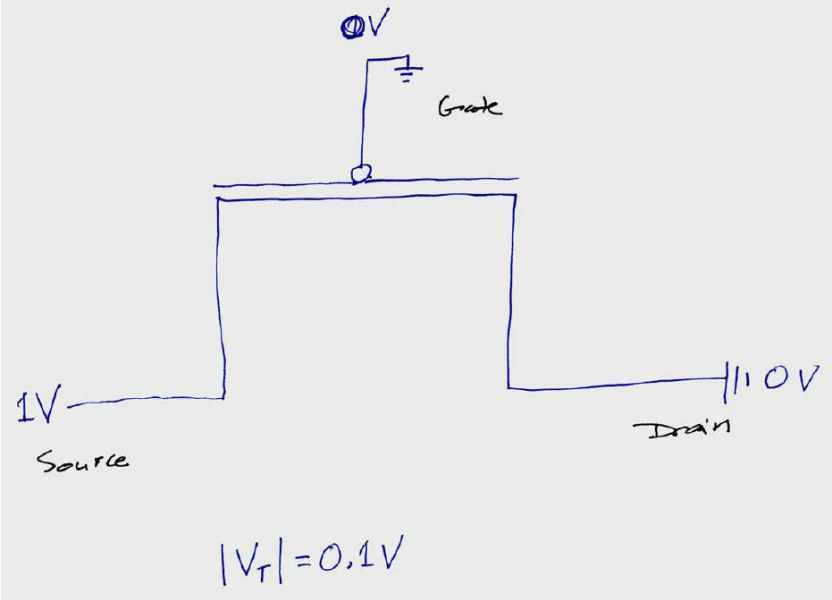
Patent Owner mischaracterizes Dr. Chapman's testimony. The record shows that, during the Second Deposition of Dr. Chapman, Patent Owner's counsel provided to Dr. Chapman hand-drawn diagrams (Exs. 2011, 2012) depicting NMOS or PMOS transistors and asked Dr. Chapman to label the source, the drain, and the gate of the depicted transistors based on Patent Owner's counsel's explanation of the voltages indicated on the diagrams. Ex. 2009, 18:21–20:8. When Dr. Chapman complied, Patent Owner's counsel asked how Dr. Chapman determined the location of the drain on the hand-drawn diagram on Exhibit 2012. *Id.* at 20:9–11. Dr. Chapman answered as follows:

> A. As you mentioned before, MOSFETs are symmetrical. So it's somewhat arbitrary. *Typically*, we *label* circuits in a style for PMOS that places the drain at the lower voltage and the source at the higher voltage. *That's the typical convention* that I've learned anyway.

Id. at 20:12–17 (emphases added).

[11] The Sur-reply mistakenly cites Exhibit 2013 as the record of the Second Deposition of Dr. Chapman.

The hand-drawn diagram on Exhibit 2012 Patent Owner's counsel provided to Dr. Chapman during the Second Deposition of Dr. Chapman is reproduced below.



The diagram above shows a schematic of a PMOS transistor Patent Owner's counsel provided to Dr. Chapman during the Second Deposition of Dr. Chapman, with Dr. Chapman's labeling of the source, the drain, and the gate of the transistor made during his deposition based on Patent Owner's counsel's explanations of the voltages indicated on the diagram. Ex. 2009, 18:20–19:18.

Thus, the record shows that, contrary to Patent Owner's assertion, Dr. Chapman did *not* make an "undisputed" admission during his Second Deposition that "for each symmetrical CMOS transistor *in each isolation path*, the electrode that is the 'source' and the electrode that is the 'drain' are *not fixed*, and *can switch back and forth* depending on which electrode is at a higher voltage potential." *See* Sur-reply 22 (emphases added); Ex. 2009, 18:20–20:17. Dr. Chapman's *labeling* of the source and the drain on the

schematic based on the "typical convention" of "labeling" a schematic of a transistor in general is a far cry from the alleged "undisputed" admission by Dr. Chapman that the "source" and the "drain" of a transistor in the isolation paths of the '588 patent "can switch back and forth depending on which electrode is at a higher voltage potential" during the operation the isolation paths. *See* Sur-reply 22; Ex. 2009, 18:20–20:17; Exs. 2011, 2012. More to the point, Dr. Chapman's testimony on the "typical convention" of "labeling" a schematic of a transistor in general says nothing about whether the '588 patent contemplates using transistors that can switch their sources and drains during operation, and, more specifically, whether the protection layer recited in claim 4 is expected or required to switch the sources and the drains of the recited N-channel devices and P-channel devices during the operation of the protection layer.

Regarding claim 4, Dr. Ipek opines in his Declaration that "[t]he devices in the protection layer's isolation paths in the corresponding embodiment are CMOS devices that *can flip* which of their terminals is the source and which is the drain depending on which terminal is at a higher voltage at any given point in time" and that claim 4 "recites the transistors' source and drain, and those can change with time." Ex. 2002 ¶ 89 (emphasis added). Dr. Ipek, however, does not explain adequately why the N-channel devices and the P-channel devices recited in claim 4 are expected or required to switch their sources and drains during the operation of the protection layer. *See id.* In addition, Dr. Ipek does not cite any supporting evidence. *See id.* Thus, we find Dr. Ipek's testimony unpersuasive as conclusory and unsupported.

More importantly, Patent Owner does not cite, nor do we discern, anything in the Specification that indicates or suggests that the '588 patent contemplates using transistors that can switch their sources and drains during the operation of the protection layer.

We note that the recitations of claim 4 corresponds to an exemplary embodiment described in the Specification (in reference to Figure 1) as follows:

> The protection layer 104 includes an N-channel transistor 113 having a source coupled to node 105 and another N-channel transistor 115 having a source coupled to node 111. VDDL is provided to the gates of transistors 113 and 115. The drain of transistor 113 is coupled to the drain of a P-channel transistor 117 and the drain of transistor 115 is coupled to the drain of another P-channel transistor 119. The source of transistor 117 is coupled to a node 121 and the source of transistor 119 is coupled to another node 123. . . . GNDH is provided to the gates of transistors 117 and 119.

Ex. 1001, 3:4–16. Patent Owner does not cite, nor do we discern, anything in the Specification that indicates or suggests the specific arrangement of the sources and drains of the transistors recited in claim 4 (and described in this embodiment) will change during the operation of the level shifter circuit.

Therefore, we find Patent Owner's argument and Dr. Ipek's testimony about flipping or changing back and forth of the sources and drains of the N-channel devices and P-channel devices recited in claim 4 unpersuasive as unsupported by evidence of record.

We also note that claim 4 is an apparatus claim reciting the specific arrangement of the transistors and nodes recited in the claim. That is, claim 4 recites limitations specifying that the sources of the N-channel devices are coupled to the first and second nodes, the sources of the

P-channel devices are coupled to the third and fourth nodes, and the drains of the N-channel devices are coupled to the drains of the P-channel devices. Ex. 1001, 17:34–49. By arguing these express recitations are "not fixed" (Sur-reply 22), Patent Owner is essentially asking we disregard all of the limitations recited in the body of claim 4. We declined to do so because, among other reasons, "meaning should be given to all of a claim's terms." *Dell Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1300 (Fed. Cir. 2016) (citing *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006)).

Based on the complete record, we agree with Petitioner that claim 4 does not require the recited "protection layer" perform the alleged "push/pull" function. Because independent claim 1 must encompass the subject matter of its dependent claim 4, we determine, absent a compelling reason to the contrary, claim 1 does not require the "protection layer" and the "isolation paths" to operate in a "push/pull" configuration.

Next, Petitioner points to a preferred embodiment described in the Specification and asserts that the alleged "push/pull" operation is not possible under the voltage conditions specified in the preferred embodiment. Reply 12–15. Petitioner asserts that the '588 patent discloses "[i]n the more specific embodiments illustrated herein, the lower voltage range [that is, the voltage across any specific transistor] is up to 1.2 V whereas the higher or full voltage range is between ground (0 V) and 3.3–3.6 V." *Id.* at 12 (citing Ex. 1001, 1:37–41). Citing the testimony of Dr. Chapman, Petitioner argues that when these voltage conditions are applied to up-shift circuit 100 of the '588 patent, "VDDH must be at least 3.3 V, GNDH must be greater than or equal to 2.1 V (3.3 V minus 1.2 V), VDDL must be less than or equal 1.2 V, and GNDL must equal 0.0 V." *Id.* (citing Ex. 1013 ¶ 8). Petitioner further

asserts that because the voltages at the third and fourth nodes are always between VDDH and GNDH, the voltages at those nodes will range from 2.1 volts to 3.3 volts. *Id.* (citing Ex. 1001, 4:23–26; Ex. 1013 ¶ 9). Petitioner similarly contends that because the voltages at the first and second nodes are always between VDDL and GNDL, the voltages at these nodes will range from 0.0 volts to 1.2 volts. *Id.* (citing Ex. 1001, 4:20–23; Ex. 1013 ¶ 9). Thus, Petitioner argues that in this preferred embodiment "the voltage at the third node *is always* greater than the voltage at the first node, and the voltage at the fourth node *is always* greater than the voltage at the second node." *Id.* at 13 (citing Ex. 1013 ¶ 10).

Petitioner argues, therefore, in this preferred embodiment, current will never flow up from the first node to the third node to "push" the voltage in the third node to a higher voltage level.[12] *Id.* at 14 (citing Ex. 1013 ¶¶ 11, 12). Petitioner similarly contends that because the voltage at the fourth node is always greater than the voltage at the second node, current will never flow up from the second node to the fourth node to "push" the voltage in the fourth node up to a higher voltage level. *Id.* (citing Ex. 1013 ¶¶ 11, 12). Petitioner argues, therefore, no "push/pull" operation is possible in this preferred embodiment. *Id.* at 15.

In its Sur-reply, Patent Owner asserts that the disclosure of the '588 patent cited by Petitioner appears in the "Background of the Invention" section of the Specification, and, therefore, does not relate to any "voltage range experienced by an individual level shifter" disclosed in the '588

[12] Citing the deposition testimony of Dr. Ipek, Petitioner notes the undisputed fact that current can only flow from a higher voltage to a lower voltage. Reply 13 (citing Ex. 1012, 110:13–111:5).

patent. Sur-reply 7, 9. To the extent Patent Owner argues the disclosure relied upon by Petitioner is not part of any embodiment of the invention described in the '588 patent, we disagree with Patent Owner's argument because the cited passage states that it describes the voltage ranges of "the more specific *embodiments* illustrated herein." Ex. 1001, 1:37–38 (emphasis added).

Next, Patent Owner contends that applying the specific voltages to the level shifter circuit of Figure 1, as proposed by Petitioner, is inconsistent with the disclosures of the '588 patent because doing so would break the thin-gate oxide transistors used in the circuit. Sur-reply 9–16. To prove its point, Patent Owner goes through a series of calculations and circuit analysis under Petitioner-specified voltage conditions to determine the voltages allegedly experienced by each transistor, inverter, node, and terminal of the level shifter circuit, when the input to the level shifter circuit is at logic high (1.2 volts). *Id.* at 10–16. Based on its calculations and circuit analysis, Patent Owner asserts that at least two transistors, namely, transistors 115 and 117 in the protection layer, would experience a voltage range of 2.1 volts across their terminals. *Id.* at 11–16. Patent Owner argues that 2.1 volts is greater than "the maximum 1.5 V voltage range that the Patent teaches will *break* the thin-gate transistors used for those transistors in the preferred embodiments." *Id.* at 16 (citing Ex. 1001, 4:29–36).

Patent Owner acknowledges, however, that under Petitioner specified voltage conditions, "[t]ransistors 117 and 115 are *off*, so they *will not pass voltage potential* from the lower electrode to the upper electrode and vice versa." *Id.* at 14 (emphases added). Patent Owner's argument is unpersuasive because Patent Owner does not explain adequately how

turned-off transistors that cannot "pass voltage potential" (or pass current) across their electrodes would "experience" a voltage potential across their electrodes to cause them to break. *See id.* at 16.

Based on the complete record and the foregoing discussion of the arguments and evidence presented by Petitioner and Patent Owner, we determine that, absent a compelling reason to the contrary, claim 1 does not require the recited "protection layer" and "isolation paths" to operate in a "push/pull" configuration.

(iv) Whether the Specification Compels Claim Interpretation Requiring "Push/Pull"

Patent Owner appears to argue that the facts of this case present a compelling reason to depart from the general rule against importing limitations from a particular embodiment described in the Specification. In its Response, Patent Owner asserts that the "push/pull" configuration described in the Specification is "a key aspect to the invention described and claimed by the Patent" (PO Resp. 51) because it relates to a purpose of the invention, which is to provide "improved noise immunity" (*id.* at 49–50 (citing Ex. 1001, 1:7–9)). Patent Owner also contends that "[t]he distinction between 'push/pull' and 'only pull' is critical to a core purpose of '588 embodiments: noise immunity." *Id.* at 36. Citing *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142 (Fed. Cir. 2012), Patent Owner asserts that the challenged claims should be interpreted narrowly to be restricted to this "purpose of the invention." PO Resp. 24 (citing *Abbott Diabetes Care*, 696 F.3d at 1149).

As discussed above, in general "a particular embodiment appearing in the written description may not be read into a claim when the claim language

is broader than the embodiment." *SuperGuide*, 358 F.3d at 875. Established exceptions to this general rule include lexicography and disavowal. *See, e.g.*, *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal") (citation omitted). Here, Patent Owner does not argue lexicography or disavowal.

Courts have also recognized that, under certain circumstances, "the embodiments of the invention set forth in the specification constituted the invention itself, in spite of claim language that could, in the abstract, be interpreted more broadly." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 907 (Fed. Cir. 2004); *see also Wisconsin Alumni Research Found. v. Apple Inc.*, 905 F.3d 1341, 1351 (Fed. Cir. 2018) ("Where . . . a patent repeatedly and consistently characterizes a claim term in a particular way, it is proper to construe the claim term in accordance with that characterization." (internal quotation marks omitted) (citations omitted)), *cert. denied*, 140 S. Ct. 44 (2019). "Whether a claim must, in any particular case, be limited to the specific embodiment presented in the specification, depends in each case on the specificity of the description of the invention and on the prosecution history." *Liebel-Flarsheim*, 358 F.3d at 907 (quoting *Cultor Corp. v. A.E. Staley Mfg. Co.*, 224 F.3d 1328, 1331 (Fed. Cir. 2000)); *see also In re Power Integrations, Inc.*, 884 F.3d 1370, 1375 (Fed. Cir. 2018) ("[T]he board must always "consider the claims in light of the specification and teachings in the underlying patent." (citation omitted)).

In *Abbott Diabetes Care* cited by Patent Owner, the Federal Circuit construed the disputed term "electrochemical sensor" under the BRI

standard to exclude "external connection cables or wires," in spite of the claim language lacking express requirement for such exclusion, because (1) "the claims themselves suggest connectivity without the inclusion of cables or wires," (2) "*every embodiment* disclosed in the specification shows an electrochemical sensor without external cables or wires," and (3) the patents at issue "'*repeatedly, consistently, and exclusively*' depict an electrochemical sensor without external cables or wires while simultaneously *disparaging* sensors with external cables or wires." 696 F.3d at 1149–50 (emphases added).

As discussed above, here, unlike *Abbott Diabetes Care*, there is nothing in the claim language that suggests that the recited "isolation paths" must operate in a "push/pull" configuration. In addition, unlike *Abbott Diabetes Care*, *not every embodiment* disclosed in the Specification here requires a "push/pull" function because, as discussed above, the Specification describes several embodiments where the "push/pull" operation is not possible. Similarly, here, in contrast to *Abbott Diabetes Care*, the Specification does *not* "repeatedly, consistently, and exclusively" describe that a protection layer or isolation paths must operate in a "push/pull" configuration because in several examples described in the Specification the protection layer and isolation paths cannot push up voltages or current. Nor is there any statement in the Specification disparaging "only pull" operations, which Patent Owner distinguishes from the "push/pull" operation (*see, e.g.*, PO Resp. 36, 51).

In *Abbott Diabetes Care*, the court also found that "the primary purpose of the invention" to provide "a small, compact device that can operate the sensor and provide signals to an analyzer without substantially

restricting the movements and activities of the patient" was a factor, in addition to the factors discussed above, supporting the restrictive construction of "electrochemical sensor" to exclude "external connection cables or wires." 696 F.3d at 1149.

In this case, Patent Owner asserts that "[t]he distinction between 'push/pull' and 'only pull' is critical to a core purpose of '588 embodiments: noise immunity." PO Resp. 36. Patent Owner argues that the "push/pull" configuration is "useful in providing noise immunity" (*id.* at 50 (citing Ex. 1001, 1:7–9)) because it "adds noise immunity to the circuit and helps the circuit reliably switch" (*id.* at 51 (citing Ex. 2002 ¶ 92). Patent Owner further asserts that the "'complementary' action" of the "push/pull" operation of the protection layer on "both [isolation] paths" "accomplishes the inventors' express goal of reducing susceptibility to noise" by "canceling [the noise] out between the isolation paths, one "pushing," the other one "pulling" the opposite direction." Sur-reply 5–6 (citing Ex. 1001, 1:59–66; 4:5–7, 4:64–5:1, 5:19–23; 9:55–58, 9:66–10:5, 10:36–40, 10:59–62; Ex. 2002 ¶¶ 33, 37–38, 43, 46, 61–62, 67, 68).

The cited passages of the Specification, however, do not describe that the "push/pull" operation is necessary to achieve improved noise immunity or reduced susceptibility to noise. For example, the Specification states as follows in the "BACKGROUND OF THE INVENTION" section: "The present invention relates in general to electronic devices, and more specifically to a cascadable level shifter cell with improved noise immunity" (Ex. 1001, 1:7–9); "It is desired to implement level shifters and output buffers capable of operating between lower level chip voltages and higher voltage peripheral components and circuits that are less susceptible to

noise." (*id.* at 1:64–66). These passages do not mention "push/pull" or two isolation paths conducting in opposite directions.

In paragraph 46 of his Declaration cited by Patent Owner, Dr. Ipek opines as follows:

> [T]he Figure 1 embodiment of the '588 Patent presents a circuit that, in response to the input signal, *cancels out noise* through *a "push/pull" action on both of its protective layer's isolation paths*. This *complementary "push/pull" action cancels out noise* because, when the two isolation paths conduct in opposite directions, any noise in the current on the two paths will tend to cancel each other out. . . . the Patent identifies process, temperature, and other environmental noise effects as all being addressed by *this complementary action*.

Ex. 2002 ¶ 46 (emphases added) (citing Ex. 1001, 4:61–5:11). Contrary to Dr. Ipek's testimony, the cited portions of the Specification do *not* describe that the "complementary action" of "push/pull" of the protection layer or the isolation paths "cancels out noise" or improves noise immunity. Instead, the Specification describes that canceling out noise or improved noise immunity is achieved by the complementary switching operation of the lower and upper circuits (i.e., the recited "first circuit" and "second circuit"), including the lower and upper nodes (i.e., the recited "first and second nodes" and "third and fourth nodes").

For example, the Specification states as follows: "The pair of *circuits 102 and 106, each including complementary switched nodes, significantly improves noise immunity* as compared to conventional level shift circuits." Ex. 1001, 4:61–63 (emphasis added). We find this passage to be a clear and unambiguous statement that improved noised immunity is achieved by the complementary switching performed by the first and second circuits.

Although the Specification next states "[t]he complementary switching of the lower nodes 105 and 111 of the lower circuit 102 between opposite voltage levels within the limits of the lower voltage range VDDL/GNDL *results in a push/pull function* of the corresponding nodes 121 and 123 of the upper circuit 106" (*id.* at 4:64–5:1 (emphasis added)), it does *not* state that this "push/pull function" reduces or cancels out noise in the system. Rather, the Specification states that "*[a]ny noise* in the system tends to *cancel* or is *otherwise compensated* by *the complementary switching action* to ensure dependable switching action regardless of environment changes, temperature variations, or process anomalies and variations." *Id.* at 5:5–10 (emphases added). These passages confirm the clear and unambiguous statement in the Specification discussed above that improved noised immunity is achieved by the complementary switching performed by the first and second circuits.

As discussed above, the Specification discloses several embodiments that do not allow a "push/pull" function, such as the embodiment where GNDH is higher than VDDL, as well as the embodiment corresponding to claim 4. In all of these embodiments, however, the level shifter circuit have the pair of lower and upper circuits (the recited "first circuit" and "second circuit"), each including complementary switched nodes, such that the upper circuit performs the complementary switching of the upper nodes in response to the lower circuit's complementary switching of the lower nodes. *See, e.g.*, *id.* at 4:15–26, 4:53–63. In other words, all of the embodiments discussed above include complementary switching by the first and second circuits, but *not* all embodiments require "push/pull." Because the Specification states unambiguously that the complementary switching

performed by the first and second circuits cancels out noise in the system or improve noise immunity, a "push/pull" function is *not* necessary to improve noise immunity or reduce noise in the system. Thus, to the extent improved noise immunity is a purpose of the invention, as Patent Owner argues, a "push/pull" function is not necessary to achieve that purpose. Accordingly, unlike *Abbott Diabetes Care*, Patent Owner's argument here about the purpose of invention of the '588 patent does *not* support a restrictive claim construction requiring a "push/pull" operation.

In summary, none of the factors existing in *Abbott Diabetes Care* are present in this case. Thus, claim construction in this case is governed by the general principle that "a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." *SuperGuide*, 358 F.3d at 875; *see also WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1323–24 (Fed. Cir. 2018) ("It is well established that claims are not limited to preferred embodiments, unless the specification clearly indicates otherwise." (citing *Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343, 1348 (Fed. Cir. 2010) ("[T]his court has repeatedly cautioned against limiting claims to a preferred embodiment."))). As discussed above, the Specification describes several embodiments that do not require a "push/pull" operation. Accordingly, based on the complete record and the foregoing discussion of the arguments and evidence presented by Petitioner and Patent Owner, we determine that the claim term "couples" recited in claim 1 does *not* require the isolation paths to operate in a "push/pull" configuration. Instead, we construe the claim term "couples" according to its plain meaning and determine that the term "couples"

encompasses potentially conductive paths that can conduct electricity under certain conditions.

Under this claim construction, we determine, based on the complete record and for the reasons explained by Petitioner in the context of claim elements 1[b] and 1[c] (Sections III.C.3.a(iii) & (iv) above), we determine that Petitioner has demonstrated sufficiently that Schucker discloses "a protection layer which couples said first and second nodes to third and fourth nodes via first and second isolation paths, respectively," as recited in claim 1.

We also note that the challenged independent claims, claims 1 and 17, include express recitations that "a first circuit . . . switches first and second nodes to opposite states" and "a second circuit . . . switches [the] third and fourth nodes to opposite states . . . in response to switching of [the] first and second nodes." Ex. 1001, 16:57–59, 16:66–17:3, 20:24–26, 20:37–39. Thus, to the extent that the descriptions in the Specification regarding noise immunity defines the invention or "constitute[s] the invention itself," *see Liebel-Flarsheim*, 358 F.3d at 907, the challenged claims expressly recite the operations of the recited first and second circuits that achieve noise immunity, i.e., the complementary switching of the lower and upper nodes of the first and second circuits.

As discussed above in the context of claim element 1[a] and claim element 1[d], Petitioner persuasively demonstrates that Schucker discloses "a first circuit . . . switches first and second nodes to opposite states" and "a second circuit . . . switches [the] third and fourth nodes to opposite states . . . in response to switching of [the] first and second nodes," as recited in claim 1. *See* Pet. 26–28, 40–42. As also discussed above, Patent Owner

does not contest Petitioner's argument that Schucker discloses the recitations of claim elements 1[a] and 1[d]. *See* PO Resp. 35–52. Thus, to the extent the challenged claims are to be construed to require noise immunity, we determine that Schucker discloses the claimed subject matter of noise immunity.

c. Conclusion on Claim 1

Based on the complete record and the foregoing discussion of the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has demonstrated sufficiently that Schucker discloses all limitations recited in claim 1. Accordingly, based on the complete record, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claim 1 is unpatentable under 35 U.S.C. § 102 as anticipated by Schucker.

4. Discussion — Independent Claim 17

Claim 17 is a method claim that recites limitations similar to the limitations recited in claim 1. *Compare* Ex. 1001, 16:56–17:11 (claim 1), *with id.* at 20:23–42 (claim 17). Petitioner largely refers to its discussion of the limitations of claim 1 to argue that Schucker discloses all of the limitations of claim 17. *See* Pet. 54–60. For instance, Petitioner asserts that Schucker discloses "providing a first circuit that switches first and second nodes within a first voltage range to opposite states in response to an input signal," as recited in claim 17, for the same reasons discussed in the context of claim element 1[a]. *Id.* at 54–55 (citing *id.* § IX.A.1.b.). Similarly, Petitioner contends that Schucker discloses "coupling the first node to a third node through a first isolation path which keeps the first node within the first

voltage range and which keeps the third node within a second voltage range," and "coupling the second node to a fourth node through a second isolation path which keeps the second node within the first voltage range and which keeps the fourth node within the second voltage range," as recited in claim 17, for the reasons discussed in the context of claim elements 1[b] and 1[c]. *Id.* at 55–57 (citing *id.* §§ IX.A.1.c., IX.A.1.d.).

Petitioner also addresses the limitations of claim 17 reciting "cross-coupling inverters between the third and fourth nodes and powering the inverters within the second voltage range for providing a second circuit coupled to the third and fourth nodes which switches the third and fourth nodes to opposite states within the second voltage range in response to switching of the first and second nodes," which Petitioner designates as claim element 17[d]. *Id.* at 57. Similar to its contentions on claim 1, Petitioner asserts that Figure 1 of Schucker and related text disclose all recitations of claim element 17[d]. *Id.* at 57–60 (citing Ex. 2:6–9, 2:12–16, 2:29–43, 2:51–53, 2:58–66, 3:1–3, 3:6–8, 3:33–35, 3:42–47, Fig. 1; Ex. 1004 ¶¶ 107–109).

First, Petitioner asserts that, as discussed in the context of claim elements 1[d], 1[e], and 1[f], Schucker discloses:

> "a second circuit [inverters 46, 48] that switches said third and fourth nodes [47, 49] to opposite states within said second voltage range [1.7 to 5 volts] between third and fourth supply voltages [the output of regulator 32 and node 44] in response to switching of said first and second nodes [15, 17];"
>
> "a first inverter [48] having an input coupled to said fourth node [49], an output coupled to said third node [47] and supply inputs coupled between said third and fourth supply voltages [the output of regulator 32 and node 44];"

> "a second inverter [46] having an input coupled to said third node [47], an output coupled to said fourth node [49] and supply inputs coupled between said third and fourth supply voltages [the output of regulator 32 and node 44]."

Id. at 57–58 (citing *id.* §§ IX.A.1.e., IX.A.1.f., IX.A.1.g.).

Citing the testimony of Dr. Chapman, Petitioner contends that a person of ordinary skill in the art would have understood that Schucker's inverter 46 (the recited "first inverter") and inverter 48 (the recited "second inverter") are "cross-coupling inverters" because of how Schucker describes the inputs and outputs of inverters 46, 48 as being coupled. *Id.* at 58–59 (citing Ex. 1004 ¶ 108). Specifically, Petitioner asserts that Schucker discloses that inverter 46 and inverter 48 are configured in a cross-coupled relationship as follows:

> The source of transistor 34 is coupled to an input of inverter 46 at node 47. The output of *inverter 46 is coupled to an input of inverter 48* at node 49. The source of transistor 36 is also coupled to node 49 and to an input of inverter 52. *The output of inverter 48 is coupled back to node 47 [input to inverter 46]*.

Id. at 58 (citing Ex. 1002, 2:38–43, Fig. 1). Petitioner further explains

> [T]he first and second inverters 46, 48 are described as forming a latch, which a POSITA would have also known as being provided by the cross-coupling relationship of inverters 46, 48. *See, e.g.*, [Ex. 1002,] 2:30–31, 2:37–49, 3:10–12, 3:46–47, 5:34–35, Fig. 1 . . . . The cross-coupled inverters of Schucker are between the third 47 and fourth 49 nodes. As shown in Figure 1 of Schucker, inverter 46 is between the third node 47 (at the input of inverter 46) and the fourth node 49 (at the output of inverter 46). *Id.* at 2:37–39 (Ex. 1002). Likewise, inverter 48 is between the fourth node 49 (at the input of inverter 48) and the third node 47 (at the output of inverter 48). *Id.* at 2:38–43 (Ex. 1002).

Pet. 59.

Petitioner further contends that, for the reasons discussed in the context of claim elements 1[e] and 1[f], inverters 46 and 48 are powered within the second voltage range between third and fourth supply voltages by the supply inputs provided to the inverters 46 and 48. *Id.* at 59 (citing *id.* §§ IX.A.1.f., IX.A.1.g.). Petitioner also asserts that, for the reasons discussed in the context of claim element 1[d], Schucker discloses the claimed "second circuit" that includes inverters 46, 48, such that inverters 46, 48 "provid[e] a second circuit coupled to the third and fourth nodes," as recited in claim 17. *Id.* (citing *id.* § IX.A.1.e.; Ex. 1004 ¶ 108). Thus, Petitioner argues that Schucker discloses "cross-coupling inverters between the third and fourth nodes and powering the inverters within the second voltage range for providing a second circuit coupled to the third and fourth nodes which switches the third and fourth nodes to opposite states within the second voltage range in response to switching of the first and second nodes," as recited in claim 17. *Id.* at 59–60 (citing Ex. 1004 ¶ 109).

In its Response, Patent Owner largely refers to its claim construction and patentability arguments advanced in the context of claim 1 and similarly argues that Schucker does not disclose "coupling" recited in claim 17 under Patent Owner's proposed construction of the term requiring a "push/pull" operation. *See* PO Resp. 27–29, 52–54.

One notable additional argument Patent Owner makes in the context of claim 17 is its assertion that "claim 17's 'coupling' steps . . . are *both performed 'in response to an input signal*.'" *Id.* at 28 (emphasis added). We disagree with Patent Owner's argument because the "coupling" steps recite no such limitations. *See* Ex. 1001, 20:27–30 ("coupling the first node to a third node through a first isolation path which keeps the first node within the

first voltage range and which keeps the third node within a second voltage range"), 20:31–34 ("coupling the second node to a fourth node through a second isolation path which keeps the second node within the first voltage range and which keeps the fourth node within the second voltage range").

For this additional reason and the reasons discussed above in the context of claim 1, we disagree with Patent Owner's proposed claim construction and determine that the claim term "coupling" recited in claim 17 does *not* require the isolation paths to operate in a "push/pull" configuration. Instead, we construe the claim term "coupling" according to its plain meaning and determine that the term "coupling" encompasses potentially conductive paths that can conduct electricity under certain conditions.

Under this claim construction, we determine, based on the complete record and for the reasons explained by Petitioner in the context of claim 1 and additionally with respect to claim 17, that Petitioner has demonstrated sufficiently that Schucker discloses all limitations recited in claim 17. Accordingly, based on the complete record, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claim 17 is unpatentable under 35 U.S.C. § 102 as anticipated by Schucker.

5. Discussion — Dependent Claim 4

Claim 4 depends from claim 1 and further recites

> wherein said protection layer comprises:
>
> a first N-channel device having a gate receiving said second supply voltage, a source coupled to said first node and a drain;
>
> a first P-channel device having a gate receiving said third supply voltage, a source coupled to said third node and a drain coupled to said drain of said first N-channel device;

> a second N-channel device having a gate receiving said second supply voltage, a source coupled to said second node and a drain; and
>
> a second P-channel device having a gate receiving said third supply voltage, a source coupled to said fourth node and a drain coupled to said drain of said second N-channel device.

Ex. 1001, 17:34–49.

Referencing Figure 1 of Schucker and the accompanying text, Petitioner asserts that N-channel transistor 26 and P-channel transistor 34 of Schucker disclose "a first N-channel device" and "a first P-channel device," respectively, of claim 1's "protection layer," as recited in claim 4. Pet. 46–47 (citing Ex. 1002, 1:66–69, Fig. 1; Ex. 1004 ¶ 89), 48–49 (citing Ex. 1002, 2:9–11, Fig. 1; Ex. 1004 ¶ 92).

As discussed above with respect to claim limitation 1[b], Petitioner has shown sufficiently that transistors 26, 28, 34, and 36, as arranged in Figure 1 of Schucker disclose the "protection layer" recited in claim 1. *Id.* at 28–31. Addressing claim 4, Petitioner contends that N-channel transistor 26 (i.e., the claimed "first N-channel device") has a gate receiving 3.3 volts (i.e., the claimed "second supply voltage") from terminal 54. *Id.* at 47 (citing Ex. 1002, 1:66–69). Petitioner also asserts that the source of Schucker's transistor 26 is coupled to node 15 (i.e., the claimed "first node"). *Id.* (citing Ex. 1002, 1:66–2:1). Petitioner asserts that N-channel transistor 26 also has a drain. *Id.* (citing Ex. 1002, 2:32–33; Ex. 1004 ¶ 90).

Petitioner contends that P-channel transistor 34 of Schucker (i.e., the claimed "first P-channel device") has a gate that receives

1.7 volts (i.e., the claimed "third supply voltage") from regulator circuit 32. *Id.* at 49 (citing Ex. 1002, 2:9–16). Petitioner also argues that the source of transistor 34 is coupled to node 47 (i.e., the claimed "third node"). *Id.* (citing Ex. 1002, 2:37–38). Petitioner asserts that the drain of P-channel transistor 34 is coupled to the drain of N-channel transistor 26 (i.e., the claimed "first N-channel device"). *Id.* at 49–50 (citing Ex. 1002, 2:32–33; Ex. 1004 ¶ 93).

Similarly, Petitioner provides detailed explanations and specific citations to Schucker, describing in detail how N-channel transistor 28 and P-channel transistor 36 of Schucker respectively disclose "a second N-channel device having a gate receiving said second supply voltage, a source coupled to said second node and a drain" and "a second P-channel device having a gate receiving said third supply voltage, a source coupled to said fourth node and a drain coupled to said drain of said second N-channel device," as recited in claim 4. *Id.* at 50–54 (citing Ex. 1002, 1:66–69, 2:1–2, 2:33–34, 2:9–16, 2:39–41, Fig. 1; Ex. 1004 ¶¶ 95–100).

Patent Owner does not respond separately to Petitioner's challenge to claim 4 beyond Patent Owner's arguments advanced with respect to claim 1 discussed above. *See* PO Resp. 35–52.

Based on the complete record presented and for the reasons explained by Petitioner, we determine that Petitioner has demonstrated sufficiently that Schucker discloses all of the limitations additionally recited in dependent claim 4. Accordingly, based on the complete record, we determine that Petitioner has demonstrated, by a

preponderance of the evidence, that claim 17 is unpatentable under 35 U.S.C. § 102 as anticipated by Schucker. [13]

D. Obviousness of Claim 2 Over the Combination of Schucker and Maley or Over Schucker and the Knowledge of a Person of Ordinary Skill in the Art

In these asserted grounds of obviousness, Petitioner contends that claim 2 is unpatentable under § 103(a) over the combined teachings of Schucker and Maley or over the teachings of Schucker combined with the knowledge of a person of ordinary skill in the art. Pet. 60–74; Reply 22–24. Petitioner relies upon the Chapman Declaration (Ex. 1004) and the Chapman Reply Declaration (Ex. 1013) to support its positions. *Id.* In response, Patent Owner asserts that neither Schucker nor Maley teaches "thin gate-oxide devices" recited in claim 2. PO Resp. 29–34, 54–59; Sur-reply 25–27. Patent Owner also asserts that a person of ordinary skill would not have been motivated to modify Schucker or combine Schucker with Maley. PO Resp. 59–61; Sur-reply 27–28. Patent Owner relies on the Ipek Declaration (Ex. 2002) to support its positions. PO Resp. 54–61; Sur-reply 25–28.

Upon review of all of the parties' papers and after considering the evidence of record presented during this proceeding, for the reasons explained below, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claim 2 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Schucker and Maley. We determine, however, that Petitioner has not demonstrated, by a preponderance of the evidence, that claim 2 is unpatentable under 35 U.S.C.

[13] We also find that Patent Owner has waived any argument directed to the additionally recited claim limitations of claim 4. *See* Paper 9, 5.

§ 103(a) as obvious over Schucker combined with the knowledge of a person of ordinary skill in the art.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.[14] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze the asserted ground based on obviousness with the principles identified above in mind.

2. Overview of Maley (Ex. 1003)

Maley describes an improved gate oxide protected level shifter which has a higher speed of operation. Ex. 1003, code (57). As background, Maley describes that, due to developments in CMOS technologies, the thickness of the transistor gate oxides for forming the CMOS transistor devices is getting increasingly thinner. *Id.* at 2:3–6. According to Maley, in a typical semiconductor process, the gate oxide layer is reduced to a

[14] Patent Owner does not present arguments or evidence of such secondary considerations in its Preliminary Response. Therefore, at this stage of the proceeding, secondary considerations do not constitute part of our analysis.

thickness of approximately 60 Å (angstroms) or less, and is likely to break down if a voltage of 2.4 to 2.5 volts or higher is applied across the gate. *Id.* at 2:6–10.

Maley describes that, in a level shifter circuit, P-channel transistors may be subject to a voltage difference of 3.3 volts across their drains and gates. *Id.* at 2:14–16. Thus, if the gate oxide thickness is 60 Å or less, the gate oxide in the transistors will experience a breakdown and the level shifter circuit will fail. *Id.* at 2:16–18. Maley describes that, to overcome this problem, prior art gate oxide protected level shifters used an arrangement of PMOS and NMOS transistors to limit the voltage difference at a gate oxide to be below a breakdown voltage. *Id.* at 2:18–23.

Figure 2 of Maley is reproduced below.

Fig. 2
Prior Art

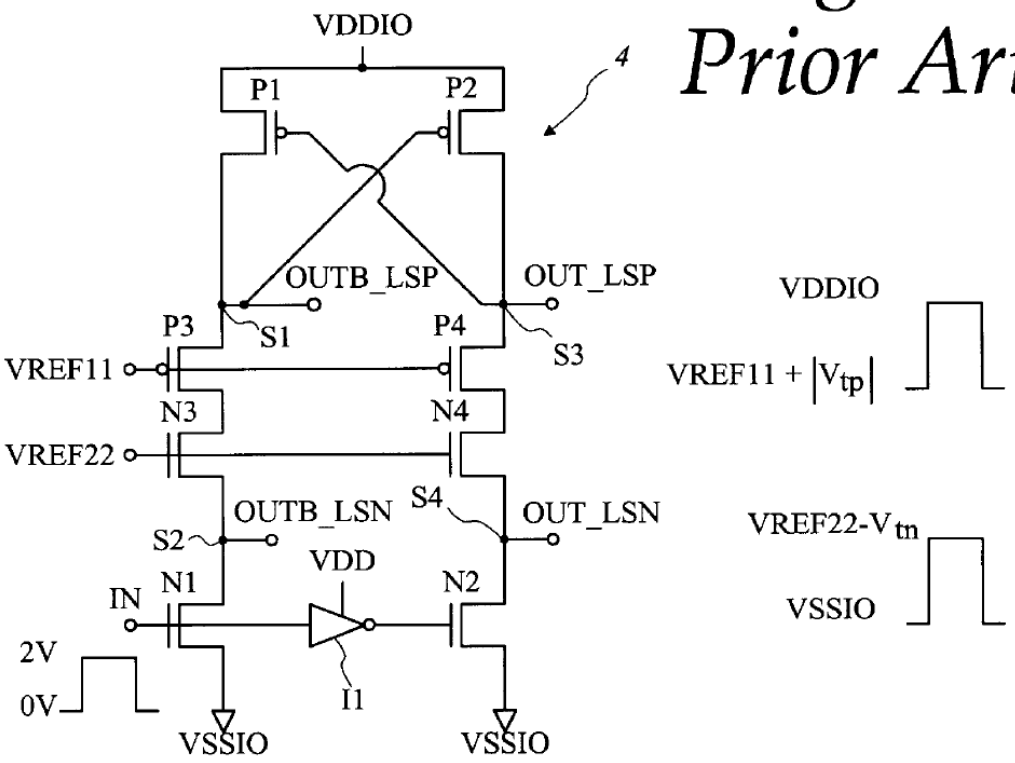


Figure 2 shows a schematic circuit diagram of a prior art gate oxide protected level shifter. *Id.* at 2:24–25.

As shown in Figure 2, level shifter 4 comprises a pair of cross-coupled P-channel MOS transistors P1 and P2, a pair of input N-channel transistors N1 and N2, and a CMOS inverter 11. *Id.* at 2:25–27. Level shifter 4 further includes PMOS transistors P3 and P4 and NMOS transistors N3 and N4, which function to prevent the gate oxide voltage of any transistor from exceeding a breakdown voltage. *Id.* at 2:30–34.

3. Claim Construction — "thin gate-oxide devices"

The parties' dispute in this proceeding over the patentability of claim 2 centers on whether Schucker or Maley teaches "thin gate-oxide devices" recited in claim 2. In the Petition, Petitioner points to the statement in the '588 patent that "[a]s used herein, the term 'thin-gate' refers to thin gate-oxide devices that are suitable for the lower voltage ranges but that would break down if exposed to higher voltage levels" (Pet. 62 (citing Ex. 1001, 1:31–36)) and asserts that a person of ordinary skill in the art would have understood that Schucker teaches "thin gate-oxide devices" because "the MOS devices in Schucker are described as not being able to withstand the full voltage range of the level shifter because of the gate oxide layer" (*id.*).

In its Response, Patent Owner asserts that a person of ordinary skill in the art would not interpret the claim term "thin gate-oxide devices" to include "Schucker's 3.3V-range devices" because the '588 patent defines such devices as "thick-gate" devices. PO Resp. 29.

We determine that the sentence from the '588 patent Petitioner relies on—i.e., "[a]s used herein, the term 'thin-gate' refers to thin gate-oxide

devices that are suitable for the lower voltage ranges but that would break down if exposed to higher voltage levels" (Ex. 1001, 1:33–35)—provides a lexicographic definition for the term "thin gate-oxide devices" because the phrases "[a]s used herein" and "the term 'thin-gate' refers to" indicate that the patentee was acting his own lexicographer and "clearly set forth a definition" of the term in the Specification. *See Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009) ("[W]e will adopt a definition that is different from the ordinary meaning when the patentee acted as his own lexicographer and *clearly set forth a definition* of the disputed claim term in either the specification or prosecution history." (emphasis added) (internal quotation marks omitted) (citation omitted)). In addition, we find the lexicographic definition, "thin gate-oxide devices that are suitable for the lower voltage ranges but that would break down if exposed to higher voltage levels," shows that the patentee "clearly, deliberately, and precisely defined the term" in the Specification. *See Sinorgchem Co., Shandong v. Int'l Trade Comm'n*, 511 F.3d 1132, 1136 (Fed. Cir. 2007).

Patent Owner argues that claim 2 recites "thin gate-oxide devices," not "thin-gate." Sur-reply 26. We do not find the differences in the precise wording of these terms to be a meaningful distinction in the context of the '588 patent because the Specification repeatedly uses terms "thin gate-oxide device" and "thin-gate device" interchangeably. *See, e.g.*, Ex. 1001, 4:26–36 (stating

> The transistors 101 and 107 are smaller *thin-gate* devices and the inverters 103 and 104 are implemented with *thin-gate* devices. *Thin-gate* devices are relatively fast but unable to withstand higher voltage levels, such as greater than 1.5 Volts (V). The

> voltage difference or range of VDDL and GNDL is sufficiently large to enable switching of the devices and yet sufficiently small to protect each *thin-gate* device of the circuit 102 from being exposed to excessive voltage levels. The transistors 113, 115, 117 and 119 of the protection layer 104 are also *thin-gate* devices.

(emphases added)). *Cf. Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1345 (Fed. Cir. 2016) ("[W]hen examining the written description for support for the claimed invention, we have held that the exact terms appearing in the claim need not be used *in haec verba*." (internal quotation marks omitted) (citation omitted)). We note that, as indicated above, the Specification also repeatedly describes that the "thin-gate" and "thin gate-oxide" devices are transistors.

As set forth above, the lexicographic definition of the disputed term does not state any specific voltage ranges for the "lower voltage ranges" or the "higher voltage levels." *See* Ex. 1001, 1:33–35. Nonetheless, Patent Owner contends that "devices that are capable of being exposed to a voltage range between 0V and 3.3–3.6V" are not "thin gate-oxide devices" recited in claim 2, but instead are "thick-gate" devices, because the Specification defines "thick-gate" as "devices capable of being exposed to a 0V–3.3V range." PO Resp. 30–31 (citing Ex. 1001, 1:35–40). The portion of the Specification cited by Patent Owner is reproduced below:

> The term "thick-gate" refers to thick gate-oxide devices that are capable of being exposed to the higher voltage ranges. In the more *specific embodiments* illustrated herein, the lower voltage range is up to 1.2 V whereas the higher or full voltage range is between ground (0 V) and 3.3–3.6 V.

Ex. 1001, 1:35–40 (emphasis added). These passages show that the '588 patent also provides an express definition for a "thick-gate" without stating

any specific voltage ranges for the term. Thus, the description of the "specific embodiments" in the Specification Patent Owner cites does not change the lexicographic definitions for "thick-gate" or "thin gate-oxide devices" to impose any specific voltage requirements. *See Martek Biosciences Corp. v. Nutrinova, Inc.*, 579 F.3d 1363, 1380 (Fed. Cir. 2009) ("When a patentee explicitly defines a claim term in the patent specification, the patentee's definition controls.").

We note that the '588 patent states that "[i]t is understood, however, that the *particular voltage levels and values are arbitrary* and may change over time, such that what is now called 'thin' may be considered 'thick' by tomorrow's standards." Ex. 1001, 1:40–44 (emphasis added). More importantly, the '588 patent states that "*[t]he present invention transcends* the particular voltage levels and ranges in that the configuration allows the lower voltage or thin-gate devices to be used in a buffer that switches higher voltage levels which would otherwise require higher voltage devices." *Id.* at 1:44–48. These passages about "the present invention" indicate that the claimed invention is not restricted to any voltage ranges and that the subject matter disclosed in the '588 patent is about the general approach of allowing the lower voltage or thin-gate devices to be used in a level shifter circuit that switches higher voltage levels, which would otherwise require higher voltage devices.

The description of exemplary embodiments in the '588 patent is also consistent with this understanding. For example, the Specification describes as follows:

> The transistors 101 and 107 are smaller thin-gate devices and the inverters 103 and 104 are implemented with thin-gate devices. Thin-gate devices are relatively fast but unable to withstand

> higher voltage levels, *such as* greater than 1.5 Volts (V). The voltage difference or range of VDDL and GNDL is sufficiently large to enable switching of the devices and yet sufficiently small to protect each thin-gate device of the circuit 102 from being exposed to excessive voltage levels. The transistors 113, 115, 117 and 119 of the protection layer 104 are also thin-gate devices. The transistors 113 and 115 receive VDDL at their gates thereby preventing the voltage of the lower circuit 102 from exceeding VDDL. The transistors 117 and 119 receive GNDH at their gates thereby preventing the voltage of the upper circuit 106 from falling below GNDH. Likewise, the upper circuit 106 is implemented with thin-gate devices and the voltage range of VDDH and GNDH is sufficiently large to enable switching of the thin-gate devices and yet sufficiently small to protect each thin-gate device from being exposed to excessive voltage levels. Yet VDDH is greater than VDDL and GNDH is greater than GNDL (for the up-shift configuration), so that the effective switching voltage level of the up-shift circuit 100 is shifted to a higher level. The voltage level across the entire up-shift circuit 100, or VDDH to GNDL, can exceed the allowable maximum voltage of any given thin-gate device since none of the devices are exposed to the entire voltage range.

Ex. 1001, 4:27–54 (emphasis added). The use of the phrase "such as" when referring to a specific voltage of 1.5 volts in the passages reproduced above, as well as the use of abstract symbolic names VDDL, VDDH, GNDL, and GNDH to describe the voltages applied to the thin gate-oxide devices, is consistent with the '588 patent's general statements about the claimed invention discussed above, such as "[t]he present invention transcends the particular voltage levels and ranges" and "the particular voltage levels and values are arbitrary."

Patent Owner further asserts that claim 2 recites "thin gate-oxide devices which are suitable for either of said first and second voltage ranges but which are not suitable to a full voltage range between said first and

fourth supply voltages," and, therefore, adopting the definition of "thin gate-oxide devices" from the Specification would render the recited claim language "suitable for either of said first and second voltage ranges but which are not suitable to a full voltage range between said first and fourth supply voltages" in claim 2 superfluous. PO Resp. 33–34. We are not persuaded by Patent Owner's argument because all that means is that the claim language of claim 2 tracks the lexicographical definition of the term "thin gate-oxide devices" provided in the Specification. Although we recognize that "narrowing a term by a superfluous limitation when the claims explicitly recited the narrowing limitation" is disfavored, *see Digital-Vending Servs. Int'l, LLC v. Univ. of Phoenix, Inc.*, 672 F.3d 1270, 1274–75 (Fed. Cir. 2012), we are also mindful that "no canon of [claim] construction is absolute in its application," *ERBE Elektromedizin GmbH v. Canady Tech. LLC*, 629 F.3d 1278, 1286 (Fed. Cir. 2010). More importantly, in our view, what we have in this case is *not* "narrowing a term by a superfluous limitation when the claims explicitly recited the narrowing limitation," but, rather, similarity between the claim language and the definition provided in the Specification.

Based on the complete record and the foregoing discussion, we construe the term "thin gate-oxide devices" according to the lexicographic definition provided in the Specification to mean "gate-oxide devices that are suitable for the lower voltage ranges but that would break down if exposed to higher voltage levels." Ex. 1001, 1:33–35. In particular, we determine that the recited "thin gate-oxide devices" are not restricted to any specific voltage ranges.

4. Discussion — Obviousness over Schucker and Maley

Claim 2 depends from claim 1 and additionally recites "wherein said first and second circuits and said protection layer each comprise thin gate-oxide devices which are suitable for either of said first and second voltage ranges but which are not suitable to a full voltage range between said first and fourth supply voltages." Ex. 1001, 17:12–17. Petitioner asserts that, according to the '588 patent, a thin gate-oxide device is a device, such as a transistor, that would break down if exposed to higher voltage levels, e.g., a voltage range including the lowest and highest voltages in a level shifter. Pet. 62 (citing Ex. 1001, 1:31–36; Ex. 1004 ¶ 112), 69 (citing Ex. 1004 ¶ 124).

Referencing Figure 1 of Schucker, Petitioner contends that Schucker teaches to use thin gate-oxide devices for transistors 26, 28, 34, and 36, i.e., the claimed "protection layer." *Id.* at 64 (citing Ex. 1002, 3:60–64), 69 (citing Ex. 1002, 2:17–31, 5:49–53), 72. Petitioner does not identify, however, any express teaching in Schucker for using thin gate-oxide devices for inverters 14 and 16 (i.e., the claimed "first circuit) and inverters 46 and 48 (i.e., the claimed "second circuit"). To address this deficiency, Petitioner asserts that Maley teaches using thin gate-oxide devices for inverters. *Id.* at 71–72 (citing Ex. 1003, 1:27–30, 1:50–54, 2:3–35, 4:50–51, 5:16–23; Ex. 1004 ¶ 128).

Petitioner argues that Maley discloses that inverters I1 and I101 depicted in Maley's Figures 2 and 3 are "CMOS devices" (*id.* at 70–71 (citing Ex. 1003, 1:27–30, 2:29, 4:50–51, Figs. 2, 3; Ex. 1004 ¶ 127)) and that a person of ordinary skill in the art would have understood that the CMOS inverters are made of N-channel and P-channel devices. *Id.* at 71

(citing Ex. 1003, 1:50–54). Petitioner asserts that a person of ordinary skill in the art would have understood that the N-channel and P-channel transistors in Maley's inverters are thin gate-oxide devices because Maley teaches that *all* transistors in the level shifters of Figures 2 and 3 are thin gate-oxide devices. *Id.* at 71–72 (citing Ex. 1003, 2:3–35, 5:16–23).

Petitioner contends that a person of ordinary skill in the art reading Schucker would have looked to Maley for its teachings because Maley and Schucker are both directed to level shifters having a first circuit, a second circuit, and a protection layer (*id.* at 72 (citing Ex. 1002, code (57), Fig. 1; Ex. 1003, Figs. 2, 3)) and both are directed to protecting their thin gate-oxide devices using protection layers (*id.* (citing Ex. 1002, 2:17–31, 2:61–66, 3:38–40, 5:49–53, Fig. 1; Ex. 1003, 2:3–54, 3:31–34, 4:38–47, 5:16–29, Figs. 2, 3; Ex. 1004 ¶ 129)).

Petitioner asserts that a person of ordinary skill in the art would have been motivated to combine the teachings of Schucker and Maley in the manner proposed by Petitioner (i.e., combining the thin gate-oxide transistors 26, 28, 34, and 36 of Schucker with Maley's CMOS inverters made of thin gate-oxide transistors) because a person of ordinary skill in the art would have been motivated to use only thin gate-oxide devices in the level shifter due to the known manufacturing complexities of mixing thin and thick gate-oxide devices. *Id.* at 73–74 (citing Ex. 1007, 1:26–29, 1:38–40, 2:36–40; Ex. 1008, 3:25–35; Ex. 1004 ¶ 130). Petitioner's declarant, Dr. Chapman, discusses the rationale to combine Schucker and Maley so as to use only thin gate-oxide devices in the level shifter, citing evidence in support of his testimony. Ex. 1004 ¶¶ 130, 117–119 (citing Ex. 1007 ("Hunt"), Ex. 1008 ("Mitarashi")).

As discussed above, Patent Owner asserts that Schucker does not teach the recited "thin gate-oxide devices" because "Schucker's 3.3V range devices are among the devices that the '588 Patent dubs 'thick-gate.'" PO Resp. 56 (citing Ex. 1001, 1:36–41). Patent Owner similarly argues that Maley does not teach the recited "thin gate-oxide devices" because "Maley's transistors have a maximum voltage range of 2.5V, over twice the range of the 'thin gate-oxide devices' taught in the '588 Patent." *Id.* at 58 (citing Ex. 1003, 5:16–23; Pet. 70). We disagree with Patent Owner's arguments because they are predicated on Patent Owner's proposed claim construction of "thin gate-oxide devices," which we do not adopt.

Patent Owner further contends that a person of ordinary skill in the art would not have been motivated to modify Schucker "to use only thin gate-oxide devices" in the proposed combination because Schucker's regulator 32 would be exposed to Schucker's full voltage range, and, therefore, cannot include "thin gate-oxide devices." PO Resp. 59–60 (citing Ex. 2002 ¶ 97).

We are not persuaded by Patent Owner's argument because Petitioner does *not* propose to "use only thin gate-oxide devices" for *all* elements of Schucker, including regulator 32. Rather, Petitioner asserts that the proposed combination of Schucker and Maley teaches the recited "first and second circuits" and "protection layer" of claim 2, all of which comprise "thin gate-oxide devices." *See* Pet. 68–74.

Based on the complete record and the foregoing discussion of the arguments and evidence presented by Petitioner and Patent Owner, we determine, for the reasons explained by Petitioner, Petitioner has shown sufficiently that the combination of Schucker and Maley teaches or renders obvious all additional limitations recited in claim 2. We also find that

Petitioner has provided sufficient articulated reasoning with rational underpinning why a person of ordinary skill in the art would have been motivated to combine Schucker and Maley as proposed by Petitioner.

Accordingly, upon considering the complete record, we determine that Petitioner has demonstrated, by a preponderance of the evidence, the subject matter of claim 2 would have been obvious under 35 U.S.C. § 103(a) over the combination of Schucker and Maley.

5. Discussion — Obviousness Over Schucker and the Knowledge of a Person of Ordinary Skill in the Art

In the alternative, Petitioner contends that claim 2 is unpatentable under § 103(a) over the teachings of Schucker combined with the knowledge of a person of ordinary skill in the art. Pet. 60–67. In our Decision on Institution, we questioned whether Petitioner was "using the knowledge of a person of ordinary skill in the art to supply any limitations *missing* from Schucker or to supply the *motivation to modify* Schucker, or both." Dec. on Inst. 37 (citing *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363 (Fed. Cir. 2016) ("In cases in which 'common sense' [or general knowledge in the art] is used to supply a *missing* limitation, *as distinct from a motivation to combine* . . . our search for a reasoned basis for resort to common sense must be searching." (emphases added))). Based on the record presented at the preliminary stage, we found that Petitioner did not explain adequately how, apart from Schucker itself, one of ordinary skill would have known about the limitation missing from Schucker, e.g., inverters made of thin gate-oxide devices. *Id.* at 37–38 (citing *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) ("In recognizing the role of common knowledge and common sense, we have emphasized the importance of a factual foundation to support

a party's claim about *what one of ordinary skill in the relevant art would have known*." (emphasis added))). Thus, based on the record presented at the preliminary stage, we found that the nature of Petitioner's obviousness argument based on Schucker combined with the knowledge of a person of ordinary skill in the art was not sufficiently clear to support a finding of reasonable likelihood for this asserted ground.

In its Reply, Petitioner does not adequately address our concerns, but instead only addresses its asserted ground based on Schucker and Maley. *See* Reply 22–25. Accordingly, based on the complete records, we determine that Petitioner has *not* demonstrated, by a preponderance of the evidence, the subject matter of claim 2 would have been obvious under 35 U.S.C. § 103(a) over the combination of Schucker and the knowledge of a person of ordinary skill in the art.

E. Patent Owner's Constitutionality Arguments

Patent Owner contends cancelling claims in this proceeding would contravene the Appointments Clause of the U.S. Constitution as *inter partes* review is unconstitutional when conducted by administrative patent judges not nominated by the President and confirmed by the Senate. PO Resp. 61. Patent Owner also argues that "[t]he Constitution also forbids retroactive application of IPR to the Patent, which was filed before the Leahy-Smith America Invents Act ('AIA'), Pub. L. No. 112-29, 125 Stat. 284 (2011) was enacted and issued before it took effect." *Id.* at 61–62.

We decline to consider these constitutional challenges as they have been addressed by the Federal Circuit in *Celgene Corp. v. Peter*, 931 F.3d

1342 (Fed. Cir. 2019) and *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019).

IV. CONCLUSION[15]

For the foregoing reasons, we conclude that Petitioner has met its burden of proof, by a preponderance of the evidence, in showing that claims 1, 2, 4, and 17 of the '588 patent are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 4, 17	102	Schucker	1, 4, 17	
2	103(a)	Schucker and Maley	2	
2	103(a)	Schucker and the knowledge of a person of ordinary skill in the art		2
Overall Outcome			1, 2, 4, 17	

[15] Should Patent Owner wish to pursue amendment of the challenged claim in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1, 2, 4, and 17 of the '588 patent are determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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