

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICROSOFT CORPORATION,
Petitioner,

v.

FG SRC LLC,
Patent Owner.

IPR2018-01599
Patent 6,076,152 B1

Before KALYAN K. DESHPANDE, JUSTIN T. ARBES, and
CHRISTA P. ZADO, *Administrative Patent Judges*.

ZADO, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We have authority to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision issues pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Microsoft Corporation (“Petitioner”)¹ has shown, by a preponderance of the evidence, that claims 11, 12, 15, and 18–21 (“challenged claims”) of U.S. Patent No. 6,076,152 (Ex. 1001, “the ’152 patent”) are unpatentable. *See* 35 U.S.C. § 316(e) (2012); 37 C.F.R. § 42.1(d) (2017).

A. Procedural History

Petitioner filed a Petition for *inter partes* review of claims 1–7, 11, 12, 15, and 18–21 of the ’152 patent. Paper 1 (“Pet.” or “Petition”). FG SRC LLC, (Patent Owner”)² subsequently filed a Preliminary Response. Paper 14 (“Prelim. Resp.”). On February 19, 2019, the Board entered a decision instituting an *inter partes* review of all claims and all grounds presented in the Petition. Paper 20 (“Institution Decision” or “Inst. Dec.”).

After institution, Patent Owner filed a Response to the Petition. Paper 37 (“Response” or “PO Resp.”). In the Response, Patent Owner states that it “surrenders challenged claims 1–7 of the ’152 Patent.” PO Resp. 4. In addition, on February 11, 2020, Patent Owner filed a statutory disclaimer of claims 1–7 of the ’152 patent. Paper 75 (Notice of statutory disclaimer); Ex. 2170 (statutory disclaimer). Accordingly, claims 1–7 have been

¹ Petitioner identifies only itself as a real party-in-interest to the Petition. Pet. 2.

² Saint Regis Mohawk Tribe, originally named as Patent Owner, assigned the ’152 patent to DirectStream, LLC on May 21, 2019. Paper 26, 1. DirectStream, LLC assigned the ’152 patent to FG SRC LLC on January 22, 2020. Paper 72, 1. Patent Owner identifies only itself as a real party-in-interest to this proceeding. *Id.*

removed from this proceeding. Petitioner filed a Reply to Patent Owner's Response. Paper 55 ("Reply"). Thereafter, Patent Owner filed a Sur-Reply to Petitioner's Reply to Patent Owner's Response. Paper 61 ("Sur-Reply").

An oral hearing was held on February 3, 2019. A transcript of the hearing is included in the record. Paper 77 ("Tr.").

B. Related Matters

The parties advise that the '152 patent has been subject to, or relates to, the following district court proceedings: *SRC Labs, LLC et al. v. Microsoft Corp.*, 2:18-cv-00321 (W.D. Wash.); and *SRC Labs, LLC et al. v. Microsoft Corp.*, 1:17-cv-01172 (E.D. Va.). Pet. 3; Paper 4, 1. Patent Owner further advises the following proceeding may affect or be affected by this proceeding: *SRC Labs, LLC and Saint Regis Mohawk Tribe v. Amazon Web Services, Inc. et al.*, 2:18-cv-00317 (W.D. Wash.). Paper 72, 1. Also, the following proceedings before the Board involve Petitioner and Patent Owner: IPR2018-01594, IPR2018-01600, IPR2018-01601, IPR2018-01604, and IPR2018-01605.

C. The '152 Patent

The '152 patent generally relates to a multiprocessor computer architecture incorporating multiple programmable memory algorithm processors ("MAP") in a memory subsystem, wherein the MAP may comprise one or more field programmable gate arrays ("FPGAs"). Ex. 1001, code(57).

The specification of the '152 patent ("Specification") describes general purpose computers, stating that they are flexible in that they can handle a variety of functions, but are slower than they would be if they were designed to handle only one particular function:

All general purpose computers are based on circuits that have some form of processing element. These may take the form of microprocessor chips or could be a collection of smaller chips coupled together to form a processor. In any case, these processors are designed to execute programs that are defined by a set of program steps. The fact that these steps, or commands, can be rearranged to create different end results using the same computer hardware is key to the computer's flexibility. Unfortunately, this flexibility dictates that the hardware then be designed to handle a variety of possible functions, which results in generally slower operation than would be the case were it able to be designed to handle only one particular function. On the other hand, a single function computer is inherently not a particularly versatile computer.

Ex. 1001, 1:15–30. The Specification states, however, that several groups had begun experimenting with creating a processor out of electrically reconfigurable circuits. *Id.* at 1:31–33. According to the Specification, this would allow the processor to be configured to execute particular functions more quickly than a processor of a general purpose computer, thereby accelerating application program execution speeds. *Id.* at 1:33–35. The Specification states, however, that certain functions cannot be implemented well in a system comprising reconfigurable processors due to limitations on the circuit densities that can be achieved. *Id.* at 1:35–39. In addition, systems including such reconfigurable processors intended for the processors to operate alone, which would present problems in high performance systems involving program applications that use several processors to solve a single problem. *Id.* at 1:41–47.

To address these issues, the Specification states that the inventors “developed a Memory Algorithm Processor (‘MAP’) multiprocessor computer architecture that utilizes very high performance microprocessors in

conjunction with user reconfigurable hardware elements.” *Id.* at 1:52–57. In a preferred embodiment, the MAP may comprise a Field Programmable Gate Array (“FPGA”). *Id.* at 1:62–64. The Specification discloses, particularly, a computer system including a *microprocessor* and one or more FPGAs:

Particularly disclosed herein is the utilization of one or more FPGAs to perform user defined algorithms in conjunction with, and tightly coupled to, a *microprocessor*. More particularly, in a multi-processor computer system, the FPGAs are globally accessible by all of the system processors for the purpose of executing user definable algorithms.

Id. at 1:66–2:4 (emphasis added). However, the Specification also discloses, broadly, a computer including a *data processor* and a MAP

Broadly, what is disclosed herein is a computer including at least one *data processor* for operating on user data in accordance with program instructions. The computer includes at least one memory array presenting a data and address bus and comprises a memory algorithm processor associated with the memory array and coupled to the data and address buses. The memory algorithm processor is configurable to perform at least one identified algorithm on an operand received from a write operation to the memory array.

Id. at 2:30–39 (emphasis added).

Figure 3 of the ’152 patent is reproduced below.

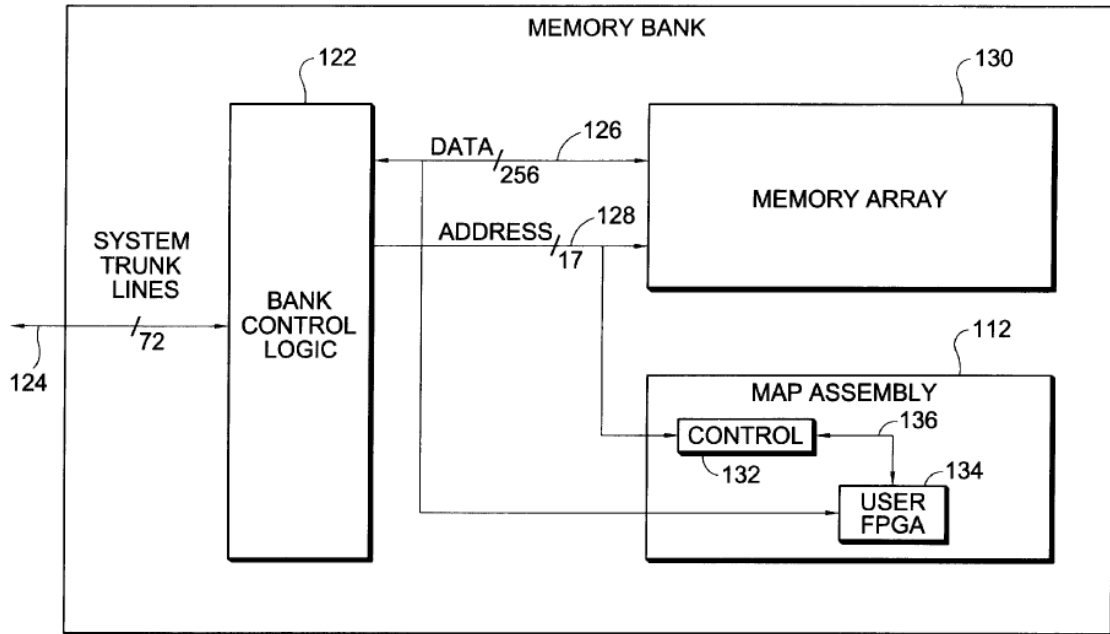


FIG. 3

120

Figure 3 is a functional block diagram of a memory bank for an individual MAP of Figure 2

Ex. 1001, Fig. 3. Figure 3 illustrates a preferred representation of memory bank 120 in MAP system computer architecture 100 that includes representative MAP 112. *Id.* at 3:47–49. Memory bank 120 includes bank control logic block 122 bi-directionally coupled to system trunk line bus 124 and to bi-directional data bus 126 and address bus 128. Buses 126 and 128 are coupled to memory array 130 and MAP assembly 112. MAP assembly 112 contains control block 132 and reconfigurable user FPGA 134, which are coupled to each other via signal lines 136. The Specification explains that bank control logic block 122 supplies an address on address bus 128 for accessing data at specified locations within memory array 130. *Id.* at 3:54–58. The Specification states that computer architecture 100 comprises multiple processors that use “uniform memory access across

common shared memory with one or more MAPs 112 located in the memory subsystem, or memory space.” *Id.* at 4:1–4.

According to the Specification, by placing MAP 112 in the memory subsystem, or memory space, MAP 112 can be accessed readily through the use of memory read and write commands, in contrast with conventional implementations that propose placement of reconfigurable logic in or near the processor such that only one processor has rapid access to the logic. *Id.* at 4:29–36. In a conventional system, reconfigurable logic must be placed near every processor in a multiprocessor system, which increases overall system cost, according to the Specification. *Id.* at 4:36–39.

D. Illustrative Claim

Of the challenged claims, claim 11 is independent. Claim 11, reproduced below with labeled limitations, is illustrative.

11. [a] a multiprocessor computer system comprising:
- [b] a plurality of data processors for executing at least one application program by operating on user data in accordance with program instructions;
 - [c] a memory bank having a data bus and an address bus connected to said plurality of data processors;
 - [d] a plurality of memory algorithm processors within said memory bank at plurality of individual memory addressable memory locations;
 - [e] means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus;
 - [f] said plurality of individual memory algorithm processors being individually memory addressable by all of said plurality of data processors; and
 - [g] said plurality of memory algorithm processors being individually configurable to perform an identified algorithm on an operand that is received from a write

operation by said at least one data processor to said memory bank as said at least one data processor executes said at least one application program.

Ex. 1001, 7:53–8:9 (letters and brackets added).

E. Prior Art and Asserted Grounds of Unpatentability

Petitioner raises the following challenges to claims 11, 12, 15, and 18–21. Pet. 3–4.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
11, 12, 18–21	102(b)	Halverson ³
11, 12, 15, 18–21	103(a)	Halverson
11, 12, 15, 18–21	103(a)	Halverson, Splash2 ⁴
15	103(a)	Halverson, Collins ⁵
15	103(a)	Halverson, Collins, Splash2
11, 12, 15, 18–21	103(a)	Halverson, Parkin ⁶
11, 12, 15, 18–21	103(a)	Halverson, Parkin, Splash2
15	103(a)	Halverson, Collins, Parkin

Petitioner relies on the declaration of Stephen Trimberger, Ph.D., Ex. 1003, to support its contentions.

II. ANALYSIS

A. Motions to Exclude

The party moving to exclude evidence bears the burden of proof to establish that it is entitled to the relief requested—namely, that the material

³ Richard Peyton Halverson, Jr., Ph.D., “The Functional Memory Approach to the Design of Custom Computing Machines,” Ph.D. diss., University of Hawaii, 1994. Ex. 1005 (“Halverson”).

⁴ Duncan A. Buell, Jeffrey M. Arnold, & Walter J. Kleinfelder, SPLASH2: FPGAS IN A CUSTOM COMPUTING MACHINE (1996). Ex. 1006 (“Splash2”).

⁵ U.S. Patent 5,671,355, filed Sep. 13, 1996 and issued Sep. 23, 1997. Ex. 1007 (“Collins”).

⁶ U.S. Patent 4,073,005, filed Jan 21, 1974 and issued Feb. 7, 1978. Ex. 1017 (“Parkin”).

sought to be excluded is inadmissible under the Federal Rules of Evidence. See 37 C.F.R. §§ 42.20(c), 42.62(a). For the reasons discussed below, Petitioner's Motion is *denied-in-part* and *dismissed-in-part*, and Patent Owner's Motion is *denied-in-part* and *dismissed-in-part*.

1. Petitioner's Motion to Exclude

a) Exhibits 2077 and 2096

Petitioner moves to exclude the declaration of one of the named inventors of the '152 patent, Jon Huppenthal (Exhibit 2077), "in its entirety as not being relevant to any issue on which trial has been instituted, and for lacking foundation, containing hearsay, and/or causing undue prejudice." Paper 62 ("Pet. Mot."), 3–6. Petitioner additionally moves to exclude portions of "Mr. Huppenthal's declaration (Ex. 2077 ¶¶ 80, 82–86) due to his refusal to answer questions concerning those portions of the declaration." *Id.* at 1–3 (citing Paper 50, 7–8).

Petitioner also moves to exclude a transcript (Exhibit 2096) of a deposition of Petitioner's declarant, Scott Hauck, Ph.D., from a different *inter partes* review (IPR2018-01604) as "not being relevant to any issue on which trial has been instituted, for containing hearsay, and/or causing undue prejudice." Pet. Mot. 6. Petitioner argues that allowing the transcript in the record would be "highly prejudicial as it presents itself with the indicia of expert testimony while being totally devoid from the necessary context of the matter from which it originates." *Id.* Patent Owner's declarant, Houman Homayoun, Ph.D, relies in his declaration on portions of Dr. Hauck's deposition transcript (Ex. 2104 ¶¶ 154–160). Paper 65 ("PO Opp. Mot."), 7.

Petitioner's Motion is dismissed as moot, as we do not rely on the material Petitioner seeks to exclude in a manner adverse to Petitioner in this Decision. As explained below, even if the testimony is considered, we are

not persuaded by Patent Owner's arguments regarding the state of the art or alleged nonobviousness of the challenged claims, and Patent Owner has not shown proof of secondary considerations that would support a conclusion of nonobviousness. *See infra* Sections II.C–II.D.

b) *Exhibits 2063, 2065, 2067, 2069, 2071–2073, 2076, 2082–2088, 2090, 2094, 2095, 2097–2103, 2105–2147, 2149, and 2162–2165*

Petitioner moves to exclude Exhibits 2063, 2065, 2067, 2069, 2071–2073, 2076, 2082–2088, 2090, 2094, 2095, 2097–2103, 2105–2147, 2149, and 2162–2165 as “not being relevant to any issues on which trial has been instituted, lacking foundation, and/or causing undue prejudice” because the exhibits were not discussed substantively and/or cited in Patent Owner's Response and Sur-Reply. Pet. Mot. 7–8. Petitioner's Motion is dismissed as moot, as we do not rely on the exhibits in a manner adverse to Petitioner in this Decision. We note that in evaluating Petitioner's asserted grounds of unpatentability, we consider only substantive arguments made by the parties in their papers during trial (i.e., the Petition, Response, Reply, and Sur-Reply). To the extent a document is filed in the record but never discussed in a paper, there is no substantive argument pertaining to that document to consider.

c) *Exhibits 2089 and 2090*

Petitioner moves to exclude Exhibits 2089 and 2090 as cumulative of other exhibits on the grounds that they appear to be duplicates of Exhibits 2079 and 2080, respectively. Pet. Mot. 8. Petitioner's Motion is dismissed as moot, as we do not rely on the exhibits in a manner adverse to Petitioner in this Decision.

d) Exhibits 2069 and 2076

Petitioner moves to exclude Exhibits 2069 and 2076 as “not being relevant to any issues on which trial has been instituted.” Pet. Mot. 8. Petitioner explains these exhibits are publications that were introduced during cross-examination of Petitioner’s declarant, and argues they are irrelevant because they were not discussed or cited in Patent Owner’s Response or Sur-Reply. *Id.* at 8–9. Petitioner’s Motion is dismissed as moot, as we do not rely on the exhibits in a manner adverse to Petitioner in this Decision.

e) Exhibits 2104 and 2148

Petitioner moves to exclude paragraphs 40 and 133 of the declaration of Patent Owner’s declarant, Dr. Homayoun, (Exhibit 2104) which refer to Exhibits 2084 and 2077. Pet. Mot. 9. Petitioner also moves to exclude paragraphs 156, 283, and 284 of the declaration of Patent Owner’s declarant, Steven Guccione, Ph.D. (Exhibit 2148), which refer to Exhibits 2077 and 2095. *Id.* Because we do not exclude the exhibits to which Dr. Homayoun and Dr. Guccione refer in their declarations, and do not rely on the paragraphs Petitioner seeks to exclude in a manner adverse to Petitioner in this Decision, we dismiss as moot Petitioner’s Motion with respect to Exhibits 2104 and 2148.

f) Patent Owner Response

Petitioner moves to exclude portions of Patent Owner’s Response referring to exhibits that Petitioner seeks to exclude. Pet. Mot. 10. Patent Owner’s Response is a paper with attorney arguments, not evidence that

may be excluded.⁷ Further, we do not exclude any of the exhibits referred to in the identified portions of the Response. Petitioner's Motion is denied as to Patent Owner's Response.

2. *Patent Owner's Motion to Exclude*

a) *Exhibits 1028, 1029, and 1030*

Patent Owner moves to exclude Exhibits 1028 and 1029 as unauthenticated under Federal Rule of Evidence 901. Paper 63 ("PO Mot."), 4–5. Patent Owner further moves to exclude exhibits 1028, 1029, and 1030 as inadmissible hearsay under Federal Rule of Evidence 802, asserting Petitioner's Reply cites to these documents to prove the truth of the technical matters disclosed therein. *Id.* at 5–6. Exhibits 1028 and 1029 are technical publications and Exhibit 1030 is a United States patent.

Petitioner submits Exhibits 1028 and 1029 are self-authenticating under Federal Rule of Evidence 902(6) and/or 902(7) because "each contain an IEEE trade inscription, copyright symbol, and [International Standard Book Number (ISBN)]." Paper 64 ("Pet. Opp. Mot."), 2–4 (citing *Ericsson Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41 at 12 (PTAB May 18, 2015) (IEEE publication authenticated under Fed. R. Evid. 901(b)(4)); *Liberty Mut. Ins. Co. v. Progressive Casualty Ins. Co.*, CBM2012-00010, Paper 59 at 37 (PTAB Feb. 24, 2014) (IEEE article self-authenticated under Fed. R. Evid. 902(6)); *ACCO Brands, Inc. v. PC Guardian Anti-Theft Prods.*, 592 F. Supp. 2d 1208, 1219 (N.D. Cal. 2008) (Macintosh Portable computers self-authenticated under Fed. R. Evid.

⁷ Petitioner did not seek authorization to file a motion to strike Patent Owner's Response. See Patent Trial and Appeal Board Consolidated Trial Practice Guide (Nov. 2019), 80–81, available at <https://www.uspto.gov/TrialPracticeGuideConsolidated> ("Trial Practice Guide").

902(7) “because they are inscribed with the Macintosh Portable trade name”)). Petitioner also argues Exhibits 1028 and 1029 are authentic under Federal Rule of Evidence 901(b)(4) based on the totality of the circumstances, namely that the papers are consistent with other papers published by the IEEE and nothing suggests they are not what they purport to be. *Id.* at 3–4. Petitioner also argues the exhibits are authentic as ancient documents under Federal Rule of Evidence 901(b)(8). *Id.* at 4–5. Specifically, each exhibit is over 20 years old and meets the requirements of Federal Rule of Evidence 901(b)(8). *Id.*

We agree with Petitioner that Exhibits 1028 and 1029 are self-authenticating under Federal Rules of Evidence 902(6) and 902(7), and that Exhibits 1028 and 1029 are ancient documents under Federal Rule of Evidence 901(b)(8) for the reasons stated by Petitioner. Pet. Opp. Mot. 2–5.

As to Patent Owner’s assertion that Exhibits 1028, 1029, and 1030 are inadmissible hearsay, Petitioner responds that these exhibits are not offered for the truth of the matters asserted, but rather are offered to show the understanding of a person of ordinary skill in the art. Pet. Opp. Mot. 5–6. Patent Owner does not identify any particular “statement” in any of the exhibits that is being offered “to prove the truth of the matter asserted in the statement,” PO Mot. 5–6, and thus fails to meet its burden to prove inadmissibility as hearsay. *See* Fed. R. Evid. 801(c); 37 C.F.R. § 42.20(c).

Accordingly, we deny Patent Owner’s Motion to Exclude Exhibits 1028, 1029, and 1030.

b) Exhibit 1026, 106:7–110:25

Patent Owner moves to exclude testimony from the deposition of one of the inventors of the ’152 patent, Mr. Huppenthal (Ex. 1026, 106:7–110:25), under Federal Rules of Evidence 401, 402, and 403, on the basis of

“form” objections stated at the following pages and line numbers of the deposition transcript: 104:20, 104:25, 105:5, 105:10, 105:20, 106:17, 107:13, 107:20, 108:19, and 109:6. PO Mot. 6–7. A motion to exclude “must identify the objections in the record in order *and must explain the objections.*” 37 C.F.R. § 42.64(c) (emphasis added). Patent Owner does not explain sufficiently its objections in the Motion to Exclude. Patent Owner vaguely asserts the deposing attorney’s questions were “vague and ambiguous because counsel introduces confusion regarding which particular computer system(s) he [was] asking about,” and “[t]he questions are also confusing because counsel does not specify any particular computer system or any particular patent claim in question.” PO Mot. 6. Patent Owner also asserts the questions are objectionable because they are tied to the scope of the patent claims, whereas Mr. Huppenthal was offered as a fact witness only. *Id.* at 6–7. Petitioner responds that the questions were neither vague nor confusing, and Mr. Huppenthal’s responses demonstrate he understood which computer systems and/or patent claim to which each question referred. Pet. Opp. Mot. 8–11. Petitioner responds further that questions about the challenged patent referred to statements in Mr. Huppenthal’s declaration about the patent, and therefore were within the scope of his declaration. *Id.* at 10–11.

Patent Owner’s Motion is dismissed as moot, as we do not rely on Exhibit 1027, 106:7–110:25, in a manner adverse to Patent Owner in this Decision.

c) Exhibit 1032, 10:3–20:4

Patent Owner moves to exclude testimony from Mr. Huppenthal’s second deposition (Exhibit 1032, 10:3–20:4) as not relevant under Federal Rules of Evidence 401, 402, and 403. PO Mot. 7–8. Patent Owner submits

Petitioner relies on this testimony in the Reply to support its arguments regarding construction of the claim term “means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus.” *Id.* According to Patent Owner, the questions posed to Mr.

Huppenthal are objectionable because they were not “tied in any way to the disclosures of the patent specification,” and instead related to potentially undisclosed and/or proprietary implementation details of real-world production systems. *Id.* Petitioner responds that Patent Owner has failed to meet its burden to show the testimony it seeks to exclude is irrelevant, because the testimony relates directly to statements Mr. Huppenthal makes in his declaration. Pet. Opp. Mot. 11–12. According to Petitioner, the line of questioning to which Patent Owner objects relates specifically to the statement in Mr. Huppenthal’s declaration that “[w]ith the exception of some of the technology described in [the ’152 patent], none of this new technology existed in the prototype system delivered to [] ORNL,” for which Mr. Huppenthal was asked “[w]hen you say ‘some of the technology’ there, what technology are you referring to?” Ex. 1032, 5:8–6:5; Ex. 2077 ¶ 80.⁸

Patent Owner’s Motion is dismissed as moot, as we do not rely on Exhibit 1032, 10:3–20:4, in a manner adverse to Patent Owner in this Decision. *See infra* Sec. II.C.5 (construction of the “means coupling” claim limitation).

⁸ Patent Owner submitted Mr. Huppenthal’s declaration as an exhibit in several related IPRs, not always as the same exhibit number. During the deposition, Petitioner’s counsel referred to Exhibit 2080—the exhibit number for Mr. Huppenthal’s declaration in a different IPR—which corresponds to Exhibit 2077 in this proceeding.

d) Exhibit 1033, 28:14–30:3

Patent Owner moves to exclude deposition testimony from Dr. Homayoun (Exhibit 1033, 28:14–20:4) taken in a different IPR proceeding that Patent Owner asserts is not relevant because it involves a patent with a priority date different from that of the '152 patent. PO Mot. 8–9. Patent Owner's Motion is dismissed as moot, as we do not rely on Exhibit 1033, 28:14–20:4, in a manner adverse to Patent Owner in this Decision.

e) Exhibits 1031 and 1035

Patent Owner moves to exclude Exhibits 1031 and 1035 under Federal Rules of Evidence 401 and 402 on the grounds that they are not cited in any paper submitted by Petitioner or any declaration in this proceeding. PO Mot. 9. Patent Owner's Motion is dismissed as moot, as we do not rely on the exhibits in a manner adverse to Patent Owner in this Decision. We note that in evaluating Petitioner's asserted grounds of unpatentability, we consider only substantive arguments made by the parties in their papers during trial (i.e., the Petition, Response, Reply, and Sur-Reply). To the extent a document is filed in the record but never discussed in a paper, there is no substantive argument pertaining to that document to consider.

f) Exhibits 1032, 1033, 1034, 1035, and 1036

Exhibits 1032, 1033, 1034, 1035, and 1036 each are deposition transcripts for declarants in this proceeding, including Mr. Huppenthal, Dr. Homayoun, and Dr. Guccione. Patent Owner moves to exclude “any uncited portion of each deposition testimony” under Federal Rule of Evidence 401, 402, and 403 on the grounds that Petitioner has failed to show that this testimony is relevant. PO Mot. 9. Patent Owner does not identify any specific testimony, and thus fails to meet its burden to show it is entitled to the relief it seeks. *See* 37 C.F.R. § 42.20(c). Furthermore, we note that

broadly excluding all uncited testimony is unwarranted. For example, uncited testimony surrounding cited testimony may be considered to provide context for the cited testimony. Accordingly, we deny Patent Owner's Motion as to these exhibits.

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art in the field of the '152 patent in the relevant time frame (1997) would have been a person with a Bachelor's degree in electrical engineering, computer engineering, computer science, or in a related field, and would have had four years of experience with the design or use of FPGA based systems or network adapters. Pet. 4. Petitioner asserts that, in the alternative, such a person would have had an advanced degree in one of those fields and two years of related experience. *Id.* at 4–5. Moreover, such a person, according to Petitioner, would have been knowledgeable about computer architectures and how FPGAs could be included in them. *Id.* at 5. Such a person also would have been knowledgeable about software algorithms that could be implemented on FPGAs and how to configure FPGAs to carry out such implementation. *Id.* (citing Ex. 1003 ¶¶ 39–40).

Patent Owner disputes Petitioner's assessment of the level or ordinary skill in the art, but does not provide a proposed level of ordinary skill in the art that we should apply in this proceeding.⁹ PO Resp. 34–36. Patent

⁹ Patent Owner's declarant, Dr. Homayoun, agrees with "the level of education and skill" that a person of ordinary skill in the art would have according to Petitioner. *See* Ex. 2048 ¶ 17; Ex. 2104 ¶ 123. Dr. Homayoun also testifies that a person of ordinary skill in the art would have had knowledge of "the unique problems involved with designing reconfigurable computer systems and programming FPGAs and FPGA based systems." Ex. 2048 ¶ 17.

Owner contends Petitioner's assessment is incorrect because a person of ordinary skill in the art would not have had the detailed FPGA knowledge assumed by Petitioner's definition. *Id.* Patent Owner further contends the technical problem the '152 patent sought to address is in the field of High Performance Computing ("HPC"). *Id.* at 4–25. Concatenating the experience Petitioner argues an artisan would have had with Patent Owner's assessment of the technical field, Patent Owner argues the result would have been a "mythical person" knowledgeable about both FPGAs and High Performance Computing. *Id.* at 34–36. According to Patent Owner, it would have been rare to find a person knowledgeable in both disciplines, and that any such person would have had more education and experience than that proposed by Petitioner. *Id.*

Patent Owner's assertions are unavailing. First, Patent Owner relies on the Declaration of Dr. Guccione to support its assertion that there were few engineers at the time of the '152 patent who knew how to program FPGAs to run software algorithms. PO Resp. 34–35 (citing Ex. 2148 ¶¶ 87, 196–201). Dr. Guccione testifies, for example, that implementing algorithms in FPGAs (i.e., hardware) is more complex than implementing algorithms in software, and therefore requires a different skillset. Ex. 2148 ¶ 87. We find Dr. Guccione's testimony, however, is at odds with what is reflected in the prior art of the period. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978); Reply 12 (arguing numerous prior art references disclose computer architectures using FPGAs in a manner similar to that disclosed in the '152 patent). For example, Halverson, a Ph.D. thesis by a doctoral student, describes programming FPGAs, therefore indicating Petitioner's assessment of the

education and experience required in the field of programming FPGAs is accurate. *See generally* Ex. 1005; *also see generally* Ex. 1006 (textbook about FPGA-based computing machines); Ex. 1007 (patent relating to a reconfigurable computer network interface device including FPGAs); Ex. 1028; Ex. 1029, 486; Ex. 1030, code (57).

Second, we find insufficient evidence that the level of ordinary skill in the art would have required specialized knowledge in the field of High Performance Computing. Patent Owner cites to portions of the '152 patent that describe enhancing overall processing speed in a multiprocessor computer architecture incorporating a number of memory algorithm processors, but has not shown why these systems are HPC architectures, much less limited to being HPC architectures. *Id.* at 4–5. The '152 patent does not limit the invention to HPC, but rather more broadly states that “[t]he present invention relates, in general, to the field of computer architectures incorporating multiple processing elements. More particularly, the present invention relates to a multiprocessor computer architecture incorporating a multiprocessor computer architecture incorporating a number of memory algorithm processors in the memory subsystem to significantly enhance overall system speed.” Ex. 1001, 1:8–14. The one mention of “high performance systems” in the '152 patent describes using hundreds or even tens of thousands of processors to solve a single problem in a timely manner. *Id.* at 1:41–49. This description, however, is non-limiting, and indicates a shortcoming of high performance systems, namely that issues such as sharing a single copy of an operating system may arise when hundreds or tens of thousands of processors are used to solve a single problem using reconfigurable processors. *Id.* This evidence does not

suggest the '152 patent is directed only to HPC systems involving multiple, much less hundreds or thousands, of processors.

Additional evidence suggests just the opposite. Claims 1–7 of the '152 patent (which Patent Owner surrendered during this proceeding) were directed to systems that included only one processor (i.e., “at least one processor”). PO Resp. 4; Ex. 1001, 6:52–7:6 (claim 1). Although Patent Owner surrendered this subject matter in response to our institution of review of these claims, Patent Owner made clear it did so for proceeding-induced reasons, explaining it did so “solely for purposes of avoiding distraction and focusing attention on the claims at the heart of the disclosures.” PO Resp. 4. Patent Owner affirmed it makes no admission the surrendered claims are unpatentable, and no such inference should be made. *Id.* Moreover, Patent Owner asserted infringement of claims 1–7 against Petitioner in the related district court case, thereby indicating Patent Owner considered a single processor system to be part of the invention. Ex. 1010, 2 (Patent Owner’s disclosure of asserted claims and infringement contentions). Also, claims 1–7 had already expired at the time of surrender—in other words, for the entire term of the patent, the owner of the '152 patent considered this subject matter to be part of the invention.

We also find unavailing Patent Owner’s argument that in assessing the level of skill in the art, Petitioner erred by focusing on the technical solution—using programmable computing elements—rather than on the technical problem to be solved. PO Resp. 36; Sur-Reply 8–9. Patent Owner provides no legal basis to support its contention that the only appropriate factor to consider in determining the hypothetical person of ordinary skill in the art is the technical problem to be solved. Contrary to Patent Owner’s assertion, several factors may be considered, including the types of problems

encountered in the art, prior art solutions to those problems, rapidity with which innovations are made, sophistication of the technology, and educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962–963 (Fed. Cir. 1986).

Moreover, such factors may or may not be present in every case, and one or more of the factors may predominate. *Id.* Here, we have considered the entirety of the '152 patent disclosure, and the prior art of record. Further, to the extent Patent Owner disputes the number of *actual* persons with the proposed education and technical experience at the time of the '152 patent, we note that “[t]he person of ordinary skill is a *hypothetical* person who is presumed to be aware of all the pertinent prior art.” *Custom Accessories*, 807 F.2d at 962 (emphasis added).

We note the '152 patent discloses use of FPGAs in the title of the patent, the Abstract, and Background of the Invention, in addition to being described throughout the patent specification and appearing in the claims. Specifically, the '152 patent is directed to *memory algorithm processors*, i.e., a reconfigurable element—*preferably an FPGA*. Ex. 1001, 1:54–65. The title of the patent is “Multiprocessor Computer Architecture Incorporating a Plurality of *Memory Algorithm Processors* in the Memory Subsystem.” *Id.* at code (54) (emphasis added). The Abstract discloses “[a] multiprocessor computer architecture incorporating a plurality of programmable hardware *memory algorithm processors* (‘MAP’) . . . The MAP may comprise one or more field programmable gate arrays (‘FPGAs’).” *Id.* at code (57) (emphasis added). The Background of the Invention states “[t]he present invention relates, in general, to the field of computer architectures incorporating multiple processing elements. More particularly, the present invention relates to a multiprocessor computer

architecture incorporating a number of *memory algorithm processors*.” *Id.* at 1:8–12 (emphasis added). In addition, Petitioner provides argument and evidence that, contrary to Patent Owner’s assertion, the problem addressed by the ’152 patent involves providing a flexible and reconfigurable computing platform, e.g., such as with FPGAs. Pet. 87 (citing Ex. 1001, 1:15–30). We agree with Petitioner. The Background of the Invention discloses there were problems with using reconfigurable circuits, acknowledging “[r]ecently, several groups have begun to experiment with creating a processor out of circuits that are electrically reconfigurable,” then stating there were a number of problems with using reconfigurable processors, e.g., FPGAs. Ex. 1:31–49.

For the foregoing reasons, we adopt Petitioner’s proposal as to the level of ordinary skill in the art, except that we do not include Petitioner’s proposal that the relevant field of experience would include, as an alternative to FPGAs, network adapters, as we discern no basis to include network adapters. Pet. 4. We note that had we not adopted Petitioner’s proposal that the relevant experience be specific to FPGAs—in particular, had we not articulated a specialty within the field of computer architecture—it would not have altered the outcome of this Decision. As we noted above, the level of skill in the art also may be reflected in the prior art. *See Okajima*, 261 F.3d at 1355; *GPAC*, 57 F.3d at 1579; *Oelrich*, 579 F.2d at 91. Halverson, Splash2, and Collins, for example, reflect the appropriate level of skill in the art, as we noted above. We also note that to the extent we determine Petitioner has demonstrated certain claims are unpatentable as obvious, below, we make such finding under an even lower level of skill than that suggested by Patent Owner’s arguments—namely, we determine the claims would have been obvious even without assuming the level of skill

in the art requiring specialized knowledge in the field of High Performance Computing. *See Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366 (Fed. Cir. 2012) (“[I]t is generally easier to establish obviousness under a higher level of ordinary skill in the art.”).

C. Claim Construction

1. Introduction

The parties agree that the ’152 patent has expired, and apply a district court claim construction standard. Pet. 8; Prelim. Resp. 18; *see also* PO Resp. 36 (adopting the district court claim construction standard). Accordingly, we apply the district court claim construction standard. *See* 37 C.F.R. § 42.100(b) (2017). Consistent with that standard, claim terms are given their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc)). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). We determine that the following terms require construction.

2. “*data processor*”

Claim 11 recites “a plurality of data processors for executing at least one application program by operating on user data in accordance with program instructions.” Ex. 1001, 7:54–56.

Prior to institution, Petitioner proposed to construe “data processor” as “a processor designed to execute instructions that operate on data.” Pet. 10. Patent Owner proposed to construe “data processor” as “a microprocessor.” Prelim. Resp. 23–25. At institution, we preliminarily determined that the term “data processor” is not limited to a “microprocessor,” but rather is properly construed as a “processor for operating on user data in accordance with program instructions or steps.” Inst. Dec. 11. Patent Owner now agrees that the term “data processor” is not limited to “a microprocessor,” and does not dispute that a “data processor” is a “processor for operating on user data in accordance with program instructions or steps.” PO Resp. 37–39. However, Patent Owner asserts that our construction does not capture a critical aspect of the term “data processor.” *Id.* at 38. Patent Owner asserts the proper construction of “data processor” is “a processor for operating on stored data in accordance with program instructions or steps that have been read by the processor from memory, which the processor executes on successive cycles of the processor clock.” *Id.* at 38. Petitioner disputes Patent Owner’s interpretation, but does not dispute the construction we adopted at institution. Reply 13–14.

We construe the term “data processor” as we did at institution, i.e., as a “processor for operating on user data in accordance with program instructions or steps.” Our construction is supported by the intrinsic record. The ’152 patent does not expressly define the term “data processor.” Therefore, we give the term its plain and ordinary meaning as would be

understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d 1313. Although the '152 patent does not expressly define the term, consistently throughout the entire Specification it indicates that a processor executes functions or programs defined by a set of steps or instructions. For example, the Specification states:

All general purpose computers are based on circuits that have some form of processing element. These may take the form of microprocessor chips or could be a collection of smaller chips coupled together to form a processor. In any case, these *processors are designed to execute programs that are defined by a set of program steps.*

Ex. 1001, 1:15–20 (emphasis added). The Specification also states that “[r]ecently, several groups have begun to experiment with creating a processor out of circuits that are electrically reconfigurable. This would allow the *processor to execute a small set of functions* more quickly and then be electrically reconfigured to execute a different small set.” *Id.* at 1:31–35 (emphasis added). Moreover, the Specification specifies that a *data* processor “operat[es] on user data in accordance with program instructions.” *Id.* at 2:30–32. The intrinsic record, therefore, supports our construction of the term “data processor.”

We reject Patent Owner’s proposed construction, which is not supported by the intrinsic record. Patent Owner does not cite to the intrinsic record to support its construction. PO Resp. 38–39. Specifically, Patent Owner, citing Dr. Guccione’s declaration, asserts “the patent specification makes clear that the ‘data processor’ of the invention is a von Neumann-style, stored instruction processor.” *Id.* at 38 (citing Ex. 2148 ¶¶ 213–214). Patent Owner further asserts that a “critical aspect of von Neumann

processors” is that they “store” instructions. *Id.* Patent Owner does not cite to any support in the intrinsic record, but instead relies on Dr. Guccione’s unsubstantiated testimony. *Id.* (citing Ex. 2148 ¶¶ 213–216). Dr.

Guccione’s cited testimony is conclusory, and entitled to little weight. Dr. Guccione asserts, without sufficiently providing the underlying basis for his testimony, that a skilled artisan would have understood that the following disclosure of the ’152 patent refers to a von Neumann style memory stored instruction set processor:

All general purpose computers are based on circuits that have some form of processing element. These may take the form of microprocessor chips or could be of a collection of smaller chips coupled together to form a processor. In any case, these processors are designed to execute programs that are designed to execute programs by a set of program steps.

Ex. 1001, 1:15–20¹⁰ (cited at Ex. 2148 ¶ 213). The disclosure Dr. Guccione cites (Ex. 1001, 1:15–20) does not explicitly refer to a von Neumann style architecture. Nor does it refer explicitly to “storing” instructions in a processor. As Petitioner points out, Dr. Guccione’s testimony is devoid of analysis. Reply 13–14. Dr. Guccione incorporates by reference over 40 pages of technical background regarding computer architecture to support his testimony. Ex. 2148 ¶¶ 213–215 (citing Section VI(B) of the declaration). But, citing to 40 pages improperly places the burden on the Board to ascertain what particular evidence Dr. Guccione relies on to support his assertion, and fails to provide adequate explanation to support Dr. Guccione’s testimony.

¹⁰ Dr. Guccione cites to the column and line numbers of U.S. Patent 6,247,110 B1 (“the ’110 patent”) (continuation of the ’152 patent). Ex. 2148 ¶ 181. Here, he cites to 1:23–27 of the ’110 patent, which corresponds to 1:15–20 of the ’152 patent.

Moreover, even if we were to find this disclosure in the Specification (Ex. 1001, 1:15–20) describes a von Neumann style architecture, Patent Owner has not shown this description is directed to the invention or intended to limit the invention. This disclosure merely provides background (it is part of the Background of the Invention), and the '152 patent expressly states it is a description of forms a processor “*may take*.” Ex. 1001, 1:15–20 (emphasis added). Patent Owner provides, and we discern, no evidence that this statement is intended to narrow the scope of the invention or to define the term “data processor.”

We also note Patent Owner provides no basis for including in the construction of “data processor” the requirement that the “processor executes on successive cycles of the processor clock.” PO Resp. 38–39. We discern no evidence in the record to support this construction. The claim language does not recite this feature, and we discern nothing in the '152 patent disclosure requiring this feature.

Finally, we note Patent Owner proposes that we construe the term “plurality of data processors” to mean “more than one data processor.” PO Resp. 39. Petitioner does not dispute this construction. We agree with Patent Owner that the plain and ordinary meaning of a “plurality of data processors” is “more than one data processor.” Accordingly, we construe “a plurality of data processors” in claim 11 to mean “more than one data processor.”

3. “*memory bank*”

Claim 11 recites “a memory bank having a data bus and an address bus connected to said plurality of data processors.” Ex. 1001, 7:57–58. Petitioner submit that the term “memory bank” should be construed as a

group of devices connected together, i.e., a bank, and used as a memory.

Pet. 11. Patent Owner proposes to construe the term “memory bank” as a collection of similar memory cell array devices, with the collection of memory cell arrays comprising the memory bank sharing electrical and physical connections such that on any memory cycle where *any* data within *any* array cell is read or written: (1) *all* of the array cells in the bank are accessible for memory transactions (through electrical activation and/or other prerequisites to memory access) and also (2) separate memory array cells within the bank are each capable of being accessed by various system processors *in parallel* with the other cell arrays on the same memory cycle.

PO Resp. 45–46. Petitioner responds that Patent Owner’s “narrow (and lengthy) construction for ‘*memory bank*’ [] has no support in the intrinsic record,” and that Patent Owner relies solely on extrinsic evidence and *ipse dixit* statements. Reply 14. For the reasons expressed below, we adopt Petitioner’s construction.

The ’152 patent does not expressly define the term at issue. Therefore, we give the term “memory bank” its plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d 1313.

The ’152 patent specification uses the term “memory bank” only four times:

The memory interconnect fabric 14 is then also coupled to M ***memory banks*** comprising ***memory bank*** subsystems 16₀ (Bank 0) through 16_M (Bank M)

Ex. 1001, 3:14–16 (emphases added);

With reference additionally now to FIG. 3, a preferred implementation of a ***memory bank*** 120 in a MAP system computer architecture 100 of the present invention is shown for a representative one of the MAPs 112 illustrated in the preceding figure. Each ***memory bank*** 120 includes a bank control logic block 122 bi-directionally coupled to

the computer system trunk lines, for example, a 72 line
bus 124

id. at 3:47–53 (emphases added). In addition, Figure 3 of the ’152 patent includes an illustrative example of a memory bank that includes bank control logic 122, memory array 130, MAP assembly 112, data bus 126, and address bus 128. *Id.* Fig. 3, 3:47–53. The intrinsic evidence, therefore, illustrates a memory bank as a collection of devices used as a memory, consistent with Petitioner’s proposed construction. *See also* Pet. 11–13 (Petitioner arguing the intrinsic evidence supports its construction).

Petitioner explains that its construction also comports with the plain meaning of the term “bank,” which one technical dictionary—*The New IEEE Standard Dictionary of Electrical and Electronics Terms*—defines as “[a]n aggregation of similar devices (for example, transformers, lamps, etc.) connected together and used in cooperation,” and another technical dictionary—*Microsoft Press Computer Dictionary*—defines as “[a]ny group of similar electrical devices connected together for use as a single device.” Pet. 10–11 (citing Ex. 1009, 92; Ex. 1008, 42). The latter dictionary further provides examples of a “bank” that are pertinent here because they relate to memory, even providing a “memory bank” as an example. Pet. 11 (citing Ex. 1008, 42 (defining “bank” as “[a] section of memory, usually a size convenient for a CPU to address,” and stating, “[f]or example, an 8-bit processor can address 65,536 bytes of memory; therefore, a 64-kilobyte (64-KB) memory bank is the largest that the processor can address at once.”)). In determining the ordinary and customary meaning of “bank” as understood by a person of ordinary skill in the art, it is appropriate to consult a general dictionary definition for guidance. *Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343, 1348 (Fed. Cir. 2010). Here, the technical dictionary

definitions of “bank” and “memory bank,” particularly in the *Microsoft Press Computer Dictionary*, relate specifically to computing and are consistent with the term’s use in the ’152 patent specification. We weigh this extrinsic evidence accordingly, and find it supports Petitioner’s proposed construction.

We agree with Petitioner that Patent Owner’s construction is unduly narrow and not supported by the intrinsic record. Reply 14. Patent Owner does not cite to, nor do we find, any evidence in the intrinsic record that supports importing the numerous limitations proposed by Patent Owner into the meaning of the term “memory bank.” PO Resp. 39–46. Instead, Patent Owner relies on the unsubstantiated testimony of Dr. Guccione that a skilled artisan would have understood the term “memory bank” as it is used in the ’152 patent to be a “term of art” within the field of High Performance Computing that had the very specific definition proposed by Patent Owner. *Id.*; *but see id.* at 41 (acknowledging that “the term has occasionally taken on additional meanings”). We find insufficient evidence in the record to support the assertion that a skilled artisan would have understood the ’152 patent’s use of the term “memory bank” to be directed specifically to High Performance Computing. As we discussed above, we are not persuaded that the ’152 patent specification is intended to limit the invention to High Performance Computing systems. *Supra* Sec. II.B. Mr. Huppenthal and Dr. Guccione also testified that a person of ordinary skill in the art would have understood the term “memory bank” to mean “a group of interconnected memory devices that are accessible by a processor through a single access port”—a definition that mirrors Petitioner’s construction in large part and includes none of the limitations proposed by Patent Owner in its construction. *See* Ex. 2077 ¶ 17; Ex. 1034, 173:12–20; *see also* Ex. 2043,

39:19–41:9 (similar testimony from Patent Owner’s other declarant, Tarek El-Ghazawi, Ph.D.).

We also find unpersuasive Patent Owner’s citation to examples of memory banks in CRAY computers (High Performance Computing systems) and selective citation to a specific type of memory system—i.e., interleaved memory system—in technical publications to support its definition of “memory bank.” PO Resp. 40–45 (citing Exs. 2078–2080; Ex. 2154; Ex. 2158). The documents are not dictionaries, and at best, they provide examples of memory banks used in specific CRAY High Performance Computing systems (Ex. 2078–2080) or other highly specific interleaved memory designs (Ex. 2154, Ex. 2158). Patent Owner selects various features in the exemplary, specific memory banks, without explaining sufficiently why these features are necessary for a group of devices to be considered a “memory bank” as this term is used in the ’152 patent. *Id.* In addition to three specific CRAY computer references (Ex. 2078–2080), Patent Owner relies on two specific examples of interleaved memory and disk systems in a textbook about memory systems that is roughly 600 pages, wherein the textbook states such interleaved memory is “usually given only minor attention.” PO Resp. 43 (citing Ex. 2154, 262 (Fig. 5.5), 266 (Fig. 5.6)); Ex. 2154, 231; *also see generally id.* at 231–256 (chapter dedicated to interleaved memory and disk systems as a specific type of memory system). Patent Owner also relies on an example, in a roughly 1000 page textbook about memory systems, of interleaved memory “deployed to overcome the shortcomings” of other DRAM systems that also are described in the book. PO Resp. 41; Ex. 2158, 442.

Both Patent Owner and Dr. Guccione omit reference to or mention of the non-interleaved systems described in these references. *See* PO Resp. 41–

45. The examples of interleaved memory systems are clearly neither intended to define the term “memory bank,” nor intended to limit the definition of the term “memory bank.” *See generally* Exs. 2078–2080; Ex. 2154; Ex. 2158. On the contrary, the second textbook upon which Patent Owner and Dr. Guccione rely explains how the term “memory bank” is used in the book, and the use is not limited to the interleaved memory example and is broader than Patent Owner’s construction: “the word *bank* is only used to denote a set of independent memory arrays inside a DRAM device.” Ex. 2158, 443; *see also id.* at 347 (stating that a “bank” is a “set of memory arrays that operates independently of other sets”).

For the forgoing reasons, we construe the term “memory bank” as “a group of devices connected together and used as a memory.”

4. “*individually [memory] addressable,*” “*memory address[ed],*”
“*individual memory addressable memory locations*”

The challenged claims recite the following recitations relating to the terms “individual memory addressable memory locations,” “individually memory addressable,” “[mutually] memory addressable,” and “memory accessible through normal memory access protocol”:

Claim	Term(s)
11	• “a plurality of [MAPs] within said memory bank at a plurality of <u>individual memory addressable memory locations</u>” • “said plurality of reconfigurable [MAPs] being <u>individually memory addressable</u> by all of said plurality of data processors”
12	• “wherein all of said plurality of [MAPs] are <u>memory addressable</u> by all of said plurality of data processors”
13	• “wherein all of said plurality of [MAPs] are <u>mutually memory addressable</u>”
19	• “wherein each of said plurality of [MAPs] is <u>memory accessible through normal memory access protocol</u>”

We preliminarily construed “memory addressable” to mean the MAPs can be accessed using a memory address, and “individually memory addressable” to mean a particular individual MAP may be accessed through use of a memory address. Inst. Dec. 16.

Patent Owner proposes to construe “memory addressable” as “a unit of memory storage that has an associated memory address that permits the memory storage unit to be addressed for memory transactions (*i.e.*, read or written).” PO Resp. 47. Patent Owner proposes the term “individually memory addressable” should be construed to mean that “a memory unit has a memory address that distinguishes it from all other memory units of the same type, and that it is capable of being addressed for memory transactions independently of all other memory units of the same type.” *Id.* Petitioner responds that we correctly construed “individually memory addressable” in the Institution Decision, and disputes Patent Owner’s proposed construction, arguing it finds no support in the intrinsic record and is based only on

attorney argument. Reply 15–16. For the reasons set forth below, we reject Patent Owner’s proposed construction, and adopt the construction set forth in the Institution Decision.

The ’152 patent does not expressly define the terms at issue. Therefore, we give these terms their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d 1313. We note further that the ’152 patent does not even use these terms at all, except in the claims. Moreover, these terms do not appear in the originally filed claims, but rather were added by amendment. Ex. 1002, 32–35 (originally filed claims); *id.* at 67–72 (amended claims). However, the Specification alludes to memory addressability, stating:

Still further provided is a computer system memory structure which includes one or more FPGAs for the purpose of using normal memory access protocol to access it

Ex. 1001, 2:16–18;

The computer architecture 100 comprises a multiprocessor system employing uniform memory access across common shared memory with one or more MAPs 112 located in the memory subsystem, or memory space

id. at 4:1–4; and

By placing the MAP 112 in the memory subsystem or memory space, it can be readily accessed through the use of memory read and write commands . . . [i]n contrast, other conventional implementations propose placement of any reconfigurable logic in or near the processor

id. at 4:29–34.

Also, with the amendment adding the terms at issue to claims of the ’152 patent, applicants remarked:

Cloutier does not provide a computer system wherein . . . the data processor's memory bank contains memory algorithm processors that are memory addressable by the data processor --- that is, the data processor views the memory algorithm processors merely as part of the data processor's memory

Ex. 1002, 75;

By placing MAPs 112 in the MEMORY SPACE that is associated with the plurality of PROCESSORS 108, any given MAP 112 can be readily accessed by a [sic] any given PROCESSORS 108 merely through the use of a memory read operation or a memory write operation

id. at 76; and

Critical to the whole of the presently claimed invention are the features . . . (4) Each of the processors 108 'views' each individual one of the plurality of USER FPGAs 134 merely as an individual memory addressable locations within memory bank 120; (5) Each of the USER FPGAs 134 is configured to act as a data processing machine when it is memory addressed by a data processor 108; (6) In this way, processors 108 can memory address any given USER FPGA 134, whereupon the addressed USER FPGA 134 operates as a secondary data processor to assist that processor 108 in the execution of the application program

id. at 79.

Accordingly, the intrinsic record provides that MAPs are viewed by the data processor as being part of the processor's memory, and therefore can be accessed by the processor by addressing the respective memory location. Having reviewed the claim language, the Specification, and the file history, we determine, on the full trial record, that "memory addressable" means that the MAPs can be accessed using a memory address, and that "individual[ly] memory addressable" means that a particular individual MAP may be accessed through use of a memory address. *See,*

e.g., Ex. 1002, 75 (“By placing MAPs 112 in the MEMORY SPACE . . . any given MAP 112 can be readily accessed by a [sic] any given PROCESSORS 108 merely through the use of a memory read operation.”).

We reject Patent Owner’s proposed constructions, which are not supported by the intrinsic record. Patent Owner does not cite to the intrinsic record to support its constructions, nor explain why a person of ordinary skill in the art would have understood the phrases to be limited as set forth in its proposed constructions. PO Resp. 47–48. Instead, Patent Owner relies on Dr. Guccione’s declaration, which is conclusory, and provides neither explanation nor citation to intrinsic evidence. He merely states his view as to what a skilled artisan would understand these terms to mean, without providing any underlying facts or evidence to support his testimony. Ex. 2148 ¶¶ 239–240. Accordingly, this testimony is entitled to little weight. 37 C.F.R. § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Finally, we note that prior to institution, Petitioner proposed that the MAPs in claim 11 must be accessible using “normal memory address protocol.” Pet. 18. In the Institution Decision, we rejected such interpretation as unduly narrow because dependent claim 19, which depends from claim 11, recites “wherein each of said plurality of memory algorithm processors is memory accessible through normal memory access protocol.” Inst. Dec. 16. During trial, neither party raised the issue of whether the memory accesses in claim 11 are limited to using “normal memory access protocol.” We maintain our preliminary interpretation.

5. *“means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus”*

The parties do not contest that the phrase “means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus” is governed by 35 U.S.C. § 112(6).¹¹ Pet. 19; PO Resp. 48. Each party identifies what it contends would be the recited function and corresponding structure(s), if the Board were to construe the phrase “means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus” under § 112(6). Pet. 18–22; PO Resp. 48–53; Reply 16–20; Sur-Reply 19–20.

The parties agree the recited function is “coupling said plurality of individual memory algorithm processors to said data bus and to said address bus.” Pet. 19; PO Resp. 49–50. The parties disagree as to the corresponding structure.

Petitioner argues Figure 3 shows three potential candidate corresponding structures. Pet. 19–22. Figure 3 of the ’152 patent, reproduced below, is illustrative.

¹¹ Paragraph 6 of 35 U.S.C. § 112 was renamed as paragraph (f) when § 4(c) of the Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284, 329 (2011) (“AIA”) took effect on September 16, 2012. Because the patent application resulting in the ’152 patent was filed before the effective date, we refer to the pre-AIA version of § 112.

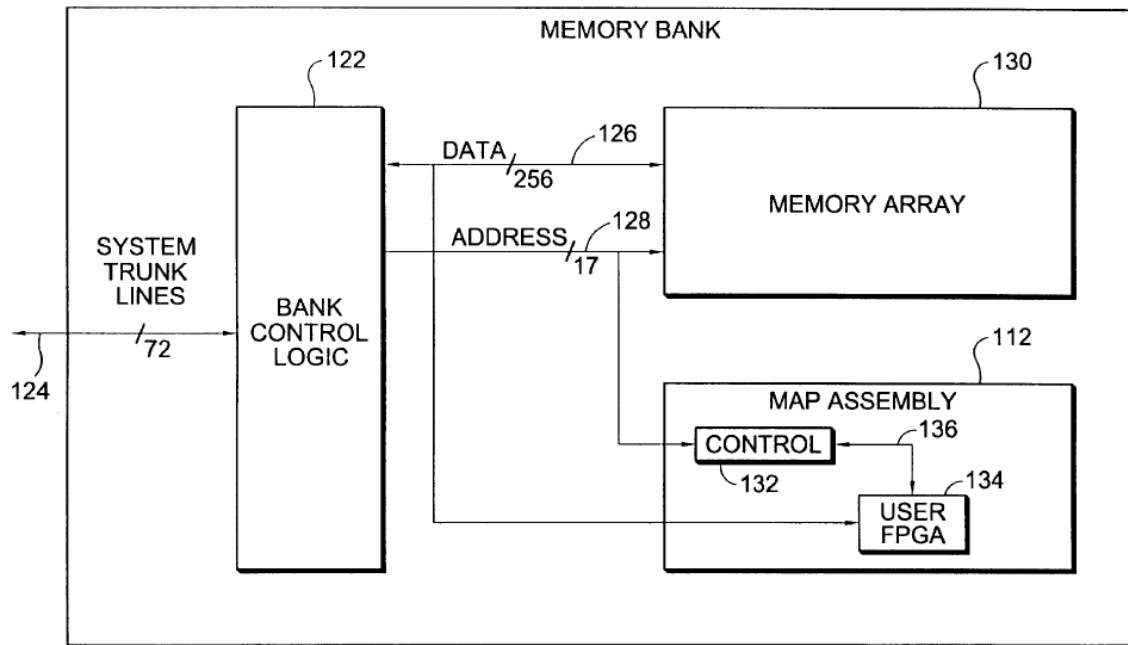


FIG. 3

Figure 3 depicts a functional block diagram of a memory bank comprising a MAP assembly, bank control logic, and memory array.

Ex. 1001, Fig. 3. Figure 3 depicts a functional block diagram of a memory bank comprising bank control logic 122 coupled to bi-directional data bus 126 and bi-directional address bus 128. The two busses are also coupled to MAP assembly 112 and memory array 130. *Id.* at 3:47–58. Petitioner rules out control block 132 as the corresponding structure because, according to Petitioner, it does not perform the recited function, namely it does not couple anything to the data bus. Pet. 20–21. As to the remaining two candidate structures—i.e., 1) bank control logic 122, and 2) the collection of wires and connectors that comprise the address bus and data bus themselves—Petitioner provides alternative unpatentability analyses depending on which structure the Board determines to be the corresponding structure. *Id.* at 21–22.

Patent Owner asserts the corresponding structure is bank control logic 122, data bus 126, address bus 128, control block 132, and MAP assembly 112. PO Resp. 50–53. Patent Owner argues the corresponding structure specifically must include the feature of “uniform memory access” because the ’152 patent specification recites this feature. *Id.* at 52 (citing Ex. 1001, 3:51–4:4¹²).

We determine the claim phrase at issue is governed by § 112(6) because the claim uses the word “means” followed by functional language and does not recite structure sufficient to perform the recited function. *Envirco Corp. v. Clestra Cleanroom, Inc.*, 209 F.3d 1360, 1364 (Fed. Cir. 2000). Moreover, we agree with the parties that the specified function is the language recited in claim 11, i.e., “coupling said plurality of individual memory algorithm processors to said data bus and to said address bus.”

As to the corresponding structure, per the claim language it is the structure that couples the plurality of individual MAPs to the data bus and address bus of the memory bank, wherein the buses are connected to the claimed plurality of processors. Ex. 1001, 7:57–58, 7:62–64. Figures 1 and 3 of the ’152 patent are illustrative. Figure 1 is reproduced below with Board annotations in red.

¹² Patent Owner appears to erroneously cite to column and line numbers of the ’110 patent that discuss control block 122 and “uniform memory access,” namely the ’110 patent at 3:58–4:11. *See* PO Resp. 52 (acknowledging the citation is to the ’110 patent). The corresponding column and line numbers in the ’152 patent are 3:51–4:4, which we assume Patent Owner intended to cite.

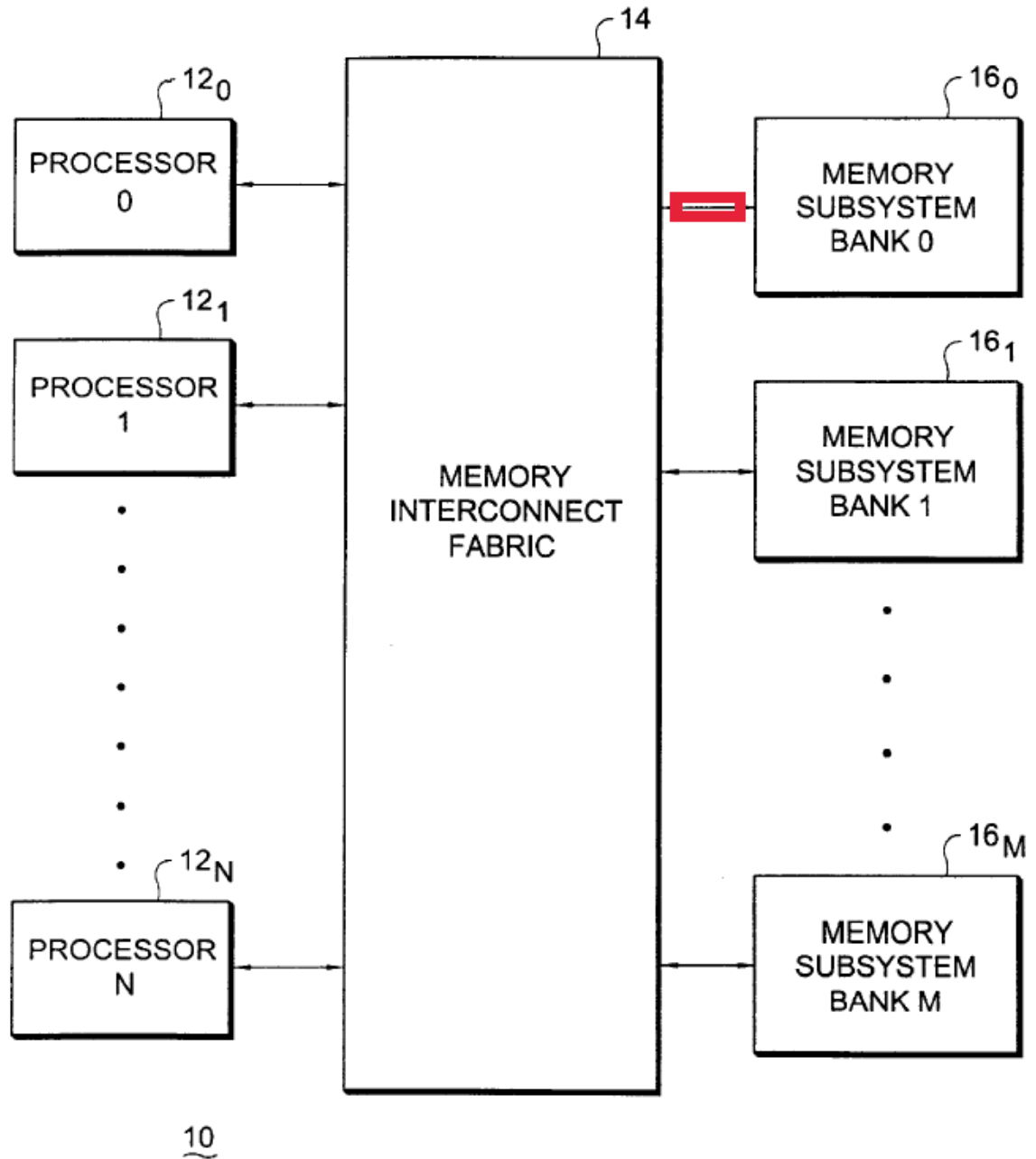


FIG. 1

Figure 1 is a high level functional block diagram of a multiprocessor architecture.

Ex. 1001, Fig. 1 (annotated). Figure 1 is a high level functional block diagram of a multiprocessor architecture. *Id.* at 2:59–60. Figure 1 shows a

plurality of processors 12_0 to 12_N , connected to a plurality of memory banks 16_0 to 16_N . *Id.* at 3:10–16. The plurality of processors connect to the plurality of memory banks through connections and memory interconnect fabric 14. *Id.*

We determine that line bus 124 shown in Figure 3 corresponds to “said data bus” and “said address bus,” as recited in the claim term at issue. The claim specifies that “said data bus” and “said address bus” are the data bus and the address bus of the memory bank, and that these buses are connected to the claimed plurality of processors. Ex. 1001, 7:57–58. As seen in Figure 1, the connection annotated in red is a bus of a memory bank, i.e., memory subsystem bank 0, and it is connected (via memory interconnect fabric 14) to a plurality of processors 12_0 to 12_N . *Id.* Fig. 1. We find that, like the connection annotated in red in Figure 1, line bus 124 shown in Figure 3 connects memory bank 120 to a plurality of processors.

According to the specified function, the coupling means must couple “said data bus” and “said address bus”—i.e., line bus 124—to a memory algorithm processor. We find MAP assembly 112 in Figure 3 corresponds to the memory algorithm processor. The Specification supports this finding, explaining, consistent with Figure 3, that each MAP “may comprise a Field Programmable Gate Array (‘FPGA’) operating as a reconfigurable unit.” Ex. 1001, 1:63–65.

Based on the foregoing, the structure corresponding to the specified function is the set of components coupling line bus 124 to MAP assembly 112. As shown in Figure 3, these components include bank control logic 122, data bus 126, and address bus 128. Ex. 1001, Fig. 3.

We disagree with Patent Owner that the corresponding structure includes MAP assembly 112, or any components therein, because MAP

assembly 112 is the thing that is coupled, not the coupling means itself.
PO Resp. 50–51.

We also disagree with Patent Owner’s argument that “the corresponding structure must include the disclosure of ‘uniform memory access’ that is recited in 3:58–4:11 of the ’110 Patent.” PO Resp. 52.¹³ Patent Owner asserts, without explanation, that “[t]his is the patent’s disclosed ‘Bank Control Logic’ that is essential for managing share memory access among the processors to the common shared memory.” *Id.* Patent Owner’s assertion is not persuasive because it is not supported with sufficient underlying explanation. Moreover, we find the cited disclosure of “uniform memory access” is not referring to bank control logic 122. The first portion of the disclosure Patent Owner cites describes Figure 3 (showing control logic block 122 within a single memory block); however the portion that discloses “uniform memory access” pertains to Figure 2 (showing multiple memory blocks and multiple processors). Ex. 1001, 3:51–4:4, Fig. 2, Fig. 3. The disclosure of “uniform memory access” states that computer architecture 100, i.e., the multiprocessor and multiple MAP system shown in Figure 2, “employ[s] uniform memory access across common shared memory with one or more MAPs 112 located in the memory subsystem, or memory space.” Ex. 1001, 4:2–4. Accordingly, “uniform memory access” refers to a feature relating to access across the multiple MAPs shown, for example, in Figure 2, rather than a feature of an individual memory bank (and control logic block 122 within such bank). Ex. 1001, 3:51–4:4, Fig. 2, Fig. 3. We therefore agree with Petitioner that the ’152

¹³ The corresponding column and line numbers in the ’152 patent are 3:51–4:4.

patent does not state clearly that the Bank Control Logic of Figure 3 is what implements the “uniform memory access” or clearly links such functionality to the recited function of the coupling means in claim 11. Reply 19–20.

For the foregoing reasons, we determine the phrase “means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus” is governed by § 112(6). The recited function is “coupling said plurality of individual memory algorithm processors to said data bus and to said address bus,” and the corresponding structure in the specification of the ’152 patent is bank control logic 122, data bus 126, and address bus 128, and equivalents thereof.

D. Asserted Unpatentability

As we noted above, Petitioner asserts that claims 11, 12, and 18–21 of the ’152 patent are unpatentable as anticipated by Halverson, and that claims 11, 12, 15, and 18–21 are unpatentable as obvious over Halverson, either alone or in combination with other prior art references. Pet. 30–91.

Patent Owner argues Petitioner has not shown unpatentability of the challenged claims.

For the reasons discussed herein, we determine Petitioner has demonstrated, by a preponderance of the evidence, that claims 11, 12, 15, and 18–21 are unpatentable.

1. Halverson as Prior Art

Halverson is a dissertation by Richard Peyton Halverson, Jr. titled, “The Functional Memory Approach to the Design of Custom Computing Machines.” Ex. 1005. Halverson states on the title page that it is a dissertation submitted to the graduate division of the University of Hawaii in partial fulfillment of the requirements for the degree of doctor of philosophy in communication and information sciences. *Id.* at Intro 1. Halverson is

dated August 1994. *Id.* The parties dispute whether Halverson was publicly accessible, and therefore, available as prior art under 35 U.S.C. § 102(b) as Petitioner asserts. *See* Pet. 22; PO Resp. 60.

A printed publication is not effective as a prior art reference until the date it becomes publicly accessible. *In re Hall*, 781 F.2d 897, 899 (Fed. Cir. 1986). “Whether a reference qualifies as a printed publication under § 102 is a legal conclusion based on underlying fact findings.” *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 772 (Fed. Cir. 2018). “A reference is considered publicly accessible if it was ‘disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, can locate it.’” *Id.*

Petitioner argues that Halverson was published in August 1994, and was indexed and shelved at the Hamilton Library at the University of Hawaii at Manoa (“Library”) as early as August 1994, and at least as of 1995. Pet. 22–23. Patent Owner asserts, without any underlying explanation, that “Petitioner offers no evidence to meet” its burden to show Halverson is a printed publication and “the Halverson reference is not a printed publication for purposes of this IPR.” PO Resp. 60. Contrary to Patent Owner’s assertion, Petitioner provides persuasive evidence that Halverson was publicly available.

Petitioner submits, with the Petition, the declaration of Dr. Halverson, Ex. 1018 (“Halverson Declaration”), in which he affirms that he submitted his dissertation to the Library and confirmed it was shelved at the Library at least since 1995. Ex. 1018 ¶ 8. He states that two months after submitting his dissertation, he visited the Library and confirmed it was indexed properly, including by “subject, title, and author.” *Id.* Dr. Halverson

confirmed its public accessibility by looking it up in the catalog indexing system and finding it on the shelf in its correctly indexed location. *Id.* Dr. Halverson further states that it was the policy of the Library to make publications like his dissertation available publicly on or shortly after the date on which the publication is received. *Id.* ¶ 9.

Dr. Halverson's testimony is corroborated by the declaration of James L. Mullins, Ph.D. Ex. 1019. Dr. Mullin is a retired academic librarian with over 40 years of experience between 1974 and the present, including Instructor/Catalog Librarian at Georgia Southern College, Director of Library Services at Indiana University South Bend, University Librarian & Director at Villanova University, and Dean of Libraries & Professor at Purdue University. *Id.* ¶¶ 2, 5–6, App'x A, 26. He served as a university librarian during the relevant timeframe, namely August 1994 (date on Halverson's title page) and the filing date of the '152 patent. *Id.*

Dr. Mullins explains that the Machine-Readable Cataloging ("MARC") formatted records standard was developed by the Library of Congress in the 1960s and in the 1970s became the U.S. national standard for disseminating bibliographic data, was in place in the relevant time frame, and persists through the present. *Id.* ¶ 13. He further explains that a MARC-compatible library is one that has a catalog consisting of MARC records for each of its items, and that every major library in the world is MARC-compatible. *Id.*

Dr. Mullins also explains that the Online Computer Library Center (OCLC) is a group created to establish, maintain, and operate a computerized library network, including increasing the availability of library resources to library patrons. *Id.* ¶ 14. The group and its members are responsible for maintaining the WorldCat database

(<http://www.worldcat.org/>), used by independent institutional libraries throughout the world. *Id.*

Dr. Mullins also describes a complimentary library organization, Research Library Group (“RLG”), formed in 1974 by several research universities as an alternative to OCLC. *Id.* ¶ 15. RLG created a database of bibliographic records identified as RLIN using the MARC format to create its OPAC and holding records at member institutions. *Id.*

Dr. Mullins includes as attachments to his declaration catalog records from various sources. *Id.* ¶¶ 34–39, Attachments 1B–E. For example, Attachment 1D includes OPAC and MARC records downloaded from the University of Hawaii. *Id.* ¶ 38, Attachment 1D. Dr. Mullins explains that the 008 field of these records indicates the catalog record for Halverson’s dissertation was created on February 27, 1996. *Id.* ¶¶ 21 (describing the 008 field), 38; *see also id.* at Attachment 1D (field 008 having an entry of 960227). Based on the OPAC and MARC records, Dr. Mullins states that, in his opinion, Halverson was publicly available as of the date the catalog record was created. *Id.* ¶¶ 38–40. He notes further that the MARC record included not only the title and author, but also subject, namely “Field Programmable Gate Arrays.” *Id.* ¶ 38.

We credit Dr. Halverson’s testimony that the dissertation was deposited and catalogued by title (“The Functional Memory Approach to the Design of Custom Computing Machines”), author, and subject (“Field Programmable Gate Arrays”) at the Library prior to February 27, 1996. Ex. 1018 ¶¶ 8–9. Dr. Halverson’s testimony is consistent with Dr. Mullins’ testimony and the catalogue records for the dissertation. Ex. 1019 ¶¶ 38–40, Attachments 1A–D. We also find Dr. Mullins’ testimony and the library records upon which he relies are competent evidence of general library

practice. *Hall*, 781 F.2d at 899 (“The probative value of routine business practice to show the performance of a specific act has long been recognized. Therefore, we conclude that competent evidence of the general library practice may be relied upon to establish an approximate time when a thesis became accessible.”) (citations omitted). Therefore, we find persuasive Dr. Mullins’ and Dr. Halverson’s evidence that Halverson was catalogued and indexed by subject, title, and author by February 27, 1996. We find the evidence is sufficient to establish Halverson was made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, could have located it (e.g., by title or subject).

Patent Owner does not provide any substantive challenge to Petitioner’s showing that Halverson is prior art. As we noted above, Patent Owner asserts, without any underlying explanation, that “Petitioner offers no evidence to meet” its burden to show Halverson is a printed publication and “the Halverson reference is not a printed publication for purposes of this IPR.” PO Resp. 60. Patent Owner’s statement, without any underlying explanation, is insufficient to rebut the evidence, discussed above, presented by Petitioner. We note Patent Owner improperly incorporates by reference portions of Dr. Guccione’s declaration by providing a string citation without explaining the significance of the citation or providing any analysis, and we therefore do not consider this improperly referenced testimony. *Id.* (citing Ex. 2148 ¶¶ 251–255); 37 C.F.R. § 42.6(a)(3). Even if we had considered the improperly referenced material, it would not alter the outcome of this Decision. Dr. Guccione’s testimony essentially amounts to his personal knowledge, namely that he personally was not aware of Halverson in the relevant time frame. Ex. 2148 ¶¶ 251–255. This is insufficient to rebut

Petitioner's evidence and arguments showing Halverson's public availability.

For the reasons stated above, we determine Halverson is prior art to the '152 patent.

2. *Halverson (Ex. 1005)*

Halverson, titled "The Functional Memory Approach to the Design of Custom Computing Machines," generally describes a software system and related hardware architecture in which high level language programs are compiled into gate level logic circuitry configured to specifically execute the program. Ex. 1005, Intro 5. The system includes a processor that can be dynamically reconfigured to suit different applications (custom computing machine or "CCM"). *Id.* The CCM is designed based on the concept of functional memory ("FM") constructed using FPGAs in parallel with conventional random access memory ("RAM"). *Id.* FM is used by a processor to compute expressions of a high level language program using the logic of the FPGAs. *Id.* According to Halverson, when program expressions are computed in FM, the necessary instruction set reduces to a minimal number of moves and jumps. *Id.*

Halverson explains that a functional memory computer ("FMC") consists of a von Neumann processor connected to a memory via a standard address bus. *Id.* at 26. Halverson describes a FMC prototype including four FPGAs in FM and a minimal processor (comprising a fifth FPGA). *Id.* at Intro 5. Figure 2.15 of Halverson, reproduced below, is illustrative.

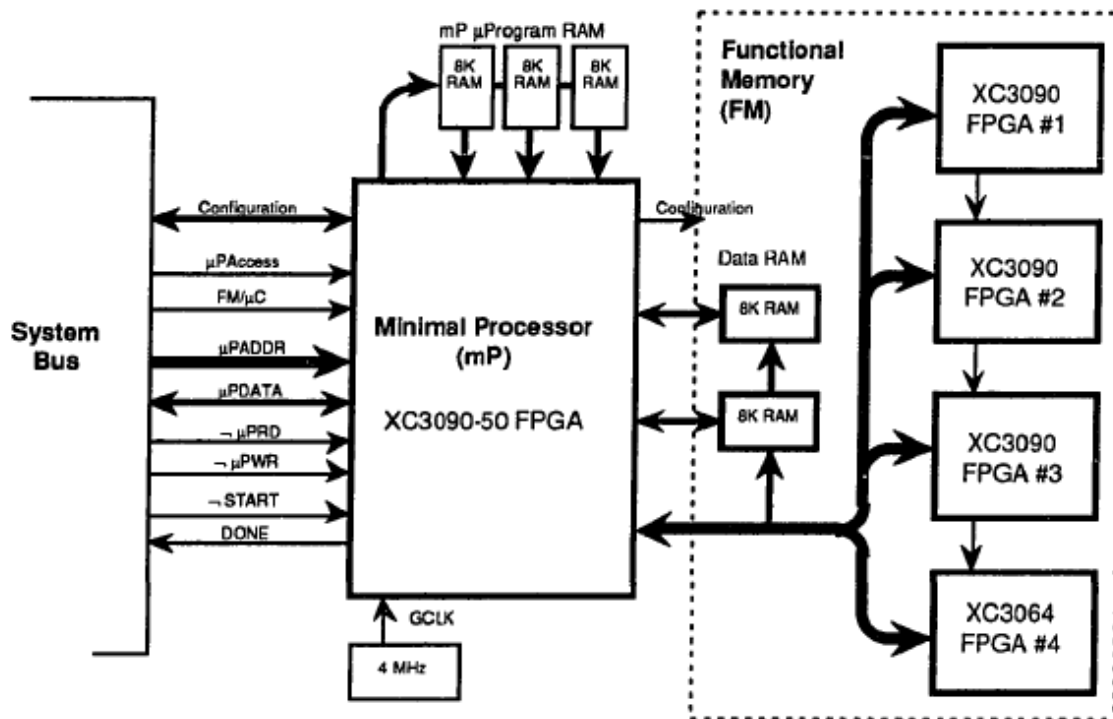


Figure 2.15. Functional Memory Computer Board Block Diagram

Figure 2.15 is a block diagram of a functional memory computer board

Ex. 1005, 46 (Fig. 2.15). Figure 2.15 shows minimal processor (“mP”) connected through a bus to FM. FM includes data RAM and four FPGAs, wherein data RAM and FPGAs are connected to the bus. In addition, mP is connected via busses, including μPADDR and μPDATA busses, to a system bus. Although not pictured, Halverson states that the FMC is initialized and controlled by a system processor, which in this case is a 11.059 MHz i8031 connected serially to an IBM PC. *Id.* at 46–47.

Figure 2.16, not reproduced here, provides architectural detail of mP, which “is designed only to move memory words from location to location.” *Id.* at 47.

3. *Splash2 (Ex. 1006)*

Splash2 is a book describing the Splash 2 reconfigurable computer system created by the Supercomputing Research Center in the 1990s.

Ex. 1006, xi. “Splash 2 is an attached processor system using Xilinx XC4010 FPGAs as its processing elements.” *Id.* “[T]he XC4010 contains a 20 x 20 array of Configurable Logic Blocks (CLBs).” *Id.* at 11. Figure 2.3 of Splash2 is reproduced below.

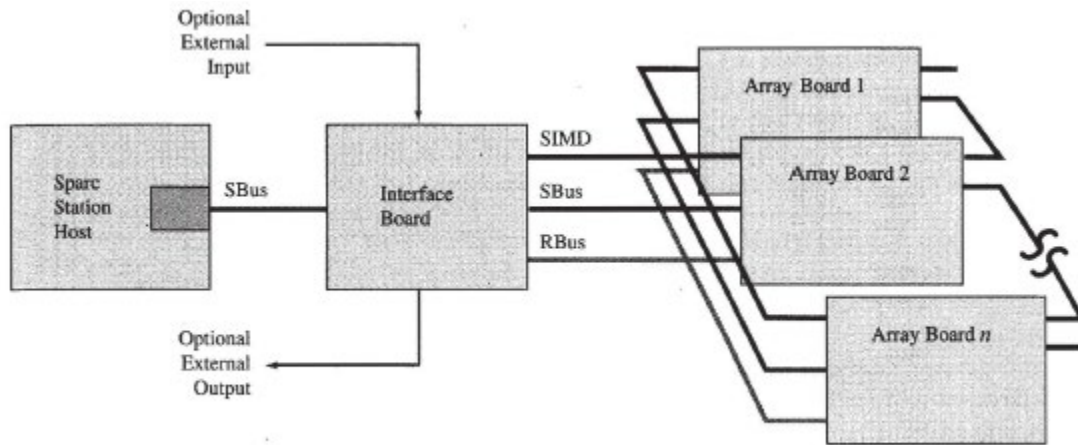


FIGURE 2.3 Splash 2 System Architecture

Figure 2.3 is a block diagram of the Splash 2 system architecture

Ex. 1006, 13 (Fig. 2.3). Figure 2.3 depicts the system architecture of the Splash 2 system, including a set of array boards connected to a SPARCstation 2 host via an interface board. *Id.* at 12–13. Figure 2.4 of Splash2 is reproduced below.

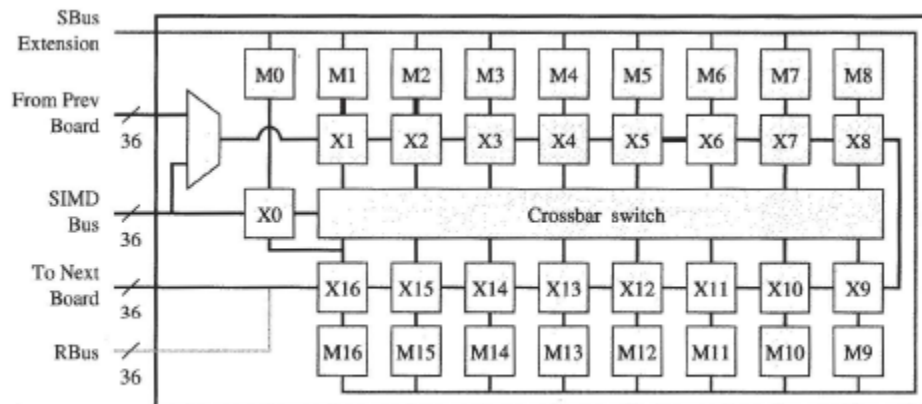


FIGURE 2.4 Array Board Architecture

Figure 2.4 illustrates an array board architecture

Ex. 1006, 14 (Fig. 2.4). Figure 2.4 depicts the architecture of one of the array boards. Each array board “contains 17 Xilinx XC4010 FPGA chips as its processing elements. Sixteen of these are connected in a linear array to create a linear data path and the seventeenth provides a broadcast capability to the other 16 chips.” *Id.* at 13 (internal citations omitted). “Viewed as a machine with a linear data path, the SIMD Bus can be used to transmit data from the Interface Board to the first FPGA on the first Array Board. The data can then be moved through the linear data path on that board, then to the first FPGA on the second Array Board, and so on.” *Id.* at 14. The linear data path is bidirectional. *Id.*

4. *Collins (Ex. 1007)*

Collins, titled “Reconfigurable Network Interface Apparatus and Method,” generally describes reconfigurable computer network interface device 10 including reconfigurable controller 12, reconfigurable bus interface 10, and configuration control arrangement 20, and on-board memory 16 for storing configuration instructions. Ex. 1007, code (57). Collins explains that when a computer on a network using one network topology desired to communicate with a computer on a different network using a different network topology, a network interface device, e.g., bridge, router, gateway, brouter, or hub, was needed to provide the desired inter-network communications. *Id.* at 1:43–2:62. These devices, according to Collins, were specifically configured to operate between certain specific network topologies, but could not be reconfigured to operate between other network topologies. *Id.* at 2:15–20. As a result “[i]f [a] user desired to change and use a different network type at a later date, the entire network system had to be replaced with a new network system,” which generally required a new interface card for each computer in the network. *Id.* at 2:28–

34. Collins states there was a need, therefore, for a network interface card that could communicate with a variety of network protocols and could be reconfigured easily to accept different network media types. *Id.* at 2:50–55.

To address the identified needs, Collins states it was an object of the invention to provide a network interface apparatus that is reconfigurable to accept different media types, bus structures, and network communication types. *Id.* at 2:58–63. To accomplish this object, Collins provides an apparatus including a reconfigurable controller, reconfigurable transceiver, and a reconfigurable bus interface, together with memory for storing configuration information and operational information for several different network types and bus types. *Id.* at 3:1–6. Collins discloses that preferably the memory is on-board and comprises RAM. *Id.* at 5:36–40.

5. *Parkin (Ex. 1017)*

Parkin, titled “Multi-processor Computer System,” generally describes “multiprocessing where a plurality of processors share a common memory and whose operations are in some manner interrelated.” Ex. 1017, 1:5–9. Parkin explains

A very large number of data processing operations are characterized by the necessity of performing a plurality of small to medium scale computing jobs or tasks. Often, these tasks may require very large amounts of rapidly retrievable data but relatively small amounts of processing and computation. At other times, these computing tasks are interrelated in a pattern which is normally unpredictable. If a large number of these tasks is involved, computation may be delayed, whether a single large scale or small scale processor is involved, while the needed programs are being retrieved for execution. For such kinds of operations, cost can be significantly reduced by structuring the computing devices according to the architectural plan forming part of this invention.

Execution of each task occurs in one (or conceivably more) of a plurality of processors.

Ex. 1017, 1:45–60. Parkin discloses that the processors all communicate with main memory into which data and program instructions may be loaded. *Id.* at 2:5–7.

6. Principles of Law

“Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference,” *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1255–56 (Fed. Cir. 1989), and that the claim limitations be “arranged or combined in the same way as recited in the claim[],” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). However, “the reference need not satisfy an *ipsissimis verbis* test.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness, if present. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). When evaluating a claim for obviousness, we also must “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

The Supreme Court has made clear that we apply “an expansive and flexible approach” to the question of obviousness. *KSR*, 550 U.S. at 415. Whether a patent claiming the combination of prior art elements would have been obvious is determined by whether the improvement is more than the predictable use of prior art elements according to their established functions. *Id.* at 417. Reaching this conclusion, however, requires more than a mere showing that the prior art includes separate references covering each separate limitation in a claim under examination. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention. *Id.*

7. *Anticipation by Halverson*

As we noted above, Petitioner asserts that claims 11, 12, and 18–21 of the ’152 patent are unpatentable as anticipated by Halverson. For the reasons discussed below, we determine Petitioner has demonstrated, by a preponderance of the evidence, the unpatentability of claims 11, 12, and 18–21 as anticipated by Halverson.

a) *Claim 11*

Although claim 1 has been disclaimed, Petitioner’s analysis for claim 11 refers frequently to its analysis for claim 1. Therefore, we consider Petitioner’s analysis for claim 1 where the Petition’s claim 11 analysis refers to claim 1.

- (1) *Preamble and Limitation 11[b]* (“a plurality of data processors for executing at least one application program by operating on user data in accordance with program instructions”)

Claim 1 recites “a computer system having at least one data processor for executing an application program.” Claim 11 recites “[a] multiprocessor system” (preamble) and “a plurality of data processors for executing at least one application program by operating on user data in accordance with program instructions” (limitation 11[b]). With regard to claim 1, which requires only one data processor, the Petition presents two alternative mappings of Halverson to the claimed “data processor.” For the first mapping, Petitioner asserts Halverson’s minimal processor, contained in the functional memory computer (“FMC”) board, is a data processor. Pet. 31–34. For the second mapping, Petitioner asserts Halverson’s i8031 processor and IBM PC microprocessor each are a data processor. *Id.* at 41–42. Unlike claim 1, which requires only one data processor, claim 11 recites a plurality of data processors. Petitioner contends that Halverson discloses a plurality of data processors, namely it discloses a minimal processor, i8031, and IBM PC microprocessor. *Id.* at 71.

For disclosure that the plurality of data processors are “for executing at least one application program by operating on user data in accordance with program instructions,” as recited in limitation 11[b], Petitioner explains that Halverson discloses multiple processors executing one application program because Halverson states its architecture “allows a mixture of [i8031] microcomputer boards and FMC boards to execute in parallel.” Pet. 70 (citing Ex. 1005, 46). Petitioner also identifies two application programs in Halverson: 1) “Shortest Path Program Example,” implemented by the minimal processor, and 2) image processing applications, e.g., an

image magnification program, portions of which are executed in the IBM PC and portions of which are executed in the i8031 processor, according to Petitioner. *Id.* at 34–38, 43–45.

Patent Owner argues Halverson neither discloses, nor renders obvious, a plurality of data processors that execute one application program. PO Resp. 62–64. Specifically, Patent Owner argues that Halverson’s FMC includes only a single processor, namely the minimal processor. *Id.* at 62. However, as acknowledged by Patent Owner, Petitioner does not argue that the FMC includes a plurality of processors. *Id.*; Pet. 31–38, 43–45, 70. Rather, Petitioner argues that the minimal processor operating in tandem with either the i8031 and/or microprocessor within the IBM PC, discloses a plurality of processors that execute one application program. Pet. 31–38, 43–45, 70. Patent Owner disputes this argument, too, on the grounds that, contrary to Petitioner’s assertion, the minimal processor in Halverson does not operate in tandem with the IBM PC microprocessor to execute an application program, and therefore Halverson’s IBM PC microprocessor “could not be considered part of a ‘multiprocessor.’” PO Resp. 63–64. According to Patent Owner, Halverson discloses the opposite, namely that before the FMC and associated minimal processor can run a program, the IBM PC microprocessor must be completely disconnected from the FMC board, and cannot reconnect with the FMC board during the program “runtime.” *Id.* at 63–64 (citing Ex. 1005, 58–60; Ex. 2148 ¶ 277).

We find Petitioner’s arguments to be persuasive. For example, for the image processing program that magnifies an image, Petitioner shows that Halverson discloses executing the program using two data processors. Pet. 43–44. As explained by Petitioner, Halverson discloses that the program includes a convolution program for estimating pixels, which is performed by

the FPGAs in functional memory. *Id.* at 43 (citing Ex. 1003 ¶¶ 150–154). But, other portions of the program must execute on the attached processors, i.e., the i8031 and IBM PC microprocessor, according to Petitioner. *Id.* (citing Ex. 1003 ¶¶ 150–154). These functions include compiling configuration information for the FPGAs, launching and initializing the program, writing input image data to the FPGAs, and displaying the resulting magnified image to a user. *Id.* at 43–44 (citing Ex. 1003 ¶¶ 134–135). We find Petitioner’s argument persuasive because, for example, moving data from system memory to the FPGAs, and presenting resulting data on a connected display, are functions performed by the system’s data processors, not by the FPGAs that perform calculations on data, such as convolution operations on image data. *Id.* (citing Ex. 1003 ¶¶ 134–135). Similarly, Petitioner identifies an optical character recognition program, arguing persuasively that a plurality of data processors execute the program, namely the i8031 and IBM PC microprocessor (i.e., data processors) initialize the program and write data to the FPGAs and the FPGAs (including the minimal processor asserted to by a data processor) execute processing on the optical characters to perform recognition. *Id.* at 44–45.

Rather than dispute Petitioner’s arguments and evidence that multiple processors in Halverson, i.e., i8031, the IBM PC microprocessor, and minimal processor are involved in executing the magnifying program and optical character recognition program, Patent Owner argues Halverson’s the i8031 and IBM PC must be disconnected from the functional memory board containing the FPGAs. PO Resp. 63–64. Even if we were to credit Patent Owner’s assertion that the board in Halverson containing the FPGAs must be disconnected from the i8031 and IBM PC, Patent Owner does not

identify, nor do we discern, language in limitation 11[b] that would preclude this. *Id.*

For the foregoing reasons, we determine Petitioner has made a persuasive showing as to the preamble and limitation 11[b].

(2) *Limitation 11[c] (“a memory bank having a data bus and an address bus connected to said plurality of data processors”)*

Limitation 11[c] recites “a memory bank having a data bus and an address bus connected to said plurality of data processors.” We construe the term “memory bank” as “a group of devices connected together and used as a memory.” *Supra* Sec. II.C.3.

Petitioner presents two alternative mappings of Halverson to the recited “memory bank,” based on the above-discussed two alternative mappings of Halverson to a data processor, *supra* Sec. II.D.7.a.1. With reference to the first mapping in which Halverson’s minimal processor is asserted to be a data processor, Petitioner argues functional memory corresponds to the claimed “memory bank.” Pet. 39, 71. Applying our construction of the term “memory bank,” we are persuaded Halverson’s functional memory is a “memory bank” because it comprises a group of devices connected together, e.g., four FPGAs, RAM, and buses, and is used as a memory, i.e., it is mapped through and accessed by a normal memory access protocol for use as a memory by a data processor. *Id.* Also, as argued by Petitioner, and shown in Figure 2.15, functional memory (i.e., asserted memory bank) has a data bus and address bus connecting to the minimal processor (i.e., asserted data processor). *Id.*; Ex. 1005, 46 (Fig. 2.15). However, the minimal processor is a single data processor. The claim requires a data bus and address bus connecting to a plurality of processors. To address this requirement, Petitioner argues persuasively that

the data bus and address bus connect to a plurality of processors because Halverson's data bus and address bus connecting functional memory to the minimal processor also connects, through the minimal processor and additional buses, to i8031 and the IBM PC (i.e., asserted plurality of data processors). Pet. 71 (citing Ex. 1005, 46 (Fig. 2.15)).

With reference to the second mapping in which Halverson's i8031 and IBM PC microprocessor are asserted to be data processors, Petitioner argues the combination of the minimal processor and functional memory corresponds to the claimed "memory bank." Pet. 71. As we discussed above, we are persuaded Halverson's functional memory discloses a memory bank, and we discern nothing in the claim language that precludes the memory bank from including a minimal processor. Petitioner argues persuasively that Halverson's data bus and address bus connect to a plurality of processors because Halverson discloses that functional memory includes a data bus and address bus (disclosed as part of the system bus) connected to i8031 and the IBM PC. *Id.* (citing Ex. 1005, 46 (Fig. 2.15)).

Patent Owner responds that Petitioner has not identified a "memory bank" in Halverson, as Patent Owner construes this term. PO Resp. 64. In particular, Patent Owner argues "[i]f the proper definition of Memory Bank is used then there are no FPGAs in Halverson that can be accessed by processor(s) in parallel." *Id.* As we discussed in our claim construction, we reject Patent Owner's unduly narrow construction of "memory bank." *Supra* Sec. II.C.3. Pertinent to Patent Owner's argument, our construction of "memory bank" does not require the FPGAs in Halverson to be accessed by processors in parallel. *Id.* Therefore, Patent Owner's argument does not undermine Petitioner's showing that Halverson discloses a "memory bank."

For the foregoing reasons, we determine Petitioner has made a persuasive showing as to limitation 11[c].

- (3) *Limitation 11[d] (“a plurality of memory algorithm processors within said memory bank at plurality of individual memory addressable memory locations”)*

Limitation 11[d] recites “a plurality of memory algorithm processors within said memory bank at plurality of individual memory addressable memory locations.” Petitioner argues persuasively that each of the four FPGAs in Halverson’s functional memory is a memory algorithm processor, because each FPGA is a memory-resident reconfigurable processing device, i.e., each processing device is seen by data processors as part of the data processor’s memory, and can be accessed by addressing a portion of memory. Pet. 46–49. We credit Petitioner’s assertion because Halverson discloses that the FPGAs are connected with RAM, and receive the same memory commands, addresses, and data issued to RAM. *Id.* at 47 (citing Ex. 1005, 26–28, Fig. 2.1, Fig. 2.15; Ex. 1003 ¶ 156). Furthermore, as argued by Petitioner, the only method Halverson discloses of communicating with configured FPGAs in the functional memory is by issuing memory commands, thereby indicating data processors external to the functional memory view the FPGAs as part of the data processors’ memory. *Id.* at 48 (citing Ex. 1005, 27–27, 55–56, § 3.2, Fig. 2.1, Fig. 2.15; Ex. 1003 ¶ 157). In addition, Halverson explains that with functional memory, “the FPGA is programmed to contain registers which can be written when RAM locations are written . . . [and to] output when certain addresses are read When data are stored into the RAM, they may be also captured simultaneously in FPGA registers.” *Id.* at 48–50 (quoting Ex. 1005, 27). As explained by Petitioner, because the FPGAs in Halverson

are written to and read from just as with RAM locations, data processors use the FPGAs by addressing a portion of memory. *Id.* at 49 (citing Ex. 1003 ¶ 158).

With regard to the recitation in limitation 11[d] that the memory algorithm processors are at a “plurality of individual memory addressable memory locations,” as we discussed in our claim construction, we construe “individual memory addressable” to mean that a particular individual MAP may be accessed through use of a memory address. *Supra* Sec. II.C.4. We agree with Petitioner that Halverson discloses addresses that represent the individual address of a particular FPGA. Pet. 49–51. For example, Figure 3.9 of Halverson shows that each of addresses “334E” and “3356” represent the individual address of the FPGA designated as SPC1. *Id.* at 50–51. Also, Figure 3.9 shows that the address “3352” represents the individual address of the FPGA designated as SPC2. *Id.* We find, therefore, that the FPGAs in Halverson are separately accessible by the data processor. *Id.* Accordingly, applying our construction of “individual memory addressable,” we find that Halverson discloses FPGAs at “individual memory addressable memory locations,” i.e., it discloses that a particular individual MAP may be accessed through use of a memory address.

Patent Owner argues that under its construction Halverson does not disclose that the FPGAs are at “individual memory accessible memory locations.” PO Resp. 65–66. Applying its construction, Patent Owner argues that the FPGAs in Halverson are never individually addressed, but rather are addressed in tandem with RAM in the functional memory. *Id.* In other words, when a memory address is used to access an FPGA, that same address is used to access RAM in tandem. *Id.* We find this argument unavailing. As we discussed in our claim construction, we reject Patent

Owner's claim construction. *Supra* Sec. II.C.4. The claim language does not preclude the address used to access an individual MAP from also being used to access a location in RAM in tandem. As we discussed immediately above, Halverson discloses addressing an individual FPGA. It is immaterial that the address also accesses a location in RAM in tandem.

For the foregoing reasons, we determine Petitioner has made a persuasive showing as to limitation 11[d].

- (4) *Limitation 11[e] (“means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus”)*

Limitation 11[e] recites “means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus.” As we discussed above, we construe this term under 35 U.S.C. § 112(6). *Supra* Sec. II.C.5. The recited function is “coupling said plurality of individual memory algorithm processors to said data bus and to said address bus,” and the corresponding structure is bank control logic 122, data bus 126, and address bus 128, and equivalents thereof. *Id.*

Petitioner argues persuasively that Halverson discloses a structure like bank control logic 122, or an equivalent thereof, because Halverson discloses a multiplexor for outputting addresses to functional memory over an address bus and a multiplexor for outputting data to functional memory over a data bus, as illustrated in Figure 2.16 of Halverson. Pet. 56–57 (citing Ex. 1005, 48–49, Fig. 2.16; Ex. 1003 ¶ 179). Halverson also discloses an OR gate for selecting the returned result from the multiple devices of the functional memory. *Id.* at 57–58 (citing Ex. 1003 ¶ 180). As argued by Petitioner, multiplexors and OR gates are logic elements that control and/or manage access to the FPGAs and RAM of functional memory, and therefore

are the same structure, or equivalent, to bank control logic 122. *Id.* at 58–59 (citing Ex. 1003 ¶ 181). We are persuaded bank control logic 122, like the structures in Halverson, controls and manages access to FPGAs and memory because Figure 3 of the ’152 patent shows, for example, control logic block 122 coupled to computer system trunk lines on one side and bi-directional data bus 126 and address bus 128 coupled to MAP assembly 112, and describes bank control logic 122 as being coupled to a data bus and supplying addresses on an address bus for accessing data at specified locations within memory array 130. Ex. 1001, 3:51–60, Fig. 3.

Petitioner also argues persuasively that Halverson discloses a structure like data bus 126 and address bus 128, or an equivalent thereof, because Halverson discloses a data bus and address bus from the four FPGAs in functional memory, like the data bus and address bus from MAP assembly 112 in the ’152 patent. Pet. 58 (citing Ex. 1003 ¶ 182); Ex. 1001, Fig. 3; Ex. 1005, 46 (Fig. 2.15).

Patent Owner argues that under its construction Halverson does not disclose “means coupling said plurality of individual memory algorithm processors to said data bus and to said address bus.” PO Resp. 64–65. Applying its construction, Patent Owner argues that nothing in Halverson is remotely like the “uniform memory access” scheme Patent Owner alleges is disclosed in the ’152 patent specification. *Id.* As we discussed in our claim construction, we do not construe this term to require “uniform memory access” as part of bank control logic 122. *Supra* Sec. II.C.5. Therefore, Patent Owner’s argument that Halverson does not disclose the “uniform memory access” scheme of the ’152 patent does not undermine Petitioner’s showing.

Patent Owner also contends Petitioner has failed to meet its burden to prove unpatentability on the grounds that the Petition does not satisfy the requirements of 37 C.F.R. § 42.104(b)(3) because the claim construction proposed in the Petition is not Petitioner's "own" construction.

PO Resp. 49. Section 104(b)(3) of title 37 states "[w]here the claim to be construed contains a means-plus-function or step-plus-function limitation as permitted under 35 U.S.C. 112(f), the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function." 37 C.F.R. § 42.104(b)(3). As discussed above, Petitioner identifies the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function. Pet. 19–22. Therefore, we find no violation of § 42.104(b)(3).

For the foregoing reasons, we determine Petitioner has made a persuasive showing as to limitation 11[e].

- (5) *Limitation 11[f] ("said plurality of memory algorithm processors being individually memory addressable by all of said plurality of data processors")*

Limitation 11[f] recites "said plurality of memory algorithm processors being individually memory addressable by all of said plurality of data processors." As we discussed in our claim construction, we construe "individually memory addressable" to mean that a particular individual MAP may be accessed through use of a memory address. *Supra* Sec. II.C.4. As we discussed above for limitation 11[d], we are persuaded by Petitioner's evidence and argument that Halverson discloses addresses that represent the individual address of a particular FPGA (i.e., memory algorithm processor). *Supra* Sec. II.D.7.a.3; Pet. 49–51, 73. For example, Figure 3.9 of Halverson

shows that each of addresses “334E” and “3356” represent the individual address of the FPGA designated as SPC1. *Id.* at 50–51. Also, Figure 3.9 shows that the address “3352” represents the individual address of the FPGA designated as SPC2. *Id.* We find, therefore, that the FPGAs in Halverson are separately accessible by the data processor. *Id.* Accordingly, applying our construction of “individually memory addressable,” we find that Halverson discloses FPGAs, i.e., “said plurality of memory algorithm processors,” as “being individually memory addressable by all of said plurality of data processors.”

Also discussed above, Patent Owner’s argument that under its construction Halverson does not disclose that the FPGAs are at “individual memory accessible memory locations,” PO Resp. 65–66, does not undermine Petitioner’s showing because we do not adopt Patent Owner’s construction. *Supra* Sec. II.D.7.a.3.

For the foregoing reasons, we determine Petitioner has made a persuasive showing as to limitation 11[f].

- (6) *Limitation 11[g] (“said plurality of memory algorithm processors being individually configurable to perform an identified algorithm on an operand that is received from a write operation by said at least one data processor to said memory bank as said at least one data processor executes said at least one application program”)*

Limitation 11[g] recites “said plurality of memory algorithm processors being individually configurable to perform an identified algorithm on an operand that is received from a write operation by said at least one data processor to said memory bank as said at least one data processor executes said at least one application program.”

Petitioner shows Halverson discloses this limitation. Pet. 59–65, 73. As argued by Petitioner, the FPGAs in Halverson, i.e., said plurality of

memory algorithm processors, are individually configurable to perform an identified algorithm. *Id.* at 60–64. We find Petitioner’s argument persuasive because Halverson discloses that each FPGA has interface logic implemented inside it that consists of registers for each operand of an expression, and that each operand corresponds to an application program variable which has a designated memory address that may be accessed using a write operation. *Id.* at 60–61 (citing Ex. 1005, 28, 31), 64–65 (citing Ex. 1005, 16).

In its arguments, Patent Owner does not refer to this claim limitation specifically.

For the foregoing reasons, we determine Petitioner has made a persuasive showing as to limitation 11[g].

(7) *Conclusion*

Upon review of the record, for the foregoing reasons, Petitioner has demonstrated, by a preponderance of the evidence, that claim 11 is unpatentable under § 102(b) as anticipated by Halverson.

b) *Claims 12 and 18–21*

Claims 12 and 18–21 each depend directly from claim 11. Petitioner identifies where each limitation recited in claims 12 and 18–21 is disclosed by Halverson. Pet. 52–55, 73–74 (claim 12); *id.* at 46–51, 65, 74 (claim 18); *Id.* at 47–48, 52–55, 74 (claim 19); *id.* at 66, 68–69, 74–75 (claims 20, 21). Patent Owner does not provide arguments beyond those presented for claim 11, discussed above *supra* Sec. II.D.7.a. PO Resp. 60–66.

Having reviewed the record, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 12 and 18–21 are unpatentable under § 102(b) as anticipated by Halverson.

8. *Obviousness over Halverson, Alone or in Combination with Other Prior Art*

Petitioner contends claims 11, 12, 15, and 18–21 would have been obvious over: 1) Halverson; 2) Halverson and Splash2; 3) Halverson and Parkin; and 4) Halverson, Parkin, and Splash2. Pet. 4. Petitioner also contends claim 15 would have been obvious over: 1) Halverson and Collins; 2) Halverson, Collins, and Splash2; and 3) Halverson, Collins, and Parkin. *Id.*

a) *Objective Indicia*

Obviousness is a question of law based on underlying findings of fact. *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). One of the underlying findings of fact include, when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham*, 383 U.S. at 17–18. Here, Patent Owner contends “[v]arious objective indicia of nonobviousness are supported and corroborated by evidence submitted by [Patent Owner].” PO Resp. 74.

Patent Owner lists various alleged types of indicia of nonobviousness, including long-felt need, teaching away, well-known limitations, commercial success,¹⁴ and unexpected results, and provides citations to various documents ostensibly to support Patent Owner’s allegations. *Id.* at 74–77. Patent Owner, however, fails to provide any argument or analysis demonstrating the nonobviousness of the claims. At best, Patent Owner’s citations are an inappropriate incorporation by reference of documents. 37 C.F.R. § 42.6(a)(3). Patent Owner neither argues that there is a presumption of a nexus between the claims and the

¹⁴ Patent Owner stated at the hearing, however, that it is “not claiming commercial success in this case.” Tr. 89:18–90:1.

objective indicia of nonobviousness, nor does Patent Owner otherwise provide any explanation establishing a nexus between any objective evidence of nonobviousness and the challenged claims. *See generally* PO Resp. 73–77. For example, Patent Owner does not explain how the cited testimony shows skepticism in the industry regarding the multiprocessor computer systems recited in claims 11, 12, 15, and 18–21. Nor does Patent Owner provide any explanation or analysis demonstrating that any products embody the claimed multiprocessor computer systems to establish nexus or show commercial success. Accordingly, we conclude that Patent Owner’s evidence purportedly showing long-felt need, teaching away, well-known limitations, commercial success, and unexpected results does not weigh in favor of nonobviousness of the challenged claims.

b) Halverson

Petitioner argues that to the extent we find certain features recited in claims 11, 12, and 18–21 are not disclosed in Halverson, such features would have been obvious to include in Halverson. Pet. 75–84, 88–91. As we discussed above, we find that Halverson discloses each of the limitations in claims 11, 12, and 18–21. *Supra* Sec. II.D.7. A disclosure that anticipates under 35 U.S.C. § 102 also renders the claim unpatentable under 35 U.S.C. § 103, for anticipation is the epitome of obviousness. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019); *In re Fracalossi*, 681 F.2d 792, 794 (CCPA 1982); *In re Pearson*, 494 F.2d 1399, 1402 (CCPA 1974). Therefore, for the reasons stated regarding anticipation of claims 11, 12, and 18–21 by Halverson, and upon consideration of Patent Owner’s arguments regarding objective indicia of nonobviousness, *supra* Sec. II.D.8.a, we conclude that Halverson renders these claims obvious under the grounds presented by Petitioner.

As to claim 15, Petitioner does not assert anticipation by Halverson. Claim 15 recites “[t]he multiprocessor computer system of claim 11 including: at least one memory device associated with said plurality of memory algorithm processors for storing a plurality of pre loaded identified algorithms.” Petitioner acknowledges Halverson does not explicitly disclose this limitation. Pet. 84–85. However, according to Petitioner and Dr. Trimberger, this feature would have been obvious in view of Halverson. *Id.* Petitioner and Dr. Trimberger assert that a skilled artisan would have recognized there are only a finite number of places to store such information in a computer system, each of which would necessarily include a memory device. *Id.* at 85 (citing Ex. 1003 ¶ 222). We credit Petitioner’s and Dr. Trimberger’s assertion that a person of ordinary skill in the art would have understood one such location to store information is a read-only memory device associated with the FPGA because it is supported by two patent references reflecting the knowledge of an ordinarily skilled artisan, which both show an EEPROM configured to store data for programmable FPGAs. *Id.* at 85 (citing Ex. 1012, 7:29–34; Ex. 1013, 16:2–17); Ex. 1003 ¶ 222. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020) (noting that “the inquiry into whether any ‘differences’ between the invention and the prior art would have rendered the invention obvious to a skilled artisan necessarily depends on [an ordinarily skilled] artisan’s knowledge,” and determining that the Board did not err in relying on “expert evidence, . . . corroborated by” evidence in the record, to find that a particular feature was “within the general knowledge of a skilled artisan”). For the foregoing reasons, we find that a skilled artisan would have known to include a memory device associated with the FPGAs in Halverson for

storing a plurality of pre loaded identified algorithms. Patent Owner does not provide arguments for claim 15.

Having reviewed the record, including evidence of objective indicia of nonobviousness, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 11, 12, 15, and 18–21 are unpatentable under § 103 as obvious over Halverson.

c) Halverson and Splash2

Petitioner contends claims 11, 12, 15, and 18–21 would have been obvious over the combination of Halverson and Spash2, asserting “[t]o the extent one might argue that Halverson alone does not sufficiently disclose [‘a multiprocessor computer system comprising,’ as recited in claim 11], it would have been obvious to do so based on the knowledge of a Skilled Artisan.” Pet. 82–84. As we discussed above, we find Halverson discloses each of the limitations of claims 11, 12, and 18–21. *Supra* Sec. II.D.7. We also determine above that Petitioner has demonstrated that claim 15 is unpatentable under § 103 as obvious over Halverson. *Supra* Sec. II.D.8.b. For the same reasons discussed above, *supra* Sec. II.D.7 and II.D.8.b, Petitioner has shown claims 11, 12, 15, and 18–21 are unpatentable as obvious over the combination of Halverson and Splash2.

We find further that Petitioner also has shown the claims to be unpatentable in light of Splash2’s teachings. As explained by Petitioner, “[providing] for multiple processors, such as workstations, to access multiple memory arrays, to improve processor performance,” was well-known in the art. Pet. 83 (quoting Ex. 1002, 50). Splash2 discloses such an architecture, and specifically includes a Sun SPARC station (i.e., multiprocessor workstation) as a host and several array boards on which are mounted FPGAs. *Id.* at 83–84 (citing Ex. 1006, 12, 20, Fig. 3.1). The ’152

patent acknowledges that standard multiprocessor architectures were conventional. Ex. 1001, 2:59–60, Fig. 1. Petitioner also provides a persuasive rationale to combine Halverson with multiprocessors as described in Spash2, namely that, as admitted by applicant during prosecution of the '152 patent, providing multiprocessors to access multiple memory arrays was a well-known technique to improve processor performance. Pet. 83 (citing Ex. 1002, 50; Ex. 1003 ¶ 245). We are persuaded, therefore, that it was well-known to use a multiprocessor with an array of FPGAs, and that a skilled artisan would have been motivated to use a multiprocessor, such as that disclosed in Splash2, in the system of Halverson in order to improve processor performance.

Patent Owner responds that neither Spash2 nor Halverson discloses a multiprocessor system. PO Resp. 68. Patent Owner does not elaborate on this assertion, but instead provides only a string of citations, which at best is an improper incorporation of arguments by reference, without any explanation to support its assertion. 37 C.F.R. § 42.6(a)(3). Therefore, we disagree with Patent Owner's assertion. Moreover, as we discussed above, we are not persuaded Halverson fails to disclose a multiprocessor. *Supra* Sec. II.D.7.a.1. Also, contrary to Patent Owner's assertion that Splash2 does not disclose a multiprocessor, Splash2 discloses using a Sun SPARC station as a host, which was well-known at the time to be implemented as a SPARC multiprocessor. Pet. 83–84 (citing Ex. 1016, 475–478); Reply 31–32.

Patent Owner also submits that Petitioner has not shown a motivation to combine Halverson with other prior art and that Petitioner uses hindsight reasoning. PO Resp. 69–73. Patent Owner argues “particularly in light of Halverson's primary teachings of minimizing the processor and reducing the operations on that processor as much as possible,” Petitioner provides

insufficient rationale to modify Halverson in a way that would undo its primary purpose of shifting nearly all processing to the FPGAs. *Id.* at 70 (citing Ex. 2148 ¶¶ 306–314). However, Patent Owner does not explain sufficiently its assertion, namely why the modifications proposed by Petitioner would allegedly undo the primary purpose of Halverson. *Id.* We therefore do not agree with this assertion. Patent Owner also reiterates its arguments that Halverson does not have a multiprocessor, FPGAs located in memory space, or disclosure of “means coupling.” *Id.* at 70–71. However, as discussed above, we disagree that Petitioner has failed to show Halverson discloses these features. *Supra* Sec. II.D.7.a. Patent Owner also argues Petitioner resorts to hindsight reasoning and *ipse dixit* errors by assuming all the benefits and ignoring all the drawbacks in “cobbling together prior art.” PO Resp. 72. However, Patent Owner’s argument is premised on its flawed assumption that the ’152 patent is limited to High Performance Computing systems. *Id.*

Having reviewed the record, including evidence of objective indicia of nonobviousness, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 11, 12, 15, and 18–21 are unpatentable under § 103 as obvious over Halverson and Splash2.

d) Halverson and Collins (with or without Splash2)

Petitioner contends claim 15 would have been obvious over the combination of Halverson and Collins, with or without Splash2, asserting that to the extent one might argue that it would not have been obvious to include the limitation of claim 15 in view of Halverson, it would have been obvious to do so in view of Collins. Pet. 85–88. As we discussed above, Petitioner has demonstrated that claim 15 is unpatentable under § 103 as obvious over Halverson. *Supra* Sec. II.D.8.b. For the same reasons

discussed above, *supra* Sec. II.D.8.b, Petitioner has shown claim 15 unpatentable as obvious over the combination of Halverson and Collins, with or without Splash2.

We find further that Petitioner also has shown claim 15 to be unpatentable in light of the teachings of Collins. Claim 15 recites “[t]he multiprocessor computer system of claim 11, including: at least one memory device associated with said plurality of memory algorithm processors for storing a plurality of pre loaded identified algorithms.” Petitioner shows Collins discloses storing a plurality of pre loaded algorithms in a FLASH EEPROM (i.e., at least one memory device) that is associated with a plurality of memory algorithm processors. Pet. 85–87 (citing Ex. 1007, Fig. 1, 9:35–36, 3:33–35, 8:29–32; Ex. 1008, 170, 178–179; Ex. 1003 ¶ 224–225, 227). Petitioner also shows that Halverson and Collins are analogous art to the ’152 patent, because each is in the field of using reconfigurable computing using FPGAs. *Id.* at 87 (citing Ex. 1003 ¶ 222; Ex. 1001, 1:15–30, 4:40–51; Ex. 1005, 26–27; Ex. 1007, 2:52–55, 3:31–35).

Petitioner also provides a rationale to combine Halverson with Collins, namely that Collins describes a well known structure used to quickly provide access to the configuration and operation instructions required to program FPGAs. *Id.* at 87–88 (citing Ex. 1003 ¶ 229). We find this persuasive. As we discussed above, Petitioner and Dr. Trimberger assert that a skilled artisan would have recognized there are only a finite number of places to store instructions in a computer system, each of which would necessarily include a memory device. *Id.* at 84 (citing Ex. 1003 ¶ 222). We credit Petitioner’s and Dr. Trimberger’s assertion that a person of ordinary skill in the art would have understood that one such location to store information is a read-only memory device associated with the FPGA

because it is supported by two patent references reflecting the knowledge of an ordinarily skilled artisan, which both show an EEPROM configured to store data for programmable FPGAs. *Id.* (citing Ex. 1012, 7:29–34; Ex. 1013, 16:2–17); Ex. 1003 ¶ 222. Collins provides a specific example of a read-only memory device associated with FPGAs to store instructions. As argued by Petitioner, inclusion of read-only memory storage, such as the EPROM disclosed in Collins, “would have been the arrangement old elements (EPROM storage) with each performing the same function it had been known to perform (storing configuration information) and yielding no more than one would expect from such an arrangement (a read only memory device associated with the FPGAs that is preprogrammed with instructions or configuration information).” Pet. 88 (citing Ex. 1003 ¶ 231).

Patent Owner submits that Petitioner has not shown a motivation to combine Halverson with other prior art and that Petitioner uses hindsight reasoning. PO Resp. 69–73. Patent Owner argues “particularly in light of Halverson’s primary teachings of minimizing the processor and reducing the operations on that processor as much as possible,” Petitioner provides insufficient rationale to modify Halverson in a way that would undo its primary purpose of shifting nearly all processing to the FPGAs. *Id.* at 70 (citing Ex. 2148 ¶¶ 306–314). However, Patent Owner does not explain sufficiently its assertion, namely why the modifications proposed by Petitioner would allegedly undo the primary purpose of Halverson. *Id.* We therefore do not agree with this assertion. Patent Owner also reiterates its arguments that Halverson does not have a multiprocessor, FPGAs located in memory space, or disclosure of “means coupling.” *Id.* at 70–71. However, as discussed above, we disagree that Petitioner has failed to show Halverson discloses these features. *Supra* Sec. II.D.7.a. Patent Owner also argues

Petitioner resorts to hindsight reasoning and *ipse dixit* errors by assuming all the benefits and ignoring all the drawbacks in “cobbling together prior art.” PO Resp. 72. However, Patent Owner’s argument is premised on its flawed assumption that the ’152 patent is limited to High Performance Computing systems. *Id.*

Having reviewed the record, including evidence of objective indicia of nonobviousness, we determine that Petitioner has demonstrated, by a preponderance of the evidence, that claim 15 is unpatentable under § 103 as obvious over Halverson and Collins, with or without Splash2.

e) Halverson and Parkin (with or without other references)

Petitioner contends: 1) claims 11, 12, 15, and 18–21 are unpatentable under § 103 as obvious over Halverson and Parkin; 2) claims 11, 12, 15, and 18–21 are unpatentable under § 103 as obvious over Halverson, Parkin, and Splash2; and 3) claim 15 is unpatentable under § 103 as obvious over Halverson, Collins, and Parkin. Pet. 88–91. As we discussed above, we determine claims 11, 12, and 18–21 are anticipated by Halverson. *Supra* Sec. II.D.7. We also determine above that Petitioner has demonstrated that claim 15 is unpatentable under § 103 as obvious over Halverson, that claims 11, 12, 15, and 18–21 are unpatentable under § 103 as obvious over Halverson and Splash2, and that claim 15 is unpatentable under § 103 as obvious over Halverson and Collins. *Supra* Sec. II.D.8.b–d. Petitioner relies on Parkin in the event that it is argued claim 11 requires executing an application program by splitting tasks among multiple “data processors.” Pet. 89. Neither party makes such argument. As such, we need not, and do not, reach Petitioner’s alternative grounds of unpatentability based on combinations involving Parkin.

E. Constitutionality of the Proceedings

Patent Owner “objects to the entirety of these proceedings based on the Federal Circuit’s recent opinion in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019).” Sur-Reply 27. Patent Owner argues that “the current structure of the Board violates the Appointments Clause.” *Id.* (quoting *Arthrex*, 941 F.3d at 1335). Patent Owner “requests that this proceeding be dismissed in its entirety on the grounds that the panel lacks the constitutional authority to enter a final decision in this case.” *Id.* at 28.

However, Patent Owner’s constitutional challenge as to this issue—whether the as-constituted panel is constitutional—has been addressed by the Federal Circuit’s decision. *See Arthrex*, 941 F.3d at 1337 (“This as-applied severance . . . cures the constitutional violation.”). Accordingly, we do not consider this issue any further.

III. CONCLUSION

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
11, 12, 18–21	§ 102(b)	Halverson	11, 12, 18–21	
11, 12, 15, 18–21	§ 103(a)	Halverson	11, 12, 15, 18–21	
11, 12, 15, 18–21	§ 103(a)	Halverson, Splash2	11, 12, 15, 18–21	
15	§ 103(a)	Halverson, Collins	15	
15	§ 103(a)	Halverson, Collins, Splash2	15	
11, 12, 15, 18–21	§ 103(a)	Halverson, Parkin		
11, 12, 15, 18–21	§ 103(a)	Halverson, Parkin, Splash2		
15	§ 103(a)	Halverson, Collins,		

		Parkin		
Overall Outcome			11, 12, 15, 18–21	

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that Petitioner has demonstrated by a preponderance of the evidence that claims 11, 12, 15, and 18–21 of U.S. Patent No. 6,247,110 B1 are *unpatentable*;

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 62) is *denied-in-part* and *dismissed-in-part*;

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 63) is *denied-in-part* and *dismissed-in-part*; and

FURTHER ORDERED that because this is a Final Written Decision, any party to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2018-01599
Patent 6,076,152

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