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Paper 32
Date: February 26, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

IPR2018-01784
Patent 6,101,145

Before MICHELLE N. WORMMEESTER, GARTH D. BAER, and STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 1, 6, and 15 of U.S. Patent No. 6,101,145 (Ex. 1001, "the '145 patent") under 35 U.S.C. §§ 311–319. Under 37 C.F.R. § 42.107(b), North Star Innovations, Inc. ("Patent Owner") waived its Preliminary Response (Paper 7).

In our Institution Decision (Paper 8, "Inst. Dec."), we instituted review based on all challenged claims and all grounds advanced in the Petition. We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has shown by a preponderance of the evidence that claim 15 of the '145 patent is unpatentable but has not shown by a preponderance of the evidence that claims 1 and 6 are unpatentable. *See* 35 U.S.C. § 316(e) (2012).

II. BACKGROUND

A. Procedural History

After we instituted review, Patent Owner filed a Response (Paper 14, "Resp."), Petitioner filed a Reply (Paper 26, "Reply"), and Patent Owner filed a Sur-reply (Paper 30, "Sur-reply"). On January 16, 2020, we held an oral hearing. *See* Paper 31 ("Tr.").

B. Related Proceedings

Petitioner and Patent Owner identify the following civil action where Patent Owner has asserted the '145 patent against Petitioner: *North Star Innovations, Inc. v. Kingston Technology Co.*, No. 8:17-cv-1833 (C.D. Cal. filed Oct. 20, 2017). Pet. 1–2; Paper 4, 1–2; Paper 5, 1.

Petitioner and Patent Owner identify other petitions challenging the patentability of claims in other patents asserted by Patent Owner against Petitioner in the above-identified civil action: IPR2018-01794 (U.S. Patent No. 6,917,555), IPR2019-00102 (U.S. Patent No. 5,943,274), and IPR2019-00104 (U.S. Patent No. 6,127,875). Pet. 2; Paper 4, 2; Paper 5, 1.

C. The '145 Patent (Ex. 1001)

The '145 patent, titled "Sensing Circuit and Method," issued on August 8, 2000 from an application filed on December 21, 1998. Ex. 1001, codes (22), (45), (54). The patent has expired. *See* Pet. 22; Resp. 20.

The '145 patent discloses sense amplifiers, i.e., circuits for sensing data from a memory array and providing the sensed data to an output data bus. Ex. 1001, 2:45–67, 3:39–67, 5:62–6:12, 7:56–8:10, code (57), Figs. 2–4. The patent states that the "invention relates to sense amplifiers, and more specifically to an improved sensing circuit and method which reduces the occurrence of invalid data being transmitted to an output data bus." *Id.* at 1:4–7.

The '145 patent explains that invalid data transitions or "glitches" cause problems because they "consume AC power." Ex. 1001, 1:18–22; *see id.* at 1:22–2:23; Ex. 2001 ¶ 34. The patent identifies three potential sources of invalid data transitions: (1) a sense amplifier, (2) a data storage device, and (3) an inactive memory block of a larger system. Ex. 1001, 1:23–24, 1:36–37, 1:49–52; *see id.* at 2:62–67, 5:19–29; Ex. 1003 ¶ 79; Ex. 2001 ¶¶ 41–43, 50; Resp. 3–5.

Regarding the first potential source, the '145 patent explains that a sense amplifier may cause invalid data transitions because the sense amplifier (1) "will try to sense what is appearing at its inputs" immediately

when activated and before "new data arrives from the memory array" and (2) "will begin to send what is sensed (e.g., invalid data) to the output data bus." Ex. 1001, 1:22–27, 3:3; *see* Ex. 2001 ¶ 41. "If the polarity of what" appears at the sense amplifier's inputs differs from both the polarity of the data on the output data bus and the data to be sensed from the memory array, the "output data bus will transition from the previous data on the bus, to the invalid data (the data sensed during the time between the sense amplifier being enabled and valid data appearing at its inputs), and finally to the newly sensed valid data." Ex. 1001, 1:27–35; *see* Ex. 2001 ¶ 41. For instance, the transition on the output data bus could appear as 1-0-1 or 0-1-0, with the intervening value appearing only briefly. *See* Ex. 1001, 9:8–11; Ex. 2001 ¶ 41.

Regarding the second potential source, the '145 patent explains that a data storage device may cause invalid data transitions when "the data being stored from the previous operation is opposite in polarity from what is appearing on the output data bus and from the data to be sensed from the memory array." Ex. 1001, 1:40–44; *see* Ex. 2001 ¶ 42. When that occurs, "the output data bus will transition from the valid data that was appearing on the bus to the data stored in the storage device from a previous operation then to the newly sensed data from the memory array." Ex. 1001, 1:44–48; *see* Ex. 2001 ¶ 42.

Regarding the third potential source, the '145 patent explains that an inactive memory block of a larger system may cause invalid data transitions because "there is no guarantee as to what signals will be driven onto the output data bus prior to the sense amplifier sensing the valid data from the

memory array and providing that valid data to the output data bus." Ex. 1001, 1:49–56; *see* Ex. 2001 ¶ 43.

To eliminate invalid data transitions due to an inactive memory block of a larger system, "[d]ata storage devices of inactive [memory] blocks are preloaded with the valid data appearing on the output data bus via a feedback circuit, thereby preventing potentially invalid data otherwise stored in an in active [sic] storage device from being transferred to the output data bus upon activation." Ex. 1001, 2:62–67, code (57); *see id.* at 5:19–57, 7:18–39, 8:35–39, 9:12–25, 9:52–59, Figs. 3–4; Ex. 1003 ¶¶ 79–81; Ex. 2001 ¶¶ 50–51. Thus, "the data sensing circuit is further improved by eliminating invalid data transitions from appearing on the output data bus through use of feedback." Ex. 1001, 2:58–62, code (57); *see id.* at 5:19–57, 9:52–59; Ex. 2001 ¶¶ 44–46.

Figure 2 of the '145 patent is reproduced below:

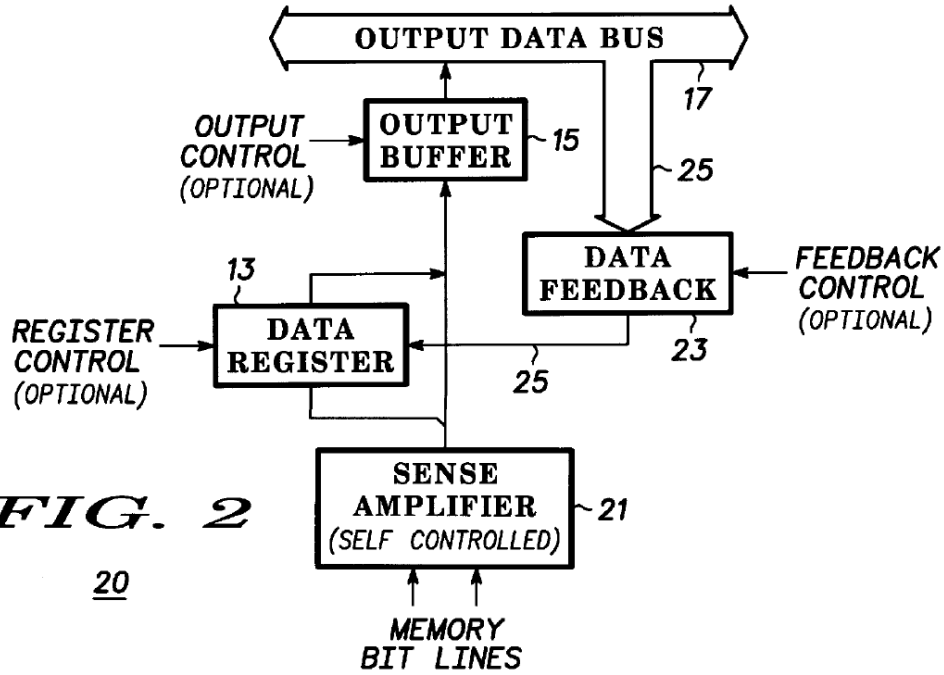


Figure 2 "illustrates a sensing scheme 20" including "sense amplifier 21 coupled for sensing data from a memory bit line of a memory array, data storage device 13 coupled between sense amplifier 21 and output data bus 17, and a data feedback circuit 23 coupled between output data bus 17 and data storage device 13." Ex. 1001, 3:39–45; *see id.* at 2:34–35. "Sensing scheme 20 further comprises output buffer 15 coupled for receiving data from data storage device 13 and sense amplifier 21." *Id.* at 3:45–47. Output buffer 15 is also coupled for "driving the received data on to output data bus 17." *Id.* at 3:46–48. According to the '145 patent, "the memory array is coupled to and utiliz[es] output data bus 17." *Id.* at 5:51–52.

Figure 3 of the '145 patent is reproduced below:

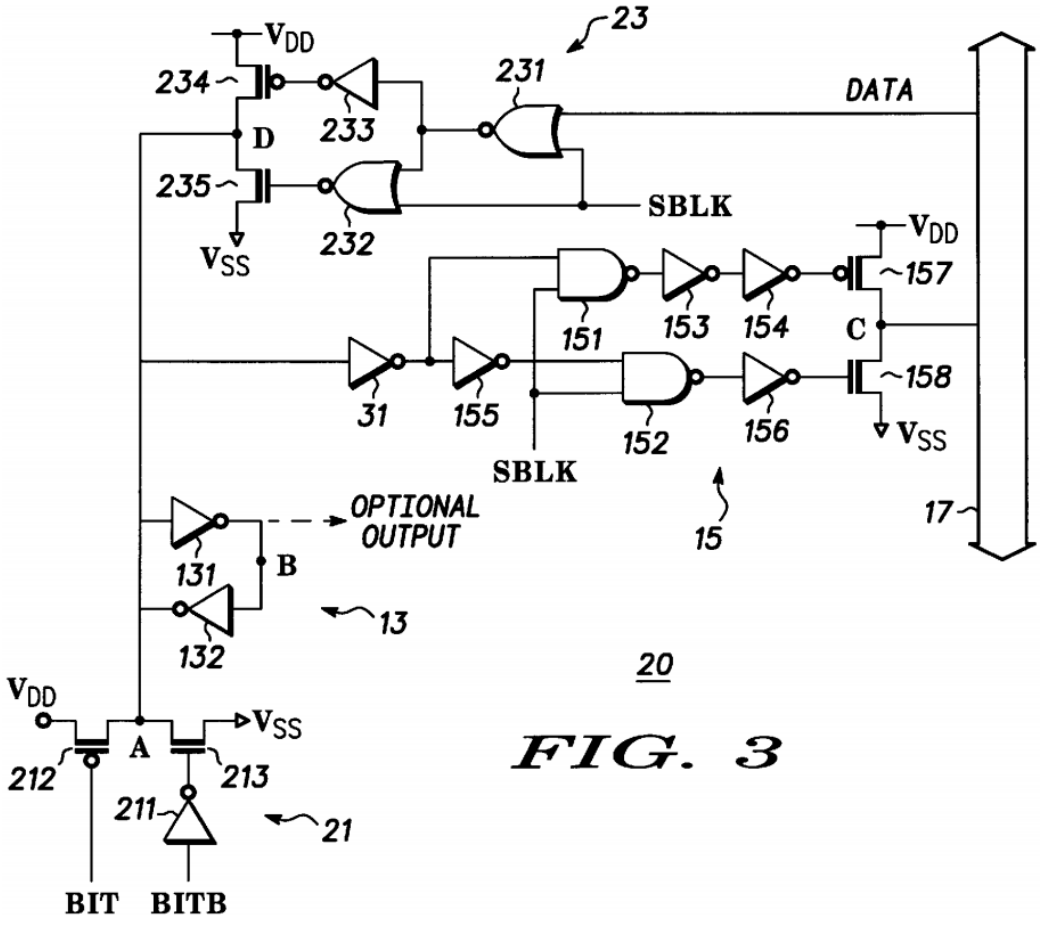


FIG. 3

Figure 3 "illustrates a logic level diagram of an embodiment of sensing scheme 20" in Figure 2. Ex. 1001, 5:62–63; *see id.* at 2:36–38. In Figure 3, sensing scheme 20 includes sense amplifier 21, data storage device 13, output buffer 15, inverter 31 coupled between data storage device 13 and output buffer 15, output data bus 17, and data feedback circuit 23 coupled between output data bus 17 and data storage device 13. *See id.* at 5:63–7:55.

Figure 4 of the '145 patent is reproduced below:

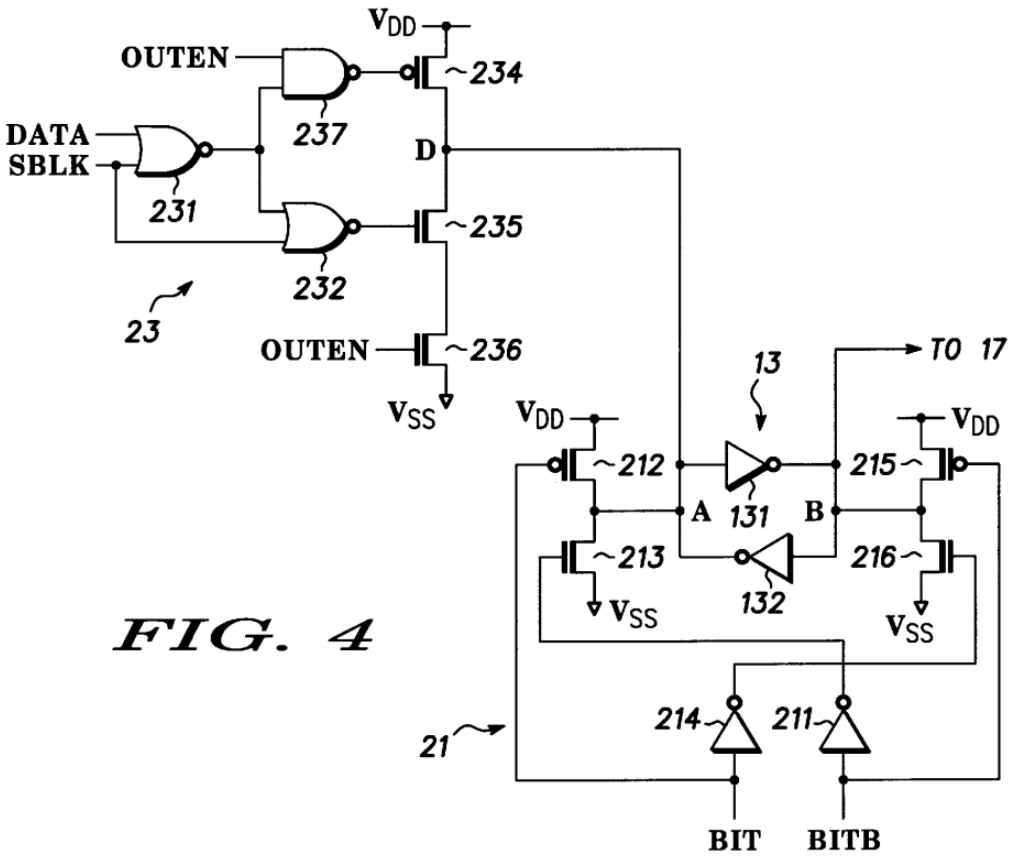


FIG. 4

Figure 4 "illustrates some alternate circuit implementations of select components of sensing scheme 20" compared to Figure 3. Ex. 1001, 7:56–57; *see id.* at 2:39–41. In Figure 4, sensing scheme 20 includes sense amplifier 21, data storage device 13, and data feedback circuit 23 coupled between output data bus 17 (not shown) and data storage device 13. *See id.* at 7:57–9:45.

D. The Challenged Claims

Petitioner challenges independent claims 1 and 15 and dependent claim 6. Pet. 4, 31–56. The challenged claims read as follows:

> 1. A sensing circuit for sensing data from a memory array and providing the sensed data to an output data bus, the circuit comprising:
>
> a sense amplifier coupled to the memory array;
>
> a data storage device coupled between the sense amplifier and the output data bus; and
>
> a data feedback circuit having an input terminal coupled to the output data bus and an output terminal coupled to the data storage device.
>
> 6. The circuit of claim 1 further comprising an output buffer having an input terminal coupled to the data storage device and an output terminal coupled to the output data bus.
>
> 15. A method for controlling data transitions on an output data bus of a semiconductor device having a memory array comprising the steps of:
>
> sensing data appearing on a bit line of the memory array;
>
> driving the sensed data onto the output data bus; and
>
> providing a feedback signal representative of the sensed data appearing on the output data bus to inactive memory blocks of the memory array coupled to the output data bus.

Ex. 1001, 10:11–19, 10:62–64, 12:29–37.

E. The Asserted Prior Art

For its challenges, Petitioner relies on U.S. Patent No. 5,563,835 to Oldham, titled "Sense Amplification in Data Memories," filed on January 27, 1995, and issued on October 8, 1996 (Ex. 1005, "Oldham").

F. Testimonial Evidence

To support its challenges, Petitioner relies on two declarations of Bruce Jacob, Ph.D. (Ex. 1003, "Jacob Decl."; Ex. 1010, "Jacob Reply Decl."). Patent Owner relies on the declaration of Sunil P. Khatri, Ph.D. (Ex. 2001, "Khatri Decl."). The record includes a transcript of Dr. Khatri's deposition (Ex. 1011, "Khatri Dep.") and a transcript of Dr. Jacob's deposition (Ex. 2004, "Jacob Dep.").

G. Asserted Grounds of Unpatentability

We instituted an *inter partes* review of claims 1, 6, and 15 on the following grounds:

Claims Challenged	35 U.S.C. §	Reference
1, 6, 15	102(b)[1]	Oldham
1, 6, 15	103(a)	Oldham

Inst. Dec. 20.

H. Burden

Petitioner bears "the burden of proving . . . unpatentability by a preponderance of the evidence." 35 U.S.C. § 316(e); *see* 37 C.F.R. § 42.1(d) (2018).

III. PATENTABILITY ANALYSIS

A. Level of Ordinary Skill in the Art

Factors pertinent to determining the level of ordinary skill in the art include (1) the educational level of the inventor; (2) the type of problems

[1] On March 16, 2013, the amendments to 35 U.S.C. §§ 102 and 103 in the Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), took effect. Because the '145 patent's filing date predates the AIA's amendments to §§ 102 and 103, this decision refers to the pre-AIA versions of §§ 102 and 103.

encountered in the art; (3) prior-art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of workers active in the field. *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–97 (Fed. Cir. 1983). Evidence for these factors may not exist in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, these factors are not exhaustive, but are merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). Further, the prior art itself may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Here, Petitioner asserts that a person of ordinary skill in the art would have had "either an undergraduate degree in electrical engineering (or equivalent subject), with at least two years of post-graduate experience designing memory arrays, or a master's degree in electrical engineering (or equivalent subject), with at least one year of post-graduate experience in designing memory arrays." Pet. 26 (citing Ex. 1003 ¶ 22); *see* Ex. 1003 ¶ 22. Petitioner also asserts that "a higher level of education could make up for less experience, and vice versa." Pet. 26; *see* Ex. 1003 ¶ 23. Patent Owner states that "[f]or purposes of this proceeding," it "is not challenging Petitioner's proposed definition of" a person of ordinary skill in the art. Resp. 24; *see* Ex. 2001 ¶ 26. Thus, we adopt Petitioner's proposed definition as consistent with the '145 patent and the asserted prior art.

B. Claim Construction

1. BACKGROUND

As noted above, the '145 patent has expired. *See* Pet. 22; Resp. 20. Because the '145 patent has expired, we construe disputed claim terms according to the principles articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017). Further, the parties agree that we should construe disputed claim terms according to *Phillips*. *See* Pet. 22; Resp. 20–21, 24.

According to *Phillips*, claim terms "are generally given their ordinary and customary meaning" as understood by "a person of ordinary skill in the art." *Phillips*, 415 F.3d at 1312–13. "[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent," including the other claims ("both asserted and unasserted") and the written description. *Id.* at 1313–14, 1321. Further, "the prosecution history can often inform the meaning of the claim language by demonstrating how" an inventor or an examiner understood the claim language. *Id.* at 1317. Thus, the meaning of a disputed claim term may be determined by "look[ing] principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

2. "COUPLED"

Claims 1, 6, and 15 each use the term "coupled." *See* Ex. 1001, 10:11–19, 10:62–64, 12:29–37. As an example, claim 1 recites "a sense

amplifier coupled to the memory array" and "a data storage device coupled between the sense amplifier and the output data bus." *Id.* at 10:14–19. As another example, claim 6 recites "an output buffer having an input terminal coupled to the data storage device and an output terminal coupled to the output data bus." *Id.* at 10:62–64.

Petitioner proposes that we construe "coupled" in claims 1, 6, and 15 to mean "directly or indirectly connecting, such as through intervening circuit elements." Pet. 23, 26. Based on the '145 patent's preferred embodiments, Petitioner contends that "the term 'coupled' is not limited to *direct* coupling." *Id.* at 23–25 (emphasis in original).

For the Figure 2 embodiment, Petitioner notes that the '145 patent states that "the memory array is coupled to and utiliz[es] output data bus 17." Pet. 25 (citing Ex. 1001, 5:50–53). Petitioner then asserts that Figure 2 shows "multiple intervening circuit elements—such as the sense amplifier and output buffer—between the memory bit lines coming from the memory array" and output data bus 17. *Id.*

For the Figure 3 embodiment, Petitioner notes that claim 1 recites "a data storage device coupled between the sense amplifier and the output data bus." Pet. 23. Petitioner then asserts that Figure 3 shows data storage device 13 connected indirectly to output data bus 17 through inverter 31 and output buffer 15. *Id.* at 23–25; *see* Ex. 1001, 6:47–51, 6:56–59, 6:64–66, Fig. 3.

In addition, Petitioner notes that claim 6 recites "an output buffer having an input terminal coupled to the data storage device and an output terminal coupled to the output data bus." Pet. 24. Petitioner then asserts that Figure 3 shows output buffer 15's input terminal connected indirectly to data

storage device 13 through inverter 31. *Id.* at 24–25; *see* Ex. 1001, 6:47–51, 6:64–66, Fig. 3. Consistent with that assertion, the '145 patent states that "[d]ata sensed by sense amplifier 21 is latched into storage device 13 and provided to output buffer 15 via inverter 31." Ex. 1001, 6:64–66.

Based on the '145 patent's claim language and description of preferred embodiments, Petitioner contends that a construction limiting "coupled" to "a direct connection" would "exclude disclosed embodiments." Pet. 26.

Patent Owner does not address Petitioner's arguments about the meaning of "coupled" in claims 1, 6, and 15. *See* Resp. 24. Instead, Patent Owner contends that "under the *Phillips* standard," the Response accords the claims "their ordinary and customary meaning as would have been understood by" an ordinarily skilled artisan "at the time of the invention" consistent with the intrinsic evidence. *Id.*

Based on the intrinsic evidence, we agree with Petitioner that "coupled" in claims 1, 6, and 15 encompasses "directly or indirectly connecting." As Petitioner contends, a construction limiting "coupled" to "a direct connection" would exclude the Figure 3 embodiment from claim scope. A construction excluding a preferred embodiment is "rarely, if ever correct." *PPC Broadband, Inc. v. Corning Optical Commc'ns RF, LLC*, 815 F.3d 747, 755 (Fed. Cir. 2016). "[W]here claims can reasonably [be] interpreted to include a specific embodiment, it is incorrect to construe the claims to exclude that embodiment, absent probative evidence on the contrary." *Oatey Co. v. IPS Corp.*, 514 F.3d 1271, 1277 (Fed. Cir. 2008). Here, we perceive no such probative evidence.

3. OTHER ISSUES

To the extent that the parties raise patentability issues requiring additional claim construction, we address claim construction in our patentability analysis when considering the particular patentability issue. *See infra* §§ III.C.3(d), III.C.5(a). We do so to provide better context to explain the dispute about claim construction and our resolution of the dispute.

C. Anticipation by Oldham: Claims 1, 6, and 15

1. ANTICIPATION UNDER 35 U.S.C. § 102

"[T]o demonstrate anticipation, the proponent must show 'that the four corners of a single, prior art document describe every element of the claimed invention.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Xerox Corp. v. 3Com Corp.*, 458 F.3d 1310, 1322 (Fed. Cir. 2006)). The prior-art document "must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Hence, a patent challenger cannot rely on portions from different embodiments in a prior-art document to demonstrate anticipation. *See id.* at 1369, 1371.

We analyze the anticipation issues according to these principles.

2. OVERVIEW OF OLDHAM (EX. 1005)

Oldham discloses circuits for sensing data from a memory array and providing the sensed data to an output data bus, i.e., sense amplifiers. Ex. 1005, 1:5–6, 3:50–60, 4:25–29, 5:20–27, 6:38–39, 8:1–2, Figs. 2–4; *see* Ex. 1003 ¶¶ 84–91; Ex. 2001 ¶¶ 68–77. Oldham describes a problem due to

invalid data transitions or "glitches" that waste power. Ex. 1005, 2:1–38; *see* Ex. 1003 ¶¶ 84, 86. Specifically, Oldham explains that a "sense amplifier can initially output one value, and then quickly over-write it with a new value once sensing has taken place." Ex. 1005, 2:11–13; *see* Ex. 1003 ¶ 86.

Oldham states that "[i]t is an object of the invention to avoid output glitches in data memories." Ex. 1005, 2:42–43, 2:53–54; *see* Ex. 1003 ¶ 86. Oldham discloses several embodiments of sense-amplifier circuits designed to achieve that objective. Ex. 1005, 4:25–29, 5:20–8:25, Fig. 2 (sense-amplifier circuit 80), Fig. 3 (sense-amplifier circuit 80'), Fig. 4 (sense-amplifier circuit 80"); *see* Ex. 1003 ¶ 87; Ex. 2001 ¶ 68.

Oldham's Figure 2 is reproduced below:

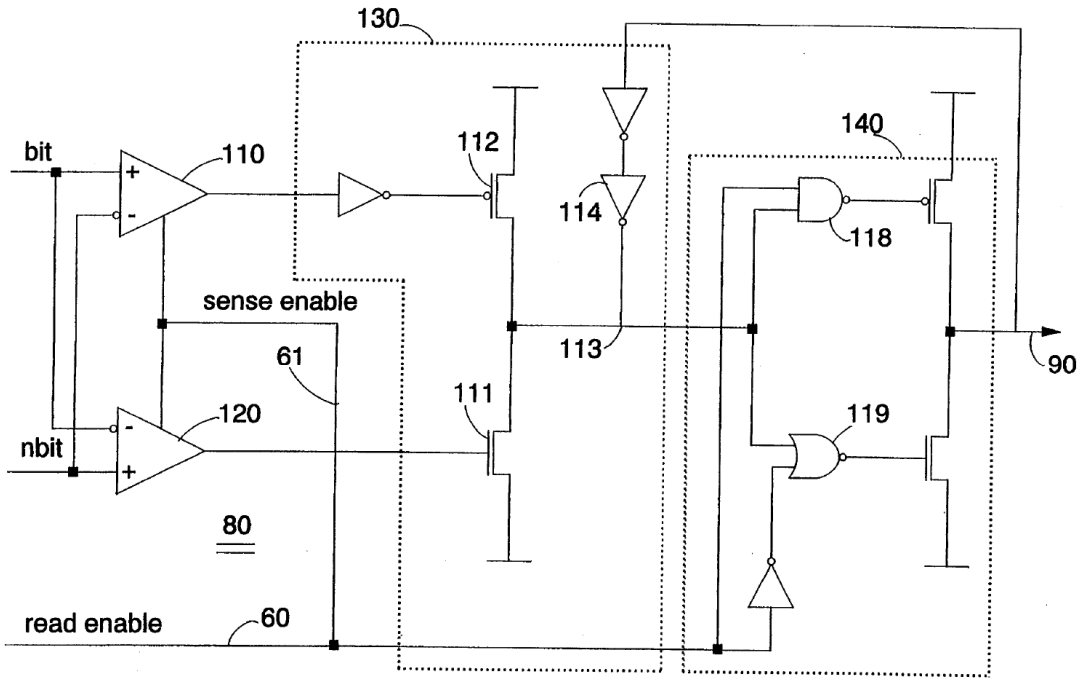


Fig. 2

Figure 2 illustrates sense-amplifier circuit 80 including "two sense amplifiers 110, 120, a latch circuit 130 and a tri-state buffer circuit 140." Ex. 1005, 5:20–23; *see* Ex. 1003 ¶ 88; Ex. 2001 ¶ 69. Sense-amplifier

circuit 80 "receives the bit and nbit signals from a pair of bit-lines 30 [in Figure 1] and generates [a] buffered output signal" at output 90. Ex. 1005, 5:23–26; *see* Ex. 1003 ¶ 88; Ex. 2001 ¶¶ 69–70. Output 90 connects to a shared output data bus. Ex. 1005, 5:26–27, 6:12–16; *see id.* at 5:16–19, 6:36–37; Ex. 1003 ¶¶ 88, 107; Ex. 2001 ¶¶ 76–77.

Latch circuit 130 includes transistors 111 and 112, the unnumbered inverter connected to transistor 112's input, and a "feedback path from the output 90 to a node 113" at the output of transistors 111 and 112. Ex. 1005, 5:61–63, Fig. 2; *see* Ex. 1003 ¶¶ 87, 90; Ex. 2001 ¶¶ 74, 123. The feedback path includes "a pair of inverters," i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input. Ex. 1005, 5:63–65, Fig. 2; *see* Ex. 1003 ¶¶ 90, 109; Ex. 2001 ¶¶ 74, 89, 123. Output 90 "is fed back into the latch circuit as part of its operation." Ex. 1005, 6:17–20, Fig. 2; *see* Ex. 1003 ¶¶ 90, 111, 114, 129; Ex. 2001 ¶ 76.

"The output of the latch circuit 130 (at the node 113) is buffered by the tri-state buffer circuit 140 and presented" at output 90. Ex. 1005, 6:17–20; *see* Ex. 1003 ¶ 90; Ex. 2001 ¶ 76. "The logical state of the node 113 therefore represents the previous state of the output 90 (which may be driven by other devices connected to the shared bus) until that output is overwritten with a new value" determined by either transistor 111's "logic low" output or transistor 112's "logic high" output. Ex. 1005, 5:65–6:4, 6:12–16; *see* Ex. 1003 ¶ 90; Ex. 2001 ¶¶ 74–75.

Tri-state buffer circuit 140 includes "a logical-NAND gate 118, a logical-NOR gate 119 and a pair of output transistors," i.e., the unnumbered p-channel transistor connected to NAND gate 118 and the unnumbered n-channel transistor connected to NOR gate 119. Ex. 1005, 6:21–23,

6:32–37; *see* Ex. 1003 ¶ 121; Ex. 2001 ¶ 76. In addition to receiving the output of latch circuit 130, tri-state buffer circuit 140 receives a read-enable signal as an input. Ex. 1005, 6:21–24; *see* Ex. 1003 ¶ 121; Ex. 2001 ¶ 77. Specifically, the read-enable signal "is supplied as an input to the NAND gate 118 and, in inverted form, to the NOR gate 119." Ex. 1005, 6:23–26; *see* Ex. 1003 ¶ 121; Ex. 2001 ¶ 77.

A "high" read-enable signal enables NAND gate 118 and NOR gate 119 such that "output 90 is identical to the logic level at the node 113." Ex. 1005, 6:27–30; *see* Ex. 1003 ¶ 121; Ex. 2001 ¶ 77. A "low" read-enable signal causes the output transistors connected to NAND gate 118 and NOR gate 119 to switch off, thus presenting a high impedance and "allow[ing] other tri-state buffers access to the common bus." Ex. 1005, 6:30–37; *see* Ex. 1003 ¶ 121; Ex. 2001 ¶ 77.

3. INDEPENDENT CLAIM 1

Petitioner argues that Oldham's Figure 2 embodiment anticipates claim 1. *See* Pet. 31–41. To support its argument, Petitioner presents the highlighted version of Figure 2 reproduced below:

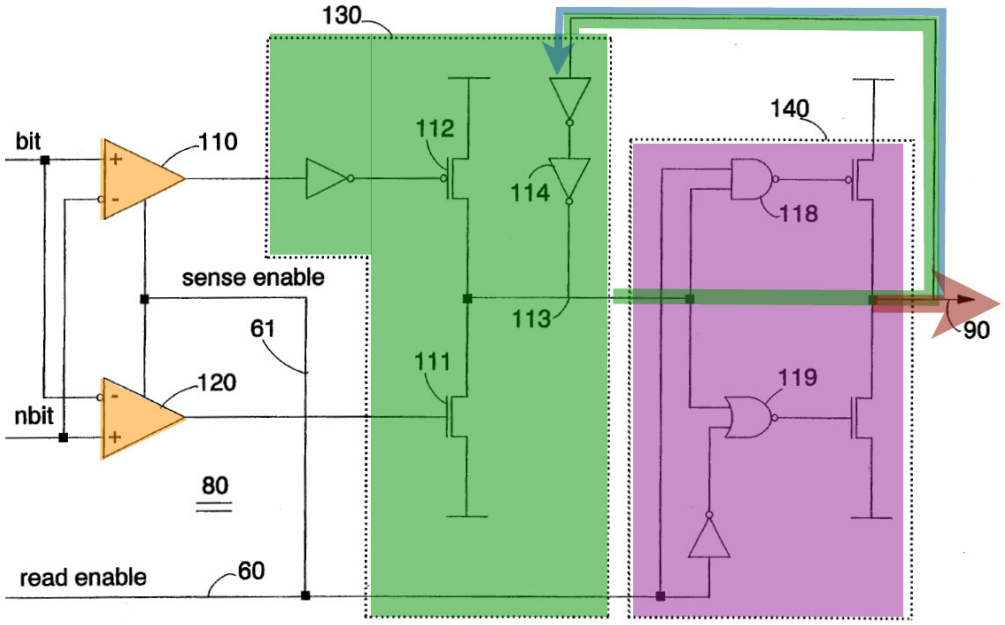


Fig. 2

According to Petitioner, this highlighted version of Figure 2 shows:

(1) two sense amplifiers "highlighted in orange,"

(2) a data latch "highlighted in green,"

(3) a feedback path "highlighted in blue,"

(4) an output data bus "highlighted in red," and

(5) an output buffer "highlighted in purple."

Pet. 30 (citing Ex. 1003 ¶¶ 87–91); *see* Ex. 1003 ¶ 87.

To put the Figure 2 embodiment in context, Petitioner presents the highlighted version of Oldham's Figure 1 reproduced below:

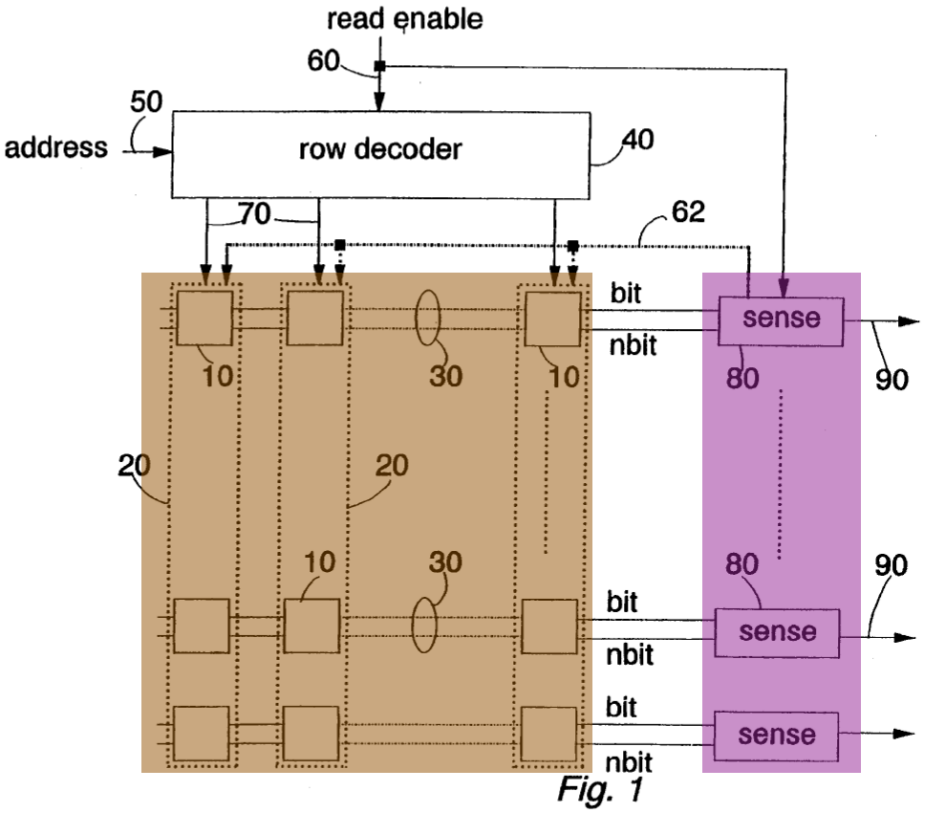


Fig. 1

According to Petitioner, this highlighted version of Figure 1 shows a random-access memory comprising an array of memory cells 10 "highlighted in brown" and multiple sense-amplifier circuits 80 "highlighted in purple." Pet. 28 (citing Ex. 1003 ¶ 84; Ex. 1005, 4:36–38, Fig. 1); *see* Ex. 1003 ¶ 84. Further, Petitioner asserts that output 90 connects to "a common (shared) data bus." Pet. 29 (citing Ex. 1005, 5:25–26).

(a) Preamble

Claim 1's preamble recites "[a] sensing circuit for sensing data from a memory array and providing the sensed data to an output data bus." Ex. 1001, 10:11–13. Petitioner asserts that Oldham's Figure 2 embodiment satisfies claim 1's preamble because Oldham discloses multiple sense-amplifier circuits "configured for sensing data from 'an array of memory cells 10 arranged as a number of rows 20 of memory cells'" and Figure 2

shows sense-amplifier circuit 80. Pet. 31–33 (quoting Ex. 1005, 4:37–38); *see* Ex. 1003 ¶¶ 102–105; Ex. 1005, 4:23–25, 4:36–38, Figs. 1–2. Petitioner also asserts that (1) sense-amplifier circuit 80 generates "an output signal 90 representing the stored bit in the corresponding memory cell 10 in the currently selected row 20" and (2) tri-state buffering in sense-amplifier circuit 80 "allows the output 90 to be connected to a shared system data bus." Pet. 32–33 (citing Ex. 1005, 5:14–19); *see* Ex. 1003 ¶¶ 104–105; Ex. 1005, 5:14–19, 6:17–37, Figs. 1–2.

Patent Owner does not make any arguments specific to claim 1's preamble. *See, e.g.*, Resp. 25–35.

Generally, a preamble does not limit a claim. *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002). Here, we need not decide whether claim 1's preamble limits the claim because we agree with Petitioner that Oldham's Figure 2 embodiment satisfies claim 1's preamble. Specifically, sense-amplifier circuit 80 senses data from a memory array and provides the sensed data to an output data bus, and thus satisfies claim 1's preamble. Ex. 1005, 5:14–6:37, Figs. 1–2; *see* Ex. 1003 ¶¶ 102–105.

(b) The "Sense Amplifier" Limitation

Claim 1 requires "a sense amplifier coupled to the memory array." Ex. 1001, 10:14. Petitioner asserts that Oldham's Figure 2 embodiment satisfies this limitation for two reasons. Pet. 34–36; *see* Ex. 1003 ¶¶ 106–108. First, Petitioner contends that Oldham discloses sense-amplifier circuit 80 "configured for sensing data from 'an array of memory cells 10 arranged as a number of rows 20 of memory cells'" in Figure 1. Pet. 34 (quoting Ex. 1005, 4:37–38); *see* Ex. 1003 ¶¶ 106–107; Ex. 1005,

4:23–25, 4:36–38, Figs. 1–2. Second, Petitioner contends that sense-amplifier circuit 80 includes a "pair of sense amplifiers 110 and 120" coupled "via the bitlines 'bit' and 'nbit,' to the memory array" in Figure 1. Pet. 35–36; *see* Ex. 1003 ¶ 108. According to Petitioner, "[t]he bit / nbit pairs 30 coming from the memory array 10/20 [in Figure 1] are also shown as input[s] to sense amplifiers 110 and 120" in Figure 2's "detailed illustration" of sense-amplifier circuit 80. Pet. 35; *see* Ex. 1003 ¶ 107.

Patent Owner does not make any arguments specific to claim 1's "sense amplifier" limitation. *See, e.g.*, Resp. 25–35.

We agree with Petitioner that Oldham's Figure 2 embodiment satisfies claim 1's "sense amplifier" limitation. Specifically, sense-amplifier circuit 80 includes sense amplifiers 110 and 120. Ex. 1005, 5:20–23, Fig. 2; *see* Ex. 1003 ¶¶ 88, 105, 107; Ex. 2001 ¶ 69. Sense amplifiers 110 and 120 each receive signals on the bit and nbit lines coupled to each sense amplifier's inverting and noninverting input terminals. Ex. 1005, 5:23–26, Fig. 2; *see id.* at 5:28–53; Ex. 1003 ¶¶ 87–88, 105, 107; Ex. 2001 ¶ 70. In addition, Oldham explains that "[t]he invention makes use of two sense amplifiers to read data stored in one memory cell." Ex. 1005, 2:59–60. Further, as shown in Figure 1, the bit and nbit lines couple a sense-amplifier circuit, e.g., sense-amplifier circuit 80, to a memory cell in Figure 1's memory array. Ex. 1005, 4:36–44, 4:63–64, Fig. 1; *see* Ex. 1003 ¶¶ 84, 103, 106.

For the reasons discussed above, Oldham's Figure 2 embodiment satisfies claim 1's requirement for "a sense amplifier coupled to the memory array."

(c) The "Data Storage Device" Limitation

Claim 1 also requires "a data storage device coupled between the sense amplifier and the output data bus." Ex. 1001, 10:15–16. Petitioner asserts that Oldham's Figure 2 embodiment satisfies this limitation because Figure 2 illustrates latch circuit 130 and Oldham "makes clear" that "latch circuit 130 is a data storage device." Pet. 36–38; *see* Ex. 1003 ¶¶ 109–113. To support its assertion, Petitioner presents the highlighted version of Figure 2 reproduced below:

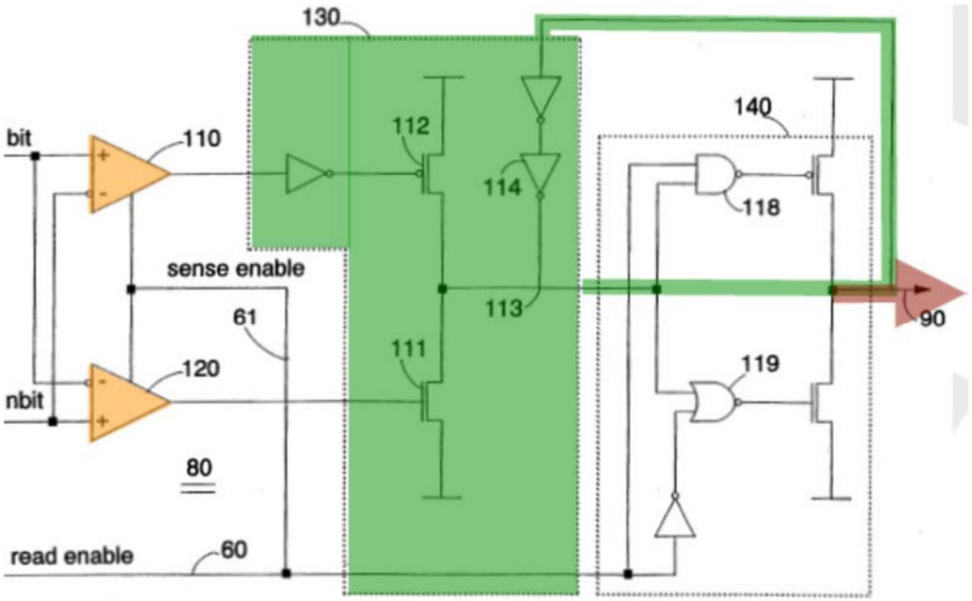


Fig. 2

According to Petitioner, this highlighted version of Figure 2 "shows the latch circuit 130 highlighted in green and coupled between the sense amplifiers 110 / 120 (highlighted in orange) and the output 90 (highlighted in red)." Pet. 37; *see* Ex. 1003 ¶¶ 109, 112.

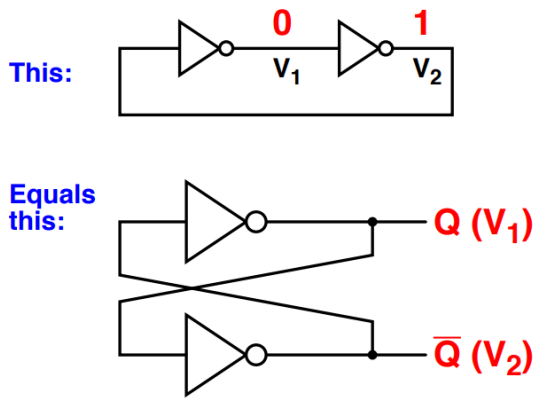
Petitioner contends that latch circuit 130 includes transistors 111 and 112 and a "feedback path from the output 90 to a node 113" at the output of transistors 111 and 112. Pet. 38 (citing Ex. 1005, 5:61–63); *see* Ex. 1003 ¶¶ 90, 111. Petitioner also contends that the feedback path includes "a pair

of inverters," i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input. Pet. 38–39; *see* Ex. 1003 ¶¶ 90, 111.

Dr. Jacob testified that latch circuit 130 includes the following: (1) a "tristate buffer" at "the left-hand side of" the latch circuit "comprising transistors 111 and 112" that "is used to write data to the latch"; (2) a "pair of cross-coupled inverters that retain the data"; and (3) a "feedback path from the output 90 to a node 113" at the output of transistors 111 and 112. Ex. 1003 ¶¶ 109–112. He explained that the "pair of cross-coupled inverters (114 and the one above it)" form "a data storage device." *Id.* ¶ 112; *see id.* ¶ 91.

In addition, Dr. Jacob described "the concept of feedback" as a "fundamental concept[] of data storage." Ex. 1003 ¶ 64; *see* Pet. 15–16. He explained that a pair of cross-coupled inverters provides "a stable positive feedback loop that has two stable states" and the pair "can retain data." Ex. 1003 ¶ 65; *see id.* ¶ 28; Ex. 2004, 20:8–21:5, 25:19–26:9; Pet. 16. Further, he identified a pair of cross-coupled inverters as a "latch." Ex. 1010 ¶¶ 10 n.1, 60 (blue highlighting in second diagram and accompanying text); *see* Ex. 1003 ¶¶ 109, 112; Ex. 2004, 20:8–21:5. And he described a latch as one of "the simplest static storage devices typically used in systems today." Ex. 1010 ¶ 10 n.1.

Dr. Jacob supplied the following diagram to illustrate a latch:



Data retention as a positive feedback loop.

This diagram shows equivalent representations for a latch, i.e., two serially connected inverters in the upper part of the diagram and a pair of cross-coupled inverters in the lower part of the diagram. Ex. 1003 ¶¶ 64–66; Ex. 1010 ¶ 10 & n.1; *see* Ex. 2004, 20:8–21:5; *see* Pet. 15–16.

Consistent with Dr. Jacob's testimony, the '145 patent identifies a latch as a "data storage device." Ex. 1001, 3:6–7; *see id.* at 4:64–66.

Patent Owner does not dispute that latch circuit 130 in Figure 2 includes transistors 111 and 112 and a "feedback path from the output 90 to a node 113" at the output of transistors 111 and 112 or that the feedback path includes "a pair of inverters," i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input. *See* Resp. 29–31, 31 n.1; Sur-reply 7–13; Ex. 2001 ¶ 74.

We agree with Petitioner that Oldham's Figure 2 embodiment satisfies claim 1's "data storage device" limitation. In particular, Oldham explains that "during a read operation, the output of only one of the sense amplifiers" 110 and 120 "will rise to a high logical state," while the other sense amplifier's output "will remain at a low logical state." Ex. 1005, 5:46–50; *see* Ex. 2001 ¶ 72. The transient high logical state at one sense

amplifier's output "sets the output of the latch circuit 130" at node 113 "to one of two possible states." Ex. 1005, 5:54–56, 5:61–63, 6:17; *see* Ex. 1003 ¶ 89; Ex. 2001 ¶ 73.

Specifically, when sense amplifier 110 outputs a logic high, transistor 112 in latch circuit 130 receives a logic low as an input and outputs a logic high at node 113. Ex. 1005, 5:65–6:2, Fig. 2; Ex. 1003 ¶ 90; Ex. 2001 ¶ 74. Similarly, when sense amplifier 120 outputs a logic high, transistor 111 in latch circuit 130 receives a logic high as an input and outputs a logic low at node 113. *See* Ex. 1005, 6:2–4, Fig. 2; Ex. 1003 ¶ 90; Ex. 2001 ¶ 74.

A feedback path connects output 90 to node 113. Ex. 1005, 5:61–63, 6:17–20, Fig. 2; Ex. 1003 ¶¶ 90–91, 111–112; Ex. 2001 ¶ 74. The feedback path includes an unnumbered inverter and a so-called "weak," i.e., inverter 114. Ex. 1005, 5:63–65, Fig. 2; Ex. 1003 ¶¶ 90, 111; Ex. 2001 ¶ 74. Hence, when transistor 112 outputs a logic high, "the logic high output of that transistor will override the output of the inverter 114 to force the node 113 high." Ex. 1005, 5:65–6:2, Fig. 2; Ex. 1003 ¶¶ 90–91, 112; Ex. 2001 ¶ 74. Similarly, when transistor 111 outputs a logic low, "the logic low output of that transistor will override the output of the inverter 114 to force the node 113 low." Ex. 1005, 6:2–4, Fig. 2; Ex. 1003 ¶¶ 90–91, 112; Ex. 2001 ¶ 74.

During the idle state of sense amplifiers 110 and 120, in contrast to a read operation, "the input to the transistor 111 is logic low and the input to the transistor 112 is logic high, so the weak inverter [114] is not overridden." Ex. 1005, 6:5–7; Ex. 1003 ¶¶ 90, 111; Ex. 2001 ¶ 74. "The logical state of the node 113 therefore represents the previous state of the output 90" until

"that output is overwritten with a new value by the sense amplifier circuit." Ex. 1005, 6:12–16; Ex. 1003 ¶¶ 90, 111; Ex. 2001 ¶ 75. Accordingly, latch circuit 130 stores data and constitutes "a data storage device."

Further, Oldham's Figure 2 (reproduced above in § III.C.2) shows latch circuit 130 coupled between sense amplifiers 110 and 120 and the output data bus, i.e., coupled indirectly through tri-state buffer circuit 140. Ex. 1005, Fig. 2; *see* Ex. 1003 ¶¶ 109–110, 113.

For the reasons discussed above, Oldham's Figure 2 embodiment satisfies claim 1's requirement for "a data storage device coupled between the sense amplifier and the output data bus."

(d) The "Data Feedback Circuit" Limitation

Claim 1 additionally requires "a data feedback circuit having an input terminal coupled to the output data bus and an output terminal coupled to the data storage device." Ex. 1001, 10:62–64. Petitioner asserts that Oldham's Figure 2 embodiment satisfies this limitation because Figure 2 depicts a data feedback circuit from output 90 that "is fed back into the latch circuit as part of its operation." Pet. 39–41 (emphasis omitted) (quoting Ex. 1005, 6:17–21); *see* Ex. 1003 ¶¶ 114–116. To support its assertion, Petitioner presents the highlighted version of Figure 2 reproduced below:

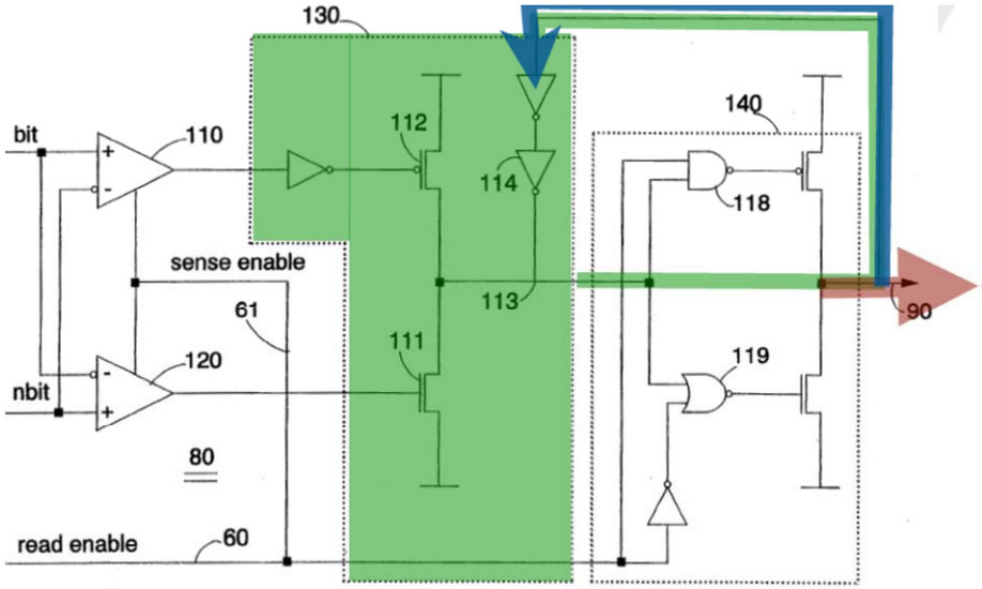


Fig. 2

According to Petitioner, this highlighted version of Figure 2 shows the data feedback circuit "highlighted in blue," the data storage device "highlighted in green," and the output data bus "highlighted in red." Pet. 40–41; Reply 2–3; *see* Ex. 1003 ¶¶ 115–116. According to Dr. Jacob, "[t]he data feedback circuit has as its input the output data bus 90 (in red), and as its output the latch circuit 130 (in green), the claimed data storage device." Ex. 1003 ¶¶ 116, 139.

Patent Owner disputes that Oldham's Figure 2 embodiment satisfies claim 1's "data feedback circuit" limitation. *See* Resp. 25–35; Sur-reply 1–14. Specifically, Patent Owner asserts that claim 1 recites "three separate and distinct elements: (i) a sense amplifier, (ii) a data storage device, and (iii) a data feedback circuit." Resp. 25; *see* Sur-reply 1–2. Patent Owner contends that "the claim language itself confirms that these separately listed elements are separate and distinct components." Resp. 26–27. Patent Owner also asserts that the claim recites "specific structural limitations of the sensing circuit, where the various components are

interconnected to each other," and "[a]s such, they must be separate and distinct." Sur-reply 2; *see id.* at 4.

In addition, Patent Owner contends that "the entirety of the specification of the '145 patent confirms that the separately listed elements of independent claim 1 are separate and distinct components." Resp. 27–28; *see* Sur-reply 2–3. Patent Owner also contends that "nothing in the specification suggests that these separately listed elements could be the same or overlapping structures." Resp. 28–29; *see* Sur-reply 1–2, 5.

Further, Patent Owner argues that Oldham's Figure 2 embodiment lacks a "data feedback circuit" separate and distinct from a "data storage device." *See* Resp. 29–32; Sur-reply 6–14. In particular, Patent Owner contends that the conductor that "Petitioner identifies as the feedback path is not a separate and distinct element, but instead is an integral part of latch circuit 130." Resp. 32. Patent Owner also contends that Petitioner attempts "to satisfy two separate and distinct elements of claim 1, i.e., the data storage device and the data feedback circuit, by pointing to a single structure from Oldham." *Id.* at 32, 35.

In response, Petitioner quotes Oldham's disclosure that "'the **output** from latch circuit 130 (at the node 113)' is '**fed back into the latch** as part of its operation' via the feedback path from output 90 to the latch 130." Reply 3 (emphasis added by Petitioner) (quoting Ex. 1005, 6:17–21). Petitioner then contends that "the latch 130 . . . must be considered as separate from the feedback path in Oldham" because "Oldham describes that the output of one circuit, the latch 130, is fed back into that circuit by another circuit, the feedback path." *Id.*; *see* Ex. 1010 ¶¶ 20–21.

In addition, Petitioner disagrees that claim 1 "only covers apparatuses with entirely separate and distinct structures corresponding to each element." Reply 9. Petitioner asserts that in Oldham's Figure 2 the structure constituting the claimed "data feedback circuit" differs from the structure constituting the claimed "data storage device," although Petitioner concedes the structures overlap. *See id.* at 11.

In particular, Petitioner identifies the following elements in Figure 2 as the claimed "data storage device": transistors 111 and 112; the unnumbered inverter connected to transistor 112's input; node 113; the two serially connected inverters, i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input; and the conductor connected between output 90 and the unnumbered inverter's input. Pet. 30–31, 36–37; *see* Reply 2–4, 11; Ex. 1003 ¶¶ 92, 109. Further, Petitioner identifies the following elements in Figure 2 as the claimed "data feedback circuit": the two serially connected inverters, i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input; and the conductor connected between output 90 and the unnumbered inverter's input. Reply 11; *see id.* at 16; Pet. 40–41.

Petitioner then contends that "latch 130 and feedback path have separate functions" and that "latch 130 includes numerous circuit elements separate from the feedback path that perform data input and storage functions apart from the feedback path." Reply 11.

We agree with Patent Owner that Oldham's Figure 2 embodiment lacks the claimed "data feedback circuit." For the reasons explained below, we conclude that claim 1 requires distinct structural elements for the "data storage device" and the "data feedback circuit." But Petitioner does not

identify distinct structural elements for each of those claim limitations in the Figure 2 embodiment.

We start by analyzing the claim language. Claim 1 lists three separate circuit elements: (1) a sense amplifier, (2) a data storage device, and (3) a data feedback circuit. Ex. 1001, 10:11–19. "Where a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s]' of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) (alteration in original) (quoting *Gaus v. Conair Corp.*, 363 F.3d 1284, 1288 (Fed. Cir. 2004)).

Nothing in claim 1 suggests that the "data storage device" and the "data feedback circuit" can be the same structural elements. Rather, claim 1 requires that the "data feedback circuit" be "coupled to" the "data storage device." Ex. 1001, 10:17–19. The requirement for coupling between the claimed circuit elements indicates that distinct structural elements must correspond to the claimed circuit elements. For instance, if the "data storage device" and the "data feedback circuit" were the same structural elements, then the "data feedback circuit" would be coupled to itself. But that would render the claim nonsensical. A construction that renders a claim nonsensical "cannot be correct." *Becton*, 616 F.3d at 1255 (citing *Schoenhaus v. Genesco, Inc.*, 440 F.3d 1354, 1357 (Fed. Cir. 2006)).

Moreover, nothing in the '145 patent's other claims suggests that the "data storage device" and the "data feedback circuit" can be the same structural elements. Ex. 1001, 10:20–12:58. Dependent claim 5 further defines the "data storage device" by reciting certain components, and dependent claims 8 and 9 further define the "data feedback circuit" by

reciting certain components. *Id.* at 10:54–61, 11:1–39. In those claims, there is no overlap between the "data storage device" components and the "data feedback circuit" components. *Id.*

The '145 patent's specification supports the conclusion that claim 1 requires distinct structural elements for the "data storage device" and the "data feedback circuit." Figure 2 (reproduced above in § II.C) depicts distinct blocks for the "data storage device," i.e., data register 13, and the "data feedback circuit," i.e., data feedback circuit 23. Ex. 1001, 2:34–35, 3:39–45, Fig. 2. Figures 3 and 4 (reproduced above in § II.C) include more detail for the "data storage device" and the "data feedback circuit" and depict distinct components corresponding to the claimed circuit elements. *Id.* at 2:36–41, Figs. 3–4; *see id.* at 5:58–9:45.

In Figure 3, the following components correspond to the "data storage device": inverter 131 and inverter 132 that "form a latch that holds the data." Ex. 1001, 6:34–40, Fig. 3; *see id.* at 10:54–61; Ex. 2001 ¶ 55. In Figure 3, the following components correspond to the "data feedback circuit": NOR gate 231, NOR gate 232, inverter 233, PMOS transistor 234, and NMOS transistor 235.[2] Ex. 1001, 7:18–31, Fig. 3; *see id.* at 11:1–17; Ex. 1003 ¶¶ 79–80; Ex. 2001 ¶ 57.

In Figure 4, the following components correspond to the "data storage device": inverter 131 and inverter 132 that "form a latch that holds the data." Ex. 1001, 6:34–40, 8:4–22, Fig. 4; *see id.* at 10:54–61; Ex. 2001 ¶ 61. In Figure 4, the following components correspond to the "data feedback circuit": NOR gate 231, NOR gate 232, PMOS transistor 234, NMOS

[2] "PMOS" stands for P-type metal-oxide semiconductor, and "NMOS" stands for N-type metal-oxide semiconductor.

transistor 235, NMOS transistor 236, and NAND gate 237. Ex. 1001, 7:22–24, 8:35–47, Fig. 4; *see id.* at 11:18–39; Ex. 1003 ¶ 81; Ex. 2001 ¶ 62.

Hence, each embodiment disclosed in the '145 patent includes distinct structural elements for the "data storage device" and the "data feedback circuit." Moreover, in each embodiment there is no overlap between the components corresponding to the "data storage device" and the components corresponding to the "data feedback circuit." Thus, nothing in the '145 patent's specification suggests that the "data storage device" and the "data feedback circuit" can be the same structural elements.

In addition, nothing in the '145 patent's prosecution history suggests that the "data storage device" and the "data feedback circuit" can be the same structural elements. *See generally* Ex. 1002. For example, the Examiner allowed the claims in the first Office action but provided no statement of reasons for allowance. *Id.* at 55–58.

For the reasons discussed above, we conclude that claim 1 requires distinct structural elements for the "data storage device" and the "data feedback circuit." To demonstrate anticipation, however, Petitioner does not identify distinct structural elements corresponding to each claimed circuit element in Oldham's Figure 2 embodiment.

Rather, as discussed above, Petitioner identifies the following elements in Figure 2 as the claimed "data storage device": transistors 111 and 112; the unnumbered inverter connected to transistor 112's input; node 113; the two serially connected inverters, i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input; and the conductor connected between output 90 and the unnumbered inverter's input. Pet. 30–31, 36–37; *see* Reply 2–4, 11; Ex. 1003 ¶¶ 92, 109. Further, Petitioner

identifies the following elements in Figure 2 as the claimed "data feedback circuit": the two serially connected inverters, i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input; and the conductor connected between output 90 and the unnumbered inverter's input. Reply 11; *see id.* at 16; Pet. 40–41.

Petitioner relies on overlapping structural elements for the "data storage device" and the "data feedback circuit." Specifically, Petitioner identifies the two serially connected inverters in latch circuit 130 and the conductor connected between output 90 and the unnumbered inverter's input for both the "data storage device" and the "data feedback circuit." Thus, the structural elements that Petitioner identifies for the "data feedback circuit" constitute a subset of the structural elements that Petitioner identifies for the "data storage device." Because claim 1 requires distinct structural elements for the "data storage device" and the "data feedback circuit," Petitioner has not demonstrated that Oldham's Figure 2 embodiment includes every element of claim 1 arranged as required by the claim.

Quoting *Linear Technology Corp. v. International Trade Commission*, 566 F.3d 1049 (Fed. Cir. 2009), Petitioner asserts that "the difference in functions and 'additional components' in latch 130 as compared to the feedback path confirm that those circuits are 'different and distinct in their topology and their operation.'" Reply 11. But the circumstances in *Linear* differ from the circumstances here.

There, certain claims required a "first circuit" for generating a "first feedback signal," a "second circuit" for generating a "first control signal," and a "third circuit" for generating a "second control signal." *Linear*, 566 F.3d at 1052–53. An Administrative Law Judge of the International

Trade Commission construed the "second circuit" and the "third circuit" as "precluding shared use of the same circuitry," i.e., "that every element in the second circuit [must] be completely distinct from every element in the third circuit." *Id.* at 1055. The Commission disagreed. *Id.* The Commission determined that "even a difference such as having an additional [component] can cause the circuits to be different and distinct in their topology and their operation." *Id.* (alteration in original).

The Federal Circuit agreed with the Commission that the "second circuit" and the "third circuit" did not "require entirely separate and distinct circuits." *Linear*, 566 F.3d at 1055, 1060. The court reasoned that "there is nothing in the claim language or specification that supports narrowly construing the terms to require a specific structural requirement or entirely distinct 'second' and 'third' circuits." *Id.* at 1055. In addition, the court noted that the "specification expressly disclose[d] that the 'second circuit' and 'third circuit' can share common components." *Id.* Hence, when analyzing the infringement issues, the court decided that certain circuitry unique to the "third circuit" distinguished the "third circuit" from the "second circuit" in the accused devices. *Id.* at 1061–62; *see id.* at 1056 n.3.

Here, in contrast to *Linear*, Petitioner does not identify any circuitry unique to the "data feedback circuit" that distinguishes it from the "data storage device" in Oldham's Figure 2 embodiment. *See* Pet. 30–31, 36–37; Reply 2–4, 11. Instead, as discussed above, the structural elements that Petitioner identifies for the "data feedback circuit" constitute a subset of the structural elements that Petitioner identifies for the "data storage device." As Patent Owner asserts, the structural elements for the "data storage

device" subsume the structural elements for the "data feedback circuit." *See* Sur-reply 3–4 n.1.

Petitioner concedes that "the feedback path from output 90 to node 113 is part of the operation of latch 130 and they work in conjunction in Oldham." Reply 7. But Petitioner contends that the feedback path and latch 130 "also function separately." *Id.* According to Petitioner, sense-amplifier circuit 80 exhibits "two modes of operation." *Id.* at 8. Patent Owner admits that the circuit "has two states, active (read enabled) and inactive (read disabled)." Sur-reply 7–8.

Petitioner asserts that in a first or active mode, "data is being driven to the output bus (read enable is high or one) such that the feedback path is not active as it is not updating the latch." Reply 8; *see* Ex. 1010 ¶¶ 25–26, 39–40, 60. Petitioner asserts that in a second or inactive mode, "data is not being driven to the output bus (read enable is low or zero) such that the feedback path is active and updating the latch." Reply 8; *see* Ex. 1010 ¶¶ 25–26, 39–40, 60.

That sense-amplifier circuit 80 exhibits "two modes of operation" does not alter the fact that Petitioner relies on overlapping structural elements for the "data storage device" and the "data feedback circuit." Different operational modes do not equate to different structural elements. *See* Tr. 10:14–22. Moreover, the feedback path serves an important purpose in sense-amplifier circuit 80 when it operates in each mode, as Dr. Jacob's testimony demonstrates.

For the first or active mode, Dr. Jacob provided conflicting testimony. When addressing anticipation, he stated that "the feedback path ***is not*** *doing anything useful*" in the active mode because "the sensed value and the output

bus are the same." Ex. 1010 ¶ 39 (emphasis in original). But when addressing obviousness, he contradicted his earlier statement. *See id.* ¶ 60.

When addressing obviousness, Dr. Jacob explained that in the active mode the two serially connected inverters in latch circuit 130 and the conductor connected between output 90 and the unnumbered inverter's input form "a path that retains the data being driven out onto the bus, so that the sense amplifiers can start sensing a new value without disrupting what the output buffer is driving onto the bus." *Id.* Retaining the data being driven out onto the bus permits decoupling the sense amplifiers from the output. Ex. 2004, 48:12–49:16. And decoupling the sense amplifiers from the output permits the circuit to perform certain operations earlier than it otherwise would have, such as precharging the bit and nbit lines and sensing a new value. *Id.* at 48:12–51:3; *see* Ex. 1010 ¶ 60.

In addition, Dr. Jacob admitted that "the feedback path is part of the latch's operation." Ex. 1010 ¶ 21. That admission comports with Oldham's disclosure that "[t]he output of the latch circuit 130 (at the node 113) is buffered by the tri-state buffer circuit 140 and presented as the buffered output 90, which in turn is fed back into the latch circuit as part of its operation." Ex. 1005, 6:17–20.

Also, Dr. Jacob explained that a pair of cross-coupled inverters provides "a stable positive feedback loop that has two stable states" and the pair "can retain data." Ex. 1003 ¶ 65; *see id.* ¶ 28; Ex. 2004, 20:8–21:5, 25:19–26:9; Pet. 16. He described the two serially connected inverters in latch circuit 130 as a pair of cross-coupled inverters. Ex. 1003 ¶¶ 109, 112; Ex. 1010 ¶ 60 (blue highlighting in second diagram and accompanying text). Further, as discussed above for claim 1's "data storage device" limitation,

Dr. Jacob described "the concept of feedback" as a "fundamental concept[] of data storage." Ex. 1003 ¶ 64; *see* Pet. 15–16. Moreover, he admitted that the feedback loop with the feedback path "actually retains or stores the data." Ex. 2004, 21:6–13.

Thus, by allowing latch circuit 130 to "actually retain[] or store[] the data," the feedback path serves an important purpose when the circuit operates in the first or active mode.

The feedback path also serves an important purpose when the circuit operates in the second or inactive mode. Dr. Jacob explained that "the feedback path is enabled" in the inactive mode "to store the bus's data value on node 90 at node 113." Ex. 1010 ¶ 39 (emphasis omitted); *see id.* ¶ 57; Ex. 2004, 40:18–41:1, 42:15–43:7. He further explained that the enabled feedback path precharges "the circuit's internals to whatever is currently on the bus, so that when the circuit *does* become active, its initial output will be the same as the bus and will not 'glitch' as it might without the circuit-precharging activity." Ex. 1010 ¶ 60 (emphasis in original); *see id.* ¶ 57.

Thus, by preventing "glitches" that waste power, the feedback path serves an important purpose when the circuit operates in the second or inactive mode. *See* Ex. 1005, 2:1–4, 2:35–38; *see also* Ex. 1001, 1:18–22.

In the Reply, Petitioner relies on the dotted box for latch circuit 130 in Oldham's Figure 2 (reproduced above in § III.C.2) to distinguish the structural elements for the "data storage device" from the structural elements for the "data feedback circuit." *See* Reply 4–5; *see* Ex. 1010 ¶ 10. Specifically, Petitioner asserts that "latch circuit 130 in Oldham, by itself, is depicted with a dotted box as shown in Figure 2." Reply 4. According to Petitioner, "it is clear from Oldham's written description and Figure 2" that

"Oldham discloses a separate and distinct data storage device in the form of latch 130 that outputs its value at node 113 and receives feedback from output 90 via a separate feedback path circuit that runs from output 90 back into latch 130." *Id.* at 5; *see* Ex. 1010 ¶ 24.

But Dr. Jacob's testimony refutes Petitioner's assertions. Dr. Jacob relied on latch circuit 130 and the feedback path from output 90 back into latch circuit 130 for the claimed "data storage device." Ex. 1003 ¶¶ 87, 91–92, 109, 112; *see* Ex. 2004, 21:22–22:5, 25:6–26:9, 72:4–19, 76:9–15. Among other things, he provided the highlighted version of Figure 2 reproduced below:

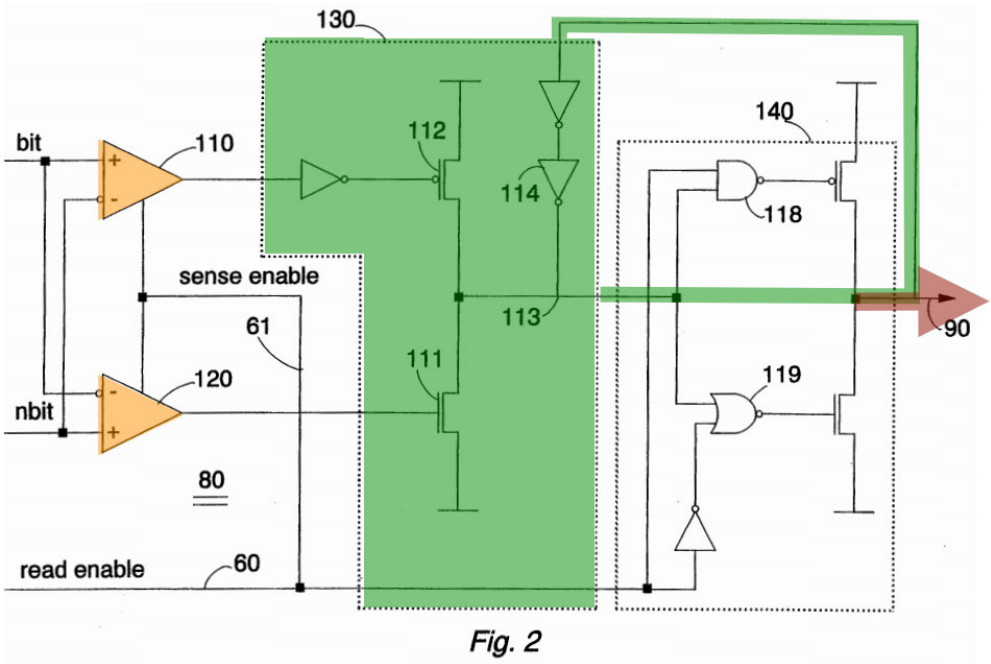


Figure 2 from Oldham, with sense amplifiers in orange, data storage device in green, and output data bus in red.

According to Dr. Jacob, this highlighted version of Figure 2 shows two sense amplifiers highlighted in orange, a data storage device highlighted in green, and an output data bus highlighted in red. Ex. 1003 ¶ 109. This highlighted version of Figure 2 shows the feedback path from output 90

back into latch circuit 130 highlighted in green, i.e., as part of the data storage device. *Id.* ¶¶ 109, 112; *see* Ex. 2004, 21:22–22:5, 22:15–23:4, 25:6–26:9.

Dr. Jacob explained that while Oldham discloses "a data storage device, [i.e.,] Oldham's latch circuit 130 . . . drawn in a dotted line," he "included also the feedback path that turns it into a static latch." Ex. 2004, 21:22–22:4; *see id.* at 76:9–15. He said, "[T]hat's not what Oldham says is the latch. I added that." *Id.* at 22:4–5. He further explained that "in Figure 2 the things that are highlighted in green are -- are highlighting the functionality of the system." *Id.* at 22:22–24. In addition, as discussed above, Dr. Jacob admitted that the feedback loop with the feedback path "actually retains or stores the data." *Id.* at 21:6–13.

Hence, Petitioner misplaces its reliance on the dotted box for latch circuit 130 in Oldham's Figure 2 to distinguish the structural elements for the "data storage device" from the structural elements for the "data feedback circuit." The dotted box for latch circuit 130 in Figure 2 does not override circuit operation.

For the reasons discussed above, Petitioner does not identify structural elements for the "data feedback circuit" distinct from the structural elements for the "data storage device" in Oldham's Figure 2 embodiment. Consequently, that embodiment does not satisfy claim 1's requirement for "a data feedback circuit having an input terminal coupled to the output data bus and an output terminal coupled to the data storage device."

(e) Whether Oldham Anticipates Claim 1

For the reasons discussed above, Petitioner has not shown by a preponderance of the evidence that Oldham's Figure 2 embodiment includes

every element of claim 1 arranged as required by the claim. Hence, Petitioner has not shown by a preponderance of the evidence that claim 1 is unpatentable under § 102(b) as anticipated by Oldham.

4. DEPENDENT CLAIM 6

Claim 6 depends directly from claim 1. Ex. 1001, 10:62–64. Thus, claim 6 incorporates all of claim 1's limitations. *See* 35 U.S.C. § 112 ¶ 4. For the reasons discussed above for claim 1, Petitioner has not shown by a preponderance of the evidence that claim 6 is unpatentable under § 102(b) as anticipated by Oldham.

5. INDEPENDENT CLAIM 15

(a) Preamble

Claim 15's preamble recites "[a] method for controlling data transitions on an output data bus of a semiconductor device having a memory array." Ex. 1001, 12:29–30. Petitioner asserts that Oldham's Figure 2 embodiment satisfies claim 15's preamble because a "feedback circuit" in Figure 2 controls data transitions on an output data bus of a semiconductor device having a memory array by reducing invalid data transitions or "glitches." Pet. 53; *see* Ex. 1003 ¶¶ 124–131. Petitioner also asserts that the '145 patent discloses a "feedback circuit" as a mechanism "to accomplish the elimination of invalid data transitions." Reply 24 (citing Ex. 1001, 5:19–33). Petitioner further asserts that the "feedback circuit" in Figure 2 has "the same functionality" as the "feedback circuit" disclosed in the '145 patent. *Id.*

Patent Owner disputes that a "feedback circuit" in Oldham's Figure 2 controls data transitions on an output data bus of a semiconductor device having a memory array. *See* Resp. 49–51; Sur-reply 23–24. According to

Patent Owner, "data transitions" in Figure 2 occur "when the values output by transistors 111 and 112 transition from low to high and vice-versa." Sur-reply 24. Patent Owner contends that "what controls data transitions in Oldham are sense amplifiers 110 and 120, PMOS transistor 112 and NMOS transistor 111." Resp. 49; *see* Sur-reply 24.

Patent Owner asserts that "if the gate of PMOS transistor 112 goes to logic low" in response to sense amplifier 110, "the logic high output of the drain of transistor 112 will override the output of the inverter 114 and force node [113] to a high logic state." Resp. 50; *see* Ex. 2001 ¶¶ 123–124. Patent Owner also asserts that "if the gate of NMOS transistor 111 goes to logic high" in response to sense amplifier 120, "the logic low output of the drain of transistor 111 will override the output of inverter 114 and force node 113 to a logic low state." Resp. 50; *see* Ex. 2001 ¶¶ 123–124. Patent Owner argues that through those operations sense amplifiers 110 and 120 in conjunction with transistors 111 and 112 "control when there is a new value to overwrite the previous state of output 90." Resp. 50–51; *see* Ex. 2001 ¶ 124.

According to Patent Owner, the feedback path "merely loops and stores the previous state of output 90 until that output is overwritten with a new value" by either a "logic high" output by PMOS transistor 112 or a "logic low" output by NMOS transistor 111. Resp. 50; *see* Ex. 2001 ¶ 124.

As explained above, a preamble generally does not limit a claim. *Allen Eng'g*, 299 F.3d at 1346. Here, we need not decide whether claim 15's preamble limits the claim because we agree with Petitioner that Oldham's Figure 2 embodiment satisfies claim 15's preamble. For the reasons explained below, the Figure 2 embodiment controls data transitions

on an output data bus of a semiconductor device having a memory array by reducing invalid data transitions or "glitches."

The '145 patent identifies an inactive memory block of a larger system as a potential source of invalid data transitions. Ex. 1001, 1:49–52; *see id.* at 2:62–67, 5:19–29; Ex. 1003 ¶ 79; Ex. 2001 ¶¶ 43, 50; Resp. 4–5. The patent explains that an inactive memory block of a larger system may cause invalid data transitions because "there is no guarantee as to what signals will be driven onto the output data bus prior to the sense amplifier sensing the valid data from the memory array and providing that valid data to the output data bus." Ex. 1001, 1:49–56; *see* Ex. 2001 ¶ 43.

To eliminate invalid data transitions due to an inactive memory block of a larger system, "[d]ata storage devices of inactive [memory] blocks are preloaded with the valid data appearing on the output data bus via a feedback circuit, thereby preventing potentially invalid data otherwise stored in an in active [sic] storage device from being transferred to the output data bus upon activation." Ex. 1001, 2:62–67, code (57); *see id.* at 5:19–57, 7:18–39, 8:35–39, 9:12–25, 9:52–59, Figs. 3–4; Ex. 1003 ¶¶ 79–81; Ex. 2001 ¶¶ 50–51. Thus, "the data sensing circuit is further improved by eliminating invalid data transitions from appearing on the output data bus through use of feedback." Ex. 1001, 2:58–62, code (57); *see id.* at 5:19–57, 9:52–59; Ex. 2001 ¶¶ 44–46.

Hence, as Petitioner asserts, the '145 patent discloses a "feedback circuit" as a mechanism "to accomplish the elimination of invalid data transitions." *See* Reply 24; Ex. 1001, 5:19–33; Ex. 1003 ¶¶ 79–81; Ex. 2001 ¶ 50. Consistent with that disclosure, claim 15 expressly recites "providing a feedback signal representative of the sensed data appearing on the output

data bus to inactive memory blocks of the memory array coupled to the output data bus." Ex. 1001, 12:34–37.

Like the '145 patent, Oldham describes a problem due to invalid data transitions or "glitches" that waste power. Ex. 1005, 2:1–38; *see* Ex. 1003 ¶¶ 84, 86, 124. Oldham states that "[i]t is an object of the invention to avoid output glitches in data memories." Ex. 1005, 2:42–43, 2:53–54; *see* Ex. 1003 ¶¶ 86, 124.

In Oldham's Figure 2 embodiment, latch circuit 130 includes transistors 111 and 112, the unnumbered inverter connected to transistor 112's input, and a "feedback path from the output 90 to a node 113" at the output of transistors 111 and 112. Ex. 1005, 5:61–63, Fig. 2; *see* Ex. 1003 ¶¶ 87, 90; Ex. 2001 ¶¶ 74, 123. Output 90 "is fed back into the latch circuit as part of its operation." Ex. 1005, 6:17–20, Fig. 2; *see* Ex. 1003 ¶¶ 90, 111, 114, 129; Ex. 2001 ¶ 76. That feedback mechanism "controls the data transitions on the output data bus," i.e., invalid data transitions. Ex. 1003 ¶¶ 130–131.

Thus, the Figure 2 embodiment employs feedback to control invalid data transitions on an output data bus of a semiconductor device having a memory array. Ex. 1005, 2:1–4, 2:35–65, 5:61–6:20, Fig. 2; *see* Ex. 1003 ¶¶ 124–131; Ex. 1010 ¶ 60.

Patent Owner's assertion that "what controls data transitions in Oldham are sense amplifiers 110 and 120, PMOS transistor 112 and NMOS transistor 111" does not relate to invalid data transitions. *See* Resp. 49–51; Sur-reply 24. Rather, that assertion relates to valid data transitions detected by sense amplifiers 110 and 120 that produce responses by transistors 111 and 112. *See* Ex. 1005, 5:28–6:4; Ex. 1010 ¶ 60; Ex. 2001 ¶¶ 69–74; *see*

also Ex. 1003 ¶ 136. But Patent Owner offers no reason to limit claim 15's preamble to valid data transitions. *See* Resp. 49–51; Sur-reply 23–24.

Claim 15's preamble recites "data transitions" and does not distinguish between valid data transitions and invalid data transitions. Ex. 1001, 12:29–31. The '145 patent's specification supports the conclusion that claim 15's preamble encompasses invalid data transitions. *Id.* at 1:36–56, 2:45–67, 5:19–57. For example, the patent explains that an "aspect of the present invention" prevents "invalid data transitions or glitches that can occure [sic] when a previously unselected [memory] block is selected." *Id.* at 5:19–24.

Consistent with that explanation, Dr. Khatri stated that the '145 patent teaches preventing "invalid data transitions or glitches that can occur when a previously unselected/inactive block is activated" by preloading the block with "the valid data appearing on the output data bus." Ex. 2001 ¶ 50 (citing Ex. 1001, 5:19–30); *see id.* ¶ 51; Resp. 7–8. Preloading occurs "via a feedback circuit." Ex. 1001, 2:62–67, code (57); *see id.* at 5:19–57, 7:18–39, 8:35–39, 9:12–25, Figs. 3–4; Ex. 1003 ¶¶ 79–81; Ex. 1010 ¶ 60; Ex. 2001 ¶ 51.

For the reasons discussed above, Oldham's Figure 2 embodiment implements "[a] method for controlling data transitions on an output data bus of a semiconductor device having a memory array" according to claim 15's preamble.

(b) The "Sensing" Limitation

Claim 15 recites "sensing data appearing on a bit line of the memory array." Ex. 1001, 12:32. Petitioner asserts that Oldham's Figure 2 embodiment satisfies this limitation for two reasons. Pet. 34–36; *see id.* at

52–54; Ex. 1003 ¶¶ 106–108, 132–134. First, Petitioner contends that Oldham discloses sense-amplifier circuit 80 "configured for sensing data from 'an array of memory cells 10 arranged as a number of rows 20 of memory cells'" in Figure 1. Pet. 34 (quoting Ex. 1005, 4:37–38); *see* Ex. 1003 ¶¶ 106–107, 132–133; Ex. 1005, 4:23–25, 4:36–38, Figs. 1–2. Second, Petitioner contends that sense-amplifier circuit 80 includes a "pair of sense amplifiers 110 and 120" coupled "via the bitlines 'bit' and 'nbit,' to the memory array" in Figure 1. Pet. 35–36; *see* Ex. 1003 ¶¶ 108, 134.

Patent Owner does not make any arguments specific to claim 15's "sensing" limitation. *See, e.g.*, Resp. 49–51.

We agree with Petitioner that Oldham's Figure 2 embodiment satisfies claim 15's "sensing" limitation. As Petitioner asserts, sense-amplifier circuit 80 includes sense amplifiers 110 and 120, and each sense amplifier "receives the bit and nbit signals from a pair of bit-lines 30" shown in Figure 1. Ex. 1005, 5:14–26, Figs. 1–2; *see* Ex. 1003 ¶¶ 106–108, 132–134; Ex. 2001 ¶¶ 68–70. According to Oldham, "[t]he invention makes use of two sense amplifiers to read data stored in one memory cell." Ex. 1005, 2:59–60. In addition, Dr. Khatri explained that "[s]ense amplifiers 110 and 120 are connected in parallel with opposite polarities, so that the non-inverting input of sense amplifier 110 is connected to the bit signal, and the non-inverting input of the sense amplifier 120 is connected to the nbit signal." Ex. 2001 ¶ 70.

For the reasons discussed above, Oldham's Figure 2 embodiment "sens[es] data appearing on a bit line of the memory array," as required by claim 15.

(c) The "Driving" Limitation

Claim 15 also recites "driving the sensed data onto the output data bus." Ex. 1001, 12:33. Petitioner asserts that Oldham's Figure 2 embodiment satisfies this limitation because sense-amplifier circuit 80 "receives the bit and nbit signals from a pair of bit-lines 30" in Figure 1 and sense-amplifier circuit 80 generates a buffered output signal at output 90. Pet. 54; *see* Ex. 1003 ¶¶ 135–136. Petitioner also asserts that output 90 connects to "a common (shared) data bus." Pet. 54; *see* Ex. 1003 ¶ 135.

Dr. Jacob explained that "[t]he sense amplifiers [110 and 120] are responsible for sensing the data, and then the tristate buffer 140 is responsible for driving the sensed data onto the output data bus." Ex. 1003 ¶ 136.

Patent Owner does not make any arguments specific to claim 15's "driving" limitation. *See, e.g.*, Resp. 49–51.

We agree with Petitioner that Oldham's Figure 2 embodiment satisfies claim 15's "driving" limitation. As Petitioner asserts, sense-amplifier circuit 80 "receives the bit and nbit signals from a pair of bit-lines 30" in Figure 1, i.e., sense amplifiers 110 and 120 each receive the bit and nbit signals. Ex. 1005, 5:14–26, Figs. 1–2; *see* Ex. 1003 ¶¶ 106–108, 132–135; Ex. 2001 ¶¶ 68–70. When enabled, sense amplifiers 110 and 120 supply signals to transistors 111 and 112 in latch circuit 130. Ex. 1005, 5:28–63, Fig. 2; *see* Ex. 1003 ¶¶ 109–111; Ex. 2001 ¶¶ 70–74. The output of transistors 111 and 112 at node 113 provides an input to tri-state buffer circuit 140. Ex. 1005, 5:61–63, 6:17–21, Fig. 2; *see* Ex. 1003 ¶¶ 90, 110–111; Ex. 2001 ¶ 76. Tri-state buffer circuit 140 supplies a buffered output signal at output 90, thus driving the sensed data onto output 90. Ex. 1005,

6:17–21; *see* Ex. 1003 ¶¶ 110–111, 135–136. Output 90 connects to a shared output data bus. Ex. 1005, 5:26–27, 6:12–16; *see id.* at 5:16–19, 6:36–37; Ex. 1003 ¶¶ 88, 107, 135; Ex. 2001 ¶¶ 76–77.

For the reasons discussed above, Oldham's Figure 2 embodiment "driv[es] the sensed data onto the output data bus," as required by claim 15.

(d) The "Providing" Limitation

Claim 15 further recites "providing a feedback signal representative of the sensed data appearing on the output data bus to inactive memory blocks of the memory array coupled to the output data bus." Ex. 1001, 12:34–37. Petitioner asserts that Oldham's Figure 2 embodiment satisfies this limitation for two reasons. Pet. 39–41; *see id.* at 52–54; Ex. 1003 ¶¶ 114–116, 137–140. First, Petitioner contends that Figure 2 depicts a data feedback circuit from output 90 that "is fed back into the latch circuit as part of its operation." Pet. 39 (emphasis omitted) (quoting Ex. 1005, 6:17–21); Ex. 1003 ¶¶ 114, 137. Second, Petitioner contends that "Oldham discloses that its data appears 'on the output bus to inactive memory blocks of the memory array coupled to the output data bus,' as claimed." Pet. 54; *see* Ex. 1003 ¶ 140.

Patent Owner does not make any arguments specific to claim 15's "providing" limitation. *See, e.g.*, Resp. 49–51.

We agree with Petitioner that Oldham's Figure 2 embodiment satisfies claim 15's "providing" limitation. In Figure 2, latch circuit 130 includes a "feedback path from the output 90 to a node 113" at the output of transistors 111 and 112. Ex. 1005, 5:61–63, Fig. 2; *see* Ex. 1003 ¶¶ 87, 90; Ex. 2001 ¶¶ 74, 89, 123. The feedback path includes "a pair of inverters," i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input.

Ex. 1005, 5:63–65, Fig. 2; *see* Ex. 1003 ¶¶ 90, 109; Ex. 2001 ¶¶ 74, 89, 123. Output 90 "is fed back into the latch circuit as part of its operation." Ex. 1005, 6:17–20, Fig. 2; *see* Ex. 1003 ¶¶ 90, 111, 114, 129, 137–139; Ex. 2001 ¶ 76. Output 90 connects to a shared output data bus. Ex. 1005, 5:26–27, 6:12–16; *see id.* at 5:16–19, 6:36–37; Ex. 1003 ¶¶ 88, 107, 135; Ex. 2001 ¶¶ 76–77. Thus, the Figure 2 embodiment provides a feedback signal representative of the sensed data appearing on an output data bus.

Further, the Figure 2 embodiment provides the feedback signal to inactive memory blocks of a memory array coupled to the output data bus. In Figure 2, the "feedback path from the output 90 to a node 113" at the output of transistors 111 and 112 exists regardless whether the read-enable signal is "high" or "low." Ex. 1005, 5:20–27, 5:61–6:37, Fig. 2; *see* Ex. 1003 ¶¶ 121, 140; Ex. 1010 ¶¶ 39, 60; Ex. 2004, 44:21–45:3. A "low" read-enable signal switches off the two unnumbered transistors in tri-state buffer circuit 140. Ex. 1005, 6:30–36; *see* Ex. 2001 ¶ 77. Switching off the transistors (1) sets the transistors to high impedance, (2) inactivates the device, and (3) allows other devices to access the shared output data bus. Ex. 1005, 6:36–37; *see id.* at 6:12–16; Ex. 1003 ¶¶ 121, 140; Ex. 1010 ¶¶ 39, 60; Ex. 2001 ¶ 77. But the feedback path still provides a feedback signal from the shared output data bus to the inactive device. Ex. 1005, 5:61–65, 6:17–21, Fig. 2; *see* Ex. 1003 ¶¶ 140–141; Ex. 1010 ¶¶ 39, 60; Ex. 2004, 45:15–24, 46:13–21.

For the reasons discussed above, Oldham's Figure 2 embodiment "provid[es] a feedback signal representative of the sensed data appearing on the output data bus to inactive memory blocks of the memory array coupled to the output data bus," as required by claim 15.

(e) Whether Oldham Anticipates Claim 15

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that Oldham's Figure 2 embodiment includes every element of claim 15 arranged as required by the claim. Hence, Petitioner has shown by a preponderance of the evidence that claim 15 is unpatentable under § 102(b) as anticipated by Oldham.

D. Obviousness over Oldham: Claims 1, 6, and 15

1. OBVIOUSNESS UNDER 35 U.S.C. § 103

A patent may not be obtained "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). An obviousness analysis involves underlying factual inquiries including (1) the scope and content of the prior art; (2) differences between the claimed invention and the prior art; (3) the level of ordinary skill in the art; and (4) where in evidence, objective evidence of nonobviousness, such as commercial success, long-felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17−18, 35–36 (1966); *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1047–48 (Fed. Cir. 2016) (en banc).

"An obviousness determination requires finding that a person of ordinary skill in the art would have been motivated to combine or modify the teachings in the prior art and would have had a reasonable expectation of success in doing so." *Regents of Univ. of Cal. v. Broad Inst., Inc.*, 903 F.3d 1286, 1291 (Fed. Cir. 2018); *In re Stepan Co.*, 868 F.3d 1342, 1345–46,

1346 n.1 (Fed. Cir. 2017). Thus, an obviousness analysis should address "whether there was an apparent reason" to combine or modify "known elements in the fashion claimed by the patent at issue." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Moreover, "mere conclusory statements" do not suffice for an apparent reason to combine or modify. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Crediting conclusory statements "risks allowing the challenger to use the challenged patent as a roadmap to reconstruct the claimed invention using disparate elements from the prior art—i.e., the impermissible *ex post* reasoning and hindsight bias that *KSR* warned against." *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1361 (Fed. Cir. 2019).

We analyze the obviousness issues according to these principles.

2. INDEPENDENT CLAIM 1

As discussed above for the anticipation ground, claim 1 differs from Oldham's Figure 2 embodiment because that embodiment lacks the "data feedback circuit" required by claim 1. *See supra* § III.C.3(d).

Petitioner asserts that to "the extent that it is alleged that Oldham does not disclose the claimed data feedback circuit," this "would have been an obvious modification" for an ordinarily skilled artisan "to make to Oldham from a finite set of known sense feedback circuit designs to further the known goal of reducing glitches in memory devices." Pet. 49–50; *see* Ex. 1003 ¶ 151.

In particular, Petitioner argues that "it was a well-known problem in the art that when data is discharged from storage cells onto an output data bus, there can be errors called 'glitches.'" Pet. 49; *see* Ex. 1003 ¶ 151.

Petitioner also argues that "[t]here were a known set of finite solutions to this problem in the prior art, including the use of a feedback path from the data bus back to a storage device." Pet. 49; *see* Ex. 1003 ¶ 151. Petitioner then contends that "Oldham explicitly discloses that it uses a feedback path" from "its output bus 90 back to the data storage device 130" to reduce glitches. Pet. 49; *see* Ex. 1003 ¶ 151.

Petitioner also asserts that to "the extent that it is alleged that Oldham does not disclose that the data feedback circuit is coupled such that its input is connected to the output data bus, and its output is connected to the data storage device, it would have been an obvious modification to Oldham" to do this. Pet. 50; Reply 18; *see* Ex. 1003 ¶ 152. In particular, Petitioner argues that data feedback circuits intended to reduce "glitch" problems function because "the feedback goes in the opposite direction as the data (it feeds back to the data source, as a form of control)." Pet. 50; Reply 18; *see* Pet. 15–17; Ex. 1003 ¶ 152.

Patent Owner approaches the obviousness analysis differently. *See* Resp. 43–45; Sur-reply 18–22. According to Patent Owner, the obviousness analysis should address "whether it would have been obvious to modify Oldham to include a data feedback circuit that is separate and distinct from the data storage device." Resp. 45; *see* Ex. 2001 ¶ 112.

Patent Owner asserts that an ordinarily skilled artisan "would have had no motivation to modify" Figure 2's sense-amplifier circuit 80 "to include a feedback path, separate and distinct from the data storage device" because that circuit "already has a feedback path to address the 'glitch' problem." Resp. 45; *see* Sur-reply 19; Ex. 2001 ¶ 113. Patent Owner also asserts that a "separate and distinct" feedback path "would serve no further

purpose than the one Oldham already discloses." Resp. 45; *see* Ex. 2001 ¶ 113.

Further, Patent Owner argues that Petitioner fails to present evidence that an ordinarily skilled artisan would have been motivated to modify sense-amplifier circuit 80 to achieve a "sensing circuit" according to claim 1. Resp. 45; *see* Sur-reply 18. Specifically, Patent Owner asserts that Petitioner fails to present evidence "regarding whether it would have been obvious to modify Oldham to include a data feedback circuit that is separate and distinct from the data storage device." Resp. 45. In addition, Patent Owner contends that "[t]he only motivation would be to invalidate the '145 patent, and a motivation based on hindsight is not a proper motivation to support a finding of obviousness." *Id.*; *see* Sur-reply 17.

In response, Petitioner argues that to "the extent that Patent Owner's view of Oldham is accepted," an ordinarily skilled artisan "would have been motivated to include a static data storage device, a simple latch (an admittedly well-known component), within latch 130 of Oldham to reduce a potential source of errors that can derive from dissipation of internal capacitance." Reply 21. To support its argument, Petitioner relies on Dr. Jacob's testimony. *Id.* at 20–21 (citing Ex. 1010 ¶¶ 59–62).

In sense-amplifier circuit 80, Dr. Jacob focused on the two serially connected inverters in latch circuit 130, i.e., inverter 114 and the unnumbered inverter connected to inverter 114's input. Ex. 1010 ¶¶ 61–62. He "suppose[d] that the internal capacitance of this circuit" was "insufficient to hold the data from the output bus" due to dissipation at node 113 or that someone "might try to eliminate that as a potential source of errors." *Id.* ¶ 62. Under those circumstances, Dr. Jacob explained that "a person of

ordinary skill could very easily connect node 113 to the input of the inverter above inverter 114, thereby creating a simple latch right there." *Id.* He stated that "[t]his would store the data statically, not dynamically." *Id.*

The following annotated version of Figure 2 shows Dr. Jacob's proposed modification to latch circuit 130. *See* Tr. 16:4–17; Sur-reply 21.

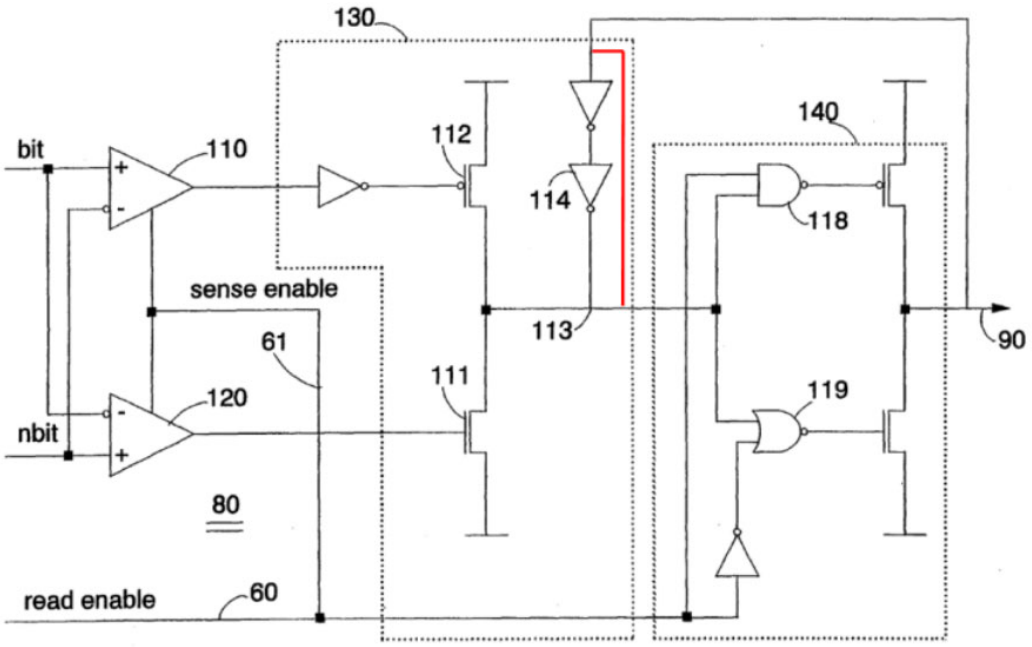


Fig. 2

This annotated version of Figure 2 shows a red conductor connecting node 113 to the input of the inverter above inverter 114.

We agree with Patent Owner that Petitioner fails to present evidence that an ordinarily skilled artisan would have been motivated to modify sense-amplifier circuit 80 to achieve a "sensing circuit" according to claim 1. As discussed above, an obviousness analysis must consider the differences between the claimed invention and the prior art. *See, e.g.*, *Graham*, 383 U.S. at 17. As also discussed above, claim 1 differs from sense-amplifier circuit 80 because that sensing circuit lacks the "data feedback circuit" required by claim 1. *See supra* § III.C.3(d). Although that

sensing circuit includes a feedback mechanism, the structural elements for that feedback mechanism constitute structural elements for the "data storage device" required by claim 1. *See id.*

Thus, the obviousness analysis should consider "whether there was an apparent reason" to modify sense-amplifier circuit 80 to include structural elements for the "data feedback circuit" distinct from the structural elements for the "data storage device." *See KSR*, 550 U.S. at 418. Petitioner does not identify an apparent reason to modify sense-amplifier circuit 80 in that way. *See* Pet. 49–50; Reply 17–21; Ex. 1003 ¶¶ 151–152; Ex. 1010 ¶¶ 59–62.

As Dr. Khatri explained, because sense-amplifier circuit 80 already includes a feedback mechanism, an ordinarily skilled artisan would have had "no reason to generate a different circuit for this purpose." Ex. 2001 ¶ 113. Moreover, disadvantages may result from increasing the number of structural elements—compared to decreasing the number or using the same number—such as increased size, increased cost, increased power consumption, and increased manufacturing complexity.

As for Dr. Jacob's proposed modification to latch circuit 130 to "connect node 113 to the input of the inverter above inverter 114," Petitioner asserts that it alters latch circuit 130 to include another latch, i.e., "an extra pair of cross-coupled inverters (a type of latch)." Reply 20–21. If so, no need exists to include another latch because latch circuit 130 already functions as a latch. Ex. 1003 ¶¶ 88–91, 109–112; Ex. 1010 ¶¶ 10, 20–21, 24–25, 60; Ex. 2001 ¶¶ 72–74; *see* Ex. 1003 ¶¶ 64–65; Ex. 1010 ¶ 10 n.1; Ex. 2004, 20:8–21:13.

Also, Dr. Jacob "suppose[d] that the internal capacitance of" the two serially connected inverters in latch circuit 130 was "insufficient to hold the

data from the output bus" due to dissipation at node 113 or that someone "might try to eliminate that as a potential source of errors." Ex. 1010 ¶ 62. But he cited no evidence of any actual or potential dissipation problem at node 113. *Id.* ¶¶ 59–62; *see* Ex. 1003 ¶¶ 151–152.

At his deposition, Dr. Jacob stated that dissipation at node 113 would occur if you sever the feedback path from output 90 to latch circuit 130. Ex. 2004, 44:7–16. But he conceded that Oldham does not contemplate severing the feedback path. *Id.* at 44:21–45:3. He also conceded that with the feedback path intact output 90 continues to update node 113 with the value from the output bus until the read-enable signal turns on tri-state buffer circuit 140. *Id.* at 45:15–24, 46:13–21. Hence, as Patent Owner asserts, "Oldham discloses no scenario that would suggest any need to protect against the value at node 113 from dissipating, since node 113 is constantly being updated with the value from the output bus." Sur-reply 20.

Further, sense-amplifier circuit 80 includes the "data storage device" required by claim 1. *See supra* § III.C.3(c). Claim 1 does not differ from the prior art due to the absence of the "data storage device." For no sound reason, however, Dr. Jacob selected the "data storage device" in sense-amplifier circuit 80 to modify. That selection appears to rest on hindsight. In particular, in selecting the two serially connected inverters in latch circuit 130 as the components to modify, he appears to have used the challenged patent as a roadmap to reconstruct the claimed invention.

For the reasons discussed above, Petitioner fails to present evidence that an ordinarily skilled artisan would have been motivated to modify Oldham's sense-amplifier circuit 80 to achieve the "sensing circuit" recited in claim 1. Hence, Petitioner has not shown by a preponderance of the

evidence that claim 1 is unpatentable under § 103(a) as obvious over Oldham.

3. Dependent Claim 6

Claim 6 depends directly from claim 1. Ex. 1001, 10:62–64. Thus, claim 6 incorporates all of claim 1's limitations. *See* 35 U.S.C. § 112 ¶ 4. For the reasons discussed above for claim 1, Petitioner has not shown by a preponderance of the evidence that claim 6 is unpatentable under § 103(a) as obvious over Oldham.

4. Independent Claim 15

As discussed above, Petitioner has shown by a preponderance of the evidence that claim 15 is unpatentable under § 102(b) as anticipated by Oldham. *See supra* §§ III.C.5(a)–(e). Because that determination resolves claim 15's patentability, there is no need to consider whether claim 15's subject matter would have been obvious over Oldham. *See, e.g.*, *In re Paulsen*, 30 F.3d 1475, 1481 (Fed. Cir. 1994) (affirming an anticipation rejection of certain claims and declining to review an obviousness rejection of the same claims); *Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (explaining that an administrative agency may render a decision based on "a single dispositive issue"). Moreover, an obviousness analysis assumes that differences exist between the claimed invention and the prior art. *See Graham*, 383 U.S. at 17. But we have found that no differences exist between claim 15 and Oldham's Figure 2 embodiment because it anticipates claim 15. Absent differences, an obviousness analysis appears misplaced.

IV. CONCLUSION

Based on the evidence presented with the Petition, the evidence introduced during the trial, and the parties' respective arguments, Petitioner has shown by a preponderance of the evidence that claim 15 is unpatentable under § 102(b) as anticipated by Oldham.[3] But Petitioner has not shown by a preponderance of the evidence that claims 1 and 6 are unpatentable under § 102(b) as anticipated by Oldham or unpatentable under § 103(a) as obvious over Oldham.

In summary:

Claims	35 U.S.C. §	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 6, 15	102(b)	Oldham	15	1, 6
1, 6, 15	103(a)[4]	Oldham		1, 6
Overall Outcome			15	1, 6

[3] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding after the issuance of this Final Written Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[4] As explained above, we did not reach the obviousness ground for claim 15.

V. ORDER

Accordingly, it is

ORDERED that claims 1 and 6 of the ’145 patent are not determined to be unpatentable;

ORDERED that claim 15 of the ’145 patent is determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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