

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

IPR2018-01794
Patent 6,917,555 B2

Before MICHAEL R. ZECHER, GARTH D. BAER, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Kingston Technology Company, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 15 and 24 of U.S. Patent No. 6,917,555 B2 (Ex. 1001, “the ’555 patent”) under 35 U.S.C. §§ 311–319. Under 37 C.F.R. § 42.107(b), North Star Innovations, Inc. (“Patent Owner”) waived its Preliminary Response (Paper 7).

In our Institution Decision (Paper 8, “Inst. Dec.”), we instituted review based on all challenged claims and all grounds advanced in the Petition. We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has shown by a preponderance of the evidence that claims 15 and 24 of the ’555 patent are unpatentable. *See* 35 U.S.C. § 316(e).

II. BACKGROUND

A. Procedural History

After we instituted review, Patent Owner filed a Response (Paper 14, “Resp.”), Petitioner filed a Reply (Paper 29, “Reply”), and Patent Owner filed a Sur-reply (Paper 34, “Sur-reply”). On January 17, 2020, we held an oral hearing. *See* Paper 35 (“Tr.”).

B. Related Proceedings

Petitioner and Patent Owner identify the following civil action where Patent Owner has asserted the ’555 patent against Petitioner: *North Star Innovations, Inc. v. Kingston Technology Co., Inc.*, No. 8:17-cv-1833 (C.D. Cal. filed Oct. 20, 2017). Pet. 2; Paper 4, 1–2; Paper 5, 1.

Petitioner and Patent Owner identify other petitions challenging the patentability of claims in other patents asserted by Patent Owner against

Petitioner in the above-identified civil action: IPR2018-01784 (U.S. Patent No. 6,101,145), IPR2019-00102 (U.S. Patent No. 5,943,274), and IPR2019-00104 (U.S. Patent No. 6,127,875). Pet. 2; Paper 4, 2; Paper 5, 1.

C. The '555 Patent (Ex. 1001)

The '555 patent, titled “Integrated Circuit Power Management for Reducing Leakage Current in Circuit Arrays and Method Therefor,” issued on July 12, 2005, from an application filed on September 30, 2003. Ex. 1001, codes (22), (45), (54). The '555 patent concerns power management for integrated circuits containing memory arrays and associated peripheral circuitry by “reducing leakage current in circuit arrays.” *Id.* at 1:1–13, 8:8–38, 9:13–29, code (57).

The '555 patent explains that “[b]attery-powered devices that incorporate integrated circuits” are “very sensitive to power consumption” and that leakage current consumes power. Ex. 1001, 1:15–19, code (57). The '555 patent also explains that leakage current “becomes a major concern with respect to times when the device is powered but not actively used.” *Id.* at 1:19–23. Hence, the invention endeavors to power down “memory arrays of an integrated circuit during low-power modes” or “during long periods of extremely low processing requirements, inactivity, or limited inactivity” to “save significant leakage current.” *Id.* at 2:7–9, 2:30–33; *see id.* at 1:27–39, 6:42–9:47.

Figure 1 of the '555 patent is reproduced below:

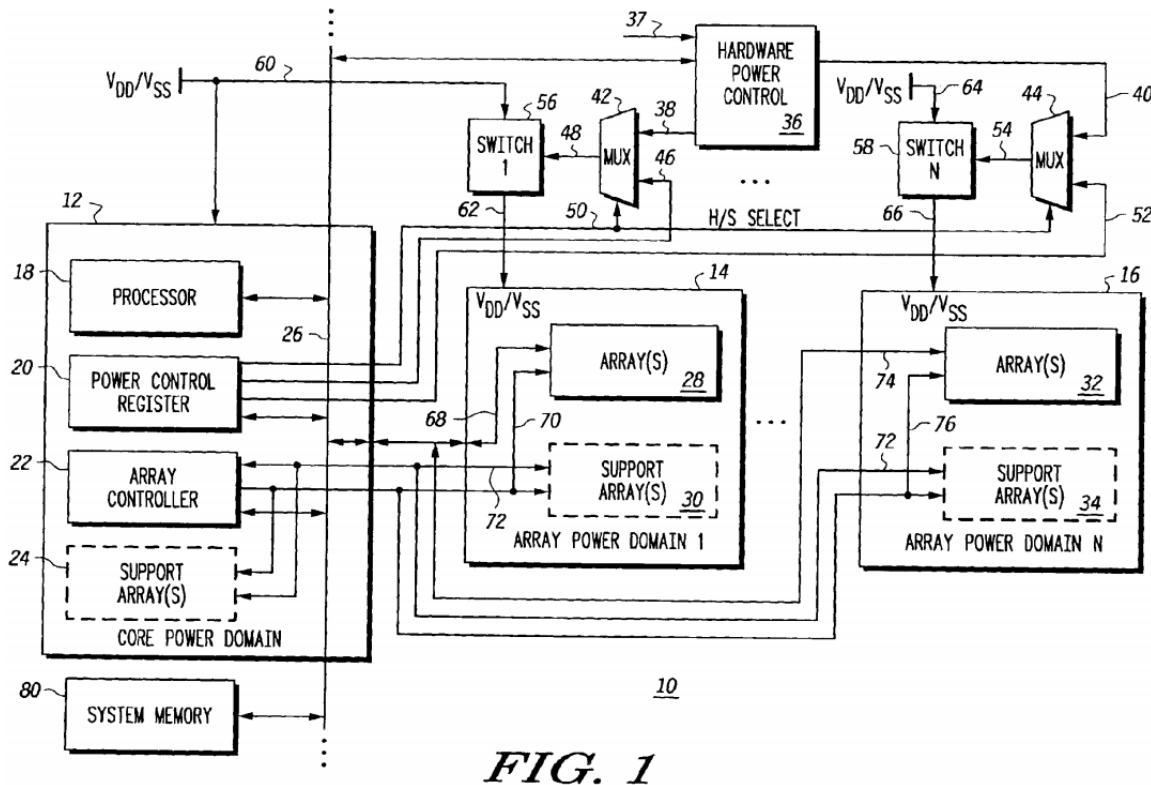


FIG. 1

Figure 1 depicts “an integrated circuit with power management for reducing leakage current.” Ex. 1001, 1:46–48, 2:47–49.

In Figure 1, integrated circuit 10 includes “a core power domain 12 and one or more array power domains (1 to N, where N is an integer)” denoted by reference numerals 14 and 16. Ex. 1001, 2:51–54. “The core power domain 12 includes processor (or processing circuitry) 18, power control register 20, and array controller 22.” *Id.* at 2:54–56. “Array power domain 14 includes one or more [memory] array(s) 28,” and “[a]rray power domain 16 includes one or more [memory] array(s) 32.” *Id.* at 2:63–67.

Integrated circuit 10 also includes switches 56 and 58. Ex. 1001, 3:25–26. “The switch output 62 of switch 56 is coupled to a power plane terminal V_{DD}/V_{SS} of array power domain 14,” and “the switch output 66 [of

switch 58] is coupled to a power plane terminal V_{DD}/V_{SS} of array power domain 16.” *Id.* at 3:36–40.

Switches 56 and 58 operate independently to power down the associated memory arrays, thus reducing leakage current. Ex. 1001, 7:13–18. “Because two power planes are created, the processor may continue executing instructions using a system memory while bypassing the memory array when the array is powered down.” *Id.* at code (57).

Figure 6 of the ’555 patent is reproduced below:

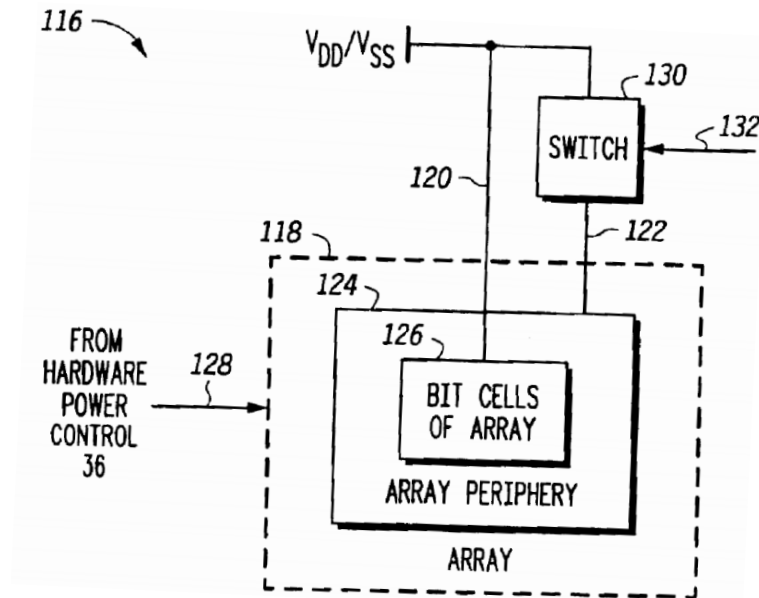


Figure 6 depicts in greater detail “a portion of the integrated circuit” in Figure 1. Ex. 1001, 1:63–64, 6:29–30.

When describing Figure 6, the ’555 patent notes that one or more memory arrays in Figure 1 may “include a configuration 116 [in Figure 6] having an array 118 with separate power terminals (120, 122) respectively for a corresponding array periphery 124 and for the corresponding bit cells 126.” Ex. 1001, 6:31–36. “In this configuration, the bit cells 126 [may]

remain powered while power for the array periphery 124 is switched [off] by switch 130.” *Id.* at 6:36–38.

D. The Challenged Claims

Petitioner challenges independent claims 15 and 24. Pet. 4, 17–54.

Claims 15 and 24 read as follows:

15. An integrated circuit having power management comprising:

processing circuitry for executing instructions;

a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane;

memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the memory array peripheral circuitry being selectively coupled to the power supply terminal for creating a second power plane that is independent of the first power plane; and

control circuitry coupled to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the control circuitry selectively removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

24. A method of power management in an integrated circuit comprising:

executing instructions with a processor;

providing a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane;

providing memory array peripheral circuitry that is peripheral to the plurality of memory bit cells;

selectively coupling the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells to the power supply terminal for creating a second power plane that is independent of the first power plane;

coupling control circuitry to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells;
and

selectively removing electrical connectivity to the power supply voltage terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

Ex. 1001, 11:39–56, 12:47–67.

E. The Asserted Prior Art

For its challenges, Petitioner relies on U.S. Patent No. 5,615,162 to Houston, titled “Selective Power to Memory,” filed on January 4, 1995, and issued on March 25, 1997 (Ex. 1003, “Houston”).

F. Testimonial Evidence

To support its challenges, Petitioner relies on two declarations of Bruce Jacob, Ph.D. (Ex. 1004, “Jacob Decl.”; Ex. 1012, “Jacob Reply Decl.”). Patent Owner relies on the declaration of Sunil P. Khatri, Ph.D. (Ex. 2001, “Khatri Decl.”). The record includes a transcript of Dr. Jacob’s deposition (Ex. 2011, “Jacob Dep.”) and transcripts of Dr. Khatri’s depositions (Ex. 2012, “Khatri 1st Dep.”; Ex. 1013, “Khatri 2nd Dep.”).

G. Asserted Grounds of Unpatentability

We instituted an *inter partes* review of claims 15 and 24 on the following grounds:

Claims Challenged	35 U.S.C. §	Reference
15, 24	102(b) ¹	Houston
15, 24	103(a)	Houston

Inst. Dec. 21.

H. Burden

Petitioner bears “the burden of proving . . . unpatentability by a preponderance of the evidence.” 35 U.S.C. § 316(e); *see* 37 C.F.R. § 42.1(d).

III. PATENTABILITY ANALYSIS

A. Level of Ordinary Skill in the Art

Factors pertinent to determining the level of ordinary skill in the art include (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) prior-art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of workers active in the field. *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–97 (Fed. Cir. 1983). Evidence for these factors may not exist in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, these factors are not exhaustive, but are merely a guide to

¹ On September 16, 2012, the Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), took effect and amended 35 U.S.C. §§ 102 and 103. Because the ’555 patent’s filing date predates the AIA’s amendments to §§ 102 and 103, this decision refers to the pre-AIA versions of §§ 102 and 103.

determining the level of ordinary skill in the art. *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). Further, the prior art itself may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Here, Petitioner asserts that a person of ordinary skill in the art would have had either “an undergraduate degree in electrical engineering (or an equivalent subject), together with at least two years of post-graduate experience designing memory arrays and power-management mechanisms,” or “a master’s degree in electrical engineering (or equivalent subject) together with at least one year of post-graduate experience in designing memory arrays and power-management mechanisms.” Pet. 8 (citing Ex. 1004 ¶ 23). Petitioner also asserts that “a higher level of education could make up for less experience, and vice versa.” *Id.* (citing Ex. 1004 ¶ 24). Patent Owner states that “[f]or purposes of this proceeding,” it “is not challenging Petitioner’s proposed definition of” a person of ordinary skill in the art. Resp. 23; *see* Ex. 2001 ¶ 26. Thus, we adopt Petitioner’s proposed definition as it is consistent with the ’555 patent and the asserted prior art.

B. Claim Construction

1. BACKGROUND

In an *inter partes* review resulting from a petition filed before November 13, 2018, as here, claim terms in an unexpired patent are given their broadest reasonable interpretation in light of the specification in which they appear. *See* 37 C.F.R. § 42.100(b) (2018); Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,347, 51,358 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b)); Resp. 18. Consistent with that

standard, claim terms generally are given their ordinary and customary meaning, as understood by one of ordinary skill in the art, in the context of the entire patent disclosure. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1061–62 (Fed. Cir. 2016); *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). “[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.” *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

2. WHETHER THE PREAMBLES IN CLAIMS 15 AND 24 LIMIT THE CLAIMS

The parties dispute whether the preambles in claims 15 and 24 limit the claims. *See* Resp. 23–26; Reply 2–8; Sur-reply 1–10. Generally, a preamble does not limit a claim. *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002). Although “there is no simple test” for determining whether a preamble limits a claim, the U.S. Court of Appeals for the Federal Circuit has “set forth some general principles to guide that inquiry.” *Am. Med. Sys., Inc. v. Biolitec, Inc.*, 618 F.3d 1354, 1358 (Fed. Cir. 2010).

A preamble limits a claim if it recites “essential structure or steps.” *Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). A preamble also limits a claim if it is “essential to understand limitations or terms in the claim body.” *Id.* In addition, a preamble limits a claim if the patentee clearly relied on it “during prosecution to distinguish the claimed invention from the prior art” because

“such reliance indicates use of the preamble to define, in part, the claimed invention.” *Id.*

A preamble may limit a claim if it recites “additional structure or steps underscored as important by the specification.” *Catalina Mktg.*, 289 F.3d at 808. A preamble may also limit a claim if the claim body relies on the preamble to provide an antecedent basis for a claim term. *Id.*

But a preamble does not limit a claim if the claim body “defines a structurally complete invention” and the preamble “state[s] a purpose or intended use for the invention.” *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997); *see Catalina Mktg.*, 289 F.3d at 808.

Whether a preamble limits a claim is “determined on the facts of each case in light of the overall form of the claim, and the invention as described in the specification and illuminated in the prosecution history.” *Arctic Cat Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1327 (Fed. Cir. 2019) (quoting *Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1357 (Fed. Cir. 2012)).

Here, Patent Owner asserts that the preambles in claims 15 and 24 each recite an “integrated circuit.” Resp. 23; *see* Sur-reply 4, 7. Based on several dictionary definitions, Patent Owner contends that the term “integrated circuit” means “one or more circuit elements provided on or within a single semiconductor substrate.” Resp. 25–26 (emphasis omitted) (citing Exs. 2004–2007); *see id.* at 23; Ex. 2001 ¶ 77. Patent Owner asserts that the term “integrated circuit” in each preamble recites “essential structure,” i.e., “a single semiconductor substrate,” and therefore limits the claims. Resp. 26; *see id.* at 28–29; Sur-reply 4–5, 7; Ex. 2001 ¶ 80.

In particular, Patent Owner contends that the term “integrated circuit” specifies “required structure for the invention” and provides a “structural definition for implementing” the invention. Sur-reply 4–5. Patent Owner also contends that claim 15’s preamble recites “the structure on which the claim[ed] circuit elements are to be implemented” and that claim 24’s preamble recites “the structure on which the claimed method of power management is to be performed.” *Id.* at 4. Patent Owner argues that deleting the term “integrated circuit” from each claim’s preamble “materially broadens” claim scope “by eliminating a specific structural definition.” *Id.* at 5.

Further, Patent Owner asserts that arranging the claimed circuitry on different semiconductor substrates instead of “a single semiconductor substrate” would unnecessarily waste “power, energy and area” contrary to “the express purpose of the ‘555 patent to save power by reducing leakage current.” Resp. 23–24; *see* Ex. 2001 ¶ 78. Patent Owner also asserts that an ordinarily skilled artisan “would understand that multiple power domains would be provided within a single substrate” instead of “spread across multiple substrates.” Resp. 25; *see* Sur-reply 7; Ex. 2001 ¶ 78.

Although Petitioner does not dispute Patent Owner’s proposed construction of the preamble term “integrated circuit,” Petitioner disputes that the preambles limit claims 15 and 24. *See* Reply 2–8; Tr. 6:5–7. Specifically, Petitioner asserts that “Patent Owner does not argue, because it cannot,” that the term “integrated circuit” provides “an antecedent basis for any other claim term, that it is essential to understanding other terms, or that the applicant relied on the preambles to distinguish prior art during prosecution.” Reply 3. Petitioner also asserts that “[n]one of those factors

are present in this proceeding.” *Id.* In addition, Petitioner contends that “Patent Owner’s conclusory argument that an ‘integrated circuit’ provides ‘essential structure’ to the claims is without merit, and the preambles should not be construed as limiting.” *Id.* at 6.

For the reasons explained below, we agree with Petitioner that the preamble term “integrated circuit” does not limit claims 15 and 24.

Claim 15’s body defines a complete invention, i.e., a structurally complete apparatus for power management. Ex. 1001, 11:39–56. The circuit elements recited in the claim body by themselves accomplish power management and reduce leakage current. *Id.* The “integrated circuit” recited in claim 15’s preamble does not participate in power management or help reduce leakage current. *Id.* Deleting the term “integrated circuit” from claim 15’s preamble does not affect apparatus operation or how the recited circuit elements cooperate. *Id.* In addition, that term is not essential to understand limitations or terms in the claim body. *Id.* Moreover, the claim body does not rely on the preamble to provide an antecedent basis for a claim term. *Id.*

Claim 24’s body defines a complete invention, i.e., an algorithmically and structurally complete method for power management. Ex. 1001, 12:47–67. The steps and circuitry recited in the claim body by themselves accomplish power management and reduce leakage current. *Id.* The “integrated circuit” recited in claim 24’s preamble does not participate in power management or help reduce leakage current. *Id.* Deleting the term “integrated circuit” from claim 24’s preamble does not affect method performance or how the recited circuitry cooperates. *Id.* In addition, that term is not essential to understand limitations or terms in the claim body. *Id.*

Moreover, the claim body does not rely on the preamble to provide an antecedent basis for a claim term. *Id.*

Also, the invention covered by claims 15 and 24 accomplishes power management and reduces leakage current, regardless whether the claimed circuitry exists on “a single semiconductor substrate” or on different semiconductor substrates. Ex. 1012 ¶¶ 30–31; Tr. 31:6–32:5; *see id.* at 21:13–21. At the oral hearing, Patent Owner conceded that the claimed circuitry arranged on different semiconductor substrates still reduces leakage current. Tr. 31:6–32:5. Hence, “a single semiconductor substrate” does not constitute “essential structure” for the claimed invention.

Although the ’555 patent’s specification repeatedly references an “integrated circuit,” the specification does not describe an “integrated circuit” as important. *See, e.g.*, Ex. 1001, 2:5–10:2 (Detailed Description), code (57). Further, the specification does not identify any feature of an “integrated circuit” as an improvement other than the power-management feature. *See, e.g., id.* The “integrated circuit” in the preamble “is entirely conventional apart from the improvement in the body of the claims.” *See Arctic Cat*, 919 F.3d at 1329–30.

In addition, Dr. Jacob stated that the ’555 patent “does not discuss the importance of integration anywhere in the specification” and that “the main point of the ’555 patent is the reduction of leakage current.” Ex. 1012 ¶ 31. Consistent with Dr. Jacob, Dr. Khatri stated that the ’555 patent “concerns generally leakage current.” Ex. 1013, 6:2–5. Dr. Khatri also stated that the ’555 patent “talks about the importance of leakage, but not about integration, per se.” *Id.* at 17:13–18.

Moreover, the patentee did not rely on the preamble during prosecution to distinguish the claimed invention from the prior art. *See generally* Ex. 1002. In the first Office action, the Examiner allowed the claims. *Id.* at 21–28. Thus, the patentee had no need to distinguish the claimed invention from the prior art applied by the Examiner.

Patent Owner’s argument that deleting the term “integrated circuit” from each claim’s preamble enlarges claim scope does not help resolve the issue whether that term limits the claims. Essentially the same argument could be made anytime a dispute arises whether a preamble limits a claim.

As for Patent Owner’s assertion that arranging the claimed circuitry on different semiconductor substrates instead of “a single semiconductor substrate” would unnecessarily waste “power, energy and area,” we disagree that the alleged waste warrants treating the term “integrated circuit” as limiting. *See* Resp. 23–24; Ex. 2001 ¶ 78. As explained above, the claimed invention accomplishes power management and reduces leakage current, regardless whether the claimed circuitry exists on “a single semiconductor substrate” or on different semiconductor substrates. Ex. 1012 ¶¶ 30–31; Tr. 31:6–32:5; *see id.* at 21:13–21. Absent a clear disclaimer of particular subject matter, that an inventor contemplated an invention’s use “in a particular manner does not limit the scope to that narrow context.”

Brookhill-Wilk I, LLC. v. Intuitive Surgical, Inc., 334 F.3d 1294, 1301 (Fed. Cir. 2003). Claims set boundaries for an invention. *See Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002). Hence, some implementations of a claimed invention may perform better than other implementations.

As for Patent Owner’s assertion that an ordinarily skilled artisan “would understand that multiple power domains would be provided within a single substrate” instead of “spread across multiple substrates,” we disagree that such an understanding warrants treating the term “integrated circuit” as limiting. *See* Resp. 25; Sur-reply 7; Ex. 2001 ¶ 78. As Dr. Jacob explained, “[t]here is nothing about the term ‘power domain’ that limits its application only to semiconductors, let alone to single-die semiconductor implementations,” and “[t]he term simply means what it says: a power domain, i.e. the domain over which a particular power supply applies.” Ex. 1012 ¶ 33. As Dr. Jacob also explained, “[w]ithin a computer system, there are also multiple power domains, because the [central processing unit], the graphics card, the disk, the [dynamic random-access memory], the monitor, the [radio-frequency] antennae, the automatically controlled case fan/s, the [universal serial bus]-based peripheral system powering the keyboard and mouse, etc.,” and “each of these can be powered separately and thereby define its own ‘power domain.’” *Id.* ¶ 34. Hence, we agree with Dr. Jacob that “[t]he concept of ‘power domain’ is quite clear and not at all restricted to semiconductors, single-die implementations or otherwise.” *Id.* ¶ 36.

For the reasons discussed above, the term “integrated circuit” in the preambles of claims 15 and 24 “state[s] a purpose or intended use for the invention.” *See Catalina Mktg.*, 289 F.3d at 809–10 (deciding that a preamble stated an intended use). The “rule against giving invention-defining effect to intended-use preamble language reflects a longstanding substantive aspect of the patent statute—specifically, the ‘well settled’ fundamental principle ‘that the recitation of a new intended use for an old

product does not make a claim to that old product patentable.” *Arctic Cat*, 919 F.3d at 1328 (quoting *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997)).

Based on the language of claims 15 and 24, the ’555 patent’s specification, and its prosecution history, and for the reasons discussed above, the preamble term “integrated circuit” does not limit either claim.

*C. Anticipation by Houston:
Claims 15 and 24*

1. ANTICIPATION UNDER 35 U.S.C. § 102

“[T]o demonstrate anticipation, the proponent must show ‘that the four corners of a single, prior art document describe every element of the claimed invention.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Xerox Corp. v. 3Com Corp.*, 458 F.3d 1310, 1322 (Fed. Cir. 2006)). The prior-art document “must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Hence, a patent challenger cannot rely on portions from different embodiments in a prior-art document to demonstrate anticipation. *See id.* at 1369, 1371.

A prior-art document’s “disclosure of a limited number of combination possibilities” may anticipate a claim. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1274 (Fed. Cir. 2017); *see Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1380, 1382–83 (Fed. Cir. 2015). Hence, a reference may anticipate “if that reference teaches that the disclosed components or functionalities may be combined and one of skill in the art would be able to implement the

combination.” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1344 (Fed. Cir. 2016). The “dispositive question regarding anticipation [i]s whether one skilled in the art would reasonably understand or infer from the [reference’s] teaching” that it discloses every claim element arranged as in the claim. *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991); *see Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003).

We analyze the anticipation issues according to these principles.

2. OVERVIEW OF HOUSTON (EX. 1003)

Houston concerns power management for semiconductor circuits containing memory cell arrays and periphery circuitry for memory cell arrays. Ex. 1003, 1:5–8, 1:43–52, 1:65–2:13, 3:66–4:5, 4:58–60, 5:49–64, 6:4–30, code (57). Houston explains that leakage current in a semiconductor circuit “causes a reduction in the supply voltage” that may “cause unpredictable behavior in circuit performance.” *Id.* at 1:11–16. Houston also explains that “cache memory, integrated circuits with on-chip memory, or other memory arrays can be significant sources of leakage current for a computer system.” *Id.* at 1:17–20. Houston notes that, “[e]ven when a memory array is inactive, power is still being consumed because of leakage currents.” *Id.* at 1:32–34.

According to Houston, “[r]educd power consumption is especially important in those circuit applications that use portable power supplies, such as consumer electronic products.” Ex. 1003, 1:36–40. Houston describes “[l]ow power consumption in memory devices” as a longstanding “goal of semiconductor circuit engineers.” *Id.* at 1:31–32.

To “reduce leakage current and power consumption,” Houston selectively removes power from a memory cell array or selected blocks of a memory cell array. Ex. 1003, code (57). Houston selectively removes power by (1) coupling a switch between a power supply and the memory cell array or selected blocks of the memory cell array and (2) controlling the switch “according to the active, standby, or disabled operation states of the memory.” *Id.* at code (57); *see id.* at 1:49–2:13, 2:52–4:4, Figs. 1–3. To “further reduce leakage currents and power consumption,” Houston selectively removes power from periphery circuitry for a memory cell array, e.g., by removing power “separately from the memory cell array.” *Id.* at code (57); *see id.* at 4:58–5:24, Fig. 6.

Houston’s Figure 1 is reproduced below:

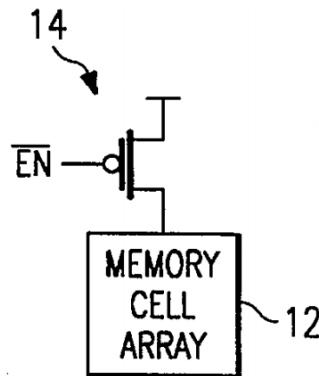


FIG. 1

Figure 1 shows memory cell array 12 of a memory device and p-channel transistor 14 for enabling and disabling memory cell array 12. Ex. 1003, 2:52–62.

Specifically, p-channel transistor 14 acts as a switch and selectively couples memory cell array 12 to a power supply. Ex. 1003, 2:58–60, code (57); *see id.* at 1:53–57. The gate of p-channel transistor 14 receives a control signal, i.e., enable/disable signal $\overline{EN}$. *Id.* at 2:60–62, Fig. 1; *see id.* at

1:53–57. When enable/disable signal $\overline{EN}$ is low, “the memory cell array 12 is active and ready for read and write operations.” *Id.* at 2:62–65. But when enable/disable signal $\overline{EN}$ is high, “the path from the power supply to the memory cell array 12 is cut off,” rendering memory cell array 12 inactive. *Id.* at 2:65–66. “The leakage current in the memory cell array 12 when the circuit is inactive is therefore greatly reduced or effectively eliminated.” *Id.* at 2:66–3:2.

Houston’s Figure 2 is reproduced below:

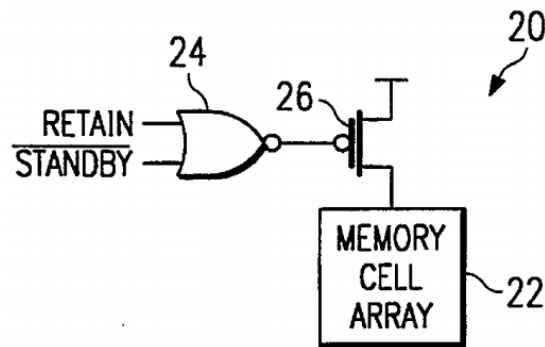


FIG. 2

Figure 2 shows memory cell array 22 and “logic to combine the information on whether or not the memory is in standby and whether or not [the] memory is to be retained when in standby and using the combined information to control power to the memory cell array.” Ex. 1003, 3:3–10; *see id.* at 2:23–24.

Specifically, p-channel transistor 26 acts as a switch and selectively couples memory cell array 22 to a power supply. Ex. 1003, 3:10–13, code (57); *see id.* at 1:58–64. The gate of p-channel transistor 26 receives the output of NOR gate 24. *Id.* at 3:10–13, Fig. 2. NOR gate 24 receives as inputs the control signals $\overline{STANDBY}$ and RETAIN. *Id.* When memory cell array 22 is not in standby ($\overline{STANDBY}$ high) or when data retention is

required (RETAIN high), NOR gate 24 produces a low output that turns on transistor 26, thus applying power to memory cell array 22. *Id.* at 3:13–17. When memory cell array 22 is in standby ($\overline{\text{STANDBY}}$ low) and data retention is not required (RETAIN low), NOR gate 24 produces a high output that turns off transistor 26, thus removing power from memory cell array 22. *Id.* at 3:17–20.

Houston's Figure 4 is reproduced below:

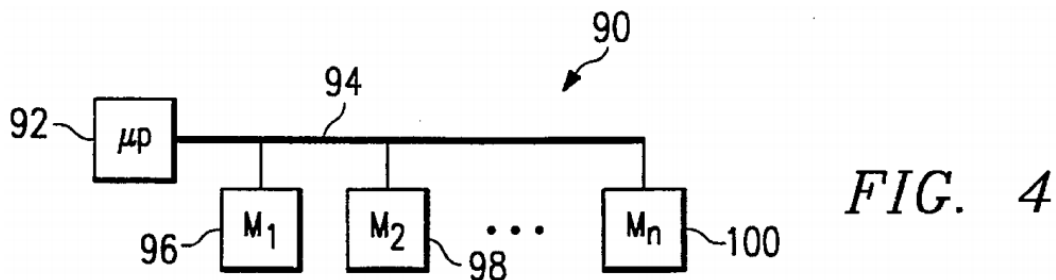


Figure 4 depicts microprocessor system 90. Ex. 1003, 2:27–28, 4:6–7.

Microprocessor system 90 includes microprocessor 92 coupled to bus 94 and memory cell arrays or memory segments 96–100 also coupled to bus 94. Ex. 1003, 4:7–9, Fig. 4. Microprocessor 92 generates control signals for the memory cell arrays or the memory segments to selectively enable and disable them. *Id.* at 4:12–28; *see id.* at 1:58–2:13. The control signals “may be in the form of enable and/or data retention signals as described above,” i.e., for Figures 1 and 2, “to selectively put the memories 96–100 in the active, standby, or disabled state.” *Id.* at 4:16–19; *see id.* at 1:58–2:13.

“The memory cell arrays or memory segments 96–100 may exist on the same semiconductor device as the microprocessor, or they may be off-chip.” Ex. 1003, 4:9–12. In addition, “[o]n or off-chip switches may

be used to controllably connect or disconnect the memories 96–100 to the supply voltage.” *Id.* at 4:32–34.

Houston’s Figure 5 is reproduced below:

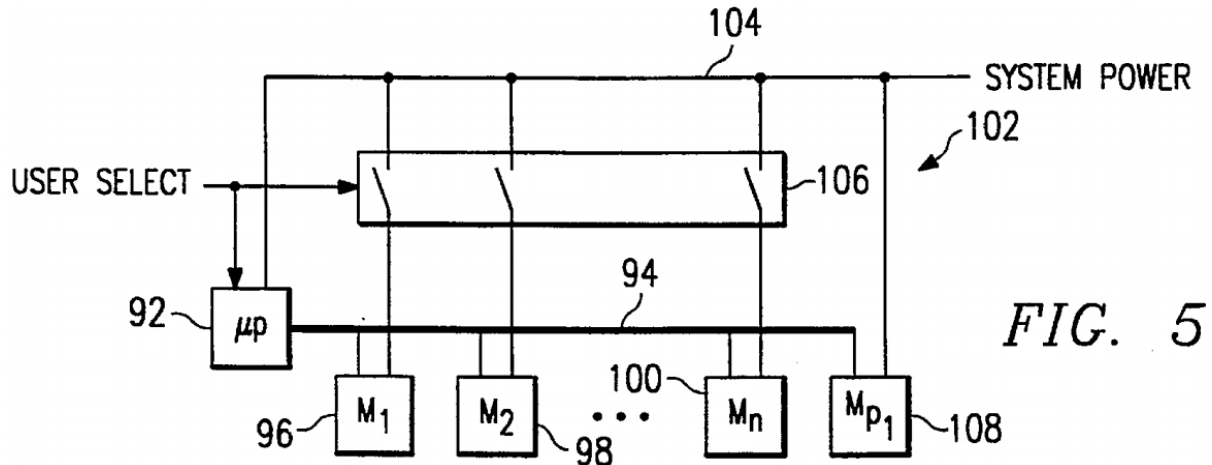


Figure 5 illustrates “alternative memory configuration 102.” Ex. 1003, 2:29–30, 4:43–44.

Memory configuration 102 includes microprocessor 92 coupled to bus 94 and memories 96–100 also coupled to bus 94. Ex. 1003, 4:43–44, Fig. 5; *see id.* at 2:29–30, 2:48–51, 4:7–9. In addition, individually controllable switches 106 couple memories 96–100 to supply voltage 104. *Id.* at 4:44–47. Moreover, memory 108 directly connects to supply voltage 104 “so that it is always enabled when the system is powered up.” *Id.* at 4:54–57.

Microprocessor 92 generates control signals “upon receipt of some user input or application program specification indicative of the amount of memory desired or required.” Ex. 1003, 4:49–52. The control signals “may include memory enable and/or data retention information as described above,” i.e., for Figures 1 and 2. *Id.* at 4:52–54; *see id.* at 1:58–64.

Houston's Figure 6 is reproduced below:

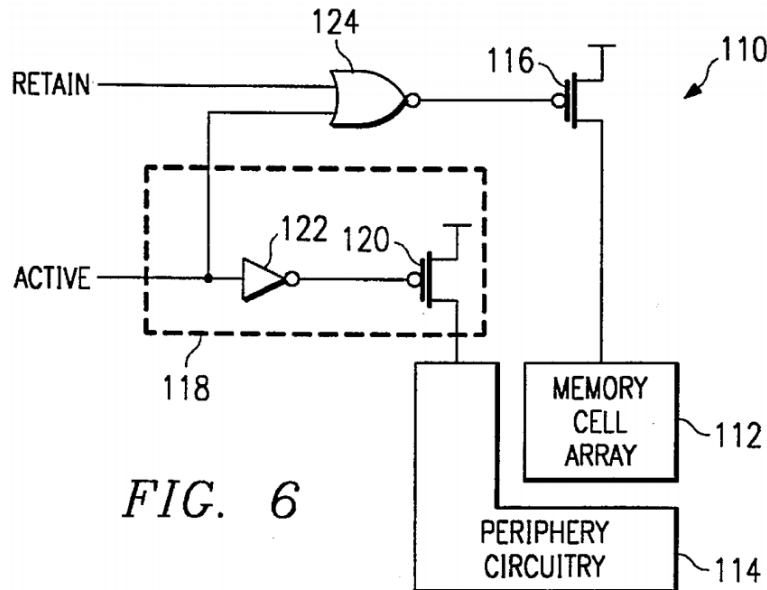


Figure 6 depicts control circuitry 110 for “selectively provid[ing] power independently to a memory cell array 112 and its periphery circuitry 114.” Ex. 1003, 4:58–60; *see id.* at 2:31–32, 5:7–13, code (57).

Specifically, p-channel transistor 116 acts as a switch and selectively couples memory cell array 112 to a power supply. Ex. 1003, 4:64–5:2, code (57). The gate of p-channel transistor 116 receives the output of NOR gate 124. *Id.* at 4:64–5:2, Fig. 6. NOR gate 124 receives as inputs the control signals ACTIVE and RETAIN. *Id.* When memory cell array 112 is in the active state (ACTIVE high) or when data retention is required (RETAIN high), NOR gate 124 produces a low output that turns on transistor 116, thus applying power to memory cell array 112. *Id.* at 4:64–5:2, 5:8–10, Fig. 6. When memory cell array 112 is not in the active state (ACTIVE low) and data retention is not required (RETAIN low), NOR gate 124 produces a high output that turns off transistor 116, thus removing power from memory cell array 112. *Id.*

Additionally, as depicted in Figure 6, logic circuit 118 includes p-channel transistor 120 and inverter 122, and logic circuit 118 controls power to periphery circuitry 114. Ex. 1003, 5:2–6, Fig. 6. Specifically, p-channel transistor 120 acts as a switch and selectively couples periphery circuitry 114 to a power supply. *Id.* at 5:4–6, Fig. 6. The gate of p-channel transistor 120 receives the output of inverter 122. *Id.* Inverter 122 receives as an input the ACTIVE control signal. *Id.* When memory cell array 112 is in the active state (ACTIVE high), inverter 122 produces a low output that turns on transistor 120, thus applying power to periphery circuitry 114. *Id.* at 5:4–8, Fig. 6. When memory cell array 112 is not in the active state (ACTIVE low), inverter 122 produces a high output that turns off transistor 120, thus removing power from periphery circuitry 114. *Id.*

Hence, memory cell array 112 receives power when it is in the active state (ACTIVE high) or when data retention is required (RETAIN high). Ex. 1003, 5:8–10, Fig. 6; *see id.* at 4:64–5:2. But periphery circuitry 114 only receives power when memory cell array 112 is in the active state (ACTIVE high). *Id.* at 5:7–8, Fig. 6. “Constructed in this manner, the periphery circuitry 114 and the memory cell array 112 are powered separately, so that power consumption by either circuit is selectively controlled.” *Id.* at 5:10–13, code (57).

3. WHETHER HOUSTON ANTICIPATES CLAIM 15

(a) Preamble

Claim 15’s preamble recites “[a]n integrated circuit having power management.” Ex. 1001, 11:39. To the extent the preamble is limiting, Petitioner asserts that Houston satisfies claim 15’s preamble because Houston discloses “a method and apparatus for providing power selectively

to memory cell arrays” using “a switch coupled between one or more memory arrays and a power supply that connects or disconnects the memory array(s) to or from the power supply in response to” control signals from a microprocessor. Pet. 20 (quoting Ex. 1003, 1:6–8); *see* Ex. 1004 ¶¶ 88–90. Petitioner also asserts that Houston’s method and apparatus “address ‘leakage current and power consumption in memory devices.’” Pet. 17 (quoting Ex. 1003, 1:43–44); *see* Ex. 1004 ¶¶ 76–78.

Patent Owner disputes that Houston satisfies claim 15’s preamble. *See* Resp. 27–34; Sur-reply 1–20. In particular, Patent Owner contends that claim 15 recites “[a]n integrated circuit” including “the following four circuit elements: (i) processing circuitry for executing instructions; (ii) a plurality of memory bit cells contained within a memory array; (iii) memory array peripheral circuitry; and (iv) control circuitry.” Resp. 28; *see id.* at 30. Patent Owner asserts that claim 15 requires “that all four circuit elements be provided on or within a single semiconductor substrate” because “the claim term ‘integrated circuit’ refers to a single substrate.” *Id.* at 28; *see id.* at 30. Patent Owner also asserts that “[t]here is no single embodiment or arrangement disclosed in Houston” that “provides all the elements of claim 15 on or within a single substrate.” *Id.* at 30.

Patent Owner’s assertions rest on its argument that claim 15’s preamble is limiting. For the reasons discussed above, we disagree with Patent Owner. *See supra* § III.B.2.

In any event, even assuming that claim 15’s preamble is limiting, we agree with Petitioner that Houston satisfies this preamble. *See* Ex. 1004 ¶¶ 88–90. Houston describes an apparatus for “selectively supply[ing] power to a memory array” that “eliminates or substantially reduces” leakage

current and power consumption, thus improving performance. Ex. 1003, 1:43–64; *see id.* at 2:66–3:2, code (57); Ex. 1004 ¶¶ 76, 89–90. More specifically, Houston discloses a microprocessor system including (1) a microprocessor; (2) on-chip memory cell arrays or memory segments, i.e., memories “exist[ing] on the same semiconductor device” as the microprocessor; and (3) on-chip switches that “controllably connect or disconnect” on-chip components to a power supply. Ex. 1003, 4:6–11, 4:32–34, Fig. 4; *see id.* at 1:65–2:13, 3:20–23, 3:30–34; Ex. 1004 ¶¶ 81, 92; Ex. 2001 ¶¶ 58–60, 92.

For the reasons discussed above, claim 15’s preamble is not limiting, but even if it were limiting, Houston discloses “[a]n integrated circuit having power management” according to claim 15’s preamble.

(b) The “Processing Circuitry” Limitation

Claim 15 recites “processing circuitry for executing instructions.” Ex. 1001, 11:41. Petitioner asserts that Houston satisfies this limitation because Houston’s Figures 4 and 5 each depict microprocessor system 90 including microprocessor 92 that generates control signals. Pet. 21–22 (citing Ex. 1003, 4:6–12, 4:43–52, Figs. 4–5); *see* Ex. 1004 ¶¶ 91–93.

In addition, Dr. Jacob described a “microprocessor” as “an integrated circuit that executes instructions.” Ex. 1004 ¶ 92 (citing Ex. 1003, 1:58–2:13, 3:3–23, 4:6–19, Fig. 4). Dr. Jacob stated that Houston “discloses application programs running on the microprocessor” and that “[r]unning application programs means executing instructions.” *Id.* ¶ 93 (citing Ex. 1003, 3:35–49, 4:43–57, Figs. 3, 5).

Patent Owner does not dispute that Figures 4 and 5 each depict microprocessor system 90 including microprocessor 92 that generates control signals. *See* Resp. 9–11, 36; Ex. 2001 ¶¶ 58–61, 92.

We agree with Petitioner that Houston satisfies claim 15’s “processing circuitry” limitation. *See* Ex. 1004 ¶¶ 91–93. For example, Figure 4 depicts microprocessor system 90 including microprocessor 92. Ex. 1003, 2:27–28, 4:6–12, Fig. 4; *see* Ex. 1004 ¶ 92; Ex. 2001 ¶¶ 58–60, 92. Microprocessor 92 executes instructions, e.g., to generate control signals for memory cell arrays or memory segments 96–100 to selectively connect them to or disconnect them from a power supply. Ex. 1003, 4:12–34; *see* Ex. 1004 ¶¶ 92–93; Ex. 2001 ¶ 60.

Similarly, Houston’s Summary of the Invention discloses a microprocessor that executes instructions, e.g., to generate control signals for memory cell arrays or memory segments. *See* Ex. 1003, 1:58–2:13. As an example, the microprocessor generates “a standby signal and a data retention signal” for selectively connecting a memory cell array to a power supply. *Id.* at 1:58–64.

As another example, the microprocessor generates the following control signals for a memory cell array segmented into memory blocks: (1) “a standby signal for each of the plurality of memory blocks indicative of an active/inactive status of the respective memory blocks”; and (2) “a data retention signal for each of the plurality of memory blocks indicative of whether data stored in the respective memory blocks are to be retained.” Ex. 1003, 1:65–2:10; *see id.* at 3:35–37, 5:66–6:4. These microprocessor-generated control signals selectively connect memory blocks having either

“a standby signal indicating an active status” or “a data retention signal indicating data retention” to a power supply. *Id.* at 2:10–13.

For the reasons discussed above, Houston discloses “processing circuitry for executing instructions,” as required by claim 15.

(c) The “Memory Array” Limitation

Claim 15 also recites “a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane.” Ex. 1001, 11:42–45.

Petitioner asserts that Houston satisfies this limitation because Houston’s Figure 6 illustrates memory cell array 112 and each “memory cell in the memory cell array 112 holds a bit of data.” Pet. 22–23; *see* Ex. 1004

¶¶ 94–95. Petitioner also asserts that Figure 6 illustrates “memory cell array 112 coupled to [a] power supply via transistor 116 to create a first power plane.” Pet. 23–24; *see* Ex. 1004 ¶¶ 96–101.

Patent Owner disputes that Figures 4 and 5 (each with microprocessor 92) relate to the same embodiment as Figure 6 (with memory cell array 112). *See* Resp. 29–34; Sur-reply 14–15 & n.1; Ex. 2001 ¶¶ 92–96. Specifically, Patent Owner asserts that “Houston discloses ten distinct memory device power control embodiments.” Resp. 30; *see id.* at 6–17 & nn.1–2; Ex. 2001 ¶¶ 49–74, 88. As shown in the following table, Patent Owner correlates the “ten distinct” embodiments to Houston’s figures:

Houston’s Figure(s)	Patent Owner’s Embodiment
Figure 1	first embodiment
Figure 2	second embodiment
Figure 3	third embodiment
Figures 4 and 5	fourth embodiment

Houston's Figure(s)	Patent Owner's Embodiment
Figure 6	fifth embodiment
Figure 7	sixth embodiment
Figure 8A	seventh embodiment
Figure 8B	eighth embodiment
Figure 8C	ninth embodiment
Figure 8D	tenth embodiment

This table shows the correlation between Houston's figures and the "ten distinct" embodiments that Patent Owner enumerates. Resp. 6–17 & n.1; *see* Ex. 2001 ¶¶ 49–73.

Patent Owner asserts that "no single" embodiment in Houston "arranges or combines all of the elements or steps in the same way as recited in claims 15 and 24." Resp. 30–31, 33; *see* Sur-reply 13–17; Ex. 2001 ¶¶ 89–91. In addition, Patent Owner contends that Petitioner improperly combines "different parts of separate embodiments of Houston to prove anticipation." Resp. 30, 33; *see* Sur-reply 14.

Regarding claim 15's "memory array" limitation, Patent Owner concedes that Figure 6 depicts "control signals that control the switches that connect" memory cell array 112 to a power supply. Resp. 31; *see* Ex. 2001 ¶ 63. But Patent Owner contends that Figure 6 and the "corresponding description in the specification" do not disclose that "these signals are necessarily generated by processing circuitry or a processor that executes instructions, or by a processor or processing circuitry that is part of the same integrated circuit as" memory cell array 112 in Figure 6. Resp. 31; *see* Ex. 2001 ¶¶ 95–96. Patent Owner also contends that "Houston does not expressly or inherently disclose a microprocessor or processing circuitry"

with respect to Figure 6, i.e., the fifth embodiment. Resp. 32; *see* Ex. 2001 ¶¶ 95–96.

Further, Patent Owner relies on Houston’s reference numerals to evidence different embodiments. *See* Tr. 42:17–26, 43:6–14. Patent Owner asserts that “Houston expressly states that ‘like numerals [are] used for like and corresponding parts of the various drawings.’” Resp. 6 (alteration by Patent Owner) (quoting Ex. 1003, 2:50–51). Patent Owner argues that “Houston describes and depicts the embodiment shown in Figs. 4 and 5 to be separate from the embodiment shown in Fig. 6, even using different reference numerals for each embodiment.” Sur-reply 14.

Petitioner disputes that Houston discloses “ten distinct” embodiments. Reply 11–17; *see* Ex. 1012 ¶¶ 9–27. Petitioner argues that Houston’s figures and their associated disclosures are “meant to be interpreted together, not viewed in vacuum.” Reply 16; *see* Ex. 1012 ¶¶ 24–25. Petitioner also argues that Houston’s specification and claims support interpreting Houston that way. *See* Reply 13–16.

Specifically, Petitioner asserts that Houston’s Summary of the Invention “does not mention separate or distinct embodiments, but instead just refers to ‘aspect[s] of *the* invention.’” Reply 16 (alteration and emphasis by Petitioner) (quoting Ex. 1003, 1:47–2:13); *see* Ex. 1012 ¶ 24. In addition, Petitioner contends that Houston’s Detailed Description of the Invention starts “by stating that ‘*[t]he preferred embodiment* [singular] of the present invention and its advantages are best understood by *referring to FIGS. 1–9*[.]’” Reply 16 (alterations and emphases by Petitioner) (quoting Ex. 1003, 2:48–49); *see* Ex. 1012 ¶ 24.

Also, Petitioner asserts that Houston's independent claim 1 and dependent claim 9 together recite a "single embodiment" with "everything that Patent Owner wrongly contends is not captured in any single embodiment of Houston." Reply 14–15; *see* Ex. 1012 ¶ 24; Ex. 2011, 37:7–38:5. According to Petitioner, claims 1 and 9 together recite the following: "a 'memory' that is 'associated with a microprocessor' and that includes a 'memory cell array' that can be selectively powered or disconnected from power by 'a first control signal and a second control signal generated by said microprocessor,'" and "'periphery circuitry' that is selectively powered or disconnected from power in response to 'said control signal and a second control signal generated by said microprocessor.'" Reply 14 (quoting Ex. 1003, 6:46–55, 7:23–28).

As further support for Petitioner's position, its expert, Dr. Jacob, stated that Houston's figures and their associated disclosures address different "aspects of the claimed invention" and provide "different levels of detail." Ex. 1012 ¶¶ 9, 22; *see* Ex. 2011, 30:8–35:10, 36:7–9, 45:5–47:7, 65:23–68:21. He also stated that some figures depict details "at the system level" and other figures depict details "at the level of components within the system." Ex. 1012 ¶ 9. According to Dr. Jacob, "you need to combine these figures to understand the invention" in Houston. Ex. 2011, 46:7–9; *see id.* at 67:11–15, 67:21–24.

Dr. Jacob elaborated about combining Houston's figures and their associated disclosures. *See* Ex. 1012 ¶¶ 9–27; Ex. 2011, 30:8–35:10, 37:7–38:5. Specifically, he stated that "a person of ordinary skill would understand that Houston discloses a cross product of the following detailed implementations":

“two *system-level* embodiments,” i.e., Figures 4 and 5;
“four *array-level* embodiments,” i.e., Figures 8A–8D;
“four *control-level* embodiments,” i.e., Figures 1, 2, 6, and 7;
“two *block-level* embodiments,” i.e., Figure 3 (optionally
controlling either an entire memory array or individual
blocks within the memory array).

Ex. 1012 ¶ 19; *see id.* ¶¶ 9–18, 20–22.

Dr. Jacob explained that “embodiments at a certain level” correspond to “options for designing that particular level.” Ex. 2011, 33:10–12. He also explained that “the *system-level*, *array-level*, *block-level*, and *control-level* embodiments each describe the Houston invention at different levels of detail and are therefore meant to be integrated with each other to produce multiple unique systems embodying Houston’s invention.” Ex. 1012 ¶ 22; *see id.* ¶ 27; Ex. 2011, 33:13–35:10.

Dr. Jacob described Houston as disclosing “potentially $2 \times 4 \times 4 \times 2 = 64$ embodiments of systems comprising microprocessors, multiple memory arrays, multiple blocks within those arrays, and the control mechanisms to power the arrays and blocks, as well as the peripheral logic for the arrays, potentially independently.” Ex. 1012 ¶ 20; *see id.* ¶ 23; Ex. 2011, 65:23–66:10. He stated that “all of these things combine to create one large system” and that “it’s all one cohesive embodiment of the invention.” Ex. 2011, 34:25–35:10; *see id.* at 46:4–9, 67:11–15, 67:21–24. He similarly stated that Houston’s potential embodiments “are all different aspects of the very same invention.” Ex. 1012 ¶ 24; *see* Ex. 2011, 32:16–33:21, 36:7–9, 66:11–25. Additionally, Dr. Jacob analogized Houston’s potential embodiments to potential automobile embodiments resulting from, for

example, different interior options, exterior options, and drivetrain options.
Ex. 1012 ¶ 23.

For the reasons explained below, we agree with Petitioner that an ordinarily skilled artisan would reasonably understand or infer that Houston's figures and their associated disclosures are "meant to be interpreted together, not viewed in vacuum." *See, e.g.*, Ex. 1012 ¶¶ 9–27, 39–40, 48; Ex. 2011, 30:8–35:10, 36:7–9, 37:7–38:5, 45:5–47:7, 65:23–68:21.

In various sections, Houston references a single invention, i.e., "the present invention." In particular, the Technical Field of the Invention references "the present invention." Ex. 1003, 1:3–8. Similarly, the Summary of the Invention references "the present invention" and describes different aspects of the invention, i.e., "one aspect of the invention," "another aspect of the invention," and "yet another aspect of the invention." *Id.* at 1:47–2:13. The Brief Description of the Drawings also references "the present invention." *Id.* at 2:16–20. In addition, the Detailed Description of the Invention starts by stating that "[t]he preferred embodiment of the present invention and its advantages are best understood by referring to FIGS. 1–9 of the drawings." *Id.* at 2:45–51. The Detailed Description ends by stating that "the present invention and its advantages have been described in detail." *Id.* at 6:40–41. Hence, when considering all these cited disclosures together, we find that Houston contemplates a single invention.

Further, Houston's disclosures for some figures cross-reference other figures. As an example, Figure 2's description states that "[t]he techniques and circuit configurations shown and described hereinafter," i.e., for other figures, "are equally applicable to" Figure 2's circuitry. Ex. 1003, 3:31–34.

As another example, Figure 3's description states that control signals "may be generated from a retain data signal and a standby signal as in FIG. 2" and that a "low power retain data signal may also be added as in FIG. 7." *Id.* at 3:40–45.

Additionally, Figure 4's description explains that microprocessor-generated control signals "may be in the form of enable and/or data retention signals as described above," i.e., for Figures 1 and 2, "to selectively put the memories 96–100 in the active, standby, or disabled state." Ex. 1003, 4:7–19; *see id.* at 2:52–3:20, Figs. 1–2. Similarly, Figure 5's description explains that microprocessor-generated control signals "may include memory enable and/or data retention information as described above," i.e., for Figures 1 and 2. *Id.* at 4:49–54; *see id.* at 2:52–3:20, Figs. 1–2.

Consistent with those disclosures, the Summary of the Invention describes an "aspect of the invention" with circuitry according to Figure 2 and microprocessor-generated control signals according to Figures 4 and 5. Ex. 1003, 1:58–64. Specifically, the Summary describes a switch "coupled between the memory array and a power supply" that "connects or disconnects the memory array from the power supply in response to a standby signal and a data retention signal." *Id.* at 1:60–64. Figure 2 shows a switch "coupled between the memory array and a power supply" that "connects or disconnects the memory array from the power supply in response to a standby signal and a data retention signal." *Id.* at 3:3–20, Fig. 2. In addition, the Summary describes the standby and data retention signals as "generated by the microprocessor." *Id.* at 1:60–64. But Figure 2 shows no microprocessor. *Id.* at 3:3–20, Fig. 2. Only Figures 4, 5, and 9

show a microprocessor. *Id.* at Figs. 4–5, 9. Thus, we find that Houston relies on different figures to support an “aspect of the invention.”

An analysis of the invention defined by Houston’s claims 1 and 9 bolsters our finding that Houston relies on different figures to support an “aspect of the invention.” Those claims read as follows:

1. A memory associated with a microprocessor [sic] comprising:
 - a memory cell array; and
 - a switch coupled between said memory cell array and a supply voltage, said switch controllably connecting and disconnecting said memory cell array and said supply voltage in response to a selected state of a first control signal and a second control signal generated by said microprocessor wherein said first control signal and said second control signal may independently vary.
9. The memory, as set forth in claim 1, further comprising:
 - periphery circuitry coupled to said memory cell array; and
 - a second switch coupled between said periphery circuitry and said supply voltage responsive to a selected state of said control signal and a second control signal generated by said microprocessor.

Ex. 1003, 6:46–55, 7:23–28.

Together, Houston’s claims 1 and 9 require a microprocessor, a memory cell array, and periphery circuitry for the memory cell array. But no figure in Houston depicts a microprocessor, a memory cell array, and periphery circuitry for the memory cell array. Ex. 1003, Figs. 1–9; *see* Ex. 2001 ¶¶ 93–98. For instance, Figures 4 and 5 each show a microprocessor and a memory cell array, but not periphery circuitry for the

memory cell array. Ex. 1003, Figs. 4–5; *see* Ex. 1013, 29:9–30:1; Ex. 2001 ¶¶ 93–94. Figure 6 shows a memory cell array and periphery circuitry for the memory cell array, but not a microprocessor. Ex. 1003, Fig. 6; Ex. 2001 ¶¶ 95–96.

Together, however, Figures 4 and 6 show a microprocessor, a memory cell array, and periphery circuitry for the memory cell array. Ex. 1003, Figs. 4, 6; *see* Ex. 1013, 31:2–19; Ex. 2011, 37:7–38:5. Together, Figures 5 and 6 also show a microprocessor, a memory cell array, and periphery circuitry for the memory cell array. Ex. 1003, Figs. 5–6; *see* Ex. 2011, 37:7–38:5. Thus, when considering the plain language of the claims, we determine that Houston relies on different figures to support an “aspect of the invention,” i.e., the invention defined by Houston’s claims 1 and 9.

That different figures support an “aspect of the invention” refutes Patent Owner’s assertion that “Houston discloses ten distinct memory device power control embodiments.” *See* Resp. 30. Moreover, Patent Owner misplaces its reliance on Houston’s reference numerals to evidence different embodiments, i.e., different reference numerals for the memories in Figures 4 and 5 compared to the memory in Figure 6. *See* Sur-reply 14. Figures 4 and 5 do not depict the same parts as Figure 6. For Figures 4 and 5, Houston describes the memories as “memory cell arrays or memory segments.” Ex. 1003, 4:6–12, 4:43–44. For Figure 6, however, Houston describes the memory as “a memory cell array.” *Id.* at 4:58–60. Hence, Houston’s use of different reference numerals for the memories in Figures 4 and 5 compared to the memory in Figure 6 does not denote different embodiments.

Because Houston references a single invention, Houston's disclosures for some figures cross-reference other figures, and different figures support an "aspect of the invention," an ordinarily skilled artisan would reasonably understand or infer that Houston's figures and their associated disclosures are "meant to be interpreted together, not viewed in vacuum," as Petitioner asserts. *See* Reply 16. More specifically, for the reasons explained below, an ordinarily skilled artisan would reasonably understand or infer that Figure 6 supplies more detail for the microprocessor systems depicted in Figures 4 and 5. *See, e.g.*, Ex. 1003, 4:6–5:13, Figs. 4–6; Ex. 1012 ¶¶ 9–27, 39–40, 48; Ex. 2011, 30:8–35:10, 36:7–9, 37:7–38:5, 65:23–68:21; Tr. 33:14–17.

Dr. Jacob explained that "all the most commonly used memory-array technologies include peripheral circuitry." Ex. 1012 ¶ 40; *see id.* ¶ 39 (citing Exs. 1014–1015). Dr. Khatri agreed that memory arrays cannot typically operate without peripheral circuitry. Ex. 1013, 15:15–16:1; *see* Ex. 2001 ¶ 38. Also, at the oral hearing, Patent Owner admitted that the memory arrays in Figure 4 have peripheral circuitry. Tr. 33:14–17. Hence, a "person of ordinary skill would understand the memory arrays in Figures 4 and 5 to include peripheral circuitry, despite this not being explicitly shown." Ex. 1012 ¶ 40; *see id.* ¶ 48.

Further, Houston expressly references Figure 2 when describing Figures 4 and 5, and Figures 2 and 6 illustrate similar control circuitry and control signals. For Figure 4, Houston states that microprocessor-generated control signals "may be in the form of enable and/or data retention signals as described above," e.g., for Figure 2, "to selectively put the memories 96–100 in the active, standby, or disabled state." Ex. 1003, 4:7–19; *see id.* at

3:3–20, Fig. 2. For Figure 5, Houston states that microprocessor-generated control signals “may include memory enable and/or data retention information as described above,” e.g., for Figure 2. *Id.* at 4:49–54; *see id.* at 3:3–20, Fig. 2.

Also, Figures 2 and 6 illustrate similar control circuitry and control signals. Although Figure 2 lacks periphery circuitry, Figures 2 and 6 depict the same components for selectively applying power to and removing power from a memory cell array. Ex. 1003, 3:10–13, 4:64–5:2, code (57), Figs. 2, 6. In particular, each figure depicts a p-channel transistor and a NOR gate. *Id.* In Figure 2, the gate of p-channel transistor 26 receives the output of NOR gate 24. *Id.* at 3:10–13, Fig. 2. In Figure 6, the gate of p-channel transistor 116 receives the output of NOR gate 124. *Id.* at 4:64–5:2, Fig. 6.

Compared to Figure 2’s circuitry, however, Figure 6 adds periphery circuitry for a memory cell array and control circuitry for selectively applying power to and removing power from the periphery circuitry. Ex. 1003, 4:58–60, 5:2–6, Fig. 6. Specifically, Figure 6 adds periphery circuitry 114 and logic circuit 118. *Id.* Logic circuit 118 includes p-channel transistor 120 and inverter 122, and logic circuit 118 controls power to periphery circuitry 114. *Id.* at 5:2–6, Fig. 6.

In addition, the control signals in Figures 2 and 6 function similarly, i.e., the control signals $\overline{\text{STANDBY}}$ and RETAIN in Figure 2 and the control signals ACTIVE and RETAIN in Figure 6. *See* Ex. 2001 ¶¶ 53, 63. In Figure 2, when memory cell array 22 is not in standby ($\overline{\text{STANDBY}}$ high) or when data retention is required (RETAIN high), NOR gate 24 produces a low output that turns on transistor 26, thus applying power to memory cell

array 22. Ex. 1003, 3:13–17. Similarly in Figure 6, when memory cell array 112 is in the active state (ACTIVE high) or when data retention is required (RETAIN high), NOR gate 124 produces a low output that turns on transistor 116, thus applying power to memory cell array 112. *Id.* at 4:64–5:2, 5:8–10, Fig. 6.

In Figure 2, when memory cell array 22 is in standby ($\overline{\text{STANDBY}}$ low) and data retention is not required (RETAIN low), NOR gate 24 produces a high output that turns off transistor 26, thus removing power from memory cell array 22. Ex. 1003, 3:17–20. Similarly in Figure 6, when memory cell array 112 is not in the active state (ACTIVE low) and data retention is not required (RETAIN low), NOR gate 124 produces a high output that turns off transistor 116, thus removing power from memory cell array 112. *Id.* at 4:64–5:2, 5:8–10, Fig. 6.

Consistent with the correspondence between the $\overline{\text{STANDBY}}$ and ACTIVE signals in Figures 2 and 6, Houston explains that “a standby signal may be used in place of the active signal with corresponding changes in the logic.” Ex. 1003, 5:15–17.

Further, as discussed above, Figures 4 and 6 together support the invention defined by Houston’s claims 1 and 9, and Figures 5 and 6 together support the invention defined by Houston’s claims 1 and 9. Ex. 1003, Figs. 4–6; *see* Ex. 1013, 31:2–19; Ex. 2011, 37:7–38:5.

In view of (1) the memory arrays in Figures 4 and 5 having periphery circuitry, (2) Houston’s express references to Figure 2 when describing Figures 4 and 5, (3) the similarity of the control circuitry and control signals in Figures 2 and 6, (4) Figure 6’s additional control circuitry for periphery circuitry, and (5) the support provided by Figures 4 and 6 or Figures 5 and 6

for the invention defined by Houston's claims 1 and 9, an ordinarily skilled artisan would reasonably understand or infer that Figure 6 supplies more detail for the microprocessor systems depicted in Figures 4 and 5. As Dr. Jacob stated, Figures 4 and 5 "are meant to be read and interpreted in combination with" Figure 6. Ex. 1012 ¶ 24; *see id.* ¶¶ 27, 40.

Regarding claim 15's "memory array" limitation, we agree with Petitioner that Houston satisfies this limitation. For example, Figure 4 depicts microprocessor system 90 including memory cell arrays 96–100. Ex. 1003, 2:27–28, 4:6–9, Fig. 4; *see* Ex. 1004 ¶¶ 81, 95; Ex. 2001 ¶¶ 58–59. Figure 6 supplies more detail for the microprocessor system and shows a memory cell array, i.e., memory cell array 112. Ex. 1003, 4:58–60, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99; Ex. 2001 ¶ 63. The memory cell array includes a plurality of memory bit cells. Ex. 1004 ¶ 95; *see id.* ¶¶ 37–38; Ex. 2001 ¶ 37. In addition, Figure 6 depicts p-channel transistor 116 that acts as a switch and selectively couples memory cell array 112 to a power supply. Ex. 1003, 4:64–5:2, code (57), Fig. 6; *see* Ex. 1004 ¶ 99; Ex. 2001 ¶ 63. By selectively coupling memory cell array 112 to a power supply, p-channel transistor 116 creates a first power plane. Ex. 1004 ¶ 99; *see id.* ¶¶ 97–98.

For the reasons discussed above, Houston discloses "a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane," as required by claim 15.

(d) The "Memory Array Peripheral Circuitry" Limitation

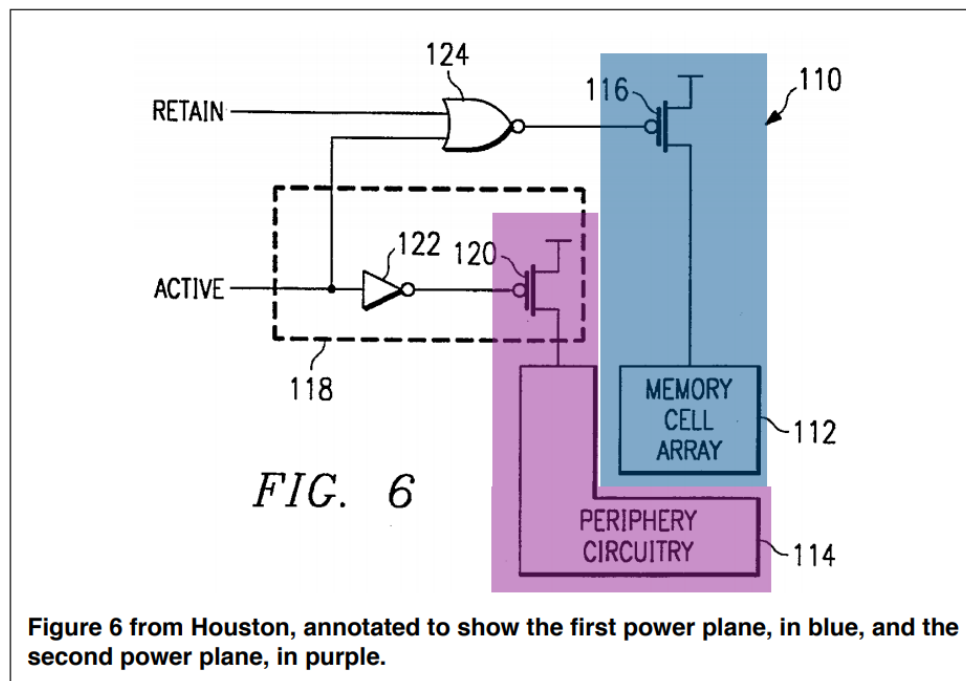
Claim 15 further recites "memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the memory array peripheral

circuitry being selectively coupled to the power supply terminal for creating a second power plane that is independent of the first power plane.”

Ex. 1001, 11:46–50. Petitioner asserts that Houston satisfies this limitation because Houston’s Figure 6 depicts “periphery circuitry 114 that is peripheral to memory cell array 112.” Pet. 24–25; *see* Ex. 1004 ¶¶ 102–105. Petitioner also asserts that Figure 6 depicts “periphery circuitry 114 coupled to a power supply via transistor 120 to create a second power plane independent of the first power plane created by coupling the memory cell array 112 to a power supply via transistor 116.” Pet. 26–27; *see* Ex. 1004 ¶¶ 106–108.

Further, Petitioner quotes Houston’s description of periphery circuitry 114 as follows: “It is understood in the art that *the periphery circuitry 114 of a memory cell array 112 may include, but not limited to, precharge and timing circuitry, row decode circuitry, sense amplifiers, data latches, and column decode circuitry* (not shown).” Pet. 25 (emphasis by Petitioner) (quoting Ex. 1003, 4:60–64). According to Dr. Jacob, “Houston’s definition of the memory’s periphery is consistent with both the ’555 patent and the well-understood meaning of *peripheral circuitry*: the periphery comprises the circuits that drive the memory array and provide the functions of, for example, reading and writing the contents of the array.” Ex. 1004 ¶ 105.

To support its position, Petitioner presents the highlighted version of Houston’s Figure 6 reproduced below:



Pet. 27; *see* Ex. 1004 ¶ 107. According to Petitioner, this highlighted version of Figure 6 “depicts the second power plane of the periphery circuitry 114 (highlighted in purple) and the first power plane of memory cell array 112 (highlighted in blue), which ‘are powered separately, so that power consumption by either circuit is selectively controlled.’” Pet. 27 (quoting Ex. 1003, 5:12–13); *see* Ex. 1004 ¶ 107.

As further support for Petitioner’s position, Dr. Jacob stated that Houston discloses (1) “the separation the memory cell array from the peripheral circuitry that drives the array” and (2) “providing separate power-supply connections for each.” Ex. 1004 ¶ 101; *see id.* ¶¶ 97–99. He explained that coupling peripheral circuitry to a power supply with a transistor switch “makes the coupling selective in the sense that the power to that subcircuit can be selectively shut off.” *Id.* ¶ 108.

Patent Owner does not dispute that Houston’s Figure 6 illustrates “memory cell array 112 of a memory device and its associated periphery

circuitry 114.” Resp. 11, 36; *see* Ex. 2001 ¶ 63. In addition, Patent Owner does not dispute that periphery circuitry 114 “is coupled to the power supply through a p-channel transistor 120” or that periphery circuitry 114 “is supplied power whenever the memory is in the active state.” Resp. 11–12; *see* Ex. 2001 ¶ 63.

We agree with Petitioner that Houston satisfies claim 15’s “memory array peripheral circuitry” limitation. In particular, Figure 6 depicts periphery circuitry 114 that is peripheral to memory cell array 112. Ex. 1003, 4:58–64, Fig. 6; *see* Ex. 1004 ¶¶ 103–104; Ex. 2001 ¶ 63. In addition, Figure 6 depicts p-channel transistor 120 that acts as a switch and selectively couples periphery circuitry 114 to a power supply. Ex. 1003, 5:4–6, Fig. 6; *see* Ex. 1004 ¶¶ 99, 107–108; Ex. 2001 ¶ 63. By selectively coupling periphery circuitry 114 to a power supply, p-channel transistor 120 creates a second power plane. Ex. 1004 ¶¶ 107–108. The second power plane created by p-channel transistor 120 is independent of the first power plane created by p-channel transistor 116. *Id.* ¶¶ 99, 107–108; *see id.* ¶ 82.

For the reasons discussed above, Houston discloses “memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the memory array peripheral circuitry being selectively coupled to the power supply terminal for creating a second power plane that is independent of the first power plane,” as required by claim 15.

(e) The “Control Circuitry” Limitation

Claim 15 additionally recites “control circuitry coupled to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the control circuitry selectively removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is

peripheral to the plurality of memory bit cells.” Ex. 1001, 11:51–56. Petitioner asserts that Houston satisfies this limitation because Houston’s Figure 6 illustrates logic circuit 118 including inverter 122 and transistor 120 “coupled to periphery circuitry 114 to control power to periphery circuitry 114.” Pet. 28 (citing Ex. 1003, 4:58–5:14, Fig. 6); *see* Ex. 1004 ¶¶ 109–114. Petitioner also asserts that inverter 122 receives as an input the ACTIVE control signal that causes transistor 120 to turn on or off to control power to periphery circuitry 114. Pet. 28–30.

As further support for Petitioner’s position, Dr. Jacob explained how the ACTIVE control signal causes transistor 120 to turn on or off to control power to periphery circuitry 114. Ex. 1004 ¶ 113. He testified, “When ACTIVE is high, the input to the switch [transistor 120] is low, therefore turning it on, which electrically connects the power supply to the peripheral circuitry, thereby turning the peripheral circuitry on.” *Id.* He also testified, “When ACTIVE is low, the input to the switch [transistor 120] is high, therefore turning it off, which electrically disconnects the power supply from the peripheral circuitry, thereby turning the peripheral circuitry off.” *Id.*

Patent Owner does not dispute that Figure 6 illustrates logic circuit 118 including “inverter 122, which receives the ACTIVE control signal, and p-channel transistor 120.” Resp. 11–12; *see* Ex. 2001 ¶ 63. In addition, Patent Owner does not dispute that, when “the ACTIVE control signal is high, power is supplied to periphery circuitry 114.” Resp. 12; *see* Ex. 2001 ¶ 63.

We agree with Petitioner that Houston satisfies claim 15’s “control circuitry” limitation. In Figure 6, logic circuit 118 includes p-channel transistor 120 and inverter 122, and logic circuit 118 controls power to

periphery circuitry 114. Ex. 1003, 5:2–6, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99, 112–113; Ex. 2001 ¶ 63. Specifically, p-channel transistor 120 acts as a switch and selectively couples periphery circuitry 114 to a power supply. Ex. 1003, 5:4–6, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99, 112; Ex. 2001 ¶ 63. The gate of p-channel transistor 120 receives the output of inverter 122. Ex. 1003, 5:4–6, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99, 112; Ex. 2001 ¶ 63. Inverter 122 receives as an input the ACTIVE control signal. Ex. 1003, 5:4–6, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99, 112; Ex. 2001 ¶ 63.

The ACTIVE control signal causes transistor 120 to turn on or off to control power to periphery circuitry 114. Ex. 1004 ¶ 113. When memory cell array 112 is in the active state (ACTIVE high), inverter 122 produces a low output that turns on transistor 120, thus applying power to periphery circuitry 114. Ex. 1003, 5:4–8, Fig. 6; *see* Ex. 1004 ¶ 113; Ex. 2001 ¶ 63. When memory cell array 112 is not in the active state (ACTIVE low), inverter 122 produces a high output that turns off transistor 120, thus removing power from periphery circuitry 114. Ex. 1003, 5:4–8, Fig. 6; *see* Ex. 1004 ¶ 113. Hence, logic circuit 118 selectively removes electrical connectivity between a power supply and periphery circuitry 114 depending on the ACTIVE control signal's logic level. *See* Ex. 1004 ¶ 113.

For the reasons discussed above, Houston discloses “control circuitry coupled to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the control circuitry selectively removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells,” as required by claim 15.

(f) Whether Houston Anticipates Claim 15

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that Houston discloses every element of claim 15 arranged as required by the claim, e.g., in Houston's Figures 4 and 6 and their associated disclosures. Hence, Petitioner has shown by a preponderance of the evidence that claim 15 is unpatentable under § 102(b) as anticipated by Houston.

4. WHETHER HOUSTON ANTICIPATES CLAIM 24

(a) Preamble

Claim 24's preamble recites "[a] method of power management in an integrated circuit." Ex. 1001, 12:47–48. To the extent the preamble is limiting, Petitioner asserts that Houston satisfies claim 24's preamble for the same reasons that Houston satisfies claim 15's preamble. *Compare* Pet. 30–31, *with id.* at 20–21; *see* Ex. 1004 ¶¶ 88–90.

Patent Owner disputes that Houston satisfies claim 24's preamble. *See* Resp. 27–34; Sur-reply 1–20. Specifically, Patent Owner asserts that "to anticipate claim 24, Houston must disclose a single embodiment or arrangement in which all of the steps are performed in a single substrate." Resp. 30–31. Patent Owner also asserts that "there is no single embodiment or arrangement disclosed in Houston that satisfies this claim requirement." *Id.* at 31.

Patent Owner's assertions rest on its argument that claim 24's preamble is limiting. For the reasons discussed above, we disagree with Patent Owner. *See supra* § III.B.2.

In any event, even assuming that claim 24's preamble is limiting, we agree with Petitioner that Houston satisfies this preamble. *See* Ex. 1004

¶¶ 88–90. Houston describes a method for “selectively supply[ing] power to a memory array” that “eliminates or substantially reduces” leakage current and power consumption, thus improving performance. Ex. 1003, 1:43–64; *see id.* at 2:66–3:2, code (57); Ex. 1004 ¶¶ 76, 89–90. More specifically, Houston discloses a microprocessor system for accomplishing the method that includes (1) a microprocessor; (2) on-chip memory cell arrays or memory segments, i.e., memories “exist[ing] on the same semiconductor device” as the microprocessor; and (3) on-chip switches that “controllably connect or disconnect” on-chip components to a power supply. Ex. 1003, 4:6–11, 4:32–34, Fig. 4; *see id.* at 1:65–2:13, 3:20–23, 3:30–34; Ex. 1004 ¶¶ 81, 92; Ex. 2001 ¶¶ 58–60, 92.

For the reasons discussed above, claim 24’s preamble is not limiting, but even if it were limiting, Houston discloses “[a] method of power management in an integrated circuit” according to claim 24’s preamble.

(b) The “Executing Instructions” Limitation

Claim 24 recites “executing instructions with a processor.” Ex. 1001, 12:49. Petitioner asserts that Houston satisfies this limitation for the same reasons that Houston satisfies claim 15’s “processing circuitry” limitation. *Compare* Pet. 31–32, *with id.* at 21–22; *see* Ex. 1004 ¶¶ 91–93. For example, Petitioner contends that Houston’s Figures 4 and 5 each depict microprocessor system 90 including microprocessor 92 that generates control signals. Pet. 31–32 (citing Ex. 1003, 4:6–12, 4:43–52, Figs. 4–5); *see id.* at 21–22.

Patent Owner does not dispute that Figures 4 and 5 each depict microprocessor system 90 including microprocessor 92 that generates control signals. *See* Resp. 9–11, 36; Ex. 2001 ¶¶ 58–61, 92.

We agree with Petitioner that Houston satisfies claim 24’s “executing instructions” limitation. For example, Figure 4 depicts microprocessor system 90 including microprocessor 92. Ex. 1003, 2:27–28, 4:6–12, Fig. 4; *see* Ex. 1004 ¶ 92; Ex. 2001 ¶¶ 58–60, 92. Microprocessor 92 executes instructions, e.g., to generate control signals for memory cell arrays or memory segments 96–100 to selectively connect them to or disconnect them from a power supply. Ex. 1003, 4:12–34; *see* Ex. 1004 ¶¶ 92–93; Ex. 2001 ¶ 60.

For the reasons discussed above, Houston discloses “executing instructions with a processor,” as required by claim 24.

(c) The “Providing a Plurality of Memory Bit Cells” Limitation

Claim 24 recites “providing a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane.” Ex. 1001, 12:50–53. Petitioner asserts that Houston satisfies this limitation for the same reasons that Houston satisfies claim 15’s “memory array” limitation. *Compare* Pet. 32–34, *with id.* at 22–24; *see* Ex. 1004 ¶¶ 94–101. For instance, Petitioner asserts that Houston’s Figure 6 illustrates “memory cell array 112 coupled to [a] power supply via transistor 116 to create a first power plane.” Pet. 33–34; *see id.* at 23–24.

As discussed above for claim 15’s “memory array” limitation, Patent Owner disputes that Figures 4 and 5 (each with microprocessor 92) relate to the same embodiment as Figure 6 (with memory cell array 112). *See* Resp. 29–34; Sur-reply 14–15 & n.1; Ex. 2001 ¶¶ 92–96.

We disagree with Patent Owner because, as discussed above for claim 15’s “memory array” limitation, an ordinarily skilled artisan would

reasonably understand or infer that (1) Houston's figures and their associated disclosures are "meant to be interpreted together, not viewed in vacuum," and (2) Figure 6 supplies more detail for the microprocessor systems depicted in Figures 4 and 5. *See, e.g.*, Ex. 1003, 4:6–5:13, Figs. 4–6; Ex. 1012 ¶¶ 9–27, 39–40, 48; Ex. 2011, 30:8–35:10, 36:7–9, 37:7–38:5, 45:5–47:7, 65:23–68:21; Tr. 33:14–17.

Accordingly, we agree with Petitioner that Houston satisfies claim 24's "providing a plurality of memory bit cells" limitation. For example, Figure 4 depicts microprocessor system 90 including memory cell arrays 96–100. Ex. 1003, 2:27–28, 4:6–9, Fig. 4; *see* Ex. 1004 ¶¶ 81, 95; Ex. 2001 ¶¶ 58–59. Figure 6 supplies more detail for the microprocessor system and shows a memory cell array, i.e., memory cell array 112. Ex. 1003, 4:58–60, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99; Ex. 2001 ¶ 63. The memory cell array includes a plurality of memory bit cells. Ex. 1004 ¶ 95; *see id.* ¶¶ 37–38; Ex. 2001 ¶ 37. In addition, Figure 6 depicts p-channel transistor 116 that acts as a switch and selectively couples memory cell array 112 to a power supply. Ex. 1003, 4:64–5:2, code (57), Fig. 6; *see* Ex. 1004 ¶ 99; Ex. 2001 ¶ 63. By selectively coupling memory cell array 112 to a power supply, p-channel transistor 116 creates a first power plane. Ex. 1004 ¶ 99; *see id.* ¶¶ 97–98.

For the reasons discussed above, Houston discloses "providing a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane," as required by claim 24.

(d) The “Providing Memory Array Peripheral Circuitry” Limitation

Claim 24 recites “providing memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.” Ex. 1001, 12:54–55.

Petitioner asserts that Houston satisfies this limitation for the same reasons that Houston satisfies claim 15’s “memory array peripheral circuitry”

limitation. *Compare* Pet. 34–36, *with id.* at 24–26; *see* Ex. 1004

¶¶ 102–105. For instance, Petitioner asserts that Houston’s Figure 6 depicts “periphery circuitry 114 that is peripheral to memory cell array 112.”

Pet. 34–35; *see id.* at 24–25.

Patent Owner does not dispute that Figure 6 illustrates “memory cell array 112 of a memory device and its associated periphery circuitry 114.”

Resp. 11, 36; *see* Ex. 2001 ¶ 63.

We agree with Petitioner that Houston satisfies claim 24’s “providing memory array peripheral circuitry” limitation. In particular, Figure 6 depicts periphery circuitry 114 that is peripheral to memory cell array 112.

Ex. 1003, 4:58–64, Fig. 6; *see* Ex. 1004 ¶¶ 103–104; Ex. 2001 ¶ 63.

For the reasons discussed above, Houston discloses “providing memory array peripheral circuitry that is peripheral to the plurality of memory bit cells,” as required by claim 24.

(e) The “Selectively Coupling the Memory Array Peripheral Circuitry” Limitation

Claim 24 also recites “selectively coupling the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells to the power supply terminal for creating a second power plane that is independent of the first power plane.” Ex. 1001, 12:56–60. Petitioner asserts that Houston satisfies this limitation for the same reasons that

Houston satisfies claim 15’s “memory array peripheral circuitry” limitation. *Compare* Pet. 36–38, *with id.* at 26–28; *see* Ex. 1004 ¶¶ 106–108. For instance, Petitioner asserts that Houston’s Figure 6 depicts “periphery circuitry 114 coupled to a power supply via transistor 120 to create a second power plane independent of the first power plane created by coupling the memory cell array 112 to a power supply via transistor 116.” Pet. 36–37; *see id.* at 26–27.

Patent Owner does not dispute that periphery circuitry 114 “is coupled to the power supply through a p-channel transistor 120” or that periphery circuitry 114 “is supplied power whenever the memory is in the active state.” Resp. 11–12; *see* Ex. 2001 ¶ 63.

We agree with Petitioner that Houston satisfies claim 24’s “selectively coupling the memory array peripheral circuitry” limitation. In particular, Figure 6 depicts p-channel transistor 120 that acts as a switch and selectively couples periphery circuitry 114 to a power supply. Ex. 1003, 5:4–6, Fig. 6; *see* Ex. 1004 ¶¶ 99, 107–108; Ex. 2001 ¶ 63. By selectively coupling periphery circuitry 114 to a power supply, p-channel transistor 120 creates a second power plane. Ex. 1004 ¶¶ 107–108. The second power plane created by p-channel transistor 120 is independent of the first power plane created by p-channel transistor 116. *Id.* ¶¶ 99, 107–108; *see id.* ¶ 82.

For the reasons discussed above, Houston discloses “selectively coupling the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells to the power supply terminal for creating a second power plane that is independent of the first power plane,” as required by claim 24.

(f) The “Coupling Control Circuitry” Limitation

Claim 24 further recites “coupling control circuitry to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.” Ex. 1001, 12:61–63. Petitioner asserts that Houston satisfies this limitation for the same reasons that Houston satisfies claim 15’s “control circuitry” limitation. *Compare* Pet. 38–39, *with id.* at 28–30; *see* Ex. 1004 ¶¶ 109–114. For instance, Petitioner asserts that Houston’s Figure 6 illustrates logic circuit 118 including inverter 122 and transistor 120 “coupled to periphery circuitry 114 to control power to periphery circuitry 114.” Pet. 38 (citing Ex. 1003, 4:58–5:14, Fig. 6); *see id.* at 28.

Patent Owner does not dispute that Figure 6 illustrates logic circuit 118 including “inverter 122, which receives the ACTIVE control signal, and p-channel transistor 120.” Resp. 11–12; *see* Ex. 2001 ¶ 63.

We agree with Petitioner that Houston satisfies claim 24’s “coupling control circuitry” limitation. In Figure 6, logic circuit 118 includes p-channel transistor 120 and inverter 122, and logic circuit 118 controls power to periphery circuitry 114. Ex. 1003, 5:2–6, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99, 112–113; Ex. 2001 ¶ 63. Specifically, p-channel transistor 120 acts as a switch and selectively couples periphery circuitry 114 to a power supply. Ex. 1003, 5:4–6, Fig. 6; *see* Ex. 1004 ¶¶ 82, 99, 112; Ex. 2001 ¶ 63.

For the reasons discussed above, Houston discloses “coupling control circuitry to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells,” as required by claim 24.

(g) The “Selectively Removing Electrical Connectivity” Limitation

Claim 24 also recites “selectively removing electrical connectivity to the power supply voltage terminal of the memory array peripheral circuitry

that is peripheral to the plurality of memory bit cells.” Ex. 1001, 12:64–67. Petitioner asserts that Houston satisfies this limitation for the same reasons that Houston satisfies claim 15’s “control circuitry” limitation. *Compare* Pet. 39–42, *with id.* at 28–30; *see* Ex. 1004 ¶¶ 109–114. For instance, Petitioner asserts that inverter 122 receives as an input the ACTIVE control signal that causes transistor 120 to turn on or off to control power to periphery circuitry 114. Pet. 40–42; *see id.* at 28–30.

Patent Owner does not dispute that, when “the ACTIVE control signal” in Figure 6 “is high, power is supplied to periphery circuitry 114.” Resp. 12; *see* Ex. 2001 ¶ 63.

We agree with Petitioner that Houston satisfies claim 24’s “selectively removing electrical connectivity” limitation. In Figure 6, logic circuit 118 selectively removes electrical connectivity between a power supply and periphery circuitry 114 depending on the ACTIVE control signal’s logic level. *See* Ex. 1004 ¶ 113. When memory cell array 112 is in the active state (ACTIVE high), inverter 122 produces a low output that turns on transistor 120, thus applying power to periphery circuitry 114. Ex. 1003, 5:4–8, Fig. 6; *see* Ex. 1004 ¶ 113; Ex. 2001 ¶ 63. When memory cell array 112 is not in the active state (ACTIVE low), inverter 122 produces a high output that turns off transistor 120, thus removing power from periphery circuitry 114. Ex. 1003, 5:4–8, Fig. 6; *see* Ex. 1004 ¶ 113.

For the reasons discussed above, Houston discloses “selectively removing electrical connectivity to the power supply voltage terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells,” as required by claim 24.

(h) Whether Houston Anticipates Claim 24

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that Houston discloses every element of claim 24 arranged as required by the claim, e.g., in Houston's Figures 4 and 6 and their associated disclosures. Hence, Petitioner has shown by a preponderance of the evidence that claim 24 is unpatentable under § 102(b) as anticipated by Houston.

5. WHETHER HOUSTON ANTICIPATES CLAIMS 15 AND 24 UNDER PATENT OWNER'S PROPOSED CONSTRUCTION OF "INTEGRATED CIRCUIT"

For the reasons explained below, Houston still anticipates claims 15 and 24 if the preamble term "integrated circuit" means "one or more circuit elements provided on or within a single semiconductor substrate" as Patent Owner asserts.

Patent Owner argues that for Houston to anticipate claim 15, Houston "must disclose a single embodiment or arrangement that includes (i) processing circuitry for executing instructions; (ii) a plurality of memory bit cells contained within a memory array; (iii) memory array peripheral circuitry; and (iv) control circuitry, all within a single semiconductor substrate." Resp. 30 (emphasis omitted). Similarly, Patent Owner argues that for Houston to anticipate claim 24, Houston "must disclose a single embodiment or arrangement in which all of the steps are performed in a single substrate." *Id.* at 30–31. Further, Patent Owner asserts that "no single embodiment or arrangement disclosed in Houston" includes the required circuitry or performs the required steps "on or within a single substrate." *Id.* at 30–31, 33; *see* Sur-reply 13–17.

We disagree with Patent Owner because the Figure 4 arrangement includes the required circuitry and performs the required steps “on or within a single substrate.” For Figure 4, Houston discloses memory cell arrays “on the same semiconductor device as the microprocessor.” Ex. 1003, 4:9–12; *see* Ex. 1004 ¶ 81; Ex. 2001 ¶¶ 59, 92. As discussed above for claim 15’s “memory array” limitation, a “person of ordinary skill would understand the memory arrays” in Figure 4 “to include peripheral circuitry, despite this not being explicitly shown.” Ex. 1012 ¶ 40; *see id.* ¶ 48; Tr. 33:14–17; *supra* § III.C.3(c). Thus, the Figure 4 arrangement includes peripheral circuitry “on the same semiconductor device as the microprocessor.”

In addition, Houston discloses control circuitry for the Figure 4 arrangement “on the same semiconductor device as the microprocessor,” i.e., on-chip switches that “controllably connect or disconnect” the memory cell arrays to a power supply. Ex. 1003, 4:9–34; *see* Ex. 2001 ¶ 60. And as discussed above for claim 15’s “memory array” limitation, an ordinarily skilled artisan would reasonably understand or infer that Figure 6 supplies more detail for Figure 4’s microprocessor system. *See, e.g.*, Ex. 1003, 4:6–5:13, Figs. 4–6; Ex. 1012 ¶¶ 9–27, 39–40, 48; Ex. 2011, 30:8–35:10, 36:7–9, 37:7–38:5, 65:23–68:21; Tr. 33:14–17; *supra* § III.C.3(c). Hence, Figure 6’s control circuitry for “selectively provid[ing] power independently to” a memory cell array and its peripheral circuitry also exists “on the same semiconductor device as the microprocessor.” *See* Ex. 1003, 4:58–60; 5:7–13; Ex. 2001 ¶ 63.

Accordingly, contrary to Patent Owner’s contention, the Figure 4 arrangement “includes (i) processing circuitry for executing instructions; (ii) a plurality of memory bit cells contained within a memory array;

(iii) memory array peripheral circuitry; and (iv) control circuitry, all within a single semiconductor substrate,” i.e., all circuitry “on the same semiconductor device as the microprocessor.” *See supra* §§ III.C.3(a)–(e). Further, the Figure 4 arrangement accomplishes power management with all circuitry “on the same semiconductor device as the microprocessor.” *See supra* §§ III.C.4(a)–(g). Thus, the Figure 4 arrangement anticipates claims 15 and 24 even if the preambles limit the claims as Patent Owner asserts.

For this additional reason, Petitioner has shown by a preponderance of the evidence that claims 15 and 24 are unpatentable under § 102(b) as anticipated by Houston.

*D. Obviousness over Houston:
Claims 15 and 24*

1. BACKGROUND

If our reviewing court determines that Houston’s Figures 4 and 6 relate to different embodiments, although we decide that they do not (as explained above for the anticipation ground), then Houston does not anticipate claim 15 or claim 24 because Houston does not include every element of the claim arranged as required by the claim. *See Net MoneyIN*, 545 F.3d at 1369–71; *see also Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1349–50 (Fed. Cir. 2019). As an example, Figure 4 lacks control circuitry for peripheral circuitry associated with the memory cell arrays or memory segments. *See* Ex. 1003, 2:27–28, 4:6–42, Fig. 4. As another example, Figure 6 lacks a microprocessor. *See id.* at 4:58–5:13, Fig. 6.

For the reasons explained below, however, the subject matter of claims 15 and 24 would have been obvious over Houston assuming that (1) Figures 4 and 6 relate to different embodiments, (2) the preambles limit the claims, and (3) the preamble term “integrated circuit” means “one or more circuit elements provided on or within a single semiconductor substrate” as Patent Owner asserts. Further, assuming that Figures 4 and 6 relate to different embodiments but the preambles in claims 15 and 24 do not limit the claims, the subject matter of the broader claims would have been obvious over Houston for at least the same reasons that the subject matter of the preamble-limited narrower claims would have been obvious.

2. OBVIOUSNESS UNDER 35 U.S.C. § 103

A patent may not be obtained “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). An obviousness analysis involves underlying factual inquiries including (1) the scope and content of the prior art; (2) differences between the claimed invention and the prior art; (3) the level of ordinary skill in the art; and (4) where in evidence, objective evidence of nonobviousness, such as commercial success, long-felt but unsolved needs, and failure of others.² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 35–36 (1966); *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1047–48 (Fed. Cir. 2016) (en banc).

² Patent Owner does not present arguments or evidence regarding objective evidence of nonobviousness. *See generally* Resp.; Sur-reply.

“An obviousness determination requires finding that a person of ordinary skill in the art would have been motivated to combine or modify the teachings in the prior art and would have had a reasonable expectation of success in doing so.” *Regents of Univ. of Cal. v. Broad Inst., Inc.*, 903 F.3d 1286, 1291 (Fed. Cir. 2018); *In re Stepan Co.*, 868 F.3d 1342, 1345–46 & n.1 (Fed. Cir. 2017). Thus, an obviousness analysis should address “whether there was an apparent reason” to combine or modify “known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

We analyze the obviousness issues according to these principles.

3. WHETHER THE SUBJECT MATTER OF CLAIMS 15 AND 24
WOULD HAVE BEEN OBVIOUS OVER HOUSTON

Patent Owner does not dispute that Houston’s Figure 4 depicts microprocessor system 90 including microprocessor 92 and memory cell arrays 96–100 or that Houston discloses memory cell arrays “on the same semiconductor device as the microprocessor.” *See* Resp. 9–10, 33 n.3, 36; Ex. 1003, 4:6–12, Fig. 4; Ex. 1004 ¶ 81; Ex. 2001 ¶¶ 59, 92. In addition, Patent Owner does not dispute that Houston’s Figure 6 illustrates “memory cell array 112 of a memory device,” “its associated periphery circuitry 114,” and control circuitry for “selectively provid[ing] power independently to” the memory cell array and its associated periphery circuitry. Resp. 11–12, 36; *see* Ex. 1003, 4:48–5:13, Fig. 6; Ex. 2001 ¶ 63.

According to Patent Owner, the subject matter of claims 15 and 24 differs from Houston because “Houston does not disclose all the elements of the claims implemented on a single integrated circuit.” Sur-reply 13; *see id.* at 16, 21–22; Resp. 34–37. Patent Owner faults Petitioner for failing to

show that it would have been obvious to an ordinarily skilled artisan “to modify Houston to integrate its microprocessor on the same integrated circuit as the other circuit elements, as required by claims 15 and 24.” Sur-reply 24–25; *see* Resp. 34–37.

Petitioner contends that any differences between the subject matter of claims 15 and 24 and Houston “would have been obvious modifications to Houston” that an ordinarily skilled artisan would have been “motivated to make with a reasonable expectation of success.” Pet. 43; *see* Ex. 1004 ¶ 116. Specifically, Petitioner asserts that it would have been obvious to an ordinarily skilled artisan to implement power management “within an integrated circuit.” Pet. 44; *see* Reply 17–18; Ex. 1004 ¶¶ 118–119. Petitioner also asserts that Houston “itself provides an express motivation to implement all of the claimed circuits on an integrated circuit by stating that the ‘memory cell arrays or memory segments,’ which have power management circuitry, ‘may exist on the same semiconductor device as the microprocessor.’” Reply 19 (quoting Ex. 1003, 4:9–12); *see* Ex. 1012 ¶ 53. Petitioner further asserts that “it would have been obvious to implement the circuitry disclosed in Houston on the same integrated circuit.” Reply 19.

To support its assertions, Petitioner cites testimony from Dr. Jacob and Dr. Khatri. *See* Reply 18–19 (citing Ex. 1012 ¶¶ 50–53; Ex. 1013, 17:20–18:1, 35:14–36:15, 39:19–40:13; Ex. 2001 ¶ 78); *see id.* at 4–5 (citing Ex. 1013, 12:9–13:1, 39:19–40:13).

Dr. Jacob stated that “integration has always been the driving force behind computer-system improvements over time.” Ex. 1012 ¶ 50. He explained that as “components are reduced in size and integrated into the same module, the same package, or the same die, their manufacturing cost

goes down, as does the cost of the communications between components in both time and power dissipation.” *Id.* He also explained that “performance tends to increase substantially as components are integrated, and thus, over time, one sees that items traditionally implemented in discrete components all get integrated together for cost and/or performance reasons.” *Id.*

Further, Dr. Jacob provided examples from 1995 to the early to middle 2000s of advances in integrating discrete components onto the same integrated circuit. Ex. 1012 ¶¶ 51–53 (citing Exs. 1016–1017). He stated that it would have been obvious “for a microprocessor designer to integrate onto the same integrated circuit (IC) a processor core and its [memory] caches—including the cache arrays, the cache peripheral circuits, and control circuitry for handling the power distribution.” *Id.* ¶ 53.

Consistent with Dr. Jacob, Dr. Khatri explained that the “the degree of integration has just increased” over time. Ex. 2012, 9:2–8. He also explained that “[t]he degree of integration has been increasing because, you know, that allows for more of the functionality of the design to be embedded on one, you know, on one silicon substrate.” *Id.* at 10:2–5.

Moreover, referencing the ’555 patent’s Figure 1, Dr. Khatri identified various components in integrated circuit 10, e.g., processor 18, power control register 20, array controller 22, arrays 28 and 32, hardware power control 36, multiplexers 42 and 44, and switches 56 and 58. Ex. 2001 ¶ 78. He stated that battery-powered devices as taught by the ’555 patent “would typically include all of these components on a single substrate in order to save energy, to save power and to reduce area.” *Id.* He also stated that “it would be an unnecessary waste of energy, power and area if hardware power control 36, switches 56 and 58 and MUXes 42 and 44 . . . were

provided on different substrates.” *Id.* He similarly stated that “it would expend unnecessary energy, expend unnecessary power and utilize excess area to spread” multiple power domains “across multiple substrates.” *Id.*

Also, Dr. Khatri explained that “[t]he importance of integration is known to a person of ordinary skill.” Ex. 1013, 17:18–19. He stated that “whenever it’s possible to put more of the functionality on one chip or on one integrated circuit, it’s always beneficial to do it because”: (1) “it makes the system smaller,” (2) “[i]t reduces power consumption,” (3) “[i]t reduces chip area,” and (4) “it also makes it faster.” Ex. 2012, 10:8–14. In addition, Dr. Khatri described the “motivation to integrate more and more of the function onto one integrated circuit” as “strong.” *Id.* at 10:15–17.

We agree with Petitioner that an ordinarily skilled artisan (1) would have been motivated to modify Houston to integrate its microprocessor on the same integrated circuit as the memories, the peripheral circuitry, and the control circuitry and (2) would have had a reasonable expectation of success in doing so. *See* Ex. 1004 ¶¶ 116–119; Ex. 1012 ¶¶ 50–53; Ex. 1013, 17:13–18:1, 35:14–36:15, 39:11–40:13; Ex. 2001 ¶ 78; Ex. 2012, 9:21–10:21.

Regarding a motivation to modify, Dr. Jacob and Dr. Khatri agreed that integrating Houston’s components on the same integrated circuit would have improved performance, e.g., by saving power and reducing delay. *See* Ex. 1012 ¶ 50; Ex. 1013, 35:14–36:15; Ex. 2001 ¶ 78; Ex. 2012, 9:21–10:17; *see also* Tr. 29:22–30:6. Improved performance is a reason that would have prompted a person of ordinary skill to modify Houston to integrate its microprocessor on the same integrated circuit as the memories, the peripheral circuitry, and the control circuitry. *See KSR*, 550 U.S. at 419–20.

As the Federal Circuit has “repeatedly held,” an “implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the ‘improvement’ is technology-independent” and the modification “results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.” *DyStar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006).

Regarding a reasonable expectation of success, Dr. Jacob stated that creating an integrated circuit with power management “would have been well within the powers of the person of ordinary skill.” Ex. 1004 ¶ 119. Dr. Khatri agreed that a person of ordinary skill “would be able to do this task” of integrating Houston’s components on the same integrated circuit. Ex. 1013, 39:11–40:13.

Patent Owner argues that “Petitioner ignores Dr. Khatri’s testimony that there are reasons against integrating all these circuit elements on a single integrated circuit,” e.g., different materials “used for different parts of a memory design” that require different semiconductor substrates. Sur-reply 23–24 (citing Ex. 1013, 36:3–4; Ex. 2012, 10:22–13:1). But Patent Owner references Dr. Khatri’s testimony about a few exceptions to the predominant aim to integrate components on the same integrated circuit. Ex. 2012, 10:22–13:1; *see id.* at 9:21–10:21; *see also* Ex. 2001 ¶ 78.

For instance, Dr. Khatri stated that “[i]t’s not always possible” and “[i]t’s not always practical” to integrate components on the same integrated circuit. Ex. 2012, 10:6–19. As a specific example, he explained that “there’s a physical limit on the size of a chip that we can actually fabricate”

and that trying “to put too much on the same chip” causes the chip to become too expensive and suffer from reliability issues. *Id.* at 11:21–12:11.

Here, Patent Owner does not direct us to evidence indicating that any of the few exceptions to the predominant aim to integrate components on the same integrated circuit applies to Houston. *See* Sur-reply 23–24 (citing Ex. 1013, 36:3–4; Ex. 2012, 10:22–13:1). Hence, no exception negates the motivation to modify Houston to integrate its components on the same integrated circuit.

For the reasons discussed above, an ordinarily skilled artisan (1) would have been motivated to modify Houston to integrate its microprocessor on the same integrated circuit as the memories, the peripheral circuitry, and the control circuitry and (2) would have had a reasonable expectation of success in doing so. Hence, the subject matter of claims 15 and 24 would have been obvious over Houston assuming that (1) Figures 4 and 6 relate to different embodiments, (2) the preambles limit the claims, and (3) the preamble term “integrated circuit” means “one or more circuit elements provided on or within a single semiconductor substrate” as Patent Owner asserts. Further, assuming that Figures 4 and 6 relate to different embodiments but the preambles in claims 15 and 24 do not limit the claims, the subject matter of the broader claims would have been obvious over Houston for at least the same reasons that the subject matter of the preamble-limited narrower claims would have been obvious.

Accordingly, for the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claims 15 and 24 are unpatentable under § 103(a) as obvious over Houston.

IV. CONCLUSION

Based on the evidence presented with the Petition, the evidence introduced during the trial, and the parties' respective arguments, Petitioner has shown by a preponderance of the evidence that claims 15 and 24 are unpatentable under § 102(b) as anticipated by Houston or, alternatively, that claims 15 and 24 are unpatentable under § 103(a) as obvious over Houston.³

In summary:

Claims	35 U.S.C. §	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
15, 24	102(b)	Houston	15, 24	
15, 24	103(a)	Houston	15, 24	
Overall Outcome			15, 24	

V. ORDER

Accordingly, it is

ORDERED that claims 15 and 24 of the '555 patent are determined to be unpatentable; and

³ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding after the issuance of this Final Written Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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