

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

Case IPR2019-00034
Patent 7,675,806 B2

Before ROBERT J. WEINSCHENK, MINN CHUNG, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

DECISION
Denying Petitioner's Request for Rehearing
37 C.F.R. § 42.71(d)

I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Request for Rehearing (Paper 12, “Request” or “Req. Reh’g”) of the Decision (Paper 11, “Dec.”), in which, based on the information presented, *inter alia*, in the Petition (Paper 3, “Pet.”), we denied institution of an *inter partes* review of claims 11, 12, 13, 15, and 17 (the “challenged claims”) of U.S. Patent No. 7,675,806 B2 (Ex. 1201, “the ’806 patent”). In its Request, Petitioner contends that the Decision misapprehended or overlooked Petitioner’s argument on how Schuckle (Ex. 1203) teaches certain claim limitations of claim 11. *See* Req. Reh’g 1–3, 6–12. The Request also asserts that the Decision misapprehended certain statements made in the Declaration of Bruce Jacob (Ex. 1202, “Jacob Decl.”). *See id.* at 10–12. In addition, the Request asserts that the Decision denying institution was based on a flawed claim interpretation (*see id.* at 1) of the claim term “first mode of operation” recited in claim 11 (*see id.* at 12–14).

As explained below, we have considered the arguments presented by Petitioner in its Request for Rehearing, but discern no reason to modify the Decision. Consequently, Petitioner’s Request for Rehearing is *denied*.

II. STANDARD OF REVIEW

“The burden of showing a decision should be modified lies with the party challenging the decision,” and the challenging party “must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed” in a paper of record. 37 C.F.R. § 42.71(d). Because Petitioner seeks rehearing of our Decision denying institution of trial based on the Petition, it must show an abuse of discretion. *See* 37 C.F.R. § 42.71(c) (“When rehearing a

decision on petition, a panel will review the decision for an abuse of discretion.”). An abuse of discretion occurs when a “decision was based on an erroneous conclusion of law or clearly erroneous factual findings, or . . . a clear error of judgment.” *PPG Indus., Inc. v. Celanese Polymer Specialties Co.*, 840 F.2d 1565, 1567 (Fed. Cir. 1988). With these principles in mind, we address the arguments presented in Petitioner’s Request.

III. ANALYSIS

Claim 11 recites four separate steps performed by “a processing core.” Ex. 1201, 10:47–57. These limitations are reproduced below with identifying labels used in the Petition:

(11[h]) a processing core located at the integrated circuit, the processing core operable to:

(11[i]) access the first memory and the second memory when in a first mode of operation, and (11[j]) to access the second memory but not the first memory when in a second mode of operation;

(11[k]) access the status information in the second mode of operation; and

(11[l]) enter the first mode of operation in response to the status information indicating data corresponding to the data stored at the first memory has changed.

See Pet. 59, 61, 63, 68, 69.

Based on the arguments and evidence presented in the Petition, the Decision found as follows:

Petitioner maps Schuckle’s “memory controller” (i.e., north bridge or memory controller 140)—*not* processor 110 of Schuckle—to the “processing core” recited in claim 11. [Pet.] 59–60 (citing Ex. 1203, 9:46–57, 10:12–14; Ex. 1202 (Jacob Decl.) ¶¶ 165, 167–168). Petitioner also maps the higher power state (i.e., the C0 or C1 state) of Schuckle to “a first mode of

operation” and the lower power state (i.e., the C2 or C3 state) of Schuckle to “a second mode of operation” recited in claim 11. *Id.* at 61 (citing Ex. 1203, 12:35–38 (claims 2, 3); Ex. 1202 ¶¶ 186–188), 63–64 (citing Ex. 1203, 7:4–19, 10:22–25, 10:43–48; Ex. 1202 ¶ 191).

Dec. 16–17. The Petition’s mapping of “Schuckle’s lower power state” to the claimed “second mode of operation” was based on Petitioner’s proposed construction of the claim term “second mode of operation” to mean “when a lower voltage is provided to the first and second memory.” Pet. 64; *see also id.* at 34–38 (discussing Petitioner’s proposed claim construction of the term “second mode of operation” to mean “when a lower voltage is provided to the first and second memory”). Consistent with these mappings, the Petition identified certain operations performed by Schuckle’s memory controller 140 as the steps performed by the claimed “processing core” recited in limitations 11[i], 11[j], and 11[k]. *Id.* at 61–69.

The Decision also found, based on the arguments and evidence presented in the Petition,

When it comes to limitation 11[l] (reciting “and [the processing core operable to] enter the first mode of operation in response to the status information indicating data corresponding to the data stored at the first memory has changed”), the Petition does not discuss Schuckle’s memory controller entering the first mode of operation, but instead relies on the operations of *processor 110* (rather than memory controller 140) of Schuckle to teach the step recited in limitation 11[l].

Dec. 18–19 (citing Pet. 69–70 (quoting Ex. 1203, 10:58–66, 11:44–53) (citing Ex. 1202 ¶¶ 199–200)). As also discussed in the Decision, in the cited paragraphs of his Declaration, Dr. Jacob similarly identified the operations of *processor 110* as corresponding to the step recited in

limitation 11[1]. *Id.* at 19 (quoting Ex. 1202 ¶¶ 199–200). After considering the argument and evidence presented in the Petition, we determined in the Decision that Petitioner did not demonstrate sufficiently how Schuckle’s memory controller 140 satisfies limitation 11[1] of claim 11. *Id.* at 21.

In its Request for Rehearing, Petitioner contends that the Petition did not rely on Schuckle’s processor 110 to teach limitation 11[1] but instead argued that Schuckle’s *memory controller* 140 performs the step recited in limitation 11[1]. Req. Reh’g 8–12. Specifically, the Request contends that the Petition presented the following argument:

The Petition explains that *memory controller 140*: (1) *exits the second mode of operation* (during which processor 110 and its L2 cache memory are inaccessible because they are in a “lower power” state); and (2) *enters into the first mode of operation* (during which processor 110 and its L2 cache memory are accessible because they are in a “higher power” state) when a cache tag status bit (“status information”) stored in the mirror tag memory indicates that data stored in the L2 cache memory (“first memory”) has changed.

Id. at 8 (emphases added). But the Request does not cite, nor do we discern, where in the Petition this argument was presented.

Although the Request cites page 69 of the Petition as allegedly showing that “*memory controller 140* ‘enter[s] the first mode of operation in response to the status information indicating data corresponding to the data stored at the first memory has changed,’ just as limitation 11[1] requires,” we find no such showing in the cited portion of the Petition. *See id.* (emphasis added) (citing Pet. 69–70).

Petitioner's discussion of limitation 11[l] in the cited portion of the Petition is reproduced below in its entirety:

As explained above for limitation 11[k], the memory controller accesses the status bit to determine whether the requested cache line from the L2 cache has been modified. *See* Section IX.A.1.k.

Schuckle further discloses that if the status bit indicates that the cache line has been modified, *the processor will exit the lower power state, thus returning to the higher power state.* Schuckle (EX1203) at 10:58–66 (“Access to a modified cache line would generally require that *processor 110* be enabled to *exit the lower power state . . .*”); 11:44–53 (“As described earlier, a status bit in the cache tag is set up to indicate whether the cache line has been modified. If it is determined the cache line is modified . . . then the program control is transferred to step 3404. . . . In step 3404, *processor 110* is enabled to *exit the low power state* since a snoop hit has occurred.”); Fig. 3B.

Thus, Schuckle teaches *entering into the higher power state (“first mode of operation”)* in response to the status bits in the mirror tag (“status information”) indicating that the data in the L2 cache has been modified (“data corresponding to the data stored at the first memory has changed”). Jacob-Decl. (EX1202) ¶¶199-200.

Pet. 69–70 (emphases added). As shown in the paragraphs reproduced above, nowhere in the cited passages did the Petition explain that “*memory controller 140 . . . exits the second mode of operation . . . and enters into the first mode of operation,*” as the Request contends. *See* Req. Reh’g 8 (emphases added). Instead, the Petition mapped “the higher power state” of Schuckle’s processor to the claimed “first mode of operation” (Pet. 69 (“the higher power state (‘first mode of operation’)”)), and argued that “[Schuckle’s] processor . . . *return[s] to the higher power state*” when “*processor 110 exit[s] the lower power state*” (*id.* (emphases added) (citing Ex. 1203, 10:58–66, 11:44–53)).

In the cited paragraphs of his Declaration, Dr. Jacob similarly identified “the higher power state” of Schuckle’s processor 110 as the claimed “first mode of operation” and opined as follows:

Schuckle discloses that, *while Processor 110 (not the same as the claimed “processing core”) is in low-power mode, corresponding to the claimed second mode of operation, Processor 110 can be brought out of low-power mode and back into the claimed first mode of operation*, if the cache-coherence operation warrants.

Ex. 1202 ¶ 199 (emphases added).

Schuckle allows the cache-coherence engine to access the Mirror Tag while the *Processor 110 is asleep, in the claimed second mode*. If the Mirror Tag’s address and status bits (including dirty bit) indicate that (a) *the processor’s caches* contain a copy of the target of the coherence message currently on the bus, and (b) the data in the targeted block has been modified, then *the Processor 110 must wake up* and respond to the coherence message by accessing its caches, thus *bringing the processor back into the claimed first mode of operation*. Thus, Schuckle satisfies [limitation 11[1]].

Id. ¶ 200 (emphases added).¹

As discussed above, the Petition similarly mapped “Schuckle’s lower power state” to the claimed “second mode of operation” based on Petitioner’s proposed claim construction of the term “second mode of

¹ The “processor” mentioned in part (b) of the quoted sentence in paragraph 200 of the Jacob Declaration appears to refer to the main processor of Schuckle, i.e., processor 110, because, among other reasons, part (a) of the same sentence mentions “the processor’s caches” as “contain[ing] a copy of the target of the coherence message currently on the bus.” See Ex. 1202 ¶ 200. As described in Schuckle, the main processor, i.e., processor 110, includes a cache (L2 cache 115), whereas memory controller 140 includes a mirror tag (mirror tag 142). Ex. 1203, 4:33–46, 5:2–6, Fig. 1.

operation” to mean “when a lower voltage is provided to the first and second memory.” Pet. 64; *see also id.* at 68 (mapping Schuckle’s “low power state” to the claimed “second mode of operation” when addressing limitation 11[k] (“during the low power state (‘second mode of operation’)”). As discussed in the Decision, Dr. Jacob in his Declaration acknowledged that Schuckle’s memory controller does “not enter” a “low-power mode,” but instead remains in a higher power state at all times. Dec. 21–22 (citing Ex. 1202 ¶ 167); *see* Ex. 1202 ¶ 167. In other words, Petitioner conceded in the Petition that Schuckle’s memory controller does *not* have a “low power state,” which the Petition mapped to the claimed “second mode of operation.” Thus, the record shows that the Petition did not map the claimed “second mode of operation” to a state of Schuckle’s memory controller 140. Nor was there any explanation in the Petition of how “memory controller 140 . . . *exits the second mode of operation*,” contrary to what the Request contends. *See* Req. Reh’g 8 (emphasis added).

Based on the foregoing and our review of the record, we find that the argument in the Request that Schuckle teaches limitation 11[l] because “[Schuckle’s] *memory controller 140 . . . (1) exits the second mode of operation . . . and (2) enters into the first mode of operation . . . when a cache tag status bit (‘status information’) stored in the mirror tag memory indicates that data stored in the L2 cache memory (‘first memory’) has changed*” was not included in the Petition and, therefore, is a new argument presented for the first time in the Request. *See* Req. Reh’g 8 (emphasis added). Indeed, as discussed above, the Request does not cite where in the Petition this argument was presented.

We could not have misapprehended or overlooked arguments or evidence that were not presented or developed in the Petition.

At best, Petitioner's arguments in its Request attempt to remedy the deficiencies in the Petition our Decision identified, by supplementing the arguments in the Petition. A request for rehearing is not a supplemental petition. Nor is it an opportunity to present new arguments or evidence that could have been presented and developed in the first instance in the Petition.

In the Request, Petitioner further argues that “in connection with limitation 11[1], Petitioner had *referenced the power state of processor 110 and L2 cache simply to refer to the corresponding mode of operation for memory controller 140*—which the Petition had already explained in detail for earlier limitations 11[i], [j], and [k].” Req. Reh'g 10 (emphases added). According to the Request, “[i]n connection with limitations 11[i] and [j], Petitioner explained that the power state (and, thus, accessibility) of processor 110 and the L2 cache is what *determines whether the memory controller 140 is in the first mode of operation or the second mode of operation.*” *Id.* at 9 (emphasis added) (citing Pet. 61).

Petitioner mischaracterizes the record because this argument was not presented in the Petition. Instead, the Petition asserted that the claimed “first mode of operation” is present in Schuckle “in the form of a *higher power state*,” which “*corresponds to the Advanced Configuration and Power Interface (‘ACPI’) states C0 and C1.*” Pet. 61 (emphasis added). As described in Schuckle, the ACPI states C0 and C1 are the states of *processor 110*, not memory controller 140. Ex. 1203, 5:40–6:40. There was no indication in the Petition that Petitioner mentioned the power state of

processor 110 “to refer to the corresponding mode of operation for memory controller 140.” *See* Pet. 61, 69–70.

The cited portion of the Petition also did *not* include the argument that “the power state (and, thus, accessibility) of processor 110 and the L2 cache” is *what determines* “whether the memory controller 140 is in the first mode of operation or the second mode of operation.” *See id.* at 61; Req. Reh’g 9 (citing Pet. 61). Instead, the Petition stated “[d]uring the higher power state, the memory controller (the ‘processing core’) is operable to access both the L2 cache (the ‘first memory’) and the mirror tag (the ‘second memory’).” Pet. 61. In other words, the Petition presented an argument how the operation of Schuckle’s memory controller allegedly satisfies the claim language of limitation 11[i], but there was no argument in the Petition that the memory controller’s access to L2 cache and mirror tag *determines* whether the memory controller is in the first mode of operation. *See id.*

The Request also asserts that the Decision misapprehended or overlooked Dr. Jacob’s testimony in the Jacob Declaration (Ex. 1202) allegedly providing the following explanation:

in Schuckle’s system, the mode of operation for memory controller 140 turns on the corresponding power state of processor 110 and its L2 cache—such that *memory controller 140 is in a first mode of operation* when processor 110 and its L2 cache are in a “higher power” state (and thus accessible to memory controller 140), and *in a second mode of operation* when processor 110 and its L2 cache are in a “lower power” state (and thus inaccessible to memory controller 140).

Req. Reh’g 11 (emphases added) (citing Ex. 1202 ¶ 191). Petitioner mischaracterizes the record because the cited paragraph of the Jacob

Declaration did not include such an explanation. Instead, Dr. Jacob stated as follows:

Schuckle discloses a mode of operation in which the second memory is accessible, but the first memory is not. Schuckle describes how *the Processor* can be *in low-power mode* and is unavailable to participate in handling cache-coherence messages from the rest of the system. *In this mode*, the memory controller and cache-coherence hardware, the claimed processing core, handle all coherence operations (“snoop” operations) on behalf of the Processor, by looking in the Mirror Tag 142, the claimed second memory, held in the memory controller 150.

Ex. 1202 ¶ 191 (emphases added). As shown above, Dr. Jacob discussed Schuckle’s processor, i.e., processor 110, being in the “low-power mode” and explained that “[i]n this mode,” i.e., when processor 110 is in the “low-power mode,” the memory controller handles “all coherence operations . . . on behalf of the Processor, by looking in the Mirror Tag 142 . . . held in the memory controller [140].” *Id.* In other words, Dr. Jacob simply described the operation of Schuckle’s memory controller when processor 110 is in the low-power mode. Contrary to what the Request alleges, Dr. Jacob did *not* explain “*memory controller 140 is in a first mode of operation* when processor 110 and its L2 cache are in a ‘higher power’ state . . . and *in a second mode of operation* when processor 110 and its L2 cache are in a ‘lower power’ state” in the cited paragraph of the Jacob Declaration. *Compare* Req. Reh’g 11 (emphases added), *with* Ex. 1202 ¶ 191. Indeed, the Request does not identify where in his Declaration Dr. Jacob provided such an explanation.

Next, the Request contends that the Decision misapprehended or overlooked “the Petition’s explanation that memory controller 140 meets [limitation 11[1]] by entering the first mode of operation when processor 110

and its L2 cache become accessible due to a transition of processor 110 and L2 cache from the ‘lower power’ to ‘higher power’ state.” Req. Reh’g 11–12. But the Request does not cite where in the Petition such an argument or explanation was presented.

Again, we could not have misapprehended or overlooked arguments or evidence that were not presented or developed in the Petition.

Nonetheless, the Request asserts that the Petition showed Schuckle’s memory controller 140 meets limitation 11[1] under the plain meaning of the claim language because

memory controller 140 gains access to the L2 cache memory—and thus enters the first mode of operation—when controller 110 and its L2 cache become available after they transition from a lower power to higher power state (due to the cache tag status bit indicating that data stored in the second (mirror tag) memory has changed).

Req. Reh’g 14. The Request contends that the claim language of claim 11 provides the plain meaning of the terms “first mode of operation” and “second mode of operation,” which the Request asserts is “the ‘processing core’ is in a ‘first mode of operation’ when it can ‘access’ both the first and second memories, and in a ‘second mode of operation’ when it can only ‘access’ the second memory.” *Id.* at 13. In other words, the Request asserts that the plain meaning of “first mode of operation” is “when the processing core can access both the first and second memories” and the plain meaning of “second mode of operation” is “when the processing core can only access the second memory.” *Id.*

Again, the Request does not identify where in the Petition such a claim construction argument was presented. Nor does it identify where in the Petition was the argument predicated on such claim construction (that is,

Schuckle's memory controller 140 "enters the first mode of operation" when the memory controller "can access both the first and second memories") presented. As discussed below, our review of the record shows that those arguments were not presented in the Petition.

In the Claim Construction section of the Petition, Petitioner discussed claim construction for only one term, "second mode of operation" recited in claim 11. *See* Pet. 34–38. There was no discussion of claim construction of the term "first mode of operation." *See id.* There was also no discussion of the purported plain meaning of the term "first mode of operation" in the Petition's discussion of limitation 11[i] and limitation 11[l], the limitations of claim 11 that include the term "first mode of operation." *See id.* at 61–63, 69–70.

In addition, a comparison of Petitioner's claim construction arguments on "second mode of operation" set forth in the Petition and the Request shows that the Request presents a new claim construction argument that was not included in the Petition. In the Petition, Petitioner argued that the claim term "second mode of operation" recited in claim 11 should be construed to mean "when a lower voltage is provided to the first and second memory." *Id.* at 34. Now, in the Request, Petitioner asserts that "second mode of operation" means "when the processing core can only access the second memory." Req. Reh'g 13.

But the Petition did not assert that the recited "second mode of operation" is a mode of operation for the "processing core." *See* Pet. 34–38. The claim construction discussion in the Petition did not even mention the term "processing core." *See id.* Petitioner's proposed construction of "second mode of operation" in the Petition—"when a lower voltage is

provided to the first and second memory”—suggests that the recited “second mode of operation” is a mode of operation for the first and/or second memory. Indeed, the Petition’s citations to the Specification relate to the operating voltages of the first and second memories. *See id.* at 37–38 (citing Ex. 1201, 1:60–66, 7:37–41). At a minimum, there was nothing in the claim construction discussion in the Petition that indicated that the “second mode of operation” is limited to the mode of operation for the “processing core.” Thus, by arguing that the plain meaning of “second mode of operation” is “when the processing core can only access the second memory,” the Request presents a different claim construction of “second mode of operation” from the construction proposed in the Petition.

Contrary to Petitioner’s contention in the Request, the record shows that there was nothing in the Petition that indicated that Petitioner was relying on the plain meaning interpretation of the term “second mode of operation” as “when the processing core can only access the second memory” and the plain meaning interpretation of the term “first mode of operation” as “when the processing core can access both the first and second memories.” Thus, the record shows that the purported plain meaning interpretation of the term “first mode of operation” was not presented in the Petition, but, rather, is presented for the first time in the Request in this proceeding.

Consequently, the Petition did not include (and could not have included) the unpatentability argument based on this newly presented construction—i.e., Schuckle’s memory controller 140 “enters the first mode of operation” when the memory controller can access both the first and second memories. *See* Req. Reh’g 2–3, 12–14.

Because the Request presents new (and insufficiently developed) claim construction arguments that were not presented in the Petition, we decline to consider Petitioner's proposed constructions of "first mode of operation" and "second mode of operation" newly presented in the Request, as well as the new unpatentability arguments in the Request that are based on those new constructions.

In the Request, Petitioner contends that the Decision relied on an erroneous claim construction of the claim term "first mode of operation" in determining that the Petition did not demonstrate sufficiently how Schuckle's memory controller performs the step recited in limitation 11[1]. Req. Reh'g 12–14. In particular, the Request contends that the Decision erred by disregarding the purported plain meaning interpretation of the term "first mode of operation" as "when the processing core can access both the first and second memories" and misapprehended Petitioner's argument in the Petition on how, under that claim construction, Schuckle's memory controller 140 teaches limitation 11[1]. *Id.* But, as discussed above, neither the purported plain meaning construction nor the unpatentability argument based on such construction was presented in the Petition. Again, we could not have misapprehended or overlooked arguments or evidence that were not presented or developed in the Petition.

To the extent the Request contends that, even if the newly presented plain meaning construction argument was not included in the Petition, the Decision should have interpreted "first mode of operation" according to the purported plain meaning construction of the term presented in the Request (*see id.* at 12–13 & n.2) and failing to do so was "error and an abuse of discretion" (*id.* at 14), we disagree. Among other reasons, it was Petitioner's

affirmative duty to explain in the Petition how the challenged claims should be construed and how, as so construed, they are unpatentable. *See* 37 C.F.R. § 42.104(b)(3)–(4). Thus, had Petitioner intended to rely on the purported plain meaning construction of “first mode of operation” as “when the processing core can access both the first and second memories” and argue, under that claim construction, Schuckle’s memory controller 140 teaches limitation 11[1], such an analysis should have been set forth explicitly in the Petition.

It was Petitioner’s burden to demonstrate sufficiently in the Petition that the cited prior art renders the challenged claims unpatentable, including showing that the Petition’s contentions are supported by evidence. *See* 35 U.S.C. § 314(a); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (“In an IPR, the petitioner has the burden *from the onset* to show *with particularity* why the patent it challenges is unpatentable.” (emphases added)) (citing 35 U.S.C. § 312(a)(3)); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (requiring “*the initial petition* identify ‘*with particularity*’ the ‘evidence that supports the grounds for the challenge to each claim.’” (emphases added)).

The record shows that, rather than overlooking or misapprehending any argument or evidence in the Petition, the Decision simply considered the arguments and explanations of the evidence Petitioner presented in the four corners of the Petition, and properly determined that the Petition did not meet the burden required on Petitioner for institution of an *inter partes* review.

IV. CONCLUSION

For the foregoing reasons, Petitioner has not demonstrated that we abused our discretion or that we misapprehended or overlooked any matter in our Decision denying institution of *inter partes* review of the challenged claims of the '806 patent. Petitioner, therefore, has not carried its burden of demonstrating that the Decision denying institution should be modified. *See* 37 C.F.R. § 42.71(d).

V. ORDER

Accordingly, it is ORDERED that Petitioner's Request for Rehearing is DENIED.

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