

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

IPR2019-00104
Patent 6,127,875

Before MICHELLE N. WORMMEESTER, GARTH D. BAER, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

WORMMEESTER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Kingston Technology Company, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–3 of U.S. Patent No. 6,127,875 (Ex. 1001, “the ’875 patent”). North Star Innovations, Inc. (“Patent Owner”) did not file a Preliminary Response. *See* Paper 6 (Waiver of Patent Owner’s Preliminary Response). Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review of challenged claims 1–3 based on all grounds presented in the Petition. Paper 7 (“Inst. Dec.”). Patent Owner filed a Response (Paper 12, “PO Resp.”), Petitioner filed a Reply (Paper 25, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 29, “PO Sur-reply”). On January 16, 2020, we conducted an oral hearing. A copy of the transcript (Paper 31, “Tr.”) is included in the record.

We have jurisdiction under 35 U.S.C. § 6(b). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–3 of the ’875 patent are unpatentable. This final written decision is issued pursuant to 35 U.S.C. § 318(a).

II. BACKGROUND

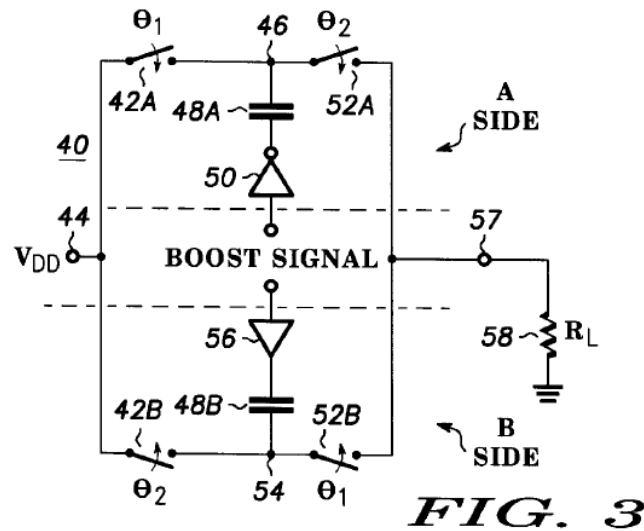
A. Related Proceedings

The parties identify two related federal district court cases. Pet. 2; Paper 3, 1. The parties also identify several related petitions for *inter partes* review. Pet. 2; Paper 3, 1.

B. The ’875 Patent

The ’875 patent describes a voltage-boosting circuit, which provides an output voltage that is greater than the supplied input voltage. Ex. 1001,

1:5–9. Figure 3, which is reproduced below, illustrates an example of a boosting circuit according to the '875 patent. *Id.* at 2:3–4, 2:18–20.



In particular, Figure 3 shows double-pumping voltage-boosting circuit 40, which has an A side and a B side. *Id.* at 2:20–23. Supply voltage V_{DD} is applied to terminal 44. *Id.* at 2:25–26. Switches 42A and 42B connect supply voltage V_{DD} to respective terminals 46 and 54 when closed, and disconnect terminal 44 from terminals 46 and 54 when opened. *Id.* at 2:24–28. The A side of circuit 40 additionally includes capacitor 48A, which is connected between terminal 46 and the output of inverting buffer driver 50. *Id.* at 2:28–30. Similarly, the B side of circuit 40 includes capacitor 48B, which is connected between terminal 54 and non-inverting buffer driver 56. *Id.* at 2:31–33. Terminals 46 and 54 are connected via respective switches 52A and 52B to output 57 of circuit 40, which is connected to load 58. *Id.* at 2:33–36. A voltage boost signal is applied to the inputs of buffer drivers 50 and 56. *Id.* at 2:36–37.

To help explain how circuit 40 operates, Figure 2A is reproduced below. *Id.* at 2:1–2.

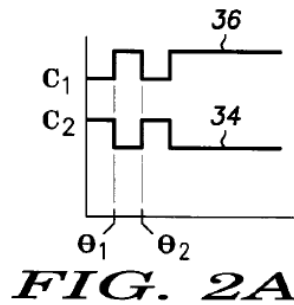


Figure 2A shows non-overlapping clock signals C1 and C2 (or clocking signals 34 and 36) that are 180 degrees out of phase with each other. *Id.* at 1:32–34, 2:39.

During first half cycle Θ_1 of clocking signals 34 and 36, switches 42A and 52B are closed, while switches 42B and 52A are opened. *Id.* at 2:38–40. Assuming that capacitor 48B has already been charged to V_{DD} during a previous half cycle, when switch 52B is closed, the boost signal changes to a high-level state, boosting the voltage across capacitor 48B to nearly $2V_{DD}$ to drive into load 58. *Id.* at 2:40–46. As current from capacitor 48B flows into load 58, the charge across capacitor 48B starts to decrease. *Id.* at 2:46–57. At the same time, capacitor 48A is being charged to V_{DD} . *Id.* at 2:54–56. Conversely, during second half cycle Θ_2 , switches 42B and 52A are closed, while switches 42A and 52B are opened. *Id.* at 2:56–58. The boost signal also changes from the high-level state to a low-level state, boosting the voltage across capacitor 48A. *Id.* at 2:58–59. As the voltage across capacitor 48A is boosted, the A side of circuit 40 drives load 58 with a voltage nearly equal to $2V_{DD}$, while V_{DD} is applied across capacitor 48B. *Id.* at 2:59–63. Thus, during the initiation of both half cycles, the voltage drive into load 58 is raised to nearly $2V_{DD}$. *Id.* at 2:63–65.

C. Illustrative Claim

Petitioner challenges claims 1–3 of the ’875 patent. Claim 1 is independent and illustrative of the challenged claims:

1. A boost circuit having an input terminal and an output terminal, comprising:
 - a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;
 - a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;
 - a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and
 - a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.

D. Asserted Grounds of Unpatentability

Petitioner challenges claims 1–3 of the ’875 patent on one ground of anticipation under 35 U.S.C. § 102 and on one ground of obviousness under 35 U.S.C. § 103.¹ Pet. 4, 30–72. We instituted *inter partes* review of both grounds. Inst. Dec. 27. The instituted grounds are as follows.

Claims Challenged	35 U.S.C. §	Reference
1–3	§ 102	Chern ²
1–3	§ 103	Chern

¹ The Leahy-Smith America Invents Act (“AIA”) amended 35 U.S.C. §§ 102 and 103. *See* Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011). As the application that issued as the ’875 patent was filed before the effective date of the relevant amendments, the pre-AIA version of §§ 102 and 103 apply.

² Chern, U.S. Patent No. 5,126,590, issued June 30, 1992 (Ex. 1005).

In support of the instituted grounds, Petitioner relies on a Declaration (Ex. 1003) as well as a Reply Declaration (Ex. 1020) of Bruce Jacob, Ph.D. With its Response, Patent Owner submits a Declaration of Sunil Khatri, Ph.D. (Ex. 2001). The transcripts of the depositions of Dr. Jacob and Dr. Khatri are entered in the record as Exhibit 2014 and Exhibit 1019, respectively.

III. ANALYSIS

A. Claim Construction

The '875 patent expired on August 13, 2018, twenty years from its filing date of August 13, 1998. Ex. 1001, code (22); *see also* Pet. 23; PO Resp. 27. For claims of an expired patent, the Board applies the claim construction standard applied by district courts, where claim terms are generally given the ordinary and customary meaning that they would have to a person of ordinary skill in the art in question at the time of the invention. *See Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1376 (Fed. Cir. 2019); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). In particular, we apply the claim construction standard from *Phillips*.

To determine a claim term's ordinary and customary meaning as would be understood by one of ordinary skill in the art, we look to the claims, the specification, the prosecution history, and even extrinsic evidence, including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–1317. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term.

Id. at 1315. A “claim construction that excludes [a] preferred embodiment [described in the specification] is rarely, if ever, correct and would require highly persuasive evidentiary support.” *Adams Respiratory Therapeutics, Inc. v. Perrigo Co.*, 616 F.3d 1283, 1290 (Fed. Cir. 2010) (citation omitted). But “a claim construction must not import limitations from the specification into the claims.” *Douglas Dynamics, LLC v. Buyers Prods. Co.*, 717 F.3d 1336, 1342 (Fed. Cir. 2013).

Petitioner and Patent Owner propose constructions for various claim terms. Pet. 23–26; PO Resp. 30–45. For purposes of this Decision, we address the claim terms “a second phase signal that is opposite to the first phase signal,” “boost signal,” “coupled for receiving,” “inverting buffer,” and “non-inverting buffer.” See *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

1. “a second phase signal that is opposite to the first phase signal”

This term appears in claim 1. Patent Owner argues that an ordinarily skilled artisan “would have understood the plain and ordinary meaning of the phrase ‘a second phase signal that is opposite [to] the first phase signal’ to mean that ‘the first phase signal and second phase signal are inverted versions of each other, such that the time during which the first phase signal is high is equal to the time during which the second phase signal is low and vice-versa.’” PO Resp. 31 (emphasis omitted). As support, Patent Owner asserts that “in the ’875 patent, voltage boosting circuit 40 includes

switch 42A (a ‘first switch’) that is operated by a first phase signal (corresponding to C₂ in FIG. 2A), and switch 42B (a ‘second switch’) that is operated by a second phase signal (corresponding to C₁ in FIG. 2A).” *Id.* (citing Ex. 1001, Fig. 3). According to Patent Owner, Figure 2A of the ’875 patent “shows that the C₂ and C₁ signals are opposite one another such that when C₂ falls to a low state, C₁ rises to a high state, and when C₂ rises to a high state, C₁ falls to a low state,” where “the duration of the high state of C₂ equals the duration of the low state of C₁ and the duration of the low state C₂ equals the duration of the high state of C₁.” *Id.* at 31–32. Patent Owner further directs us to various patents that characterize signals as having “opposite” phases, where one signal falls to a low state (or rises to a high state) for a duration while at the same time another signal rises to a high state (or falls to a low state) for the same duration. *Id.* at 32–37 (citing Ex. 2003, 10:3–11, Fig. 5; Ex. 2004, 4:44–49, Fig. 6; Ex. 2005, Figs. 1, 2(A)–2(D)). Patent Owner relies on the declaration testimony of Dr. Khatri. *Id.* at 31–37 (citing Ex. 2001 ¶¶ 102, 104–109).

Petitioner responds that “Patent Owner’s position is based entirely on construing the term ‘opposite’ to mean ‘inverted,’” and argues that “Patent Owner’s narrowing definition should be rejected for numerous reasons.” Pet. Reply 2. In particular, Petitioner argues that Patent Owner’s proposed construction should be rejected because it is “contrary” to “what has commonly been understood by ‘opposing’ clock signals in the art; namely, ‘two clocks signals that are not high at the same time,’ so that they ‘work in opposition to each other.’” *Id.* at 2–3. Petitioner asserts that “the ’875 Patent describes operating switches of a voltage boosting circuit, as ‘illustrated in FIGS. 1, 2, and 2A,’ using ‘a pair of ***non-overlapping*** clock

signals C1 and C2, which are *180 degrees out of phase* with respect to one another.” *Id.* at 3 (citing Ex. 1001, 1:23–34). According to Petitioner, “[t]his means that these ‘opposite,’ or ‘non-overlapping,’ signals control switches so that ‘one pair should be closed while the other pair is open.’” *Id.* More specifically, Petitioner asserts, each signal “closes its corresponding switch while high and opens it while low, and so the two signals work ‘opposite each other, in that each closes its switch (makes it conductive) only when the other signal has its switch open.’” *Id.* Petitioner further directs us to various patents that describe non-overlapping clock signals that are 180 degrees out of phase with respect to each other, but that are not necessarily inversions of each other and do not necessarily have a 50/50 duty cycle. *Id.* at 4–8 (citing Ex. 1023, 6:56–7:3, Figs. 5(c), 5(d); Ex. 1024, 4:41–58, Figs. 1(c), 1(d), 2; Ex. 1025, 2:57–4:8, Figs. 2, 3); *see* PO Sur-reply 12 (explaining that “signals . . . are not 50% duty cycle, in that the durations of their high and low states are unequal.”). Petitioner contends that construing the claims to require the phase signals to be inversions of each other “would exclude the customary meaning of ‘non-overlapping’ clock signals, which, . . . is the only description that the specification of the ’875 Patent provides for timing signals C₁ and C₂,” and, in turn, “would exclude not only a preferred embodiment, but the only description of the timing relationship provided in the ’875 Patent.” Pet. Reply 8. Petitioner relies on the declaration testimony of Dr. Jacob. *Id.* at 3–8 (citing Ex. 1020 ¶¶ 13, 17–21, 34–39).

Petitioner further argues that “Patent Owner’s proposed construction is also incorrect because Patent Owner seeks to limit the term ‘opposite’ to the stylized timing shown in Figure 2A of the ’875 Patent,” even though the

'875 patent “describes that the clock signals C_1 and C_2 . . . in Figure 2A are ‘non-overlapping’ and are ‘180 degrees out of phase with respect to one another.’” *Id.* at 9 (citing Ex. 1001, 1:23–35). Petitioner contends that this description “just means that the clock signals in the '875 Patent are never high at the same time and are phase shifted by 180 degrees, not that they are inverted.” *Id.* at 9–10. Petitioner also adds that “because the '875 Patent chose to use the broader term, ‘opposite,’ rather than the narrower term ‘inverted,’ Patent Owner’s construction is unduly limiting and not supported by the intrinsic evidence.” *Id.* at 10. Petitioner relies on the declaration testimony of Dr. Jacob. *Id.* (citing Ex. 1020 ¶¶ 15–33).

Lastly, Petitioner argues that Patent Owner’s proposed construction “should also be rejected because it is uncontested that Figure 2A just shows sequencing, but not realistic timing behavior.” *Id.* at 10–11. Petitioner asserts that “timing signals like C_1 and C_2 shown in Figure 2A of the '875 Patent cannot have sharp edges, as depicted, because such unrealistic timing would not allow one switch to close before the other switch is fully open, as discussed and claimed in the '875 Patent.” *Id.* at 11; *see also id.* at 12 (“[T]he sharp edges in Figure 2A . . . are not accurate, because it is not possible for current to immediately shut-off or turn-on.”). Petitioner relies on the declaration testimony of its declarant Dr. Jacob as well as the deposition testimony of Patent Owner’s declarant Dr. Khatri. *Id.* at 11–14 (citing Ex. 1019, 58:6–59:17; Ex. 1020 ¶¶ 181–192, 202).

Patent Owner counters that Petitioner impermissibly changes its claim construction theory. PO Sur-reply 3. Pointing first to the Petition, Patent Owner asserts that “Petitioner explained specifically what it meant when it alleged that [Chern’s signals ϕ_3 and ϕ_4] were ‘opposite to’ each other,”

namely, that “‘clock $\phi 3$ and clock $\phi 4$ are the same signal, shifted 180 degrees (half a clock cycle) relative to one another,’ such that, ‘when clock $\phi 3$ is high, clock $\phi 4$ is low, and that when clock $\phi 3$ is low, clock $\phi 4$ is high.’” *Id.* (quoting Pet. 39) (emphasis omitted). Pointing next to Petitioner’s Reply, Patent Owner asserts that “Petitioner and Dr. Jacob now contend that it is only necessary that the two phase signals not both be high at the same time, such that they ‘work in opposition to each other.’” *Id.* at 5 (quoting Pet. 3³) (emphasis omitted). Patent Owner alleges that Petitioner has “come up with a new theory and new claim construction” because Patent Owner “showed that during two different time intervals . . . , when $\phi 3$ is low, $\phi 4$ is also low.” *Id.* at 4 (citing PO Resp. 48–49).

Patent Owner further argues that “Petitioner’s new arguments regarding ‘opposite’ phase signals are wholly contrary to the ’875 claims and specification, and impermissibly broaden the scope of the claims beyond what is described in the specification.” *Id.* at 6. As support, Patent Owner points to various patents showing that the term “non-overlapping” may refer to inverted signals with 50% duty cycle. *Id.* at 8–11 (citing Ex. 2010, 5:54–55, Fig. 5; Ex. 2011, 4:23–25, Fig. 4; Ex. 2012, 1:31–43, Fig. 2). Patent Owner directs us to the particular teaching that “clock signals that do not have mutually opposite phases” may “divide their respective high or low states into unequal intervals,” and, “while [the] clock signals . . . preferably do not overlap, their rise and fall times may be unsynchronized.” *Id.* at 11–

³ Patent Owner cites page 3 of the Petition, but the quoted language appears at page 3 of Petitioner’s Reply.

12 (citing Ex. 2012, 3:26–33).⁴ According to Patent Owner, this teaching “distinguishes the non-overlapping *inverted* signals such as those disclosed by the ’875 patent from the non-overlapping *non-inverted* signals And it is only the non-overlapping *inverted* signals that [this teaching] describes as ‘opposite.’” *Id.* at 12.

Patent Owner adds, “While neither the claims nor the specification use the word ‘inverted,’ the entire ’875 patent makes clear that ‘opposite’ signals are signals that are inverted versions of each other.” PO Sur-reply 12–13. In particular, Patent Owner contends that “during each half cycle, two switches are closed while the other two are opened.” *Id.* As support, Patent Owner directs us to where the ’875 patent teaches that “in operation, during the first half cycle, Θ_1 , of the clocking signals 34 and 36, switches 42A and 52B are closed while switches 42B and 52A are opened,” and that “during the second half cycle, Θ_2 , switches 42B and 52A are closed while switches 42A and 52B are opened. *Id.* (quoting Ex. 1001, 2:38–40, 2:56–58). Patent Owner also directs us to where the ’875 patent teaches that “either capacitive device 48A or capacitive device 48B is driving load 58 *at all times.*” *Id.* (quoting Ex. 1001, 3:3–7) (emphasis added by Patent Owner). Patent Owner contends that “[t]he only way that the 875 circuit can operate as described by the patent is if the phase signals that operate the switches are inverted from each other, such that all four switches are never open at the same time.” *Id.* at 14; *see also id.* at 15 (“If there are intervals of time when

⁴ We note that Exhibit 2012 is extrinsic evidence, namely, a U.S. patent with a filing date of March 29, 1999, which is later than the ’875 patent’s filing date of August 13, 1998.

all the switches are open at the same time, then during those time intervals, no voltage will be driven to the output.”).

Based on the record before us, we determine that Patent Owner’s proposed construction improperly requires the first and second phase signals to be *inverted versions* of each other. Even if “[t]he only way that the 875 circuit [in Figure 3] can operate as described by the patent is if the phase signals that operate the switches are inverted from each other,” as Patent Owner contends, the specification “is not a substitute for, nor can it be used to rewrite, the chosen claim language.” *See* PO Resp. 14–15; *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004); *see also Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (expressly rejecting “the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment”). We recognize that “understanding the claim language may be aided by the explanations contained in the written description,” but “it is important not to import into a claim limitations that are not a part of the claim.” *SuperGuide*, 358 F.3d at 875. Thus, “a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment.” *Id.* As our reviewing court has explained, “it is the *claims*, not the written description, which define the scope of the patent right.” *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1347 (Fed. Cir. 1998).

Here, the claim language itself recites nothing about the phase signals being inverted versions of each other. Although the ’875 patent specification discloses an embodiment in Figures 2 and 3 where the phase signals are inverted versions of each other, nowhere does the specification

limit “opposite” to that embodiment. *See* Ex. 1001, 2:1–2 (“FIG. 2A shows the clocking signals useful for explaining the operation of the present invention.”), Figs. 2A, 3; Tr. 9:2–5 (Petitioner’s counsel conceding during oral argument that the phase signals shown in Figure 2A of the ’875 patent are inverted versions of each other). Indeed, the term “opposite” does not appear anywhere in the written description. *See generally* Ex. 1001.

Moreover, the ’875 patent describes the embodiment of Figure 3 in terms of preference. For example, the ’875 patent states that Figure 3 shows “double pumping voltage boosting converter 40 of the *preferred* embodiment of the present invention.” Ex. 1001, 2:18–20 (emphasis added). Our reviewing court has “cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification.”

Williamson v. Citrix Online, LLC, 792 F.3d 1339, 1346–47 (Fed. Cir. 2015) (quoting *Teleflex, Inc. v. Ficoso N. Am. Corp.*, 299 F.3d 1313, 1328 (Fed. Cir. 2002)).

We note Patent Owner’s extrinsic evidence, which includes various patents showing that “opposite” signals refer to inverted signals. The intrinsic evidence of record, however, shows that “opposite” signals may additionally refer to non-inverted signals. During prosecution of the application for the ’875 patent, the Examiner relied on Soejima,⁵ a prior-art patent, for teaching “in Fig. 3A a circuit comprising a first booster (10) and a second booster (11),” where “clock pulses supplied to the boosters are opposite each other in phases.” Ex. 1002, 53 (Office Action, mailed Nov.

⁵ Soejima, U.S. Patent No. 5,644,534, issued July 1, 1997 (Ex. 1016).

24, 1999) (cited by Pet. 22).⁶ To illustrate, Figures 3A and 3B of Soejima are reproduced below.

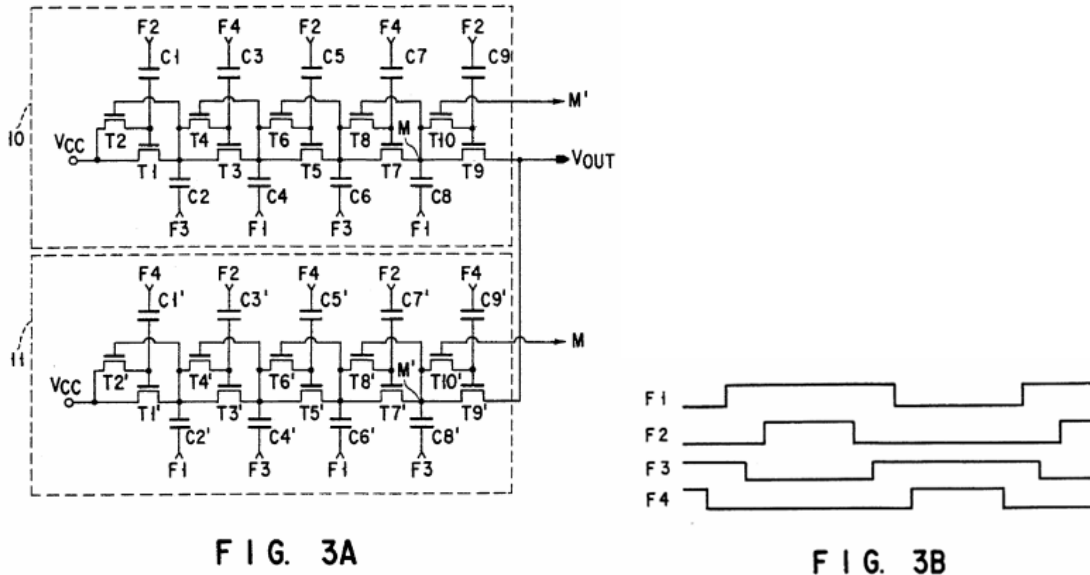


Figure 3A shows a booster circuit with first booster circuit section 10 and second booster circuit section 11, and Figure 3B shows clock pulses for controlling the booster circuit in Figure 3A. Ex. 1016, 3:53–56, 3:66–4:25. Soejima teaches that “input pulses F2 and F4, and F1 and F3 are inputted to positions of the first and second booster circuit sections,” such that “[i]nput positions of F2 are replaced with those of F4 between the first and second booster circuit sections,” and “positions of F1 are replaced with those of F3 therebetween.” *Id.* at 2:66–3:4. Specifically, the “clock pulses are inputted to second terminals of the [plurality of] first and [plurality of] second capacitors [of each booster circuit section], the second terminals . . . of the

⁶ Although the Examiner relied on Soejima for originally-filed claim 1, which was later cancelled, we note that originally-filed claim 19, which ultimately issued as claim 1 of the '875 patent, recited the limitation “a second phase signal that is opposite to the first phase signal.” *Id.* at 47 (Preliminary Amendment, filed Feb. 22, 1999), 53.

first booster circuit section and the second terminals . . . of the second booster circuit section being terminals which correspond to each other and which are supplied with *clock pulses opposite each other in phase.*” *Id.* at 2:36–65 (emphasis added). Thus, Soejima’s Figure 3B depicts “opposite” signals; but, as can be seen from the figure itself, none of the signals is an inverted version of another signal. *See id.* at Fig. 3.

As noted above, “we need only construe terms . . . to the extent necessary to resolve the controversy.” *Nidec*, 868 F.3d at 1017. For purposes of this Decision, we do not construe the entire scope of “a second phase signal that is opposite to the first phase signal.” Instead, we determine on this record that the claim term “a second phase signal that is opposite to the first phase signal” is not limited to signals that are inverted versions of each other; but it may nevertheless encompass signals that are inverted versions of each other. This is consistent with the intrinsic evidence as well as the extrinsic evidence cited by the parties discussed above. Thus, two signals may be “opposite” to each other where one signal falls to a low state (or rises to a high state) for a duration while at the same time the other signal rises to a high state (or falls to a low state) for a different duration. That is, one signal may fall to a low state while the other rises to a high state at the same point in time, but not necessarily for the same amount of time. Additionally, two signals may be “opposite” to each other where the signals “are inverted versions of each other, such that the time during which [one] signal is high is equal to the time during which the [other] signal is low and vice-versa.” *See* PO Resp. 31 (Patent Owner’s proposed construction).

2. “boost signal”

The term “boost signal” appears in claims 1 and 2. Patent Owner argues that “‘boost signal’ is not a common term of art in the field of electrical and computer engineering,” and that an ordinarily skilled artisan’s “understanding of the meaning of this claim term at the time of the invention of the ’875 patent would be the meaning as informed by the specification of the ’875 patent,” namely, “a voltage signal provided to the voltage boosting circuit such that either a non-inverted or inverted version of that signal is received by the second terminal of a capacitor, thereby causing the voltage of the first terminal to be increased.” PO Resp. 37–39 (emphasis omitted). As support, Patent Owner contends that the ’875 patent teaches that a “BOOST SIGNAL is provided to both the input of the inverting buffer 50 and the input of the non-inverting buffer 56.” *Id.* at 38; *see* Ex. 1001, Fig. 3. Patent Owner further contends,

[D]uring operation of the voltage boosting circuit of the ’875 patent, in each side (A or B) of the circuit, the capacitor (48A or 48B, respectively) in that side is first charged to V_{DD} during one half cycle, while its associated switch (42A or 42B, respectively) is closed. Also, during that same half cycle, the signal that is applied to the second terminal of the capacitor in that side (which will either always be a non-inverted or always be an inverted version of BOOST SIGNAL, depending on the side) will be in a low state. Then, during the following half cycle, the signal that is applied to the second terminal of the capacitor in that side (which again will always be either a non-inverted or inverted version of BOOST SIGNAL) will change to a high state. That high state will cause the voltage of the first terminal of the capacitor in that side to be increased (or “boosted”) from V_{DD} to nearly $2V_{DD}$.

PO Resp. 38–39 (citing Ex. 1001, 2:38–65 (describing Figure 3)).

In its Reply, Petitioner counters that “boost signal” does carry “a plain and ordinary meaning,” which an ordinarily skilled artisan would have understood to be “a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage.” Pet. Reply 16–17 (citing *Micron Tech., Inc. v. N. Star Innovations, Inc.*, IPR2019-00998, Paper 29 at 7–12 (PTAB Oct. 22, 2019) (Final Written Decision) (construing “boost signal” in the context of the ’875 patent)). Petitioner relies on the declaration testimony of Dr. Jacob. *Id.* (citing Ex. 1020 ¶¶ 6, 50, 54).

Petitioner further characterizes Patent Owner’s proposed construction as “unduly narrow.” *Id.* at 16. As support, Petitioner contends that Patent Owner’s proposed construction “would impermissibly render other language in Claim 1, such as ‘a second terminal coupled for receiving,’ redundant and superfluous, and it would also impermissibly import limitations from the specification into the claim.” *Id.* at 17 (citing *Micron*, IPR2019-00998, Paper 29 at 9–11); *see also id.* at 18–19 (“Patent Owner’s proposed construction should be rejected here, just as it was in the *Micron Final Decision*, because it is contrary to the customary meaning of ‘boost signal,’ would render other claim language superfluous, and it would impermissibly limit the term to the embodiment shown in Figure 3 of the ’875 Patent.”).

Based on the record before us, we agree with Petitioner that Patent Owner’s proposed construction is unduly narrow. Claim 1 recites two capacitors, namely, “a first capacitor having . . . a second terminal coupled for receiving a boost signal” and “a second capacitor having . . . a second terminal coupled for receiving the boost signal.” Construing “boost signal” to mean, in part, that the signal “is received by the second terminal of a

capacitor” would render the claim language “a second terminal coupled for receiving” in these instances redundant and superfluous. *See Dig.-Vending Servs. Int’l, LLC v. Univ. of Phx., Inc.*, 672 F.3d 1270, 1275 (Fed. Cir. 2012) (noting “the importance of construing claim terms in light of the surrounding claim language, such that words in a claim are not rendered superfluous”).

Further, Patent Owner’s proposed construction improperly requires the second terminal of a capacitor to receive the *non-inverted or inverted version* of the boost signal. The claim language recites nothing about the non-inverted or inverted version of the boost signal. Although the ’875 patent describes a boosting circuit in Figure 3 where the second terminal of a capacitor receives a non-inverted or inverted version of a boost signal, thereby causing the voltage of the first terminal of the capacitor to be increased, as Patent Owner argues, nowhere does the specification limit “boost signal” to that circuit. *See* PO Resp. 38–39. Moreover, the circuit in Figure 3 is described in terms of preference. Ex. 1001, 2:18–20; *see Williamson*, 792 F.3d at 1346–47 (noting that our reviewing court has “cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification”).

We turn now to Petitioner’s proposed construction of “boost signal” (i.e., “a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage”). The ’875 patent states that its “invention relates to voltage boosting converters and, more particularly to a double pumping voltage boosting circuit for providing an output voltage greater than a supplied input voltage.” Ex. 1001, 1:5–8. As to Figure 3, the ’875 patent also describes two distinct signals applied to the voltage boosting circuit, namely, a voltage boost signal and supply voltage

V_{DD}. *Id.* at 2:23–28, 2:36–37. Consistent with the '875 patent, we adopt Petitioner's proposed construction of "boost signal" and construe the claim term to mean "a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage." Our construction encompasses, but is not limited to, Patent Owner's proposed construction of the term (i.e., "a voltage signal provided to the voltage boosting circuit such that either a non-inverted or inverted version of that signal is received by the second terminal of a capacitor, thereby causing the voltage of the first terminal to be increased"), which corresponds to the embodiment in Figure 3 of the '875 patent.

3. *"coupled for receiving"*

As discussed above, claim 1 recites "a first capacitor having . . . a second terminal coupled for receiving a boost signal" and "a second capacitor having . . . a second terminal coupled for receiving the boost signal." Patent Owner argues that "[t]he claim language 'terminal coupled for receiving . . . signal' is not a common term of art in the field of electrical and computer engineering," and that an ordinarily skilled artisan's "understanding of the meaning of this claim language at the time of the invention of the '875 patent would be the meaning as informed by the '875 specification," namely, "terminal . . . is connected in a manner such that the signal received . . . is either always a non-inverted version of the boost signal or always an inverted version of the boost signal." PO Resp. 39–42 (emphasis omitted). As support, Patent Owner directs our attention to Figure 3 of the '875 patent and contends,

BOOST SIGNAL is applied to the inputs of non-inverting buffer 56 and inverting buffer 50. A non-inverted version of BOOST SIGNAL is output by the non-inverting buffer 56, and an inverted version of BOOST SIGNAL is output by the inverting buffer 50. As a result, the signal that is received by [the] ‘second terminal’ of the capacitor 48B is *always* a non-inverted version of BOOST SIGNAL, and the signal that is received by the ‘second terminal’ of capacitor 48A is *always* an inverted version of BOOST SIGNAL.

Id. at 40–41 (citing Ex. 1001, Fig. 3). Patent Owner adds that “[t]here is no disclosure in the ’875 patent that discloses any signal received by the second terminal of either the first or second capacitors that is not either always a non-inverted version of BOOST SIGNAL or always an inverted version of BOOST SIGNAL.” *Id.* at 41.

In its Reply, Petitioner argues that Patent Owner’s proposed construction “cannot be correct as a matter of law because the claims of the ’875 Patent recite nothing about inverted or non-inverted versions and, therefore, Patent Owner is again simply trying to limit the claim phrase to exactly what is depicted in Figure 3 of the ’875 Patent.” Pet. Reply 21 (citing *Micron*, IPR2019-00998, Paper 29 at 15–16 (construing “coupled for receiving” in the context of the ’875 patent)). Petitioner adds that Patent Owner’s proposed construction “is also contrary to the plain meaning of the phrase ‘coupled for receiving.’” *Id.* According to Petitioner, “the ‘terminal is “coupled,”” meaning ‘there is an electrical connection to the terminal,’ and the ‘coupling is “for” receiving a signal, such that the connection is capable of receiving a signal; that is its purpose.’” *Id.* (quoting Ex. 1020 ¶ 103).

Based on the record before us, we determine that Patent Owner’s proposed construction is overly narrow. In particular, it improperly requires that the signal received is either always a *non-inverted version* of the boost

signal or always an *inverted version* of the boost signal. The claim language recites nothing about the non-inverted version or the inverted version of the boost signal. Although the '875 patent specification discloses an embodiment in Figure 3 where the second terminal of a capacitor is connected so that the signal it receives is either always a non-inverted version of the boost signal or the inverted version of the boost signal, nowhere does the specification limit “coupled for receiving” the boost signal to that embodiment. Indeed, the '875 patent describes the embodiment of Figure 3 in terms of preference. Ex. 1001, 2:18–20.

In addition, we agree with Petitioner that “for” conveys purpose. Petitioner does not dispute Patent Owner’s contention that “coupled” means “connected.” Pet. Reply 21 (“Namely, the ‘terminal is “coupled,”’ meaning ‘there is an electrical connection to the terminal[.]’”); *see also* PO Resp. 41–42 (“[T]he term ‘second terminal of the first capacitor coupled for receiving a boost signal’ would have been understood by a [person of ordinary skill in the art] to mean ‘the second terminal of the first capacitor is connected in a manner such that the signal received by that second terminal is either always an non-inverted version of the boost signal or always an inverted version of the boost signal.’”) (emphasis omitted). Accordingly, we construe “coupled for receiving” to mean “connected in order to receive.” Thus, “a first capacitor having . . . a second terminal coupled for receiving a boost signal” refers to a first capacitor having a second terminal that is connected in order to receive a boost signal. Similarly, “a second capacitor having . . . a second terminal coupled for receiving the boost signal” refers to a second capacitor having a second terminal that is connected in order to receive the boost signal.

Based on our construction of “coupled for receiving,” we note that “terminal coupled for receiving . . . signal” encompasses, but is not limited to, Patent Owner’s proposed construction of the latter term (i.e., “terminal . . . is connected in a manner such that the signal received . . . is either always a non-inverted version of the boost signal or always an inverted version of the boost signal”), which corresponds to the embodiment in Figure 3 of the ’875 patent.

4. “*inverting buffer*”

This term appears in claim 2. Patent Owner argues that “the term ‘inverting buffer’ would have been understood by a [person of ordinary skill in the art] to mean ‘a circuit with a single input and a single output, where the output is always an inverted version of the input.’” PO Resp. 43. As support, Patent Owner contends that “[t]he ’875 patent, when referencing inverting buffer 50, uses the electrical symbol of a NOT gate,” and that “a NOT gate, also known as an inverter, is a single input, single output circuit whose output is always 1 if the input is 0, and whose output is always 0 if the input is 1.” *Id.* at 42–43.

In response, Petitioner contends that “buffer” means “[a] circuit that isolates or decouples its output from its input.” Pet. Reply 24. Petitioner asserts that Patent Owner’s proposed construction of “inverting buffer” improperly imports limitations from the specification into the claims because the claims recite nothing about a single input or a single output, nor do they recite anything about the output of a buffer always being inverted. *Id.* at 23–24 (citing *Micron*, IPR2019-00998, Paper 29 at 18–19 (construing “non-inverting buffer” in the context of the ’875 patent)). Petitioner further points

us to a manual that was published two years before the filing date of the '875 patent, which teaches that “[a]ny NAND or NOR gate can be used as an inverting buffer element,” where the NAND gates and NOR gates have multiple inputs. *Id.* at 26 (citing Ex. 2009, Fig. 3.15); Ex. 2009, Fig. 3.15. Petitioner relies on the declaration testimony of Dr. Jacob. Pet. Reply 24–26 (citing Ex. 1020 ¶¶ 156–163).

On this record, we agree with Petitioner. Patent Owner’s proposed construction improperly imports limitations from the specification into the claims. The claim language recites nothing about a single input or a single output. Although Figure 3 of the '875 patent discloses an embodiment including an inverting buffer with a single input and a single output, nowhere does the specification limit “inverting buffer” to that embodiment, which is described in terms of preference. *See* Ex. 1001, 2:18–20, Fig. 3. Moreover, extrinsic evidence of record—specifically, a prior-art manual—shows that inverting buffers may have more than one input. *See* Ex. 2009, Fig. 3.15.

Additionally, the claim language recites nothing about the output *always* being an inverted version of the input. Again, Figure 3 may disclose an embodiment with that feature, but nowhere does the specification limit “inverting buffer” to that embodiment. *See* Ex. 1001, Fig. 3.

As “we need only construe terms . . . to the extent necessary to resolve the controversy,” we do not construe the entire scope of “inverting buffer” for purposes of this Decision. *See Nidec*, 868 F.3d at 1017. Instead, we determine based on the record before us that “inverting buffer” is not limited to a circuit with a single input and a single output. For example, a circuit with multiple inputs may be an “inverting buffer.” Further, we determine

that the term “inverting buffer” also is not limited to a circuit whose output is *always* an inverted version of the input. That is, a circuit may be an “inverting buffer” if its output is an inverted version of the input at any time.

5. “*non-inverting buffer*”

This term also appears in claim 2. Patent Owner argues that “the term ‘non-inverting buffer’ would have been understood by a [person of ordinary skill in the art] to mean ‘a circuit with a single input and a single output, where the output is always a non-inverted version of the input.’” PO Resp. 45. As support, Patent Owner contends that “[t]he ’875 patent, when referencing non-inverting buffer 56, uses the common electrical symbol of a buffer gate,” and that “a buffer gate is a single input, single output circuit whose output is always 1 if the input is 1, and whose output is always 0 if the input is 0.” *Id.* at 44.

In its Reply, Petitioner contends that “buffer” means “[a] circuit that isolates or decouples its output from its input.” Pet. Reply 24. Petitioner asserts that Patent Owner’s proposed construction of “non-inverting buffer” improperly imports limitations from the specification into the claims because the claims recite nothing about a single input or a single output, nor do they recite anything about the output of a buffer always being non-inverted. *Id.* at 23–24 (citing *Micron*, IPR2019-00998, Paper 29 at 18–19 (construing “non-inverting buffer” in the context of the ’875 patent)). Petitioner further points us to a reference describing “[m]ethods of using AND gates as simple buffers” (i.e., non-inverting buffers), where the AND gates have multiple inputs. *Id.* at 26 (citing Ex. 2009, Fig. 3.27); Ex. 2009, 66 (“Note that AND gates can be converted into non-inverting buffers . . . as shown in *Figure*

3.27.’), Fig. 3.27. Petitioner relies on the declaration testimony of Dr. Jacob. Pet. Reply 24–26 (citing Ex. 1020 ¶¶ 156–163).

We agree with Petitioner. Patent Owner’s proposed construction improperly imports limitations from the specification into the claims. The claim language recites nothing about a single input or a single output. Although Figure 3 of the ’875 patent discloses an embodiment including a non-inverting buffer with a single input and a single output, nowhere does the specification limit “non-inverting buffer” to that embodiment, which is described in terms of preference. *See* Ex. 1001, 2:18–20, Fig. 3. Moreover, a prior-art manual of record shows that non-inverting buffers may have more than one input. *See* Ex. 2009, Fig. 3.27.

The claim language also recites nothing about the output *always* being a non-inverted version of the input. Figure 3 may disclose an embodiment with that feature, but nowhere does the specification limit “non-inverting buffer” to that embodiment. *See* Ex. 1001, Fig. 3.

For purposes of this Decision, we do not construe the entire scope of “non-inverting buffer.” *See Nidec*, 868 F.3d at 1017. Instead, we determine based on the record before us that “non-inverting buffer” is not limited to a circuit with a single input and a single output. For example, a circuit with multiple inputs may be a “non-inverting buffer.” We further determine that the term “non-inverting buffer” also is not limited to a circuit whose output is *always* a non-inverted version of the input. Thus, a circuit may be a “non-inverting buffer” if its output is a non-inverted version of the input at any time.

B. Anticipation by Chern

Petitioner asserts that Chern anticipates claims 1–3 of the ’875 patent. Pet. 30–57. Patent Owner contests this ground. PO Resp. 45–65. For the reasons explained below, we determine that Petitioner has demonstrated by a preponderance of the evidence that Chern anticipates claims 1–3.

1. Overview of Chern

Chern describes a charge pump for biasing a semiconductor substrate or well to a voltage that is greater than the supply voltage. Ex. 1005, 1:5–9, 2:66–3:1. Figure 2, which is reproduced below, illustrates an example of Chern’s charge pump. *Id.* at 2:50–51.

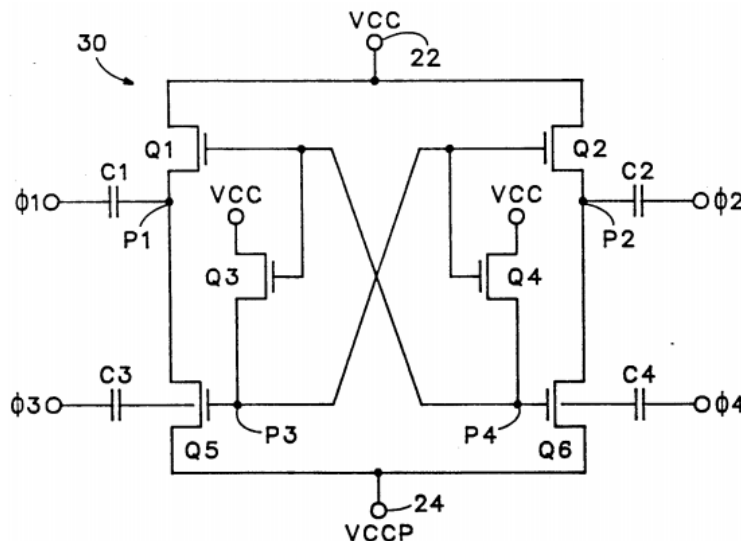


FIG. 2

Figure 2 shown above illustrates the basic circuit configuration of charge pump 30. *Id.* at 3:10–11. Charge pump 30 includes six transistors Q1–Q6. *Id.* at 3:10–12. Four transistors Q1–Q4 are coupled to supply voltage VCC at terminal 22. *Id.* at 3:20–22.

Charge pump 30 also includes four capacitors C1–C4 and output terminal 24 for biasing a semiconductor substrate or well. *Id.* at 3:18–20.

Capacitor C1 receives clock signal ϕ_1 , and it is coupled to transistors Q1 and Q5 at circuit node P1. *Id.* at 3:24–28. Capacitor C2 receives clock signal ϕ_2 , and it is coupled to transistors Q2 and Q6 at circuit node P2. *Id.* at 3:28–32. Capacitor C3 receives clock signal ϕ_3 , and it is coupled to transistors Q2, Q3, Q4, and Q5 at circuit node P3. *Id.* at 3:32–36. Capacitor C4 receives clock signal ϕ_4 , and it is coupled to transistors Q1, Q3, Q4, and Q6 at circuit node P4. *Id.* at 3:36–40.

Transistors Q5 and Q6 are additionally coupled to output terminal 24, which, in turn, is coupled to the substrate or well. *Id.* at 3:40–42. These charging transistors, Q5 and Q6, deliver current to the substrate or well. *Id.* at 3:42–44. The substrate or well is biased to boosted voltage VCCP whose value is $2 V_{CC} - V_T$, where V_T is a transistor threshold voltage. *Id.* at 1:34–37, 3:45–49.

To help explain how charge pump 30 operates, Figure 3 is reproduced below.

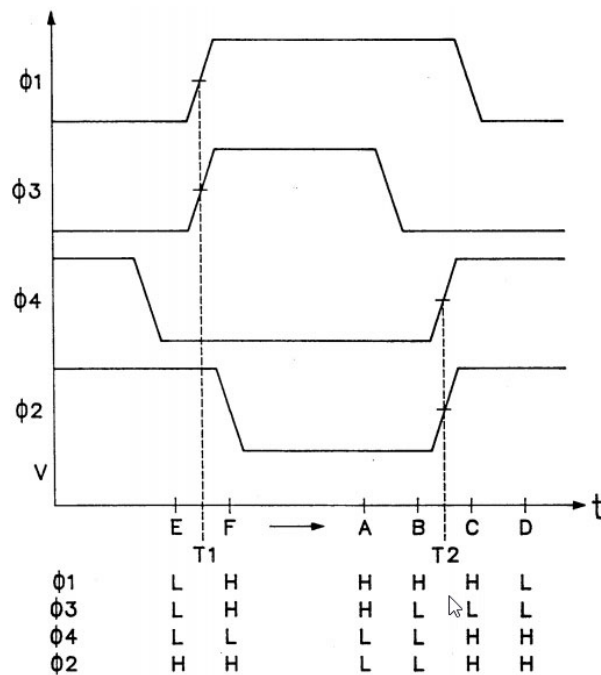


FIG. 3

Figure 3 shown above includes a timing diagram and a table showing the phase relationship between the four-phase clock (comprising clock signals $\phi 1$ – $\phi 4$) and charge pump 30. *Id.* at 2:52–54, 3:50–52. The clock signals are in specific logic states during each of six time intervals A–F. *Id.* at 3:61–63. For example, during time interval A, clock signals $\phi 1$ and $\phi 3$ are in logic high states (H), and clock signals $\phi 2$ and $\phi 4$ are in logic low states (L). *Id.* at 3:65–68.

As an initial condition, circuit nodes P1–P4 and output terminal 24 are clamped to a voltage value of $VCC - VT$. *Id.* at 4:2–7. When the time interval changes from A to B, clock signal $\phi 3$ changes to a logic low state, and the voltage across circuit node P3 decreases from $VCC - VT$. *Id.* at 4:11–15. Transistor Q5 turns off, isolating circuit node P1 from output terminal 24. *Id.* at 4:15–16. Transistors Q2 and Q4 also turn off, isolating circuit nodes P2 and P4 from supply voltage VCC . *Id.* at 4:16–18.

When the time interval changes from B to C, clock signals $\phi 2$ and $\phi 4$ change to logic high states, and the voltages across circuit nodes P2 and P4 increase to just below $2 VCC - VT$. *Id.* at 4:19–22. Transistor Q6 turns on, discharging capacitor C2 and injecting current into the substrate or well through output terminal 24, thereby reducing the voltage across circuit node P2 to $VCC - VT$. *Id.* at 4:25–29. Transistors Q1 and Q3 also turn on, pre-charging circuit nodes P1 and P3 to VCC . *Id.* at 4:29–30. Transistor Q5 remains off. *Id.* at 4:31–33.

When the time interval changes from C to D, clock signal $\phi 1$ changes to a logic low state, establishing a potential of about VCC across capacitor C1. *Id.* at 4:37–40. The voltage across circuit node P1 remains at VCC . *Id.* at 4:40–44.

When the time interval changes from D to E, clock signal $\phi 4$ changes to a logic low state, and the voltage across circuit node P4 changes from about $2 VCC - VT$ to $VCC - VT$. *Id.* at 4:45–48. Transistor Q6 turns off, isolating circuit node P2 from output terminal 24. Transistors Q1 and Q3 also turn off, isolating circuit nodes P1 and P3 from supply voltage VCC. *Id.* at 4:48–51.

When the time interval changes from E to F, clock signals $\phi 1$ and $\phi 3$ change to logic high states, and the voltages across circuit nodes P1 and P3 increase to just below $2 VCC$. *Id.* at 4:52–55. Transistor Q5 turns on, discharging capacitor C1 and injecting current into the substrate or well through output terminal 24, thereby reducing the voltage across circuit node P1. *Id.* at 4:55–59. Transistors Q2 and Q4 also turn on, pre-charging circuit nodes P2 and P4 to VCC. *Id.* at 4:60–61. Transistor Q6 remains off. *Id.* at 4:61–63.

Lastly, when the time interval changes from F to A, clock signal $\phi 2$ changes to a logic low state, establishing a potential of about VCC across capacitor C2. *Id.* at 4:64–68. The voltage across circuit node P2 stays at VCC. *Id.* at 4:68–5:3. The process is repeated until final voltage VCCP (i.e., $2 VCC - VT$) is reached. *Id.* at 5:3–5.

In sum, charging transistors Q5 and Q6 deliver alternate current pulses to the substrate or well through output terminal 24. *Id.* at 5:10–12. Capacitors C1 and C2 are coupled respectively to the charging transistors, and provide the charge storage that is converted to a charge pulse when the capacitors are discharged. *Id.* at 5:12–16. During the first half-cycle of the four-phase clock signal, capacitor C1 is discharged through transistor Q5, and capacitor C2 is pre-charged for the next half-cycle. *Id.* at 5:16–20.

During the second half-cycle of the four-phase clock signal, capacitor C2 is discharged through transistor Q6, and the first capacitor C1 is pre-charged. *Id.* at 5:20–23. As the alternate current pulses are delivered to the substrate or well, the voltage across the substrate or well moves from initial voltage $VCC - VT$ to boosted voltage of $2 VCC - VT$. *Id.* at 5:24–28.

2. Independent Claim 1

Claim 1 is directed to a boost circuit comprising “a first switch,” “a second switch,” “a first capacitor,” and “a second capacitor.”

a. “boost circuit”

The preamble of claim 1 recites a “boost circuit having an input terminal and an output terminal.” Petitioner identifies Chern’s charge pump 30 as a “boost circuit.” Pet. 32. Referring to Figure 2 of Chern, Petitioner contends that “circuit 30 receives a supply voltage VCC at an input terminal 22 . . . and provides a boosted voltage VCCP at an output terminal 24.” *Id.* at 30; *see also* Ex. 1005, 3:20–22, 3:40–42, Fig. 2. Based on the entire trial record before us, we find that Petitioner has established that Chern discloses the preamble.⁷ Patent Owner does not dispute Petitioner’s analysis for this aspect of the claim. *See generally* PO Resp.

b. “first switch”

Claim 1 further recites “a first switch coupled between the input terminal and the output terminal and operated by a first phase signal.” For

⁷ We need not decide whether the preamble is limiting because Petitioner shows that Chern discloses the preamble.

this limitation, Petitioner provides an annotated version of Figure 2 of Chern, which is reproduced below. Pet. 35.

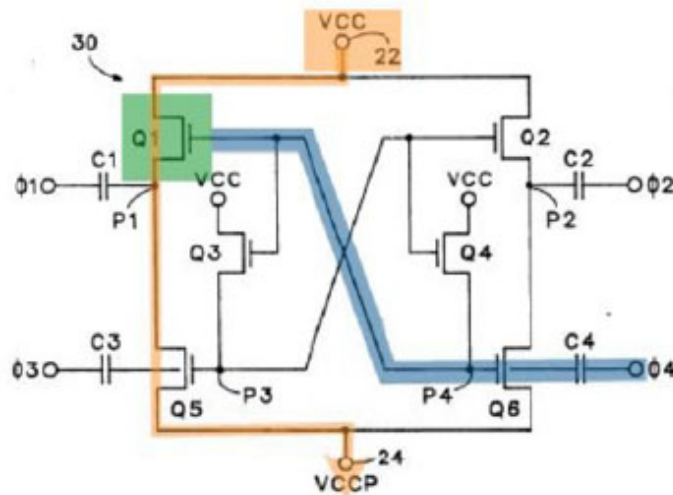


Figure 2 of Chern shown above, as annotated by Petitioner, illustrates the basic circuit configuration of charge pump 30. *See* Ex. 1005, 3:10–11. Petitioner identifies Chern’s transistor Q1 (highlighted in green) as a “first switch.” Pet. 32. As support, Petitioner directs us to where Chern teaches that the drain of transistor Q1 is coupled to supply voltage VCC at terminal 22. *Id.* at 33 (citing Ex. 1005, 3:20–22). Petitioner contends that terminal 22 (highlighted in orange) corresponds to the recited “input terminal” because terminal 22 provides the supply voltage. *Id.* Petitioner also directs us to where Chern teaches that transistor Q1 is coupled to both transistor Q5 and capacitor C1, and that transistor Q5 discharges capacitor C1 and injects current into the substrate or well through output terminal 24 when transistor Q5 is on. *Id.* at 33 (citing Ex. 1005, 3:24–27, 4:54–58). Petitioner contends that “[b]ecause transistor Q1 is coupled to capacitor C1, which in turn injects current through Chern’s output terminal 24, the transistor Q1 is coupled to the output terminal through capacitor C1.” *Id.*

Petitioner further identifies Chern's clock signal ϕ_4 as a "first phase signal." Pet. 34. As support, Petitioner points us to where Chern teaches that the gate of transistor Q1 is coupled to one end of capacitor C4 at circuit node P4, and that the other end of capacitor C4 receives clock signal ϕ_4 . *Id.* (citing Ex. 1005, 3:38–41). This is shown by the signal path highlighted in blue in Petitioner's annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 35. Petitioner additionally points us to Dr. Jacob's declaration testimony that the gate of Chern's transistor Q1 is controlled by clock signal ϕ_4 . Ex. 1003 ¶ 144 (cited by Pet. 34). Dr. Jacob relies on Chern's teaching that, when the time interval changes from B to C, clock signal ϕ_4 changes to a logic high state, and transistor Q1 turns on to pre-charge circuit node P1. *Id.* (citing Ex. 1005, 4:19–30). Dr. Jacob also relies on Chern's teaching that, when the time interval changes from D to E, clock signal ϕ_4 changes to a logic low state, and transistor Q1 turns off. *Id.* (citing Ex. 1005, 4:45–51).

Patent Owner does not dispute Petitioner's analysis for this limitation. *See generally* PO Resp. Based on the entire trial record before us, we find that Petitioner has established that Chern discloses the recited "first switch."

c. "second switch"

Claim 1 further recites "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal." For this limitation, Petitioner provides another annotated version of Figure 2 of Chern, which is reproduced below. Pet. 40.

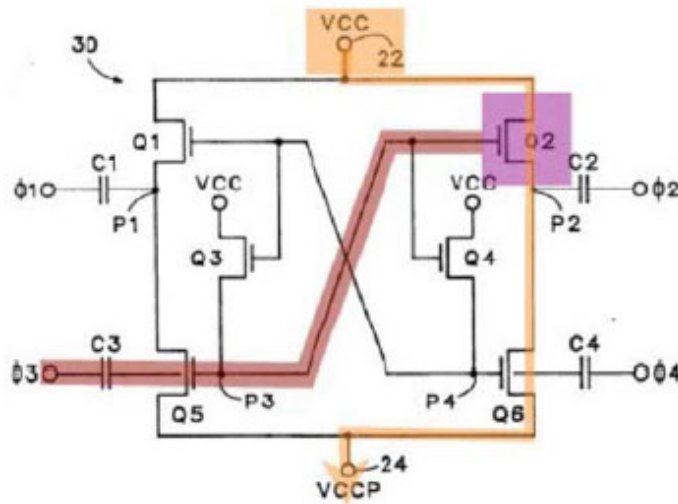


Figure 2 of Chern shown above, as annotated by Petitioner, illustrates the basic circuit configuration of charge pump 30. *See* Ex. 1005, 3:10–11. Petitioner identifies Chern’s transistor Q2 (highlighted in purple) as a “second switch.” Pet. 36. Petitioner further directs us to where Chern teaches that the drain of transistor Q2 is coupled to supply voltage VCC at terminal 22. *Id.* at 36–37 (citing Ex. 1005, 3:20–22). As discussed above, Petitioner contends that terminal 22 (highlighted in orange) corresponds to the recited “input terminal” because terminal 22 provides the supply voltage. *Id.* at 37. Petitioner also directs us to where Chern teaches that transistor Q2 is coupled to both transistor Q6 and capacitor C2, and that transistor Q6 discharges capacitor C2 and injects current into the substrate or well through output terminal 24 when transistor Q6 is on. *Id.* (citing Ex. 1005, 3:20–22,⁸ 4:25–27). Petitioner contends that “[b]ecause transistor Q2 is coupled to capacitor C2, which in turn injects current through Chern’s output terminal 24, the transistor Q2 is coupled to the output terminal through capacitor C2.” *Id.*

⁸ Petitioner cites Exhibit 1005, at column 3, lines 20 through 22, but the language to which Petitioner refers appears at column 3, lines 28 through 31.

Petitioner further identifies Chern's clock signal $\phi 3$ as a "second phase signal." Pet. 38. As support, Petitioner points us to where Chern teaches that the gate of transistor Q2 is coupled to one end of capacitor C3 at circuit node P3, and that the other end of capacitor C3 receives clock signal $\phi 3$. *Id.* at 37–38 (citing Ex. 1005, 3:34–37). This is shown by the signal path highlighted in red in Petitioner's annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 40. Petitioner also points us to Dr. Jacob's declaration testimony that the gate of Chern's transistor Q2 is controlled by clock signal $\phi 3$. Ex. 1003 ¶ 149 (cited by Pet. 38). Dr. Jacob relies on Chern's teaching that, when the time interval changes from E to F, clock signal $\phi 3$ changes to a logic high state, and transistor Q2 turns on to pre-charge circuit node P2. *Id.* (citing Ex. 1005, 4:52–61). In addition, Dr. Jacob relies on Chern's teaching that, when the time interval changes from A to B, clock signal $\phi 3$ changes to a logic low state, and transistor Q2 turns off. *Id.* (citing Ex. 1005, 4:11–18).

Claim 1 requires the second phase signal to be "opposite" to the first phase signal. For this aspect of the limitation, Petitioner directs us to where Chern teaches that, during time interval A, clock signal $\phi 3$ is in a logic high state, and clock signal $\phi 4$ is in a logic low state. Pet. 39 (citing Ex. 1005, 3:65–68, Fig. 3). As discussed above, Petitioner contends that Chern's clock signal $\phi 4$ corresponds to the recited "first phase signal" and that Chern's clock signal $\phi 3$ corresponds to the recited "second phase signal." Pet. 38, 40–41. Relying on the declaration testimony of Dr. Jacob, Petitioner further contends that Chern's signals are opposite to each other because "clock $\phi 3$ and clock $\phi 4$ are the same signal, shifted 180 degrees (half a clock cycle) relative to one another,' such that, 'when clock $\phi 3$ is high, clock $\phi 4$ is low,

and that when clock $\phi 3$ is low, clock $\phi 4$ is high.” *Id.* at 39 (quoting Ex. 1003 ¶ 152); *see also id.* at 38–39 (Petitioner’s extended version of Figure 3 of Chern, with annotations).

Based on Petitioner’s argument and evidence, we are persuaded that Chern discloses the recited “second switch.”

Patent Owner, however, disputes Petitioner’s analysis for this limitation. In particular, Patent Owner argues that Chern’s “[c]lock signals $\phi 3$ and $\phi 4$. . . are not opposite signals” because they “are not inverted versions of each other, such that the time during which $\phi 4$ is high equals the time during which $\phi 3$ is low and vice-versa.” PO Resp. 46; *see also id.* at 49 (“[T]he time during which $\phi 4$ is high is **not** equal to the time during which $\phi 3$ is low, and the time during which $\phi 4$ is low state is **not** equal to the time during which $\phi 3$ is high.”). As support, Patent Owner contends that “the fall of $\phi 4$ (the alleged ‘first phase signal’) does not coincide with the rise of $\phi 3$ (the alleged ‘second phase signal’),” as “the rise of $\phi 3$ is **intentionally delayed** so that $\phi 3$ rises **after** $\phi 4$ falls.” *Id.* at 48. Patent Owner also contends that “the rise of $\phi 4$ does not coincide with the fall of $\phi 3$,” as “the rise of $\phi 4$ is **intentionally delayed** so that $\phi 4$ rises after $\phi 3$ falls.” *Id.* at 49. According to Patent Owner, during the time that either signal is intentionally delayed, both signals “have **the same state** (they are both low).” *Id.* at 48–49. To illustrate, Patent Owner provides an annotated version of Figure 3 of Chern, which is reproduced below. *Id.* at 48.

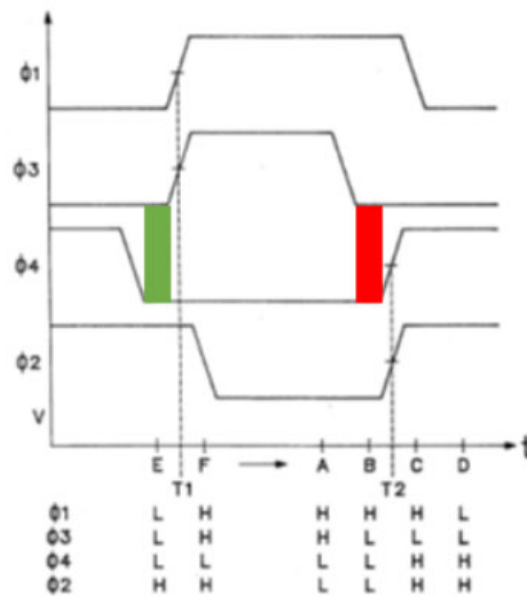


FIG. 3

Figure 3 of Chern shown above, as annotated by Patent Owner, includes a timing diagram and a table showing the phase relationship between a four-phase clock (comprising clock signals $\phi 1$ – $\phi 4$) and charge pump 30. See Ex. 1005, 2:52–54, 3:50–52. The green shading represents signal $\phi 3$'s intentional delay, which corresponds to time interval E, whereas the red shading represents signal $\phi 4$'s intentional delay, which corresponds to time interval B. PO Resp. 48–49. These annotations help show that “the time during which $\phi 4$ is high is *intentionally shorter* than the time during which $\phi 3$ is low, and the time during which $\phi 4$ is low is *intentionally longer* than the time during which $\phi 3$ is high.” PO Resp. 49. Patent Owner relies on the declaration testimony of Dr. Khatri. *Id.* at 46–49 (citing Ex. 2001 ¶¶ 138, 140–141).

Patent Owner notes Petitioner's assertion that “when clock $\phi 3$ is high, clock $\phi 4$ is low, and that when clock $\phi 3$ is low, clock $\phi 4$ is high.” *Id.* at 49–50 (quoting Pet. 38–39). According to Patent Owner, however, “[t]o determine whether $\phi 3$ and $\phi 4$ are opposite signals, they must be viewed in

their entirety,” and “[s]imply isolating a point in time (time interval A) when $\phi 3$ and $\phi 4$ are in opposite logic states does not mean that signals $\phi 3$ and $\phi 4$ are opposite signals.” *Id.* at 50. As such, Patent Owner contends, “signal $\phi 3$ is not opposite the signal $\phi 4$ ” because “there are other times during the operation of Chern’s circuit (time intervals B and E) during which $\phi 3$ and $\phi 4$ have ***the same state, by design*** (they are both low).” *Id.*

We disagree with Patent Owner’s argument, which relies on Patent Owner’s proposed construction of “a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal” (i.e., “the first phase signal and second phase signal are inverted versions of each other, such that the time during which the first phase signal is high is equal to the time during which the second phase signal is low and vice-versa”). *See* PO Resp. 31. As discussed above, Patent Owner’s proposed construction improperly requires the signals to be *inverted* versions of each other, where the time during which one signal is high is equal to the time during which the other signal is low. *See supra* Part III.A.1. Accordingly, that Chern’s signals $\phi 3$ and $\phi 4$ are not inversions of each other (i.e., the time during which one signal is high is not equal to the time during which the other signal is low), does not undermine Petitioner’s showing that Chern discloses the recited “second switch.”

d. “first capacitor” and “second capacitor”

Claim 1 further recites “a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal,” and “a second capacitor having a first terminal coupled to the

output terminal and a second terminal coupled for receiving the boost signal.” With respect to the “first capacitor” limitation, Petitioner provides yet another annotated version of Figure 2 of Chern, which is reproduced below. Pet. 43.

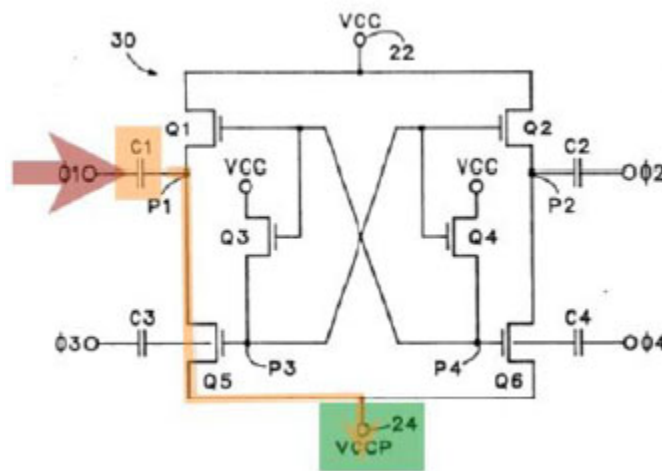


Figure 2 of Chern shown above, as annotated by Petitioner, illustrates the basic circuit configuration of charge pump 30. *See* Ex. 1005, 3:10–11. Petitioner identifies Chern’s capacitor C1 (highlighted in orange) as a “first capacitor.” *See* Pet. 41 (focusing analysis on Chern’s capacitor C1). As support, Petitioner directs us to where Chern teaches that transistor Q5 discharges capacitor C1 and injects current into the substrate or well through output terminal 24 (highlighted in green) when transistor Q5 is on. *Id.* (citing Ex. 1005, 4:55–58). Relying on the declaration testimony of Dr. Jacob, Petitioner contends that “capacitor C1 has a first terminal (a plate) coupled to the output terminal 24 through node P1 and transistor Q5.” *Id.* (citing Ex. 1003 ¶ 157). This is shown by the signal path highlighted in orange in Petitioner’s annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 43.

Petitioner also directs us to where Chern teaches that the other plate of capacitor C1 receives clock signal $\phi 1$, and identifies the other plate as a “second terminal.” *Id.* at 41–42 (citing Ex. 1005, 3:28–29). The relationship between capacitor C1 and clock signal $\phi 1$ is shown by the signal path highlighted with a red arrow in Petitioner’s annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 43. Petitioner additionally points out that Chern’s clock signal $\phi 1$ is driven by ring oscillator 12 and conditioning circuit 14, and generated by clock generator 42. *Id.* at 42 (citing Ex. 1005, 7:27–32); *see also* Ex. 1005, Figs. 6A–6B (cited by Pet. 42–43) (showing signal path with ring oscillator 12, conditioning circuit 14, clock generator 42, and capacitor C1). According to Petitioner, Chern’s clock signal $\phi 1$ (highlighted in red) provides a “boost signal” from ring oscillator 12 and conditioning circuit 14 because the voltage across circuit node P1 (which is connected to capacitor C1) increases to about 2 VCC when clock signal $\phi 1$ changes from a logic low state to a logic high state, and transistor Q5 turns on to discharge capacitor C1 and inject current into the substrate or well through output terminal 24 during the same time interval. Pet. 42 (citing Ex. 1005, 4:37–51).⁹ Petitioner relies on the declaration testimony of Dr. Jacob. *Id.* (citing Ex. 1003 ¶¶ 154–157).

With respect to the “second capacitor” limitation, Petitioner provides a further annotated version of Figure 2 of Chern, which is reproduced below. *Id.* at 46.

⁹ Petitioner cites Exhibit 1005, at column 4, lines 37 through 51, but the language to which Petitioner refers appears at column 4, lines 52 through 58.

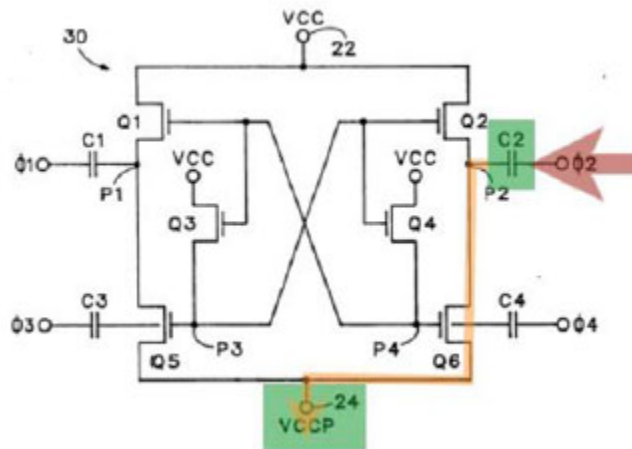


Figure 2 of Chern shown above, as annotated by Petitioner, illustrates the basic circuit configuration of charge pump 30. *See* Ex. 1005, 3:10–11. Petitioner identifies Chern’s capacitor C2 (highlighted in green) as a “second capacitor.” *See* Pet. 44 (focusing analysis on Chern’s capacitor C2). As support, Petitioner directs us to where Chern teaches that transistor Q6 discharges capacitor C2 and injects current into the substrate or well through output terminal 24 (also highlighted in green) when transistor Q6 is turned on. *Id.* (citing Ex. 1005, 4:25–27). Relying on the declaration testimony of Dr. Jacob, Petitioner contends that “capacitor C2 has a first terminal (a plate) coupled to the output terminal 24 through node P2 and transistor Q6.” *Id.* (citing Ex. 1003 ¶ 161). This is shown by the signal path highlighted in orange in Petitioner’s annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 46.

Petitioner also directs us to where Chern teaches that the other plate of capacitor C2 receives clock signal $\phi 2$, and identifies the other plate as a “second terminal.” *Id.* at 44 (citing Ex. 1005, 3:31–32). The relationship between capacitor C2 and clock signal $\phi 2$ is shown by the signal path highlighted with a red arrow in Petitioner’s annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 46. Petitioner additionally

points to Chern’s teaching that clock signal $\phi 2$ is driven by ring oscillator 12 and conditioning circuit 14, and generated by clock generator 42. *Id.* at 44–45 (citing Ex. 1005, 7:27–32); *see also* Ex. 1005, Figs. 6A–6B (cited by Pet. 45–46) (showing signal path with ring oscillator 12, conditioning circuit 14, clock generator 42, and capacitor C2). According to Petitioner, Chern’s clock signal $\phi 2$ (highlighted in red) provides a “boost signal” from ring oscillator 12 and conditioning circuit 14 because the voltage across circuit node P2 (which is connected to capacitor C2) increases to about 2 VCC when clock signal $\phi 2$ changes from a logic low state to a logic high state, and transistor Q6 turns on to discharge capacitor C2 and inject current into the substrate or well through output terminal 24 during the same time interval. Pet. 45–46 (citing Ex. 1005, 4:37–51).¹⁰ Petitioner relies on the declaration testimony of Dr. Jacob. *Id.* (citing Ex. 1003 ¶¶ 158–160).

Based on Petitioner’s argument and evidence, we are persuaded that Chern discloses the recited “first capacitor” and the recited “second capacitor.”

Patent Owner, however, disputes Petitioner’s analysis for these limitations. For example, Patent Owner argues that the signal generated by Chern’s conditioning circuit 14 is not a “boost signal” because “clock signals $\phi 1$ and $\phi 2$ are not non-inverted or inverted versions of the alleged ‘boost signal.’” PO Resp. 54. As support, Patent Owner contends that “the signal that is generated by the conditioning circuit 14 . . . is provided as the input to the four phase clock generator 42,” which “includes particular logic circuitry (including inverters and NOR gates) that . . . generates and outputs

¹⁰ Petitioner cites Exhibit 1005, at column 4, lines 37 through 51, but the language to which Petitioner refers appears at column 4, lines 19 through 27.

the clock signals $\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$,” where “signals[] $\phi 1$ and $\phi 2$ are the signals received by the second terminals of capacitors C1 and C2, respectively.” *Id.* at 52–53. According to Patent Owner, “the signal generated by conditioning circuit 14 is out of phase with both $\phi 1$ and $\phi 2$,” and, “[a]s such $\phi 1$ and $\phi 2$ are neither non-inverted nor inverted versions of the signal output by conditioning circuit 14, *i.e.*, the alleged ‘boost signal.’” *Id.* at 53.

We disagree with Patent Owner’s argument, which relies on Patent Owner’s proposed construction of “boost signal” (*i.e.*, “a voltage signal provided to the voltage boosting circuit such that either a non-inverted or inverted version of that signal is received by the second terminal of a capacitor, thereby causing the voltage of the first terminal to be increased”). As discussed above, that construction is overly narrow and improperly requires a non-inverted or inverted version of the boost signal. *See supra* Part III.A.2.

The proper construction of “boost signal” is “a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage.” *Id.* Under that construction, we find that the signal generated by Chern’s ring oscillator 12 and conditioning circuit 14 is a “boost signal,” as recited in claim 1. Chern teaches that its “substrate or well is ultimately biased to a voltage, VCCP, that is more positive than the external power supply voltage VCC.” Ex. 1005, 3:44–46. Referring to Figures 2 and 3, Chern “assume[s] as an initial condition that the circuit nodes P1–P4 and the output terminal 24 are clamped to the external positive power supply voltage minus a transistor threshold voltage ($VCC-VT$).” *Id.* at 4:1–7. Chern explains that when clock signal $\phi 1$ ’s state changes from a

logic low to a logic high, “[t]he voltage on circuit node[] P1 . . . increases to a voltage slightly less than 2 VCC,” and “[t]ransistor Q5 turns on, discharging capacitor C1 and injecting current into the substrate or well through output terminal 24.” *Id.* at 4:52–58. Chern’s circuit node P1 is connected to capacitor C1. *See id.* at Fig. 2. Chern further explains that when clock signal $\phi 2$ ’s state changes from a logic low to a logic high, “[t]he voltage on circuit node[] P2 . . . increases to a voltage slightly less than 2 VCC–VT,” and “[t]ransistor Q6 turns on, discharging capacitor C2 and injecting current into the substrate or well through output terminal 24.” *Id.* at 4:19–27. Chern’s circuit node P2 is connected to capacitor C2. *See id.* at Fig. 2. In light of these teachings, we find that Patent Owner’s argument does not undermine Petitioner’s showing that Chern discloses the recited “boost signal.”

Patent Owner further argues that Chern does not disclose the recited first capacitor’s “second terminal coupled for receiving a boost signal” or the recited second capacitor’s “second terminal for receiving the boost signal.” PO Resp. 55. In particular, Patent Owner contends that to satisfy these claim limitations, Chern’s signals “ $\phi 1$ and $\phi 2$ that are received by capacitors C1 and C2 must be either always non-inverted or inverted versions of the signal generated by conditioning circuit 14, i.e., the alleged ‘boost signal.’” *Id.* at 55–56. Patent Owner further asserts that “[w]hile capacitors C1 and C2 are coupled for receiving $\phi 1$ and $\phi 2$, respectively, $\phi 1$ and $\phi 2$ are not either always non-inverted or inverted versions of the signal generated by conditioning circuit 14.” *Id.* at 56; *see also id.* at 57 (“While the ‘second terminal’ of C1 is always receiving $\phi 1$, and the ‘second terminal’ of C2 is always receiving $\phi 2$, $\phi 1$ and $\phi 2$ are not either always non-inverted or

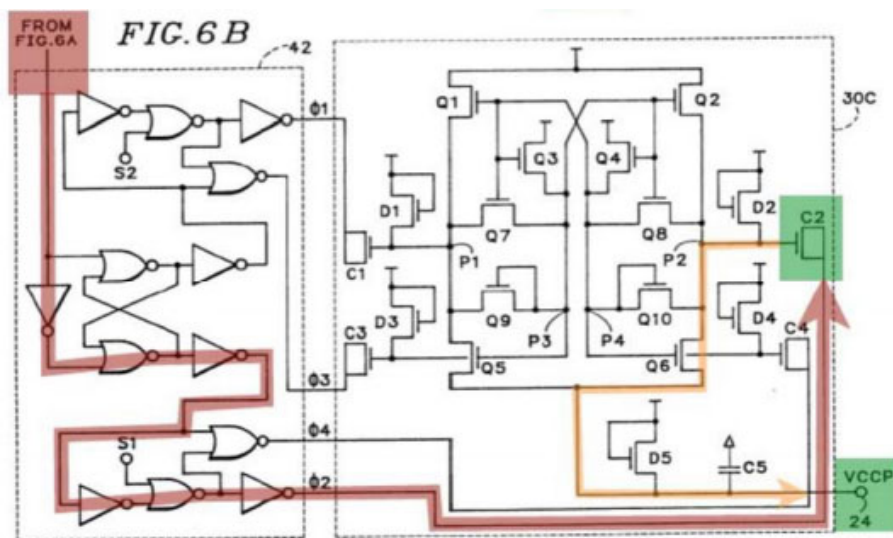
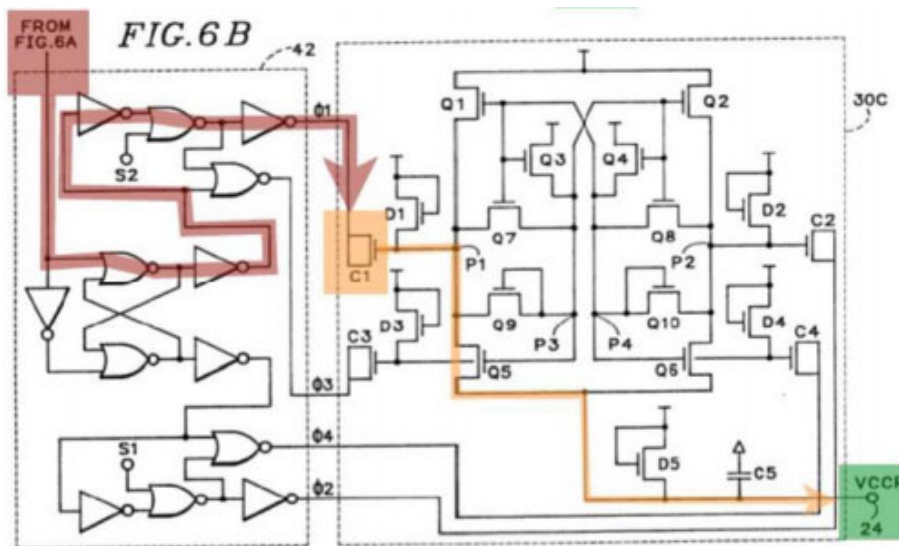
inverted versions of the alleged ‘boost signal,’ nor are they inverted versions of each other.”). According to Patent Owner, “signals $\phi 1$ and $\phi 2$ are entirely new signals generated by the logic circuit[r]y (which includes intentionally designed specific delay) of four phase clock generator 42,” where “[t]he signal that is generated by conditioning circuit 14 in Chern is merely an input into four phase clock generator 42.” *Id.* at 57. Patent Owner relies on the declaration testimony of Dr. Khatri. *Id.* at 56–57 (citing Ex. 2001 ¶¶ 161–163).

We disagree with Patent Owner’s argument. Patent Owner relies on its proposed construction of “terminal coupled for receiving . . . signal” (i.e., “terminal . . . is connected in a manner such that the signal received . . . is either always a non-inverted version of the boost signal or always an inverted version of the boost signal”). For the reasons given above, Patent Owner’s proposed construction improperly requires a non-inverted version or inverted version of the boost signal. *See supra* Part III.A.3.

As explained above, the proper construction of “coupled for receiving” is “connected in order to receive.” *Id.* Thus, “a first capacitor having . . . a second terminal coupled for receiving a boost signal” refers to a first capacitor having a second terminal that is connected in order to receive a boost signal. Similarly, “a second capacitor having . . . a second terminal coupled for receiving the boost signal” refers to a second capacitor having a second terminal that is connected in order to receive the boost signal.

Based on our construction, we find that the terminals of Chern’s capacitors C1 and C2 are coupled for receiving a boost signal, namely, the signal generated by ring oscillator 12 and conditioning circuit 14. Figures 6A and 6B of Chern show that the signal generated by ring

oscillator 12 and conditioning circuit 14 follows a path leading to capacitor C1 as well as a path leading to capacitor C2. Ex. 1005, Figs. 6A, 6B. In particular, Figure 6B shows that the signal passes through various circuit elements before reaching capacitor C1, and that the signal also passes through various other circuit elements before reaching capacitor C2. *Id.* at Fig. 6B. To illustrate, two annotated versions of Figure 6B provided by Petitioner are reproduced below. *See* Pet. 43, 46.



Each of these annotated versions of Figure 6B of Chern shows a partial diagram of a charge pump system with clock generator 42 and charge pump circuit 30C, which includes all the circuit elements of charge pump 30. *See* Ex. 1005, 7:1–6, 7:44–46. In the first annotated figure, the signal path from ring oscillator 12 and conditioning circuit 14 (*see id.* at Fig. 6A) leading to capacitor C1 is highlighted with a red arrow. Similarly, in the second annotated figure, the signal path from ring oscillator 12 and conditioning circuit 14 leading to capacitor C2 is highlighted with a red arrow. The parties do not dispute that the term “coupled” encompasses “indirectly connecting, such as through an intervening circuit.” *See* Pet. 26; PO Resp. 30. Accordingly, we find that Patent Owner’s argument does not undermine Petitioner’s showing that Chern discloses the recited first capacitor’s “second terminal coupled for receiving a boost signal” and the recited second capacitor’s “second terminal for receiving the boost signal.”

In view of the foregoing, we determine that Petitioner has demonstrated by a preponderance of the evidence that Chern anticipates claim 1.

3. Dependent Claim 2

Claim 2 depends from claim 1 and recites an “inverting buffer” as well as a “non-inverting buffer.” The claim requires the “inverting buffer” to have “an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor” and the “non-inverting buffer” to have “an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor.” For these

limitations, Petitioner provides two annotated versions of Figure 6B of Chern, which are reproduced below. Pet. 48, 51.

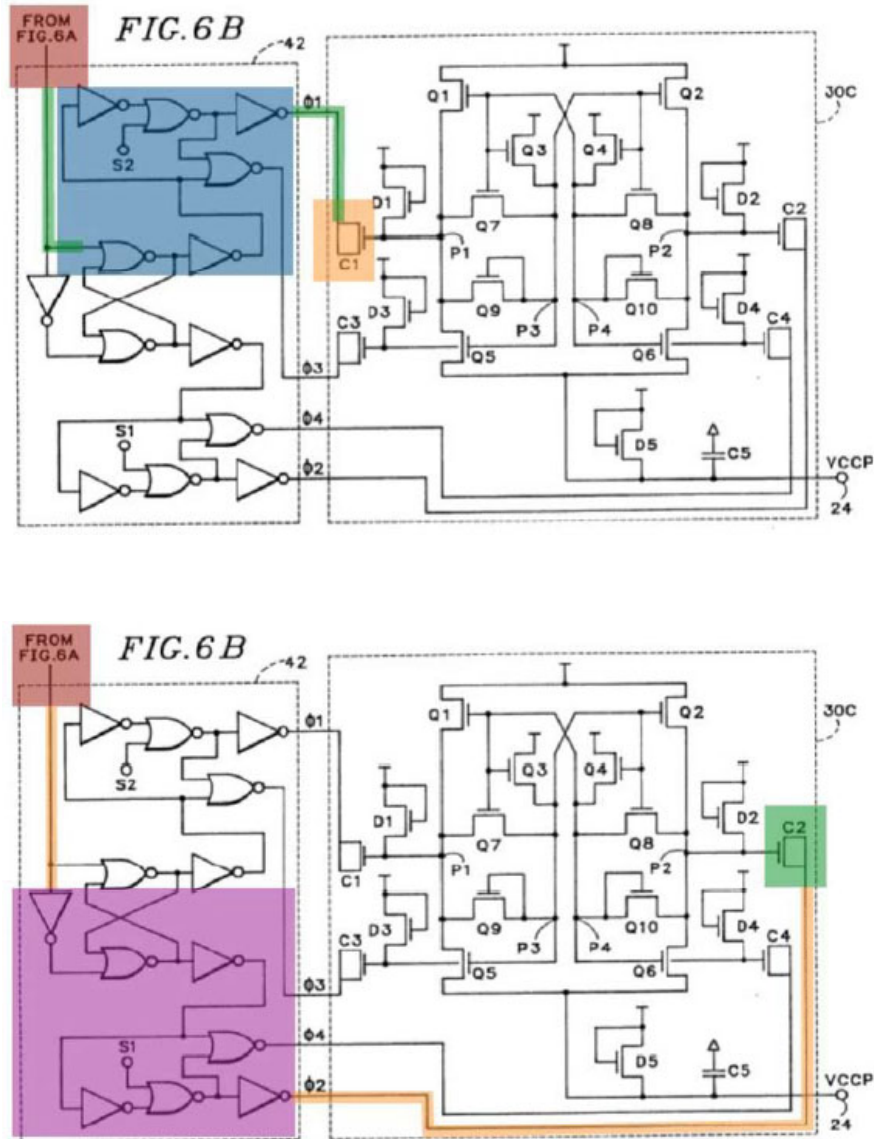
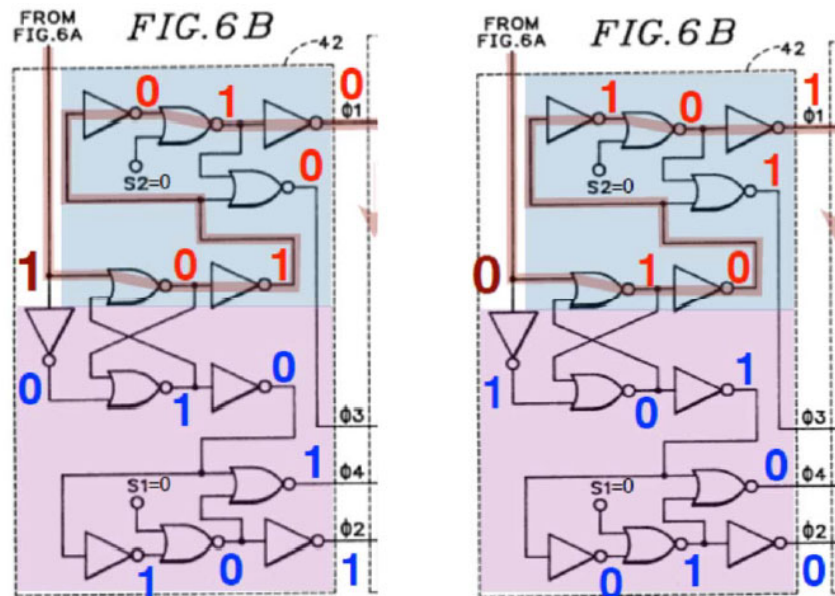


Figure 6B of Chern shown above, as annotated by Petitioner, is a partial diagram of a charge pump system including clock generator 42. See Ex. 1005, 2:60–63. Petitioner identifies the top half of clock generator 42 (highlighted in blue) as an “inverting buffer” and the bottom half of clock generator 42 (highlighted in purple) as a “non-inverting buffer.” Pet. 47, 50. As support, Petitioner directs us to where Chern teaches that clock

generator 42 receives a signal from ring oscillator 12 and conditioning circuit 14, and generates clock signals $\phi 1$ – $\phi 4$ by providing delay paths “for an inverted and non-inverted half to create a total of four clock signals.” *Id.* (citing Ex. 1005, 7:27–35). We note Petitioner’s prior contention with respect to claim 1 that the signal (highlighted in red) from ring oscillator 12 and conditioning circuit 14 corresponds to the recited “boost signal,” and that capacitor C1 (highlighted in orange) and capacitor C2 (highlighted in green) correspond to the recited “first capacitor” and the recited “second capacitor,” respectively, where the plate of capacitor C1 receiving clock signal $\phi 1$ corresponds to the recited “second terminal” of the “first capacitor,” and the plate of capacitor C2 receiving clock signal $\phi 2$ corresponds to the recited “second terminal” of the “second capacitor.” *Id.* at 48, 51.

Petitioner further provides two truncated versions of Figure 6B of Chern, with annotations, which are reproduced below. *Id.* at 49.



These truncated versions of Figure 6B, as annotated by Petitioner, focus on Chern's clock generator 42. According to Petitioner, they "show[] the behavior of all the logic gates when the input buffer signal from Figure 6A is high or '1', on the left, and the behavior [when] the input buffer signal is low or '0', on the right." *Id.* at 49. Here, the input buffer signal to which Petitioner refers is the signal from ring oscillator 12 and conditioning circuit 14. *See* Ex. 1005, Fig. 6A. Petitioner asserts that "the inverting buffer (in blue) inverts the input signal on its output, while the non-inverting buffer (in purple) produces as output the same value as the input." Pet. 49. Petitioner relies on the declaration testimony of Dr. Jacob. *Id.* (citing Ex. 1003 ¶¶ 167–168, 170).

Based on Petitioner's argument and evidence we are persuaded that Chern discloses the recited "inverting buffer" as well as the recited "non-inverting buffer."

In its Response, however, Patent Owner argues that Chern does not disclose these limitations. With respect to the "inverting buffer" limitation, Patent Owner refers to Petitioner's truncated versions of Chern's Figure 6B (*see* Pet. 49), which are reproduced above, and contends that "[t]he circuit in blue identified by Petitioner is not an 'inverting buffer'" because the blue circuit "is not a single input, single output circuit." PO Resp. 59. Patent Owner identifies three inputs, namely, "the signal that is generated by the conditioning circuit 14," "the signal S2," and "the lower NOR gate output received by the upper NOR gate from the bottom portion of four-phase clock generator 42 (highlighted in purple by Petitioner)." *Id.* at 59–60. Patent Owner further identifies two outputs, namely, signals $\phi 1$ and $\phi 3$. *Id.* at 60. In addition, Patent Owner contends that "even if the 'input' is assumed to be

the signal that is generated by the conditioning circuit 14, as Petitioner asserts, and $\phi 1$ is assumed to be the only output, $\phi 1$ is not always the inverted version of the input.” *Id.* at 60–61 (asserting that Chern’s signal $\phi 1$ is not an inverted version of the input when signal S2 is equal to 1). Patent Owner relies on the declaration testimony of Dr. Khatri. *Id.* at 59–61 (citing Ex. 2001 ¶¶ 169, 171–173).

Similarly, with respect to the “non-inverting buffer” limitation, Patent Owner contends that “[t]he circuit in purple identified by Petitioner is not a ‘non-inverting buffer’” because the purple circuit “is not a single input, single output circuit.” *Id.* at 59. For this circuit, Patent Owner identifies three inputs, namely, “the signal that is generated by the conditioning circuit 14,” “the signal S1,” and “the upper NOR gate output received by the lower NOR gate from the top portion of four-phase clock generator 42 (highlighted in blue by Petitioner).” *Id.* at 63–64. Patent Owner also identifies two outputs, namely, signals $\phi 2$ and $\phi 4$. *Id.* at 64. In addition, Patent Owner contends that “even if the ‘input’ is assumed to be the signal that is generated by the conditioning circuit 14, as Petitioner asserts, and $\phi 2$ is assumed to be the only output, $\phi 2$ is not always a non-inverted version of the input.” *Id.* at 64–65 (asserting that Chern’s signal $\phi 2$ is not a non-inverted version of the input when signal S1 is equal to 1). Patent Owner relies on the declaration testimony of Dr. Khatri. *Id.* at 63–65 (citing Ex. 2001 ¶¶ 174, 176–178).

We disagree with Patent Owner’s argument, which relies on both Patent Owner’s proposed claim construction of “inverting buffer” (i.e., “a circuit with a single input and a single output, where the output is always an inverted version of the input”) and Patent Owner’s proposed claim

construction of “non-inverting buffer” (i.e., “a circuit with a single input and a single output, where the output is always a non-inverted version of the input”). As discussed above, Patent Owner’s proposed construction of “inverting buffer” improperly requires a single input and a single output as well as an output that is always an inverted version of the input. *See supra* Part III.A.4. Patent Owner’s proposed construction of “non-inverting buffer” also improperly requires a single input and a single output as well as an output that is always a non-inverted version of the input. *See supra* Part III.A.5. Accordingly, that Chern’s circuit (shown with blue shading in Petitioner’s truncated versions of Figure 6B, which are reproduced above) may have multiple inputs and outputs and may sometimes generate an output that is an inverted version of the input does not undermine Petitioner’s showing that Chern discloses the recited “inverting buffer.” Similarly, that Chern’s circuit (shown with purple shading in the truncated versions of Figure 6B) may have multiple inputs and outputs and may sometimes generate an output that is a non-inverted version of the input does not undermine Petitioner’s showing that Chern discloses the recited “non-inverting buffer.”

In view of the foregoing, we determine that Petitioner has demonstrated by a preponderance of the evidence that Chern anticipates claim 2.

4. Dependent Claim 3

Claim 3, which also depends from claim 1, recites two additional limitations. The first limitation is “a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the

second phase signal.” For this limitation, Petitioner provides an annotated version of Figure 2 of Chern, which is reproduced below. Pet. 54.

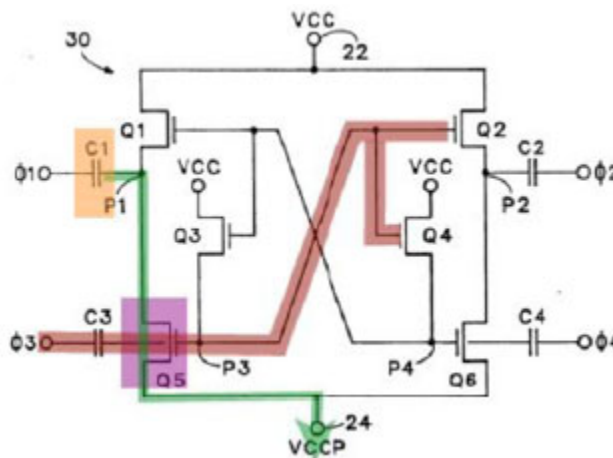


Figure 2 of Chern shown above, as annotated by Petitioner, depicts the basic circuit configuration for charge pump 30. *See* Ex. 1005, 3:10–11. Petitioner identifies Chern’s transistor Q5 (highlighted in purple) as a “third switch.” Pet. 52. As support, Petitioner directs us to where Chern teaches that the drain of transistor Q5 is coupled to one end of capacitor C1 (highlighted in orange) at circuit node P1, and that the source of transistor Q5 is coupled to output terminal 24. *Id.* at 52 (citing Ex. 1005, 3:24–27, 3:41–43). This is shown by the signal path highlighted in green. *See id.* at 54. We note Petitioner’s prior contention with respect to claim 1 that capacitor C1 corresponds to the recited “first capacitor,” where the plate of capacitor C1 that is coupled to the output terminal 24 through circuit node P1 and transistor Q5 corresponds to the “first terminal” of the “first capacitor.” *Id.* at 41, 52–53.

Petitioner further directs us to where Chern teaches that the gate of transistor Q5 is coupled to one end of capacitor C3 at circuit node P3, and that the other end of capacitor C3 receives clock signal $\phi 3$ (i.e., the recited “second phase signal”). *Id.* at 53 (citing Ex. 1005, 3:34–37). This is shown

by the signal path highlighted in red in Petitioner’s annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 54. Petitioner additionally points us to the declaration testimony of Dr. Jacob, who testifies that the gate of Chern’s transistor Q5 is controlled by clock signal $\phi 3$.

Ex. 1003 ¶ 183 (cited by Pet. 53). Dr. Jacob relies on Chern’s teaching that, when the time interval changes from E to F, clock signal $\phi 3$ changes to a logic high state, and transistor Q5 turns on to discharge capacitor C1 and inject current into the substrate or well through output terminal 24. *Id.* (citing Ex. 1005, 4:52–59). Dr. Jacob also relies on Chern’s teaching that, when the time interval changes from A to B, clock signal $\phi 3$ changes to a logic low state, and transistor Q5 turns off. *Id.* (citing Ex. 1005, 4:11–16).

The second limitation recited by claim 3 is “a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal.” For this limitation, Petitioner provides another annotated version of Figure 2 of Chern, which is reproduced below. Pet. 56.

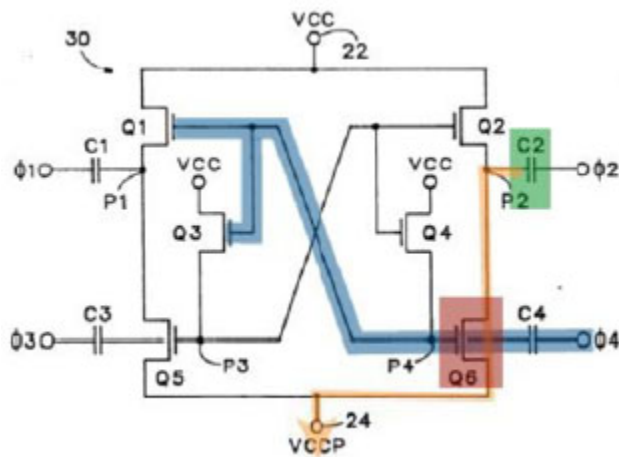


Figure 2 of Chern shown above, as annotated by Petitioner, illustrates the basic circuit configuration for charge pump 30. *See Ex. 1005, 3:10–11.* Petitioner identifies Chern’s transistor Q6 (highlighted in red) as a “fourth

switch.” Pet. 54–55. As support, Petitioner directs us to where Chern teaches that the drain of transistor Q6 is coupled to one end of capacitor C2 (highlighted in green) at circuit node P2, and that the source of transistor Q6 is coupled to output terminal 24. *Id.* at 52 (citing Ex. 1005, 3:28–31, 3:41–43). This is shown by the signal path highlighted in orange. As discussed above with respect to claim 1, Petitioner contends that capacitor C2 corresponds to the recited “second capacitor,” where the plate of capacitor C2 that is coupled to the output terminal 24 through circuit node P2 and transistor Q6 corresponds to the “first terminal” of the “second capacitor.” *Id.* at 44, 55–56.

Petitioner further directs us to where Chern teaches that the gate of transistor Q6 is coupled to one end of capacitor C4 at circuit node P4, and that the other end of capacitor C4 receives clock signal $\phi 4$ (i.e., the recited “first phase signal”). *Id.* at 55 (citing Ex. 1005, 3:38–41). This is shown by the signal path highlighted in blue in Petitioner’s annotated version of Figure 2 of Chern, which is reproduced above. *See id.* at 56. Petitioner additionally points us to the declaration testimony of Dr. Jacob, who testifies that the gate of Chern’s transistor Q6 is controlled by clock signal $\phi 4$. Ex. 1003 ¶ 188 (cited by Pet. 56). Dr. Jacob relies on Chern’s teaching that, when the time interval changes from B to C, clock signal $\phi 4$ changes to a logic high state, and transistor Q6 turns on to discharge capacitor C2 and inject current into the substrate or well through output terminal 24. *Id.* (citing Ex. 1005, 4:19–29). Dr. Jacob also relies on Chern’s teaching that, when the time interval changes from D to E, clock signal $\phi 4$ changes to a logic low state, and transistor Q6 turns off. *Id.* (citing Ex. 1005, 4:45–50).

Patent Owner does not dispute Petitioner’s analysis for the recited “third switch” or the recited “fourth switch.” Based on the entire trial record before us, we find that Petitioner has established that Chern discloses these limitations.

In view of the foregoing, we determine that Petitioner has demonstrated by a preponderance of the evidence that Chern anticipates claim 3.

C. Obviousness over Chern

Petitioner asserts that claims 1–3 of the ’875 patent would have been obvious over Chern. Pet. 57–72. According to Petitioner, its anticipation analysis “shows that there is no meaningful difference between the scope of the prior art and the limitations of [c]aims 1–3,” and it “is unaware of any secondary considerations of non-obviousness that would change this conclusion.” *Id.* at 57. Petitioner submits that Chern therefore “renders [c]aims 1–3 obvious, in addition and in the alternative to anticipating [c]aims 1–3.” *Id.* (citing *Schrader-Bridgeport Int’l v. Wasica Fin. GmbH*, IPR2014-00476, Paper 30 at 23–24 (PTAB July 22, 2015) (Final Written Decision)).

As discussed above, we determine that Petitioner has demonstrated by a preponderance of the evidence that Chern anticipates claims 1–3. *See supra* Part III.B.2–4. Because anticipation is the epitome of obviousness, a disclosure that anticipates a claim under 35 U.S.C. § 102 also renders the claim unpatentable under 35 U.S.C. § 103, absent any assertions of secondary considerations supporting non-obviousness. *See In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002) (“It is well settled that ‘anticipation is

the epitome of obviousness.”); *cf. Cohesive Techs., Inc. v. Waters Corp.*, 543 F.3d 1351, 1364 (Fed. Cir. 2008) (distinguishing anticipation from obviousness because “obviousness requires analysis of secondary considerations of nonobviousness, while secondary considerations are not an element of a claim of anticipation”). Accordingly, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3 would have been obvious over Chern.

IV. CONCLUSION

In summary:

Claims Challenged	Basis	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3	§ 102	Chern	1–3	
1–3	§ 103	Chern	1–3	
Overall Outcome			1–3	

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–3 of the ’875 patent are held *unpatentable*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2019-00104
Patent 6,127,875

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