

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC,
Patent Owner.

Case IPR2019-00638
Patent 7,827,370 B2

Before JAMESON LEE, J. JOHN LEE,
and JASON M. REPKO, *Administrative Patent Judges*.

LEE, *Administrative Patent Judge*.

DECISION
Denying Instituting of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

On January 29, 2019, Petitioner filed a Petition to institute *inter partes* review of claims 1–3, 5–7, 12–15, 19, and 25 of U.S. Patent No. 7,827,370 B2 (Ex. 1001, “the ’370 patent”). Paper 1 (“Pet.”). Patent Owner filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

To institute an *inter partes* review, we must determine that the information presented in the Petition shows “that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Having considered all submissions of both parties, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in establishing the unpatentability of any of claims 1–3, 5–7, 12–15, 19, and 25.

The Petition is *denied*, and no *inter partes* review is instituted.

B. Related Matters

The parties identify a civil action involving alleged infringement of the ’370 patent: *Memory Technologies, LLC v. Kingston Technology Corporation et al.*, No. 8-18-cv-00171-JLS-JDE (C.D. Cal.). Pet. 2, Paper 4, 1. Patent Owner further identifies the following terminated litigations involving the ’370 patent: *Memory Technologies, LLC v. SanDisk LLC et al.*, No. 8-16-cv-02163 (C.D. Cal.); *Certain Memory Devices and Components Thereof*, No. 337-TA-1034 (ITC). Paper 4, 1. Patent Owner additionally identifies another petition for *inter partes* review of claims in the ’370 patent: IPR2017-00868 (terminated prior to institution decision). *Id.* The petitioner in IPR2017-00868 is not the petitioner in this proceeding.

C. The '370 Patent

The '370 patent is directed to a method and apparatus that permanently write protects just a portion of a memory. Ex. 1001, Abstr. "Write protect" in that context means the data written into the protected area of memory cannot be written over or erased, like in the case of a read-only-memory. *See id.*, at 1:45–48. The '370 patent explains that preexisting memory cards did not provide the ability for a user to permanently write protect just a portion of a memory card, although it was possible to permanently write protect the entire card. *Id.* at 1:45–54. The '370 patent further explains that the standard Multi-Media Card (MMC) specification provided a command to write protect a portion of the memory card, but that protection can be canceled by another command and, thus, was not permanent. *Id.* at 1:66–2:1.

According to the '370 patent, a new definition for the MMC standard is provided for permanently write protecting a portion of a multi-media card. *Id.* at 2:6–8. A portion of the multi-media card can be permanently write protected while other portions are still available to the user. *Id.* at 2:8–12. Specifically, that is achieved by (1) identifying a bit in a specific data register of the memory card, (2) setting the bit to have a certain predefined value that causes a pre-existing write-protection command to mean permanent write protection of a part of the memory of the memory card, (3) writing information to that memory, and (4) executing the write-protection command concerning that memory. *Id.* at 2:12–21.

Claims 1, 12, and 25 are independent and reproduced below:

1. A method comprising:

write protecting at least one part of a memory by a command;
setting at least one bit in a data register configured to indicate that permanent write protection of the at least one part of the memory is allowed in order to redefine the command to allow permanent write protection, that cannot be unprotected by a command, of the at least one part of the memory; and
executing the command in order to permanently write protect said at least one part of the memory.

Ex. 1001, 5:55–65.

12. An apparatus comprising:

an interface controller arranged to write protect at least one part of a memory of said apparatus by a command;
a data register arranged to define at least one bit to indicate that permanent write protection of the at least one part of the memory is allowed;
a controller arranged to set the at least one bit in order to redefine the command to allow permanent write protection, that cannot be un-protected by a command, of the at least one part of the memory of said apparatus, and
the controller arranged to execute the command in order to permanently write protect said at least one part of the memory.

Id. at 6:31–43.

25. A memory device having stored therein instructions that, when executed, perform:

write protecting at least one part of a memory by a command;
setting at least one bit in a data register configured to indicate that permanent write protection of the at least one part of the memory is allowed in order to redefine the command to allow permanent write protection, that cannot be un-

protected by a command, of the at least one part of the memory; and

executing the command in order to permanently write protect said at least one part of the memory.

Id. at 8:10–21.

D. Evidence Relied Upon

Petitioner relies on the following references:¹

References		Date	Exhibit
Chevallier	U.S. Pub. App. 2004/0083346 A1	Apr. 29, 2004, filed Oct. 24, 2002	Ex. 1003
Toombs	U.S. Patent No. 6,279,114 B1	Aug. 21, 2001	Ex. 1004
Estakhri	U.S. Patent No. 6,262,918 B1	July 17, 2001	Ex. 1005

Petitioner also relies on the Declarations of R. Jacob Baker, Ph.D., P.E. (Ex. 1006).

E. The Asserted Ground of Unpatentability

Claims Challenged	Basis ²	References
1–3, 5, 6, 12–15, 25	§ 102(a) / 102(e)	Chevallier
1–3, 5, 6, 12–15, 25	§ 103(a)	Chevallier ³

¹ The '370 patent issued from Application 11/176,669, filed July 8, 2005.

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the challenged patent was filed before March 16, 2013, we refer to the pre-AIA version of § 103.

³ Petitioner actually asserts the ground as “Chevallier IN VIEW OF THE KNOWLEDGE OF A POSA [Person of Ordinary Skill in the Art].” Pet. 40.

Claims Challenged	Basis	References
1–3, 5–7, 12–15, 19, 25	§ 103(a)	Chevallier and Toombs
25	§ 103(a)	Chevallier, Toombs, and Estakhri

II. ANALYSIS

A. The Law on Anticipation and Obviousness

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference.

Therasense, Inc. v. Becton, Dickinson & Co., 593 F.3d 1325, 1332 (Fed. Cir. 2010); *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged in the same way as is recited in the claim, “the reference need not satisfy an *ipsissimis verbis* test.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990).

Thus, to establish anticipation, identity of terminology between the prior art reference and the claim is not required. “[I]t is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826 (CCPA 1968). The dispositive question is whether one skilled in the art would reasonably understand or infer from a prior art reference that every claim element as required by the

But it is unnecessary to expressly state “the knowledge of a person of ordinary skill in the art” in the alleged ground of obviousness, because all obviousness determinations are made on the basis of the level of ordinary skill in the art.

claim is disclosed in that reference. *Eli Lilly v. Los Angeles Biomedical Research Institute*, 849 F.3d 1073, 1074–75 (Fed. Cir. 2017); *see also Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003); *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991).

The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective indicia of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). One seeking to establish obviousness based on more than one reference also must articulate sufficient reasoning with rational underpinnings to combine teachings. *See KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007).

B. The Level of Ordinary Skill in the Art

Petitioner asserts that the level of ordinary skill in the art corresponds to “a person with a bachelor’s degree in electrical engineering or a closely related field, and two or three years of experience in the field of memory device circuit design.” Pet. 21–22. Patent Owner has not articulated a different level of ordinary skill and also has not disputed Petitioner’s statement of the level of ordinary skill. In this circumstance, we adopt the level of ordinary skill as articulated by Petitioner.

C. Claim Construction

For petitions filed on or after November 13, 2018, a claim shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary

meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b) (2018). Petitioner filed its Petition on January 29, 2019. Paper 1. Thus, we apply the claim construction standard as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) (“the *Phillips* standard”).

Claim terms are generally given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and even extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–1317. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

The specification may reveal a special definition given to a claim term by the patentee, or the specification may reveal an intentional disclaimer or disavowal of claim scope by the inventor. *Id.* at 1316. If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). The disavowal, if any, can be effectuated by language in the specification or the prosecution history. *Poly-America, L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016). “In either case, the standard for disavowal is exacting, requiring clear and unequivocal evidence that the claimed invention includes or does not include a particular feature.” *Id.*

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Nidec Motor*

Corp. v. Zhongshan Broad Ocean Motor Co. Ltd., 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner proposes a construction for five claim terms as follows:

1. “*a data register*” as meaning—a portion of memory containing information about a memory card—;
2. “*redefine the command to allow permanent write protection*” as meaning—cause a command that would not result in permanent write protection to result in permanent write protection—;
3. “*wherein said at least one bit has a certain predefined value*” as meaning—the bit is set to a value associated with permanent write protection—;
4. “*wherein said at least one bit is reprogrammable*” as meaning—a bit set to allow permanent write protection when a command is executed may have its value changed so that permanent write protection does not always occur—; and
5. “*memory group*” as meaning—a segment of memory—.

Pet. 16–20.

Patent Owner has not proposed a construction for any claim term, and has not expressly disputed any of the proposed constructions by Petitioner. Implicit in Patent Owner’s arguments, however, is the position that “*redefine the command to allow permanent protection*” changes the meaning of the

command not just in any single instance but for all future executions of the command until the command is redefined again. To reach our decision on whether to institute review, we need to resolve that issue, under the *Phillips* standard, concerning the proper construction of “*redefine the command to allow permanent write protection*,” a phrase that is recited in all three independent claims 1, 12, and 25. We need not construe any other term.

“*redefine the command to
allow permanent write protection*”

Petitioner’s proposed construction—cause a command that would not result in permanent write protection to result in permanent write protection—lacks sufficient clarity. It is unclear whether a single instance of permanent write protection is sufficient to meet the limitation, or whether all future executions of the redefined command must result in permanent write protection until another redefinition occurs. We determine that, in the context of the Specification of the ’370 patent, the redefinition, when accomplished, applies to all future executions of the command until it is redefined again. It is insufficient to meet the limitation if, after the redefinition, the redefined command still may function the way it used to function prior to the redefinition.

The ’370 patent describes, in the Summary of the Invention portion of the Specification:

This partial permanent write protection is achieved by identifying a bit in a specific data register of the memory card, setting that bit to have a certain predefined value *that causes write protection command to mean permanent write protection* of part of the memory of the memory card

Ex. 1001, 1:12–21 (emphasis added). Here, the “write protection command” refers generally to all executions of that command and not just a special case

thereof. The cited text conveys that after the bit is set, the write protection command whenever executed will result in permanent write protection.

The '370 patent also describes:

First embodiment of the invention for partially write protecting a portion of a MMC 1 is to define the PERM_WRITE_PROTECT bit of the CSD [card-specific data register] 2 (bit 13) in such a way that setting of this bit does not as much protect the whole card 1. Instead the bit 13 will indicate that *all the write protect groups protected with SET_WRITE_PROT command 5 (CMD28) are permanently write protected and cannot be un-protected using CLR_WRITE_PROT command 5 (CMD29).*

Id. at 2:55–62 (emphasis added). The reference to the “SET_WRITE_PROT” command, which is redefined, refers generally to all executions of that command and not just a special case thereof. The cited text conveys that after the bit is set, the write protection command whenever executed will result in permanent write protection.

The '370 patent further describes:

Second embodiment of the invention for partially write protecting a portion of a MMC 1 is to define one of the unused CSD 2 bits to indicate that a portion of the multimedia card 1 is permanently write protected. This bit can for example be the bit 17 of the CSD 2, and it can for example be called PARTIAL_PERM_WP. The write protection of the portion of MMC 1 works similarly as the write protection in the method described above. *If the PARTIAL_PERM_WP bit is set in the CSD 2, the groups protected with SET_WRITE_PROTECT command 5 (CMD28) become permanently write protected, and cannot be un-protected using CLEAR_WRITE_PROTECT command 5 (CMD29).*

Id. at 3:8–30 (emphasis added). The reference to the “SET_WRITE_PROTECT” command, which is redefined, refers generally to all executions of that command and not just a special case thereof. The

cited text conveys that after the bit is set, the write protection command whenever executed will result in permanent write protection.

The Specification further indicates that the redefinition is effective for as long as the associated permanent write protection bit is not reprogrammed, i.e., reset. *Id.* at 3:31–37. We find no description in the Specification of the '370 patent that allows a redefined command to revert back to its original meaning without clearing or resetting the bit that was set to redefine the command. We determine that, in the context of the Specification of the '370 patent and under the *Phillips* standard of claim construction, the required redefinition must be such that all future executions of the redefined command will result in permanent write protection until the bit triggering the redefinition has been cleared or reset.⁴ It is not enough to meet the limitation if, after the redefinition, the redefined command still may function the way it used to function prior to the redefinition, i.e., providing temporary write protection.

Furthermore, because the phrase at issue refers to “the command,” we need to identify the antecedent basis for it in each claim. That antecedent basis in each of independent claims 1, 12, and 25 is a command that write protects at least one part of a memory. Therefore, we additionally determine that the command, prior to its being redefined, already write protects a portion of the memory, just not permanently. Such an understanding is fully

⁴ An example of such clearing is described in the Specification of the '370 patent. Ex. 1001, 3:32–37. In that example, the triggering bit is automatically cleared each time a SET_WRITE_PROTECT command is received, to provide the user an opportunity to set or not set the bit for that write protection command. *Id.*

consistent with the Specification of the '370 patent. Ex. 1001, 2:12–21; 2:59–62.

We further clarify that the “to allow” portion of the limitation “redefine the command to allow permanent write protection,” in the context of the Specification of the '370 patent as discussed above, means the redefinition itself does not immediately cause permanent protection to occur but must wait for the redefined command to be executed. In other words, redefining the command “allow[s]” the command to always cause permanent write protection *when it is executed*, from that point onward. It does not mean that after redefinition of the write protect command, execution of the redefined command may, but does not have to, result in permanent write protection. This understanding follows from the Specification as discussed above and also is consistent with the construction Petitioner has proposed—cause a command that would not result in permanent write protection to result in permanent write protection.

- D. Alleged Unpatentability of Claims 1–3, 5, 6, 12–15, and 25 as Anticipated by Chevallier
1. Chevallier (Ex. 1003)

Chevallier is directed to Flash memory and memory block protection. Ex. 1003 ¶ 2. Chevallier describes that memory blocks should be protected against unintended write operations and that one known method of protection uses locking of a memory block. *Id.* ¶ 6. Chevallier further describes that the use of a locking function still exposes the memory blocks to inadvertent or malicious corruption of data. *Id.* ¶ 7. Chevallier states that memory blocks may be inadvertently unlocked and erased or overwritten.

Id. Chevallier further states that there is a need in the art to permanently lock memory blocks. *Id.*

Chevallier provides, in addition to the locking function for a memory block, which is not permanent, a secure function to provide permanent memory block protection. *Id.* ¶ 8. Chevallier describes that its embodiments differentiate between a lock function which is temporary and a secure function which is permanent. *Id.* ¶ 16. Chevallier describes that its temporary lock function control can be cleared and the memory blocks erased, and that its permanent secure function cannot be cleared once it is set. *Id.* Chevallier explains that according to its method, the permanent secure function is an added level of security in addition to the temporary locking function, and that the secure function overrides the temporary locking function in that even if the locking function is not set, setting of the secure function would lock the corresponding memory. *Id.* ¶ 29. That arrangement is shown in Chevallier's Figure 3, reproduced below:

301 BLOCK LOCKED	303 BLOCK SECURED	305 BLOCK STATUS
NO	NO	NOT LOCKED
NO	YES	LOCKED
YES	NO	LOCKED
YES	YES	LOCKED

Fig. 3

Figure 3 illustrates the locked or not locked status of a memory block based on application of the locking and/or secure functions. *Id.* ¶ 11.

Two bus cycles are used to implement the secure function. *Id.* ¶ 17. In the first bus cycle, the secure command is written to a specific register as control input. *Id.* ¶ 19. In the second bus cycle, the identity of the memory block or memory blocks to be secured is included in a data word and written to a specific unused address. *Id.* ¶ 21.

Chevallier describes that in one embodiment, the secure command is also the same command used for another function within the memory device, but that in that circumstance, the command would be written to a different register that is assigned to that different function. *Id.* ¶ 18. For example, Chevallier describes that in one embodiment, the secure command is the same as the locking command. *Id.* ¶¶ 8, 20.

Chevallier further discloses an embodiment in which the manufacturer of the memory device can, when making the memory device, enable or not enable the secure function capability of the manufactured device, by setting a secure function bit in the device to a predetermined value. *Id.* ¶¶ 37–38. For instance, if a customer desires that function, then the manufacturer can enable that function for the devices sold to that customer, and if the customer does not desire the secure function, then the manufacturer of the device would not enable it. *Id.* ¶ 37. Chevallier further describes that “[d]isabling the [secure] function bit of the present invention is not typically available to a user of the memory device.” *Id.* ¶ 40. Chevallier explains that “[m]aking this function bit available for general use would negate the benefits of the security that it provides.” *Id.*

2. Claims 1, 12, and 25

Each of claims 1, 12, and 25 requires setting at least one bit in a data register “to indicate that permanent write protection for at least one part of

the memory is allowed” and “to redefine the command to allow permanent write protection.” To meet this limitation, Petitioner relies on Chevallier’s disclosure of the setting of a secure function bit to enable the secure function, and Chevallier’s disclosure of an embodiment in which the secure command is the same as the lock command. Pet. 25 (citing Ex. 1003 ¶¶ 8, 16, 20, 33, 36; Ex. 1006 ¶ 154). Specifically, Petitioner states: “Chevallier discloses that when the secure function bit is set, the ‘same’ command ‘initiates the secure function’ which permanently secures ‘memory blocks specified in [a] control data word’ ‘against write and erase operations.’” Ex. 1003, ¶¶ 0008, 0033, 0036; Ex. 1006, ¶ 154.” *Id.*

The explanation provided by Petitioner, however, is unpersuasive with respect to the requirements of “to redefine the command to allow permanent write protection” as we have construed and discussed above. Nothing in Chevallier as identified by Petitioner indicates that setting the secure function bit to some value changes the meaning of the write protect command in the sense that it can no longer be used to provide temporary write protection, and can be used thereafter, until the next redefinition, solely to provide permanent write protection. The secure function bit of Chevallier, identified by Petitioner, serves only to enable the secure function (Ex. 1003 ¶¶ 37, 38, 40) and is nowhere described in Chevallier as changing the meaning of the locking command such that it no longer can be used to cause write protection of a memory block temporarily.

Indeed, with regard to Chevallier’s embodiment in which the secure command is the same as the locking command (Ex. 1003 ¶¶ 8, 20), the following description of Chevallier is instructive: “The secure command used in the present invention, in one embodiment, is also used for another

function within the memory device. However, in such an embodiment, the command is written to a different register that is assigned to that particular function.” Ex. 1003 ¶ 18. Thus, in Chevallier it is the location in memory where the command is written into that determines the meaning of the command for that one instance of execution, and not the setting of the secure function bit. We agree with Patent Owner (Prelim. Resp. 23–24) that setting the secure function bit in Chevallier does not redefine a command that previously meant temporary write protection to mean, thereafter, permanent write protection (unless it is redefined again). Indeed, based on the description of Chevallier, even after setting of the secure function bit, the lock command still serves to lock, not secure, if it is written to the recognized location for the lock command. *Id.* ¶¶ 18, 29; Fig. 3. Thus, it cannot reasonably be said that setting of the secure function bit redefines the locking command to a secure command. Moreover, Chevallier specifically states that its permanent secure function is in addition to its temporary locking function. *Id.* ¶ 29.

Petitioner also relies on claims 18 and 19 of Chevallier as disclosing the limitation of setting at least one bit in a data register to indicate that permanent write protection for at least one part of the memory is allowed, and “to redefine the command to allow permanent write protection.” Pet. 25–26. Specifically, Petitioner asserts:

Claims 18 and 19 of Chevallier disclose the “lock” command functioning as a “secure” command after enabling the secure function by the secure function bit. Ex. 1003, Claims 18–19; Ex. 1006, ¶ 155. In particular, Claim 18 recites “a plurality of lockable memory blocks” that are “temporarily lockable in response to a lock command.” Ex. 1003, Claim 18. Claim 18 discloses the method involves “enabling a secure function,”

which claim 19 discloses “is enabled by a non-volatile secure function bit.” *Id.*, Claims 18–19. Claim 18 further discloses “submitting the lock command to the memory device to activate the secure function.” *Id.*, Claim 18.

Id. These claims, however, limitation of setting at least one bit in a data register to indicate that permanent write protection for at least one part of the memory is allowed, and “to redefine the command to allow permanent write protection.”

These claims, however, are consistent with the disclosure of Chevallier discussed above, namely using the same command for the lock function and for the secure function even after the secure function is enabled. Claim 18 recites, “submitting the *lock command* to the memory device to activate the secure function” (emphasis added). Although claims 18 and 19 disclose enabling the secure function, they do not disclose that the lock command no longer performs the lock function. As with the Chevallier’s embodiments discussed above, Petitioner does not adequately explain how claims 18 and 19 necessarily disclose redefining the lock command to always perform permanent write protection, as required to satisfy the limitation at hand. Rather, when read in the context of the whole reference, they disclose that the location in memory into which the command is written, and not the value of a secure function bit, is used to determine which function the command performs. Indeed, claim 18 recites that the lock command is submitted “to the memory device” to activate the secure function.

For reasons discussed above, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claim 1, 12, and 25 is anticipated by Chevallier.

3. Claims 2, 3, 5, 6, and 13–15

Each of claims 2, 3, and 5 depends from claim 1, and claim 6 depends from claim 5. Thus, claims 2, 3, 5, and 6 all incorporate the limitations from claim 1. Petitioner's discussions of claims 2, 3, 5, and 6, however, do not relate to and do not cure the deficiency of the Petition as discussed above with respect to claim 1. Thus, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claims 2, 3, 5, and 6 is anticipated by Chevallier.

Claim 13 depends from claim 12; claim 14 depends from claim 13; and claim 15 depends from claim 14. Thus, claims 13, 14, and 15 all incorporate the limitations from claim 12. Petitioner's discussions of claims 13–15, however, do not relate to and do not cure the deficiency of the Petition as discussed above with respect to claim 12. Thus, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claims 13–15 is anticipated by Chevallier.

E. Alleged Unpatentability of Claims 1–3, 5, 6, 12–15, and 25 as Obvious over Chevallier

1. Claims 1, 12, and 25

Noting that anticipation is the epitome of obviousness, Petitioner asserts that because claims 1, 12, and 25 are anticipated by Chevallier, they would have been rendered obvious by Chevallier. Pet. 41. Thus, Petitioner's assertion of obviousness on this rationale is no better than its assertion of anticipation by Chevallier. We already determined above that Petitioner has not shown a reasonable likelihood that it would prevail in establishing that Chevallier anticipates any one of claims 1, 12, and 15.

Alternatively, Petitioner argues:

To the extent that Chevallier does not explicitly recite that the “secure function bit” is set in order to “redefine” the lock command to become the (permanent) secure command, as recited in Claims 1, 12, and 25, it would be obvious to use the bit in that manner, for example, to eliminate any ambiguity as to whether the command meant “lock” or “secure.” Ex. 1006, ¶¶ 259, 270, 276.

Id. at 41–42. The argument is unpersuasive for reasons explained below.

Petitioner does not affirmatively take the position that one with ordinary skill in the art would have found ambiguity in Chevallier’s embodiment in which the same command is used both for “locking” and for “securing.” In that regard, Petitioner refers to “any” ambiguity. The same is true with respect to Dr. Baker, who testifies: “a person having ordinary skill in the art would have been particularly motivated to use the secure function bit in that circumstance because doing so would eliminate *any ambiguity* as to whether the command meant ‘lock’ or ‘secure.’” Ex. 1006 ¶¶ 259, 270, 276 (emphasis added). Also, neither Petitioner nor Dr. Baker in the cited paragraphs of his Declaration addresses the specific disclosure in Chevallier that implements using one command to cause “locking” and the same command to cause “securing.” Chevallier describes: “The secure command used in the present invention, in one embodiment, is also used for another function within the memory device. However, in such an embodiment, the command is *written to a different register that is assigned to that particular function.*” Ex. 1003 ¶ 18 (emphasis added). Thus, there is no “ambiguity” as to whether the command means “lock” or “secure” in any instance because Chevallier uses different registers to distinguish between them. We are not sufficiently persuaded that there is ambiguity in Chevallier’s

disclosure to be resolved. Petitioner's assertion of a motivation that lies in resolving an ambiguity is not sufficiently supported by the record.

Petitioner also argues, assuming that there is ambiguity: "A POSA [person of ordinary skill in the art] would understand that Chevallier's secure function bit, which enables and disables the secure function, *could* provide the beneficial specificity—if the secure function is not enabled, then the command results in the lock function; if the bit is enabled, then the command results in the secure function." Pet. 42 (emphasis added). This argument also is not persuasive. The issue is not whether one with ordinary skill in the art "could" perform an operation but whether one with ordinary skill in the art, without application of improper hindsight, would have reason and want to do so. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015); *Fresenius USA, Inc. v. Baxter Intern., Inc.*, 582 F.3d 1288, 1299 (Fed. Cir. 2009).

Here, whether one with ordinary skill in the art would want to do in Chevallier what Petitioner proposes is not sufficiently explained. Chevallier expressly states that the secure function it provides is an added feature relative to the locking function. Ex. 1003 ¶ 29. Thus, the two functions are concurrently supported in Chevallier, not mutually exclusively at any one time. The limitation "to redefine the command to allow permanent write protection" as we have construed it above, is contrary to Chevallier's concept and implementation. Petitioner has not adequately explained why one with ordinary skill in the art would have wanted to modify Chevallier to eliminate concurrent support for both functions. For determining obviousness, the benefits, both lost and gained, in making a modification,

should be weighed against each other. *Winner Int’l Royalty Corp. v. Wang*, 202 F.3d 1340, 1348 (Fed. Cir. 2000).

For the foregoing reasons, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claims 1, 12, and 25 would have been obvious over Chevallier.

2. Claims 2, 3, 5, 6, and 13–15

Each of claims 2, 3, and 5 depends from claim 1, and claim 6 depends from claim 5. Thus, claims 2, 3, 5, and 6 all incorporate the limitations from claim 1. Petitioner’s discussions of claims 2, 3, 5, and 6, however, do not relate to and do not cure the deficiency of the Petition as discussed above with respect to claim 1. Thus, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claims 2, 3, 5, and 6 would have been obvious over Chevallier.

Claim 13 depends from claim 12; claim 14 depends from claim 13; and claim 15 depends from claim 14. Thus, claims 13, 14, and 15 all incorporate the limitations from claim 12. Petitioner’s discussions of claims 13–15, however, do not relate to and do not cure the deficiency of the Petition as discussed above with respect to claim 12. Thus, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claims 13–15 would have been obvious over Chevallier.

F. Alleged Unpatentability of Claims 1–3, 5–7,
12–15, 19 and 25 as Obvious over Chevallier and Toombs

1. Toombs

Toombs discloses providing write protection of any combination of memory groups within a multimedia memory card. Ex. 1004, 29:40–46. Toombs discloses a Card Specific Data register (CSD) in the memory card

that provides information to the memory card host for determining the communication protocol between the host and the memory card and how memory card content is accessed. *Id.* at 9:42–55, 10:23–26. The PERM_WRITE_PROTECT field of the CSD register provides data indicating permanent write protection of the entire memory card by overwriting or erasing, i.e., permanently disabling all write and erase commands for the memory card. *Id.* at 12:56–61. The TMP_WRITE_PROTECT field of the CSD register provides data indicating temporary write protection of the entire memory card against overwriting and erasing and can be reset. *Id.* at 12:62–67. The WP_GRP_SIZE field of the CSD register provides data indicating the size of a write protected group. *Id.* at 12:17–24.

2. Claims 1, 12, and 25

Petitioner alternatively adds Toombs to combine with Chevallier, to buttress its already presented obviousness assertions regarding the claim limitation of setting at least one bit in a data register “to redefine the [write protection] command to allow permanent write protection.” Pet. 45–48. According to Petitioner, Toombs discloses providing supplemental information to control the meaning of particular commands, thus redefining those commands. *Id.* at 45. For reasons discussed below, we are not persuaded either that Toombs describes using supplemental information to redefine the meaning of a command, or that Petitioner has articulated sufficient reasoning with rational underpinning to make Petitioner’s proposed combination.

Petitioner asserts:

For example, Toombs discloses a WP_GRP_ENABLE bit in the CSD register that “is used to indicate whether the write protection group is enabled.” Ex. 1004, 12:25-28. A SET_WRITE_PROT command can be used to “set[] the write protection of [] addressed write-protect group” only if the WP_GRP_ENABLE bit is set to 1 in the CSD register. *Id.*, 30:3–12. As another example, a READ_HBL_LEN field in the CDSD register controls the maximum size of a block of data that can be read using a command READ_SINGLE_BLOCK command. *Id.*, 20:5–17.

Toombs also discloses a PERM_WRITE_PROTECT bit that, when set, permanently protects the memory card such that “all write and erase commands for this card are permanently disabled.” Ex. 1004, 12:56–61. Toombs’ permanent write protection thus cannot be cleared by a command, such as Toombs’ CLK_WRITE_PROT command that clears temporary write protection. Ex. 1004, 30:8–12; Ex. 1006, ¶ 282.

Id. at 45–46. The above-quoted arguments are unpersuasive. We do not agree that enabling or disabling a command constitutes redefining the meaning of that command. In that regard, Petitioner offers no meaningful explanation. Based on our claim construction discussed above, a command would perform one function prior to the redefinition and a different function subsequent to the redefinition. Nothing described by Petitioner constitutes such redefinition of a command. As described by Petitioner, even the READ_SINGLE_BLOCK command referred to by Petitioner does not perform two different functions before and after a redefinition based on data entered in the READ_BL_LEN field in the CDSD register. Pet. 46. It always reads a single block of data. *Id.* Having a maximum size for a single block to be read does not redefine the command such that it has a different

meaning after redefinition, but merely disables it in certain circumstances, i.e., exceeding the maximum allowable size for a single readable block.

Furthermore, the addition of Toombs does not cure the deficiencies discussed above regarding lack of sufficient motivation to make the change in Chevallier to switch between the temporary locking function and the permanent securing function by redefining one command. For example, for making a change in Chevallier to incorporate redefinition of a command to execute a different function thereafter, Petitioner essentially still makes the same assertion, i.e., “to unambiguously specify, whenever the command is executed, which of the two functions is to be initiated.” *Id.* We have explained above that in Chevallier, there exists no such ambiguity, and that which one of two function is performed is determined by the location to which the command is written. Nor has Petitioner shown that Toombs suggests such an ambiguity. Petitioner’s assertion of ambiguity is not sufficiently supported by the record.

Further, as noted above, whether one with ordinary skill in the art would have wanted to do as Petitioner proposes is not sufficiently explained. Chevallier expressly states that the secure function it provides is an added feature relative to the locking function. Ex. 1003 ¶ 29. Thus, the two functions are concurrently supported in Chevallier, not mutually exclusive. The limitation “to redefine the command to allow permanent write protection” as we have construed it above, is contrary to Chevallier’s concept and implementation. Petitioner has not adequately explained why one with ordinary skill in the art would have wanted to modify Chevallier to eliminate concurrent support for both functions, including in light of Toombs.

Accordingly, Petitioner has not shown a reasonable likelihood that it would prevail in establishing unpatentability of any of claims 1, 12, and 25 as obvious over Chevallier and Toombs.

3. Claims 2, 3, 5–7, 13–15, and 19

Each of claims 2, 3, 5, and 7 depends from claim 1, and claim 6 depends from claim 5. Thus, claims 2, 3, 5, 6, and 7 all incorporate the limitations from claim 1. Petitioner's discussions of claims 2, 3, 5, 6, and 7, however, do not relate to and do not cure the deficiencies of the Petition as discussed above with respect to claim 1. Thus, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claims 2, 3, 5, 6, and 7 would have been obvious over Chevallier and Toombs.

Claims 13 and 19 each depend from claim 12; claim 14 depends from claim 13; and claim 15 depends from claim 14. Thus, claims 13, 14, 15, and 19 all incorporate the limitations from claim 12. Petitioner's discussions of claims 13–15 and 19, however, do not relate to and do not cure the deficiencies of the Petition as discussed above with respect to claim 12. Thus, Petitioner has not shown a reasonable likelihood that it would prevail in establishing that any of claims 13–15 and 19 would have been obvious over Chevallier and Toombs.

G. Alleged Unpatentability of Claim 25 as
Obvious over Chevallier, Toombs, and Estakhri

Petitioner relies on Estakhri for its teachings of a controller and a storage unit containing instructions for the controller, in case it is determined that the combined teachings of Chevallier and Toombs are found not to teach a memory device storing instructions that perform the function of a controller. Pet. 63–64. As applied by Petitioner, Estakhri does not relate to

or cure the deficiencies discussed above with regard to alleged obviousness of claim 25 over Chevallier and Toombs.

Accordingly, Petitioner has not shown a reasonable likelihood that it would prevail in establishing unpatentability of claim 25 as obvious over Chevallier, Toombs, and Estakhri.

H. Discretionary Denial of Petition under 35 U.S.C. § 325(d)

Patent Owner asserts that we should exercise discretion under 35 U.S.C. § 325(d) not to institute review in this case, for grounds of alleged unpatentability that are based in part on Toombs, because “Toombs was evaluated and applied by the Examiner against earlier versions of the claims in the Office Actions during prosecution.” Prelim. Resp. 28. We do not reach the issue of discretionary denial of the Petition, because we have determined, on the merits that Petitioner has not shown a reasonable likelihood that it would prevail in establishing unpatentability of any claim.

III. CONCLUSION

Petitioner has not shown a reasonable likelihood that it would prevail in establishing that at least 1 of the challenged claims 1–3, 5–7, 12–15, 19, and 25 is unpatentable.

IV. ORDER

It is

ORDERED that the Petition is *denied* and that no *inter partes* review is instituted for any challenged claim on any ground of unpatentability.

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