

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION,
Petitioner,

v.

BROADCOM CORPORATION,
Patent Owner.

IPR2019-01039
Patent 7,437,583 B2

Before THOMAS L. GIANNETTI, DANIEL J. GALLIGAN, and
NORMAN H. BEAMER, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, Renesas Electronics Corporation (“Petitioner”) challenges the patentability of claims 17, 18, and 20–26 of U.S. Patent No. 7,437,583 B2 (“the ’583 patent,” Ex. 1001), which is assigned to Broadcom Corporation (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 25 and 26 of the ’583 patent are unpatentable but has not proven by a preponderance of the evidence that claims 17, 18, and 20–24 of the ’583 patent are unpatentable. See 35 U.S.C. § 316(e) (“In an *inter partes* review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.”).

A. Procedural History

On May 3, 2019, Petitioner requested *inter partes* review of claims 17, 18, and 20–26 of the ’583 patent on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
17, 18, 20–24	103(a) ¹	Kiuchi, ² Van Hook ³

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. §§ 102 and 103 that became effective after the filing of the application for the ’583 patent. Therefore, we apply the pre-AIA versions of these sections.

² Kiuchi, JP H8-255034, published Jan. 10, 1996 (as translated) (Ex. 1008).

³ Van Hook, US 6,593,929 B2, issued July 15, 2003 (Ex. 1010).

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
21, 24	103(a)	Kiuchi, Van Hook, Alben, ⁴ Fallah ⁵
17, 18, 20–24	103(a)	Ninomiya, ⁶ Van Hook
21, 24	103(a)	Ninomiya, Van Hook, Alben, Fallah
25, 26	102(e)	Alben
25, 26	103(a)	Alben, Fallah, Kiuchi ⁷

Paper 2 (“Pet.”), 13. Patent Owner filed a Preliminary Response. Paper 6 (“Prelim. Resp.”); *see also* Papers 7 (Petitioner’s Reply to Patent Owner Preliminary Response), 8 (Patent Owner’s Sur-reply to Petitioner’s Reply). We instituted trial on all grounds of unpatentability. Paper 9 (“Inst. Dec.”), 13.

During the trial, Patent Owner filed a Response (Paper 15, “PO Resp.”), Petitioner filed a Reply (Paper 22, “Reply”), and Patent Owner filed a Sur-reply (Paper 25, “Sur-reply”).

An oral hearing was held on August 6, 2020, a transcript of which appears in the record. Paper 29 (“Tr.”).

B. Related Matters

The parties state that the ’583 patent is at issue in the following investigation at the International Trade Commission: *Certain Infotainment Systems, Components Thereof, and Automobiles Containing the Same*, Inv.

⁴ Alben, US 6,938,176 B1, issued Aug. 30, 2005 (Ex. 1009).

⁵ Farzan Fallah & Massoud Pedram, *Chapter 13: Circuit and System Level Power Management*, Kluwer Academic Publishers (2002) (Ex. 1006).

⁶ Ninomiya, US 5,764,968, issued June 9, 1998 (Ex. 1012).

⁷ Petitioner relies on Kiuchi in the alternative to teach certain subject matter in this ground, and, as discussed below in §§ II.H.2.d and II.H.3, we need not rely on these alternative arguments.

No. 337-TA-1119. Pet. 72; Paper 5, 2. Patent Owner states that the '583 patent is also at issue in *Broadcom Corporation v. Toyota Motor Corporation et al.*, No. 2-18-cv-00190-JRG (E.D. Tex.). Paper 5, 2.

C. Real Parties in Interest

Petitioner identifies itself and Renesas Electronics America, Inc. as real parties in interest. Pet. 71. Patent Owner identifies itself as the real party in interest. Paper 5, 2.

D. The '583 Patent and Illustrative Claims

The '583 patent generally relates to controlling clock signals in an electronic device. Ex. 1001, at code (57), 1:16–19. According to the '583 patent, in conventional integrated circuits, gates that controlled the flow of clock signals to particular devices were configured at the time of fabrication based on a particular circuit design and were not able to be reconfigured later. Ex. 1001, 2:5–11. Thus, according to the '583 patent, a device that ends up not being utilized will still receive clock signals, which wastes resources. Ex. 1001, 2:11–14. To address this purported drawback of the prior art, the '583 patent discloses distributing clock signals within an electronic device by controlling gates that control the flow of the clock signals. Ex. 1001, 2:34–52.

Challenged independent claims 17 and 25 are reproduced below.

17. A system for distributing clock signals within an electronic device, the system comprising:

at least one processor that determines a status of at least one gate that controls flow of a clock signal to at least one device coupled to said at least one gate; and

said at least one processor controls said at least one gate based on said determined status.

25. A system for distributing clock signals within an electronic device, the system comprising:
- a clock tree having a plurality of gates;
 - a hardware control logic block coupled to said clock tree that controls at least a portion of said plurality of gates;
 - at least one register that is controlled by a clock tree driver;
 - and
 - at least one processor that overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Robert Colwell, testifies that a person of ordinary skill in the art "would have a bachelor's degree in Electrical Engineering, Computer Science, or a similar discipline, with at least two years of experience working with power management and processor clock control." Ex. 1003 ¶ 89. Citing the testimony of its declarant, Mr. Bruce McNair, Patent Owner proposes a similar definition, arguing that a person of ordinary skill in the art "would have had a Bachelor's Degree in Electrical Engineering, Computer Science, or a similar discipline, with one or two years of experience in this or a related field" and "would also have been familiar with power management and processor clock control." PO Resp. 3 (citing Ex. 2008 ¶¶ 24–25).

The parties, therefore, differ on the amount of experience that is required with power management and processor clock control, and both parties' definitions are somewhat imprecise. Patent Owner's definition requires some familiarity without defining how much is enough while Petitioner's definition requires *at least* two years of experience, which is

open-ended and would include a person whose experience far exceeds that of a person of ordinary skill in the art. Neither party explains how its recited level of skill impacts the analysis such that application of one proposal versus the other would lead to different ultimate outcomes.

Based on the record before us, including the types of problems and solutions described in the '583 patent and the cited prior art, we determine that a person of ordinary skill in the art would have had a bachelor's degree in electrical engineering, computer science, or a similar discipline, with two years of experience working with power management and processor clock control. We further note that our analysis would be the same under either party's definition.

B. Claim Interpretation

The Petition was accorded a filing date of May 3, 2019. Paper 3, 1. In an *inter partes* review, for a petition filed on or after November 13, 2018, a claim “shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)).

The parties have agreed to constructions of several phrases appearing in the challenged claims. Pet. 10–11; PO Resp. 4. The only construction of consequence for this proceeding is the parties' agreement that the phrase “overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block” means “overwrites a status

of OFF or ON for at least a portion of said plurality of gates which is controlled by said hardware control logic block, the previous status having been written by said hardware control logic block.” Pet. 11; PO Resp. 4. We apply this construction below.

Patent Owner additionally argues that the “plain and ordinary meaning” of “write” “requires a memory element such as a flipflop or a register.” PO Resp. 5. Patent Owner does not direct us to any intrinsic support for this proposed construction. See PO Resp. 5–6. Rather, Patent Owner relies on the testimony of its declarant Mr. McNair, and Patent Owner argues that Dr. Colwell, Petitioner’s declarant, agrees. PO Resp. 5 (citing Ex. 2008 ¶¶ 30–32; Ex. 2009 (transcript of deposition of Dr. Colwell), 10:18–13:22).

We do not agree with Patent Owner’s additional requirement. First, when asked if “one of ordinary skill would view a write *outside of the ’583 patent* to require some sort of a storage element, like a register or a flip-flop,” Dr. Colwell testified, “I don’t think I said ‘require.’ But I think it suggests that that’s what they would expect normally.” Ex. 2009, 12:15–21 (emphasis added). Dr. Colwell further testified that “it’s not clear what the ’583 patent means.” Ex. 2009, 13:2–3. Thus, we do not see agreement between the experts on this point.

Second, even if the experts agreed, we must still construe a claim in light of the specification. See *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc) (internal quotation and citation omitted) (“[T]he specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.”); see also *DePuy Spine, Inc. v. Medtronic Sofamor Danek*,

Inc., 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17) (“In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.”). As Petitioner correctly points out, the Specification of the ’583 patent does not support requiring the hardware control logic block to write to a memory element to set the status of a gate. See Reply 25 (citing Ex. 1001, 4:57–60). The ’583 patent states that “[r]eturning to FIG. 2a, the clock tree block 210 may comprise a plurality of gates that may be controlled by the hardware control logic block 210 and/or the clock tree driver block via the register block 208.” Ex. 1001, 4:57–60. Figure 2a shows “HW Control Logic” 206 connected to “Clock Tree” 210 separately from “Registers” 208, and Figure 3 shows “Hardware Control Logic” 334 connecting to the gates separately from “Registers” 342. Ex. 1001, Figs. 2a, 3. Thus, the ’583 patent shows the hardware control logic block does not need to write to a memory element such as a flipflop or a register to write a gate’s status, i.e., to set the gate to ON or OFF.

For the foregoing reasons, we apply the parties’ construction as agreed without Patent Owner’s additional requirement.

The parties also disagree on what “at least one processor” in claim 25 encompasses, but we do not need to resolve the dispute over claim construction to resolve the patentability issues before us. See Pet. 11–13; PO Resp. 6–8. No other terms require express construction to resolve the patentability disputes before us. See, e.g., *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary

to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (citing *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990)).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence.⁸ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

⁸ Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.

*D. Obviousness over Kiuchi and Van Hook
(Claims 17, 18, and 20–24)*

Petitioner asserts that claims 17, 18, and 20–24 of the '583 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Kiuchi and Van Hook. Pet. 14–30.

1. Kiuchi

Kiuchi discloses a device with multiple clock control gate circuits for allowing and stopping the supply of clock signals at connected function circuits. Ex. 1008, code (57). Figure 1 of Kiuchi is reproduced below.

[FIG. 1]

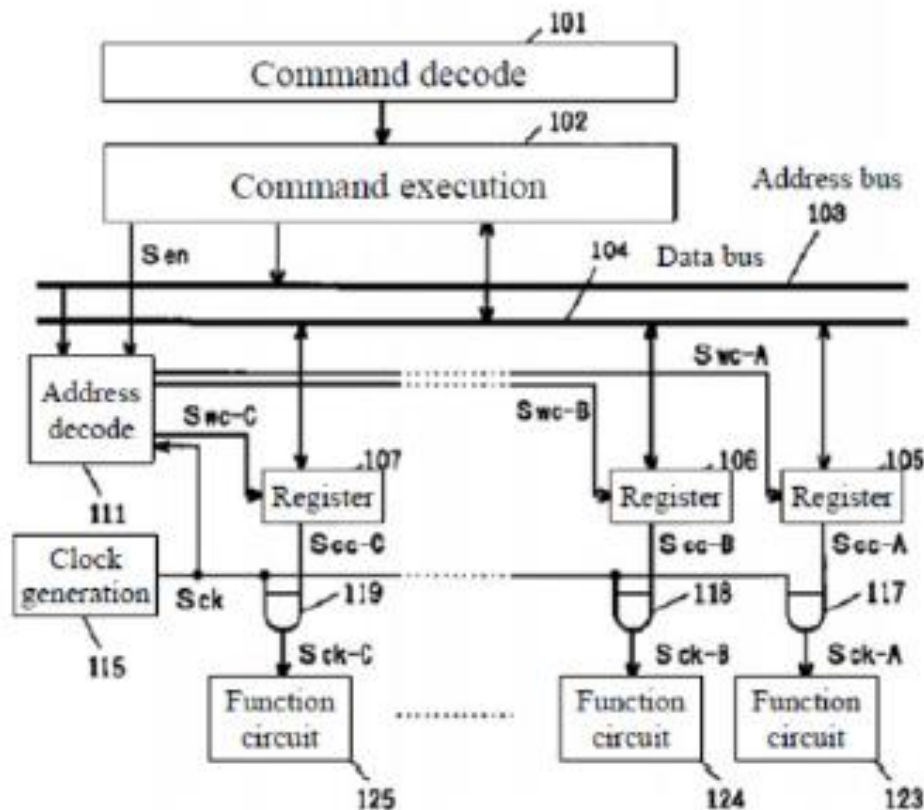


Figure 1 of Kiuchi, reproduced above, shows a device having a plurality of 1-bit registers 105, 106, and 107 connected, respectively, to AND gates 117, 118, and 119, which are connected, respectively, to function circuits 123, 124, and 125. Ex. 1008 ¶ 12. As shown in Figure 1, S_{ck} , the output of clock signal generation circuit 115, is the other input to each of AND gates 117, 118, and 119. Ex. 1008 ¶ 12. In operation, when 1-bit register 105 is set to “1,” clock signal S_{ck} passes through AND gate 117 to function circuit 123. Ex. 1008 ¶ 13. Kiuchi explains that register 105 is memory-mapped and can be controlled in the same manner as main memory by writing control data to the address at which the register is mapped. Ex. 1008 ¶ 13. The other 1-bit registers (e.g., 106, 107) are mapped and controlled in the same manner. Ex. 1008 ¶ 17.

2. *Van Hook*

Van Hook discloses a signal processor status register 470 that has field 471, which indicates when the signal processor is halted. Ex. 1010, 20:14–29. Van Hook discloses that, “to invoke processing of a new task list by signal processor 400,” main processor 100 “halts signal processor 400 (or checks to insure that the signal processor is halted) by writing to and/or reading from SP status register 470 (block 602).” Ex. 1010, 21:52–58.

3. *Independent Claim 17*

As noted above, independent claim 17 recites the following:

A system for distributing clock signals within an electronic device, the system comprising:

at least one processor that determines a status of at least one gate that controls flow of a clock signal to at least one device coupled to said at least one gate; and

said at least one processor controls said at least one gate based on said determined status.

Petitioner argues Kiuchi discloses a processor that writes to registers to allow or stop the clock supply to function circuits. Pet. 20–21 (citing Ex. 1008 ¶¶ 13, 19, Figs. 1, 3, 5, 7; Ex. 1003 ¶¶ 98–108). As discussed above, Kiuchi discloses registers that control the flow of a clock signal through AND gates to function circuits. Ex. 1008 ¶¶ 12–13, Fig. 1. Referring to Figure 1, Kiuchi explains that commands given to the command decoder come from a “central processing device.” Ex. 1008 ¶ 12. Kiuchi also discloses that the registers are readable and writeable. Ex. 1008 ¶ 13.

Petitioner argues that, although Kiuchi discloses registers that indicate whether a gate is ON or OFF (i.e., the gate’s status) and that can be read by a processor, “Kiuchi does not explicitly disclose its processors reading from a register to determine the status of a clock gate and then writing to the register based on the determined status.” Pet. 21 (citing Ex. 1003 ¶ 100). Petitioner argues Van Hook discloses that its main processor 100 reads field 471 in signal processor status register 470 to determine if the signal processor is halted and writes to “SET HALT” field 481 when it wants to halt the signal processor. Pet. 22 (citing Ex. 1010, 21:52–58, Fig. 7J). Petitioner contends that Van Hook’s “HALT” field 471 indicates whether the clock to the signal processor is halted and that “SET HALT” field 481 and “CLR HALT” field 480 are used, respectively, to stop and start the clock to the signal processor. Pet. 22 (citing Ex. 1010, 21:52–58, Fig. 7J; Ex. 1003 ¶¶ 69–75, 102).

Petitioner notes that “SP status register 470 describes halting of signal processor 400” but argues that “other sections of Van Hook clarify that halting refers to stopping a clock,” referring to Van Hook’s description of “START GCLK” field 536(4) in Figure 21D. Pet. 18–19 (citing Ex. 1008,

49:17–36, Fig. 21D; Ex. 1003 ¶¶ 77–80). In particular, Van Hook discloses that, “[w]hen reading this register 534, main processor 100 can determine . . . whether the display processor graphics clock is started (field 536(4) When writing to this same register 534, main processor 100 (or signal processor 400) can . . . start or stop the display process (fields 538(3), 538(4)” Ex. 1008, 49:17–36, *quoted in* Pet. 19. Petitioner’s declarant, Dr. Colwell, testifies that “[p]ersons of skill would have understood that the concepts of ‘halting’ (used in SP status register 470) and ‘freezing’ (status/command register 514) are similar” and that, “because Van Hook describes ‘freezing’ in terms of starting or stopping a clock signal, a [person of ordinary skill in the art] would have likewise understood that the concept of ‘halting’ would be used in a similar fashion.” Ex. 1003 ¶ 80.

Petitioner argues that a person of ordinary skill in the art would have combined Kiuchi’s disclosure of controlling clock gates with “Van Hook’s disclosure of a CPU reading from a status/command register to determine a status of a coprocessor’s clock and then conditionally write to the register to turn the clock ON or OFF” in order “to improve performance by reducing unnecessary register writes.” Pet. 23 (citing Ex. 1003 ¶¶ 104–105). Petitioner’s contentions, therefore, depend on Van Hook’s alleged disclosure that a halted processor means that the clock is stopped.

Patent Owner argues that “Van Hook merely discloses determining whether a signal processor 400 is halted and starting/halting signal processor 400” and that “[h]alting a processor is not the same as controlling clock signals.” PO Resp. 10 (citing Ex. 2008 ¶¶ 50–54). Patent Owner relies on testimony from Mr. McNair, who disagrees with Petitioner’s and Dr. Colwell’s assessment that Van Hook uses halting to mean stopping a

clock. Ex. 2008 ¶¶ 50–54, *cited in* PO Resp. 10. Mr. McNair testifies that “Van Hook does not describe register 470 as having anything to do with a clock or clock gate; it instead shows the status of a signal processor 400.” Ex. 2008 ¶ 51. Mr. McNair further testifies that “Van Hook shows that the system can write to register 470 to halt a processor or read from register 470 to determine whether a processor is halted. But it makes no mention of a clock at all in this section.” Ex. 2008 ¶ 51 (citing Ex. 1010, 21:52–64). As to Dr. Colwell’s testimony that “Van Hook makes clear that halting a coprocessor involves stopping its clock” (Ex. 1003 ¶ 78), Mr. McNair testifies that stopping a clock may be one way to halt a processor but that there are other ways, such as using a HALT instruction, which “generally just instructs the computer to temporarily halt the fetching and execution of instructions.” Ex. 2008 ¶ 52.

Weighing the evidence before us, we credit Mr. McNair’s testimony that halting in Van Hook does not mean stopping the clock over Dr. Colwell’s testimony on the subject. Dr. Colwell asserts that halting and freezing both refer to stopping a clock in Van Hook and that “[m]ain processor 100 reads START GCLK bit 536(4) to determine whether display processor 500’s clock is operating or stopped and writes FREEZE bits 538(3) and (4) to start or stop the clock.” Ex. 1003 ¶ 80. Dr. Colwell does not adequately explain why “FREEZE” fields (538(3) and 538(4)) in the command register correlate with the “START GCLK” field in the status register rather than the “FREEZE” field 536(2) in the status register. See Ex. 1003 ¶¶ 79–80. Van Hook describes “FREEZE” field 536(2) in the status register as showing “whether the display processor is stalled waiting

for access to main memory 300 (field 536(2).” Ex. 1010, 49:17–31. Thus, Van Hook does not describe freezing in terms of a clock signal.

Van Hook further describes the halting of the display processor as follows:

Display processor 500 halts *if its command buffer RAM 516 is empty* (i.e., it has processed all of the commands in the buffer, which buffer acts as a FIFO). Main processor 100 or signal processor 400 can determine if display processor 500 has halted by reading display processor status register 534 and may, if desired, pass the display processor a command that stalls the display processor temporarily (see “Sync Full” command in FIGS. 46–118).

Ex. 1010, 50:1–8 (emphasis added). In this passage, Van Hook uses the term “halts” to mean that display processor 500 stops when it has finished its tasks, which is consistent with Mr. McNair’s testimony that there are ways to halt a processor other than stopping its clock or cutting power. Ex. 2008 ¶ 52. For example, Mr. McNair describes the use of special instructions to halt computer operations as follows:

It is very common for computers, microcontrollers and signal processing devices, since the earliest and certainly all that I have used, to have a HALT instruction, which will generally not use cessation of power or disabling a clock to stop operation. Instead, the HALT instruction generally just instructs the computer to temporarily halt the fetching and execution of instructions.

Ex. 2008 ¶ 52. In Van Hook display processor 500 does not halt itself by stopping a clock signal that is an input to the display processor, as Petitioner’s analysis would suggest. Thus, in determining that a processor is halted, Van Hook does not teach determining the status of a clock gate.

Having considered the evidence and weighing the relevant testimony, we are not persuaded by Petitioner’s contention that in Van Hook, a halted

coprocessor means that “its clock is already stopped.” See Pet. 22. Because Petitioner relies on this alleged disclosure in Van Hook to teach “determin[ing] a status of at least one gate that controls flow of a clock signal,” we determine that Petitioner has not proven by a preponderance of the evidence that claim 17 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Kiuchi and Van Hook.

4. Dependent Claims 18 and 20–24

Petitioner’s obviousness contentions as to claims 18 and 20–24 do not cure the deficiencies noted above with respect to the contentions for claim 17, from which these claims depend. See Pet. 26–30. Therefore, Petitioner has not demonstrated by a preponderance of the evidence that claims 18 and 20–24 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Kiuchi and Van Hook.

*E. Obviousness over Kiuchi, Van Hook, Alben, and Fallah
(Claims 21 and 24)*

Petitioner asserts that claims 21 and 24 of the ’583 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Kiuchi, Van Hook, Alben, and Fallah. Pet. 30–38. Petitioner’s contentions in this ground rely on, but do not cure the deficiencies in, the contentions for claim 17, discussed above in § II.D.3. See Pet. 30–38. Therefore, Petitioner has not demonstrated by a preponderance of the evidence that claims 21 and 24 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Kiuchi, Van Hook, Alben, and Fallah.

*F. Ninomiya Obviousness Grounds
(Claims 17, 18, and 20–24)*

Petitioner asserts that claims 17, 18, and 20–24 of the '583 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Ninomiya and Van Hook and that claims 21 and 24 of the '583 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Ninomiya, Van Hook, Alben, and Fallah. Pet. 38–53.

Petitioner acknowledges that Ninomiya “does not explicitly disclose CPU 11 reading from clock drive control registers 122 or 135 to determine a status of a gate, and then writing to these registers depending the determined status.” Pet. 42. Referring to its contentions in the ground based on Kiuchi and Van Hook, Petitioner argues that “Van Hook renders obvious main processor 100 reading from a register to determine whether a clock in a coprocessor is ON or OFF, and then turning the clock OFF or ON depending on the determined status.” Pet. 42. As discussed above in § II.D.3 (addressing challenge based on Kiuchi and Van Hook), we are not persuaded that Van Hook discloses that a halted processor means that the clock to the processor is stopped, and, therefore, Petitioner’s contentions in this ground are deficient for the same reasons discussed in § II.D.3.

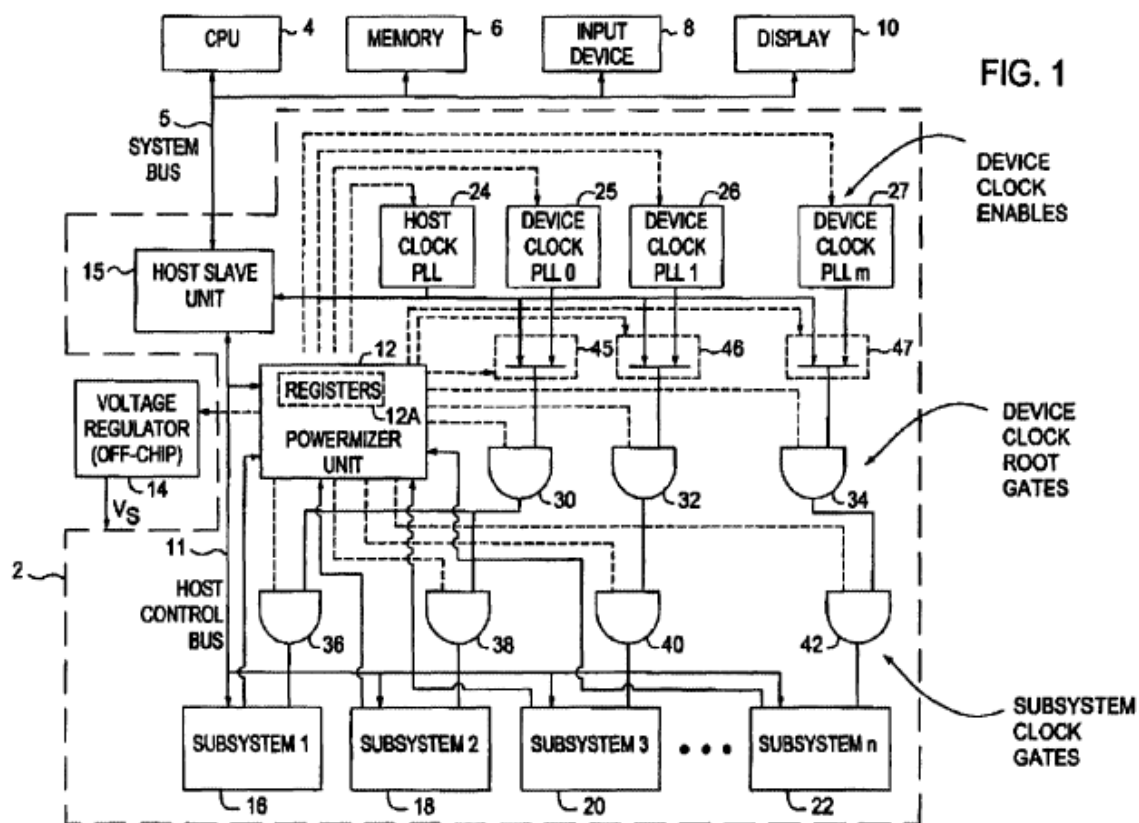
Therefore, Petitioner has not demonstrated by a preponderance of the evidence that claims 17, 18, and 20–24 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Ninomiya and Van Hook or that claims 21 and 24 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Ninomiya, Van Hook, Alben, and Fallah.

*G. Anticipation by Alben
(Claims 25 and 26)*

Petitioner asserts that claims 25 and 26 of the '583 patent are unpatentable under 35 U.S.C. § 102(e) as anticipated by Alben. Pet. 53–63.

1. Alben

Alben discloses techniques for power management in the device depicted below in Figure 1.



Alben's Figure 1, reproduced above, depicts control unit 12, which can control a clock tree for each subsystem by asserting control signals to AND gates (30, 32, 34, 36, 38, 40, 42). Ex. 1009, 5:45–6:46. Alben explains that “control unit 12 can be configured by CPU 4 (programmed with system software) to operate in any selected one of a number of different power management modes for controlling power consumption for each subsystem.”

Ex. 1009, 7:52–56. Alben discloses that system software can write a two-bit word to a register for each subsystem to specify one of four power management modes, FULLPOWER, AUTOMATIC, SUSPENDED, and RESERVED. Ex. 1001, 7:60–8:24. Further details of Alben’s disclosure are discussed in the analysis below.

2. *Claim 25*

a) *Preamble*

The preamble of claim 25 recites “[a] system for distributing clock signals within an electronic device.” Petitioner contends that Alben discloses “chip 2 with PLL clock generators 25-27 distributing clock signals to subsystems 16-22 via AND gates 30-42,” as shown in Figure 1, and therefore describes the subject matter recited in the preamble. Pet. 56 (citing Ex. 1003 ¶ 171).

Patent Owner does not dispute Petitioner’s contentions as to the subject matter recited in the preamble. *See generally* PO Resp. 27–43. We are persuaded by Petitioner’s contentions, and we find that Alben describes the subject matter recited in the preamble.⁹

b) *Clock tree*

Claim 25 recites that the system comprises “a clock tree having a plurality of gates.” Petitioner argues that Alben’s disclosure of a “device clock tree” having several AND gates describes this subject matter. Pet. 56 (quoting Ex. 1009, 5:45–52) (citing Ex. 1003 ¶ 172). Patent Owner does not

⁹ Because we find that Petitioner has shown that Alben describes this subject matter, we need not decide whether the preamble of claim 25 is limiting.

dispute Petitioner's contentions as to this subject matter. *See generally* PO Resp. 27–43.

We are persuaded by Petitioner's contentions. In particular, Alben discloses the following:

Each branch of a device clock tree that can be separately disabled by control unit 12 (and the clock asserted through such branch) is referred to as a subsystem clock. For example, the first subsystem clock is asserted through the branch from AND gate 30 through AND gate 36 to subsystem 16, and the second subsystem clock is asserted through the branch from AND gate 30 through AND gate 38 to subsystem 18.

Ex. 1009, 5:45–52. We find that Alben's disclosure of a “device clock tree” having AND gates describes “a clock tree having a plurality of gates,” as recited in claim 25.

c) Hardware control logic block

Claim 25 recites that the system comprises “a hardware control logic block coupled to said clock tree that controls at least a portion of said plurality of gates.” Petitioner argues that Alben's control unit 12 asserts control signals to AND gates and therefore describes this subject matter. Pet. 57–58 (citing Ex. 1009, 5:63–6:1, 6:18–24, 8:5–25, Fig. 1; Ex. 1003 ¶¶ 173–174). Patent Owner does not dispute Petitioner's contentions as to this subject matter and, in fact, agrees that Alben's control unit 12 controls the status of the gates. *See* PO Resp. 29–30 (“Control unit 12’ is the only disclosed control mechanism, and this is the only module that controls the status of the gates, regardless of the circumstances.”).

We are persuaded by Petitioner's contentions. Alben discloses the following:

Control unit 12 can also assert a control signal (indicative of a logical one or zero) to each of AND gates 30, 32, and 34 to

enable or disable each device clock (in the sense of allowing each device clock to be asserted, or preventing each device clock from being asserted, to the relevant subsystem or subsystems).

Ex. 1009, 5:63–6:1. We find that Alben’s disclosure of control unit 12 asserting control signals to AND gates to enable or disable device clocks describes “a hardware control logic block coupled to said clock tree that controls at least a portion of said plurality of gates,” as recited in claim 25.

d) Register controlled by clock tree driver

Claim 25 recites that the system comprises “at least one register that is controlled by a clock tree driver.” Petitioner contends that Alben’s register 12A describes “at least one register” and that Alben’s host slave unit 15 describes “a clock tree driver.” Pet. 58 (citing Ex. 1009, 6:36–59, 7:52–8:36, 10:24–12:52; Ex. 1003 ¶¶ 175–179). According to Petitioner, “[h]ost slave unit 15, which is separate from CPU 4, writes to register 12A in accordance with instructions issued from CPU 4.” Pet. 58 (citing Ex. 1009, 6:36–59, 7:52–8:36, 10:24–12:52).

Patent Owner does not dispute Petitioner’s contentions as to this subject matter. *See generally* PO Resp. 27–43.

We are persuaded by Petitioner’s contentions. Alben discloses that register 12A “includes a two-bit host register (called a ‘PM_SUBSYSTEM_CONTROL’ register” to which “[s]ystem software can write a two-bit word . . . to indicate the power management mode.”

Ex. 1009, 7:56–63. Alben discloses that “[h]ost registers are accessible via host slave unit 15,” which is also shown in Figure 1. Ex. 1009, 7:16–18, Fig. 1. Alben discloses that register 12A includes other registers as well, including “PM_DEVICE_CONTROL” register and “PM_HOST_CONTROL” register. Ex. 1009, 10:24–12:52. Thus, we find

that Alben describes “at least one register that is controlled by a clock tree driver.”

Petitioner alternatively argues that “Alben’s ‘system software’ running on CPU 4 discloses the claimed clock tree driver controlling register 12A” if “there is no requirement that the ‘clock tree driver’ must be separate from the claimed ‘at least one processor’ (*i.e.*, the clock tree driver can be software executing on a processor.[]).” Pet. 58–59 (citing Ex. 1009, 7:52–63). Patent Owner agrees with this interpretation of the claim, arguing that “the specification [of the ’583 patent] explains that the clock tree driver could be code existing on the processor.” PO Resp. 7 (quoting Ex. 1001, 4:1–7) (citing Ex. 2008 ¶ 33). Patent Owner also does not dispute Petitioner’s assertion that Alben’s system software running on the CPU describes the claimed “clock tree driver.” *See generally* PO Resp. 27–43.

Although we need not rely on Petitioner’s alternative argument in view of our finding above that Alben’s host slave unit 15 describes the claimed “clock tree driver,” we agree with Petitioner that Alben’s system software running on the CPU, which writes to register 12A via host slave unit 15 (Ex. 1009, 7:56–63), describes a “clock tree driver” under Patent Owner’s interpretation that “the clock tree driver could be code existing on the processor” (PO Resp. 7).

e) Processor that overwrites status of gates

Claim 25 recites that the system comprises “at least one processor that overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block.” As noted above in § II.B, the parties have agreed that the phrase “overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware

control logic block” means “overwrites a status of OFF or ON for at least a portion of said plurality of gates which is controlled by said hardware control logic block, the previous status having been written by said hardware control logic block.” Pet. 11; PO Resp. 4.

Petitioner argues that Alben’s disclosure of CPU 4 setting power management modes describes the claimed processor performing the overwriting operation. Pet. 60–62. Alben discloses four power management modes: “FULLPOWER,” “AUTOMATIC,” “SUSPENDED,” and “RESERVED.” Ex. 1009, 8:5–25. In FULLPOWER mode, “[n]o power management is performed on the subsystem,” whereas in AUTOMATIC mode “[c]ontrol unit 12 automatically performs power management on the subsystem with no system software intervention. The subsystem’s subsystem clocks are disabled automatically when doing so will not affect the proper behavior or performance of the subsystem.” Ex. 1009, 8:9–20. In SUSPENDED mode, “[a]ll of the subsystem’s subsystem clocks are disabled.” Ex. 1009, 8:21–22. Petitioner argues that, “in AUTOMATIC mode, control unit 12 may write a ‘0’ to an input of one of AND gates 30-42 to turn the clock gate OFF and conserve battery for a device” and then “CPU 4 may intervene to write to registers 12A to set FULLPOWER mode to force control unit 12 to overwrite the ‘0’ with a ‘1’ and force ON the clock gate for the device.” Pet. 61 (citing Ex. 1009, 2:58–67, 3:6–12, 8:9–20, Fig. 1; Ex. 1003 ¶ 183). Similarly, Petitioner asserts that CPU 4 can change the mode from AUTOMATIC to SUSPENDED and force control unit 12 to turn off a gate. Pet. 61–62 (citing Ex. 1009, 3:12–17, 8:26–36, Fig. 1; Ex. 1003 ¶ 183). Petitioner argues, therefore, that “by programming registers 12A, Alben discloses that CPU 4 overwrites a status of OFF or ON

for at least a portion of said plurality of gates which is controlled by said hardware control logic block, the previous status having been written by said hardware control logic block.” Pet. 62 (citing Ex. 1003 ¶ 183).

Patent Owner disagrees with Petitioner and argues that “[t]here is no dispute that control unit 12 controls a status of ON or OFF.” PO Resp. 35 (citing Ex. 1003 ¶ 84; Ex. 2008 ¶¶ 118–119). Patent Owner argues that CPU 4 writes to the PM_SUBSYSTEM_CONTROL register, which “will change the mode of control unit 12,” but Patent Owner argues that this “never causes control unit 12 to cede control.” PO Resp. 36 (citing Ex. 1009, 7:60–8:25). According to Patent Owner, “[i]t is the control unit 12, not the CPU 4, that actually uses the power mode to change ‘a status of OFF or ON for at least a portion of said plurality of gates.’” PO Resp. 35 (citing Ex. 1009, 8:21–25).

We agree with Patent Owner that it is undisputed that, in Alben, control unit 12 controls the gates because this is Petitioner’s position: “Control unit 12 controls gates 30-42 based on a mode of operation, including AUTOMATIC mode, FULLPOWER mode, and SUSPENDED mode.” Pet. 57 (citing Ex. 1009, 8:5–25). Alben discloses that “control unit 12 can be configured by CPU 4 (programmed with system software) to operate in any selected one of a number of different power management modes for controlling power consumption for each subsystem” and that “[s]ystem software can write a two-bit word to each ‘PM_SUBSYSTEM_CONTROL’ register to indicate the power management mode for the corresponding subsystem.” Ex. 1009, 7:52–63. Thus, CPU 4 writes to register 12A to set a particular power management mode under which control unit 12 controls the gates.

Under the parties' agreed construction, which requires a processor that "overwrites a status of OFF or ON for at least a portion of said plurality of gates which is controlled by said hardware control logic block, the previous status having been written by said hardware control logic block," we agree with Patent Owner that Petitioner has not shown that Alben describes the claimed subject matter under the exacting standard of anticipation. In particular, CPU 4, which Petitioner identifies as the claimed "at least one processor," writes to register 12A to set the power management mode, but Petitioner has not shown that any status in register 12A was previously "written by said hardware control logic block," i.e., Alben's control unit 12. Rather, Alben discloses that control unit 12 operates according to the power management mode set by CPU 4 in register 12A. Ex. 1009, 7:52–56 ("[C]ontrol unit 12 can be configured by CPU 4 (programmed with system software) to operate in any selected one of a number of different power management modes for controlling power consumption for each subsystem."); *see also* Pet. 57 ("Control unit 12 controls gates 30-42 based on a mode of operation, including AUTOMATIC mode, FULLPOWER mode, and SUSPENDED mode."). Thus, Alben's control unit 12 *reads* register 12A to determine which power management mode it should use, but Petitioner does not direct us to any disclosure in which control unit 12 *writes to* register 12A, such that any subsequent writing to register 12A by CPU 4 would satisfy the parties' agreed construction. For the same reasons, Petitioner's identification of instances in which control unit 12 will turn a clock on or off based on a change to the power management mode set by CPU 4 (Pet. 61–62) fails to show anticipation under the parties' agreed construction.

f) Determination on anticipation

Based on the foregoing, Petitioner has not demonstrated by a preponderance of the evidence that claim 25 is unpatentable under 35 U.S.C. § 102(e) as anticipated by Alben.

3. Claim 26

Because Petitioner has not proven anticipation of claim 25, Petitioner also has not demonstrated by a preponderance of the evidence that claim 26, which depends from claim 25, is unpatentable under 35 U.S.C. § 102(e) as anticipated by Alben.

*H. Obviousness over Alben, Fallah, Kiuchi
(Claims 25 and 26)*

Petitioner asserts that claims 25 and 26 of the '583 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Alben, Fallah, and Kiuchi. Pet. 63–71.

1. Fallah

Fallah is a chapter titled “Circuit and System Level Power Management” in the book *Power Aware Design Methodologies*. Ex. 1006. Petitioner asserts that Fallah was published in 2002 and is prior art under 35 U.S.C. § 102(b). Pet. 31–32. Patent Owner does not challenge the prior art status of Fallah. *See generally* PO Resp. We are persuaded that Petitioner has shown that Fallah qualifies as prior art under 35 U.S.C. § 102(b). *See* Ex. 1006, 4 (“Print ©2002 Kluwer Academic Publishers”).

Fallah discloses techniques for dynamic power management (DPM) that use hardware and software and identifies clock gating as a technique to lower power consumption. Ex. 1006, 6, 9, 19.

2. *Claim 25*

a) *Undisputed subject matter*

In this ground, Petitioner refers to its Alben anticipation contentions for the preamble and the limitations reciting “a clock tree having a plurality of gates,” “a hardware control logic block coupled to said clock tree that controls at least a portion of said plurality of gates,” and “at least one register that is controlled by a clock tree driver.” Pet. 63–64. For the reasons explained above in §§ II.G.2.a–d, we are persuaded by Petitioner’s contentions and find that Alben describes this subject matter.

b) *Processor that overwrites status of gates*

Claim 25 recites “at least one processor that overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block.” As discussed above in § II.G.2.e, Alben’s CPU 4 (“at least one processor”) writes to register 12A to set a power management mode and control unit 12 (“hardware control logic block”) reads register 12A and operates according to the power management mode set in that register. Ex. 1001, 7:52–8:25. We are not persuaded that this describes a processor that “overwrites a status of OFF or ON for at least a portion of said plurality of gates which is controlled by said hardware control logic block, the previous status having been written by said hardware control logic block,” under the parties’ agreed interpretation of this limitation. See § II.G.2.e above.

Petitioner argues that it would have been obvious to a person of ordinary skill in the art to have CPU 4 directly control the status of a gate in view of Fallah’s teachings of software-controlled power management techniques, such as clock gating. Pet. 67–70. Petitioner asserts that Fallah

discloses “various power management algorithms [that] can be implemented in *hardware and/or software*” and identifies advantages and disadvantages of hardware and software approaches. Pet. 68 (citing Ex. 1006, 9). Fallah explains that “Dynamic power management – which refers to a selective, shut-off or slowdown of system components that are idle or underutilized – has proven to be a particularly effective technique for reducing power dissipation in such systems,” and Fallah explains that DPM can be implemented in hardware and/or software, each having certain advantages over the other. Ex. 1006, 6, 9.

Petitioner also argues that Fallah “discloses ‘clock gating’ to remove selected clock pulses or turn off clocks entirely for devices that do not need them.” Pet. 68 (citing Ex. 1006, 9, 19). For example, Fallah identifies “clock gating” as one example of a power management technique. Ex. 1006, 19. Fallah explains that clock gating is “[a] simple and effective method for decreasing the dynamic power consumption” “by decreasing the switching activity in the” “[f]lip-flops of a circuit,” the “[g]ates in the fanout of the flip-flops,” and the “[c]lock tree.” Ex. 1006, 20.

Petitioner argues that “it would have been obvious to a person of ordinary skill in the art, in light of the combined teachings of the references, that simple and complex power management schemes using hardware and software control can be used for clock gating, and that software overrides of hardware should be used to implement complex power management schemes.” Pet. 69; *see also* Ex. 1003 ¶ 205 (Dr. Colwell providing testimony on this point). Petitioner argues that a person of ordinary skill in the art would have been motivated “to implement Fallah’s advantageous use of software-implemented power management, which Fallah teaches has

certain advantages over hardware-implemented power-management,” such as more flexibility and configurability. Pet. 69–70 (citing Ex. 1006, 6; Ex. 1007, 3, 14); *see also* Ex. 1003 ¶ 206 (Dr. Colwell providing testimony on this point).

Patent Owner argues that Petitioner has not provided sufficient articulated reasoning to support the combination of Alben and Fallah. PO Resp. 39–42. Patent Owner argues that Petitioner’s identified advantages in the proposed combination—flexibility and reconfigurability—“appear to be constructed via hindsight, because Petitioner [h]as merely retraced the reasoning disclosed in the ’583 patent.” PO Resp. 40 & n.5 (quoting Ex. 1001, 5:3–8). We disagree with Patent Owner because Petitioner cites evidence showing that both of these advantages were known in the prior art. As to flexibility, Fallah explains that implementing dynamic power management in hardware “comes at the expense of less flexibility” than implementing it in software. Ex. 1006, 9, *quoted in* Pet. 68. As to reconfigurability, Petitioner refers to an IEEE article from June 2000 titled “A Survey of Design Techniques for System-Level Dynamic Power Management” (Ex. 1007, “Benini”). Pet. 70 (citing Ex. 1007, 3, 14). Benini explains that “[t]here are several reasons for migrating the power manager to software,” including that “[s]oftware power managers are easy to write and to reconfigure” and that “experimentation with software is easier than with hardware.” Ex. 1007, 14. Benini’s disclosure, therefore, supports Petitioner’s contention that “software-implemented power managers are easier to reconfigure and experiment with.” Pet. 70.

Patent Owner criticizes Petitioner’s reliance on Benini based on Benini’s disclosure of “global coordination” of components, and Patent

Owner argues that “Petitioner simply does not (and cannot) explain why one of skill would have been motivated to modify a clock gating of external modules to include a similar software control as global coordination of power management system.” PO Resp. 41 (citing Ex. 1007, 3). Petitioner, however, does not contend that a person of ordinary skill in the art would apply Benini’s particular teaching of global component coordination. Rather, Petitioner cites Benini to show known advantages of software power control. See Pet. 70.

Patent Owner also argues that “Petitioner has not shown any reason why one of skill would have been motivated to improve flexibility and reconfigurability in Alben” and that Petitioner’s declarant “Dr. Colwell already describes Alben’s hardware control system as sufficiently flexible for its intended purpose, including use of different power management modes.” PO Resp. 40 (citing Ex. 2008 ¶ 130; Ex. 1003 ¶ 84). The testimony of Dr. Colwell cited by Patent Owner simply discusses the operation of Alben’s control unit 12 in different power modes. Ex. 1003 ¶ 84 (citing Ex. 1009, 5:45–6:17, 8:5–25). Dr. Colwell does not testify that there is no room for improvement in Alben, as Patent Owner’s argument suggests. Nor is there a requirement that a prior art reference must identify in itself an area in need of improvement for that reference to be used in an obviousness combination. Rather, “there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Patent Owner also argues that, because a pure software power management approach would provide the most reconfigurable option,

Petitioner’s proposed “hybrid” approach of using both hardware and software “is derived purely on hindsight.” PO Resp. 41 (citing Ex. 2008 ¶ 131); *see also* Sur-reply 21–22 (“[A] person of skill would not have developed a hybrid approach, but rather chosen a purely software approach.”). We disagree with this argument because Alben itself discloses a hybrid power management approach that relies on both hardware and software. *See* Reply 27 (“Alben already discloses a hybrid approach . . .”). In particular, as discussed above in § II.G.2.e, Alben’s system software (running on CPU 4) sets particular power management modes under which Alben’s control unit 12 (hardware) operates. Ex. 1009, 7:52–8:25.

Patent Owner further argues that Petitioner has not shown why a person of ordinary skill in the art would have been motivated to use the specific hybrid approach proposed by Petitioner in which “‘software overrides [] hardware’ and does so ‘independent of control unit 12.’” PO Resp. 41 (alteration added by Patent Owner) (quoting Pet. 67–69). More particularly, Patent Owner argues that Petitioner does not explain why a person of ordinary skill in the art would not have used control unit 12 of Alben rather than operating clock gates independent of the control unit. PO Resp. 41–42 (citing Ex. 2008 ¶¶ 131–132).

We do not understand Petitioner’s contention to be that a person of ordinary skill in the art would not have used Alben’s control unit 12 for power management. *See* Reply 27 (“Alben already discloses a hybrid approach, and a [person of ordinary skill in the art] would have no reason to dismantle Alben’s hybrid approach in favor of software-only clock control.”). Thus, Alben’s control unit 12 continues to function in Petitioner’s proposed combination. What Petitioner proposes is to allow

“software overrides of hardware . . . to implement complex power management schemes.” Pet. 69. Alben already allows system software to set power management modes under which control unit 12 operates. Ex. 1009, 7:52–8:25; *see also* § II.G.2.e above (discussing operation of control unit 12 in various power management modes). As Patent Owner acknowledges, however, this setting of power management modes “will change the mode of control unit 12, but never causes control unit 12 to cede control.” PO Resp. 36. In Petitioner’s proposed combination, the software on CPU 4 may “directly control a gate independent of control unit 12” to override the power management decisions made by control unit 12 and directly overwrite a status of a status of OFF or ON that was previously written by control unit 12, satisfying the parties’ agreed construction. *See* Pet. 67. Therefore, we disagree with Patent Owner’s assertion that Petitioner has not shown that the proposed combination teaches the claimed subject matter under the parties’ agreed construction. *See* PO Resp. 42.

Patent Owner also argues that, in Alben, the user provides input to the system software based on the user’s graphics experience, which the system software then uses to manage power consumption, and Patent Owner argues that, in Petitioner’s proposed combination, the “software . . . would be unable to determine whether the graphics interface is sufficient for that user,” such that “a software solution could not serve the same purpose as Alben.” Sur-reply 22 (citing Ex. 1009, 2:58–67). We agree that Alben discloses user input for power management because it states that “the system software can be implemented to give a user direct control over power management decisions from a dialog box of a displayed control panel.” Ex. 1009, 2:58–61. But we do not understand Petitioner’s proposed

combination to eliminate user input. Rather, Petitioner asserts that “Alben’s software control requires user input, however, and is less complex and flexible than power management techniques disclosed in Fallah” and that

[u]sing Fallah’s more complex software techniques would be the next logical step for Alben to supplement its hardware control. The combination of Alben and Fallah would be a further improvement on the problem that Alben is already trying to solve, because Fallah’s software clock gating could occur without user input, as in Alben.

Reply 27 (citing Pet. 68). Thus, Petitioner proposes to build on Alben’s approach, and we see no reason that user input must be eliminated from Alben.

Patent Owner argues that “the software solutions of Fallah would do little more than automate the power management modes used to set control unit 12” and that “[t]here is nothing in Fallah that discloses using independent software and hardware mechanisms to affect the status of individual circuit-level gates, which is the combination Petitioner now proposes.” Sur-reply 23. We disagree with this because, as Petitioner correctly asserts, Fallah “discloses ‘clock gating’ to remove selected clock pulses or turn off clocks entirely for devices that do not need them.” Pet. 68 (citing Ex. 1006, 19). As discussed above, Fallah identifies “clock gating” as one example of a power management technique and explains that clock gating is “[a] simple and effective method for decreasing the dynamic power consumption.” Ex. 1006, 19–20; *see also* Ex. 1006, 20–24 (detailed description of clock gating).

Having considered the evidence presented and in view of the parties’ arguments, we are persuaded by Petitioner’s contentions that a person of ordinary skill in the art would have been motivated to apply Fallah’s

teachings of additional software power management control to Alben's hardware/software hybrid power management scheme so that Alben's CPU 4 may "directly control a gate independent of control unit 12" to override the power management decisions made by control unit 12 and directly overwrite a status of a status of OFF or ON that was previously written by control unit 12. *See* Pet. 67–69. We find that a person of ordinary skill in the art would have been motivated to do so to achieve greater flexibility and configurability, which were known benefits of software power management, as evidenced by the disclosures of Fallah and Benini discussed above. *See* Ex. 1006, 6; Ex. 1007, 3, 14; Ex. 1003 ¶ 206 (Dr. Colwell providing testimony on this point); *see also* Pet. 69–70. As also discussed above, we find that the combined disclosures of Alben and Fallah teach "at least one processor that overwrites a status of at least a portion of said plurality of gates which is controlled by said hardware control logic block" under the parties' agreed construction.

c) Determination on obviousness

Based on the foregoing, and having considered the full trial record, we determine Petitioner has shown by a preponderance of the evidence that the subject matter of claim 25 would have been obvious to a person of ordinary skill in the art based on the combined teachings of Alben and Fallah.

d) Petitioner's reliance on Kiuchi

In this ground, Petitioner makes an alternative argument for the limitation of claim 25 reciting "at least one register that is controlled by a clock tree driver" in which Petitioner asserts that, "to the extent [Patent Owner] argues that Alben's host slave unit 15 is not a 'clock tree driver' under [Petitioner]'s construction, this would have been obvious in view of

Kiuchi.” Pet. 64–66. As discussed above in § II.G.2.d, Patent Owner does not dispute that Alben describes a “clock tree driver.” In its Response, Patent Owner does not respond to Petitioner’s combination of Alben and Kiuchi because Petitioner’s contention addresses a proposed construction that Patent Owner argues is too narrow. See PO Resp. 38 n.4. Based on our findings in § II.G.2.d, we need not rely on Petitioner’s alternative argument here based on Kiuchi.

3. *Claim 26*

Claim 26 recites, “The system according to claim 25, wherein said processor via said clock tree driver asserts or de-asserts a current value of said at least one register.” Petitioner argues that “Alben discloses that CPU 4, using system software and via host slave unit 15, writes to a location in register 12A to assert or deassert a current value of the register (*e.g.*, FULLPOWER, AUTOMATIC, SUSPENDED).” Pet. 71 (citing Ex. 1009, 1:62–67, 2:46–67, 3:6–28, 5:1–7:18, 7:52–8:36, 9:66–12:52, 14:19–38).

Patent Owner argues that Petitioner’s contention for claim 26 is inconsistent with its contentions for claim 25 because, according to Patent Owner, “Petitioner relies on the same register in Alben that it sought to remove in Alben’s combination with Fallah.” PO Resp. 43 (citing Ex. 2008 ¶¶ 134–136). We disagree that Petitioner’s proposed combination eliminates register 12A of Alben. Rather, as discussed above in § II.H.2.b, Alben’s control unit 12 continues to manage power based on the power management modes set in register 12A. See Reply 27 (“Alben already discloses a hybrid approach, and a [person of ordinary skill in the art] would have no reason to dismantle Alben’s hybrid approach in favor of software-only clock control.”).

We are persuaded by Petitioner’s contentions, and we find that Alben discloses writing to register 12A and therefore teaches “said processor via said clock tree driver asserts or de-asserts a current value of said at least one register,” as recited in claim 26. *See* Ex. 1009, 7:56–63 (“[R]egister array 12A of control unit 12 (or other circuitry of device 2 that is accessible by control unit 12) includes a two-bit host register (called a ‘PM_SUBSYSTEM_CONTROL’ register) for each of subsystems 16, 18, 20, and 22. System software can write a two-bit word to each ‘PM_SUBSYSTEM_CONTROL’ register to indicate the power management mode for the corresponding subsystem.”).

Based on the foregoing, and having considered the full trial record, we determine Petitioner has shown by a preponderance of the evidence that the subject matter of claim 26 would have been obvious to a person of ordinary skill in the art based on the combined teachings of Alben and Fallah.

Petitioner alternatively relies on Kiuchi for an additional teaching of the subject matter of claim 26 (Pet. 71), but in view of our finding that Alben teaches the subject matter recited in claim 26, we need not rely on Petitioner’s argument based on Kiuchi.

III. CONCLUSION¹⁰

For the reasons discussed above, we determine Petitioner has proven, by a preponderance of the evidence, that the some of the challenged claims are unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	References/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
17, 18, 20–24	103(a)	Kiuchi, Van Hook		17, 18, 20–24
21, 24	103(a)	Kiuchi, Van Hook, Alben		21, 24
17, 18, 20–24	103(a)	Ninomiya, Van Hook		17, 18, 20–24
21, 24		Ninomiya, Van Hook, Alben, Fallah		21, 24
25, 26	102(e)	Alben		25, 26
25, 26	103(a)	Alben, Fallah, Kiuchi	25, 26	
Overall Outcome			25, 26	17, 18, 20–24

¹⁰ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

Accordingly, it is:

ORDERED that claims 25 and 26 of the '583 patent have been shown to be unpatentable and that claims 17, 18, 20–24 of the '583 patent have not been shown to be unpatentable; and

FURTHERED ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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