

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIVERSAL IMAGING INDUSTRIES, LLC,
Petitioner,

v.

LEXMARK INTERNATIONAL, INC.,
Patent Owner.

IPR2019-01369
Patent 8,386,657 B2

Before JUSTIN T. ARBES, DAVID C. McKONE, and
MATTHEW J. McNEILL, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Petitioner Universal Imaging Industries, LLC, filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–15 of U.S. Patent No. 8,386,657 B2 (Ex. 1001, “the ’657 patent”) pursuant to 35 U.S.C. § 311(a). Patent Owner Lexmark International, Inc., filed a

Preliminary Response (Paper 6, “Prelim. Resp.”) pursuant to 35 U.S.C. § 313. Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons that follow, we do not institute an *inter partes* review.

B. Related Matters

The parties indicate that the ’657 patent is the subject of the following district court case: *Lexmark International, Inc. v. Universal Imaging Industries, LLC*, Case No. 8:18-cv-01047-EAK-AEP (M.D. Fla.). See Pet. 1; Paper 4, 3. Petitioner has filed petitions challenging other patents also asserted in the district court case in Cases IPR2019-01368, IPR2019-01378, IPR2019-01380, IPR2019-01381, IPR2019-01383, IPR2019-01385, IPR2019-01387, IPR2019-01388, and IPR2019-01389.

C. The ’657 Patent

The ’657 patent discloses a communication system having a master device in communication with uniquely addressed slave devices, such as, for example, a printer controller in communication with a replaceable printer cartridge over a shared bus. Ex. 1001, code (57), col. 9, l. 38–col. 10, l. 47. The ’657 patent describes a known “Inter-Integrated Circuit (I²C) technique” where “[t]he address of each of the slave devices is stored by hardwired means, or in a non-volatile memory that is resident in the slave devices,” and the master device communicates with a specific slave device by transmitting a command on the bus with the address of the desired device. *Id.* at col. 1,

ll. 34–45. All of the slave devices on the bus receive the command, but only the slave device with a matching address acknowledges it and begins two-way communication with the master device. *Id.* at col. 1, ll. 45–50. According to the '657 patent, this technique was not secure because an imposter device connected to the bus could communicate simply by obtaining and using any of the active addresses. *Id.* at col. 1, ll. 51–67. The '657 patent seeks to improve security by “periodically chang[ing] the slave device addresses to increase the difficulty for an imposter to communicate with the master device” and “request[ing] that a slave device change its address, but prevent[ing] the slave device from communicat[ing] the new address to the master device, thereby reducing the chances of an imposter learning the new address.” *Id.* at col. 2, ll. 15–24.

Figure 1 of the '657 patent is reproduced below.

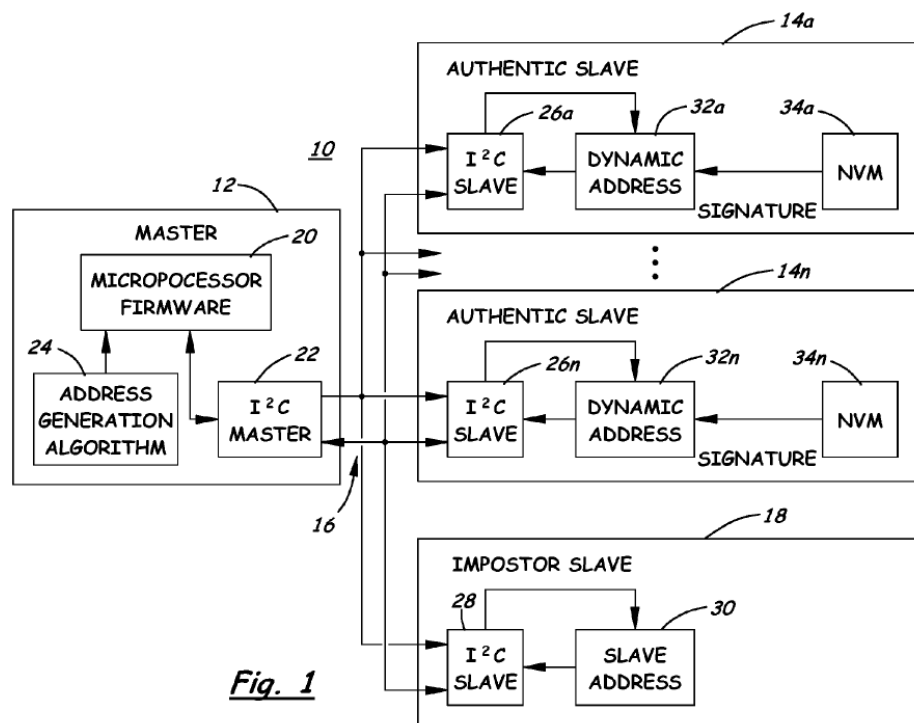


Figure 1 depicts shared bus system 10 comprising master device 12 connected via shared bus 16 to slave devices 14a–14n and imposter slave

device 18. *Id.* at col. 4, ll. 28–32. Each slave device 14 includes non-volatile memory 34 for storing a default slave address and signature code, and dynamic address generator 32 for changing its address upon request by master device 12. *Id.* at col. 5, ll. 55–62, col. 6, ll. 10–13. Dynamic address generator 32 may be “a pseudorandom address generator that generates addresses according to a predefined algorithm” that is also known to master device 12. *Id.* at col. 5, l. 62–col. 6, l. 7.

“[T]he slave addresses of the shared bus system 10 are periodically changed to thereby thwart attempts by imposters to gain access to the system.” *Id.* at col. 5, ll. 41–43. “[M]aster device 12 does not dictate to the slave device 14 what new address should be used, only that the slave device 14 should assign to itself a new address.” *Id.* at col. 5, ll. 57–60. The ’657 patent discloses that master device 12 transmits

a “change address” command on the shared bus 16 in a conventional manner. When the slave device, for example slave device 14a, receives the command and the old slave address matches the address currently provided by the dynamic address generator 32a, then the command is processed by the I²C circuit 26a. When decoded, the address change command causes the dynamic address generator 32a to be incremented, whereupon a new random address is generated and self-assigned to the slave device 14a. The request is acknowledged by the slave device 14a to the master device 12, whereupon the master device 12 determines or predicts the newly assigned address by use of the algorithm stored in the memory 24. Thus, both the master device 12 and the slave device 14a are updated as to the new slave address without transmitting the same on the shared bus 16 to the master device 12. All subsequent transmissions by the master device 12 to the slave device 14a will be by way of the newly-assigned address.

Id. at col. 6, ll. 15–32.

Dynamic generation of a slave address is shown in Figure 4 of the '657 patent reproduced below.

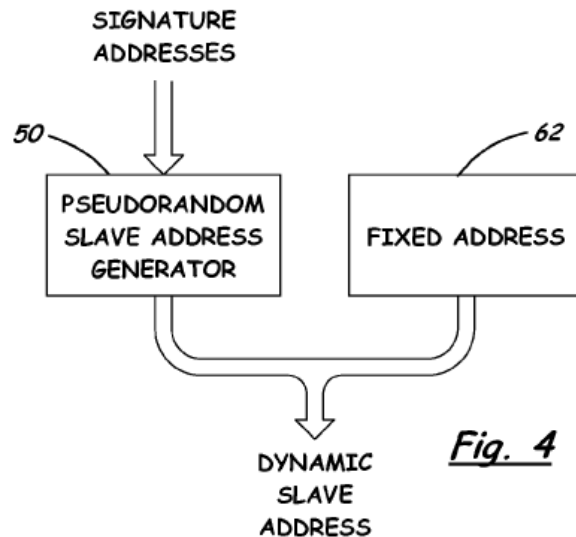


Figure 4 depicts pseudorandom address generator 50, which “provides the least significant bits of the slave device address,” and fixed address circuit 62, which “provides a fixed address that is unique to each slave device 14” as “the most significant bits of the address.” *Id.* at col. 7, ll. 31–40.

The '657 patent further discloses that “[i]n the event that the system 10 or a slave device 14 loses power, then the slave address can be reconstructed using the non-volatile memory 34.” *Id.* at col. 6, ll. 38–40, 62–65. Master device 12 issues a “soft reset” command to slave device 14, which reads non-volatile memory 34 and “retrieve[s] both a default address and a signature code to be loaded into the linear feedback shift register, or other apparatus functioning as the pseudorandom generator.” *Id.* at col. 6, ll. 40–46. “[S]lave device 14 will then operate thereafter with the default address until a change of address is requested and carried out.” *Id.* at col. 6, ll. 46–48.

D. Illustrative Claims

Claims 1, 10, and 15 of the '657 patent recite:

1. A container for ink or toner, comprising:
 - a reservoir for holding ink or toner;
 - slave circuitry for communicating with an imaging device as a slave device when connected thereto; and
 - an address generator coupled to the slave circuitry, the address generator generating plural addresses so that the slave address associated with the container can be changed;wherein the slave circuitry, when communicatively coupled to the imaging device, is responsive to a command therefrom for changing the slave address of the container, and the slave circuitry controls the address generator for changing the slave address thereof, wherein the slave address includes a variable address bit portion and a fixed address bit portion.
10. A replaceable unit having toner or ink therein, comprising:
 - slave circuitry for communicating with a printing apparatus as a slave device when the replaceable unit is coupled thereto;
 - an address generator associated with the slave circuitry, the address generator generating plural addresses so that the address of the replaceable unit can be changed;wherein the slave circuitry is responsive to a command from the printing apparatus for changing the address of the replaceable unit, and controls the address generator for changing the address thereof.
15. A replaceable unit having toner or ink therein, comprising:
 - slave circuitry for communicating with a printing apparatus as a slave device when the replaceable unit is coupled thereto;
 - an address generator associated with the slave circuitry, the address generator generating plural addresses so that the address of the replaceable unit can be changed;

wherein the slave circuitry is responsive to a command from the printing apparatus for changing the address of the replaceable unit, and controls the address generator for changing the address thereof, and wherein the address generator includes a shift register and a non-volatile memory for storing a default address, the default address used to set the shift register with a start address defined by the default address.

E. Evidence

Petitioner relies on the following prior art:

U.S. Patent No. 7,506,086 B2, issued Mar. 17, 2009 (Ex. 1005, “Mayer”);

U.S. Patent No. 5,708,831, issued Jan. 13, 1998 (Ex. 1004, “Schön”);

U.S. Patent No. 5,088,024, issued Feb. 11, 1992 (Ex. 1006, “Vernon”);

U.S. Patent Application Publication No. 2007/0236726 A1, published Oct. 11, 2007 (Ex. 1007, “Robb”);

John Kerl, *Computation in Finite Fields* (Apr. 2004) (Ex. 1012, “Kerl”);

Clive Maxfield, *Bebop to the Boolean Boogie* (2d ed. 2003) (Ex. 1011, “Maxfield”);

The I²C-Bus Specification, version 2.1, Jan. 2000 (Ex. 1003, “I²C Spec”);

Solomon W. Golomb, *Shift Register Sequences* (1982) (Ex. 1013, “Golomb”); and

M. Morris Mano, *Digital Logic and Computer Design* (1979) (Ex. 1014, “Mano”).¹

¹ Petitioner refers to Kerl, Maxfield, Golomb, and Mano collectively as the “Pseudorandom Number Generator References.” Pet. 3 n.1. When citing the asserted non-patent references, we refer to the original page numbers of the references.

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–15 of the ’657 patent are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1–3, 9–11	103(a) ²	Schön, I ² C Spec, Robb
1–3, 9–11	103(a)	Schön, Vernon, Robb
4–8, 12–15	103(a)	Schön, I ² C Spec, Robb, Maxfield, Kerl, Golomb, Mano
4–8, 12–15	103(a)	Schön, Vernon, Robb, Maxfield, Kerl, Golomb, Mano
1–3, 9–11	103(a)	Mayer, I ² C Spec, Robb
1–3, 9–11	103(a)	Mayer, Vernon, Robb
4–8, 12–15	103(a)	Mayer, I ² C Spec, Robb, Maxfield, Kerl, Golomb, Mano
4–8, 12–15	103(a)	Mayer, Vernon, Robb, Maxfield, Kerl, Golomb, Mano

II. ANALYSIS

A. Legal Standards

A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). The question of obviousness is resolved on the basis of underlying factual

² The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. § 103. Because the challenged claims of the ’657 patent have an effective filing date before the effective date of the applicable AIA amendment, we refer to the pre-AIA version of 35 U.S.C. § 103. See Ex. 1001, codes (22), (63).

determinations, including “the scope and content of the prior art”; “differences between the prior art and the claims at issue”; and “the level of ordinary skill in the pertinent art.”³ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. An obviousness determination requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418 (for an obviousness analysis, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does”). “Although the *KSR* test is flexible, the Board ‘must still be careful not to allow hindsight reconstruction of references . . . without any explanation as to *how* or *why* the references would be combined to produce the claimed invention.’” *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016) (citation omitted). Further, an assertion of obviousness “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal

³ Additionally, secondary considerations, such as “commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy.” *Graham*, 383 U.S. at 17–18. Neither party, however, has presented any such evidence for us to consider.

conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); accord *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (stating that ““conclusory statements”” amount to an “insufficient articulation[] of motivation to combine”; “instead, the finding must be supported by a ‘reasoned explanation’” (citation omitted)); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”).

B. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art at the time of the ’657 patent would have had “a bachelor’s degree in electrical and/or computer engineering with training and one or more years of experience in embedded systems including both hardware and embedded software design,” as well as “a working understanding of communication on an electronics bus.” Pet. 8 (citing Ex. 1002 ¶¶ 25–28). Patent Owner argues that an ordinarily skilled artisan would have had “a bachelor’s degree in electrical and/or computer engineering with one or more years of work experience in printer design, including hardware and/or embedded software design for printer applications.” Prelim. Resp. 7–8 (citing Ex. 2001 ¶¶ 29–33). The parties’ proposed definitions differ in that Petitioner’s definition requires experience with “embedded systems” and “communication on an electronics bus,” whereas Patent Owner’s definition more specifically requires experience with “printer design.” The Specification of the ’657 patent states that the disclosure relates to “master and slave devices communicating on a

shared bus,” and specifically, “addressing schemes to provide security to the system.” Ex. 1001, col. 1, ll. 15–19. The claims of the ’657 patent similarly each recite “slave circuitry” for communicating as a “slave device” and an “address generator” generating plural addresses. Based on the record presented, including our review of the ’657 patent and the types of problems and solutions described in the ’657 patent and cited prior art, we agree with and apply Petitioner’s proposed definition of the level of ordinary skill in the art for purposes of this Decision.

C. Claim Interpretation

We interpret the challenged claims

using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019). Neither party proposes any interpretations for the challenged claims. *See* Pet. 9; Prelim. Resp. 8. We have reviewed the parties’ papers and conclude that no term requires interpretation to determine whether to institute an *inter partes* review in this proceeding. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“Because we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy,’ we need not construe [a particular claim limitation] where the construction is not ‘material to the . . . dispute.’” (citations omitted)).

*D. Obviousness Grounds Based on Schön, I²C Spec, and Robb,
and Schön, Vernon, and Robb*

Petitioner contends that claims 1–3 and 9–11 are unpatentable over Schön, I²C Spec, and Robb, and over Schön, Vernon, and Robb, under 35 U.S.C. § 103(a), citing the testimony of Harry Direen, Ph.D., P.E., as support. Pet. 15–26 (citing Ex. 1002). Patent Owner makes various arguments in response, citing the testimony of Jeffrey J. Folkins, Ph.D., as support. Prelim. Resp. 20–45, 51–56, 60–65 (citing Ex. 2001). We are not persuaded that Petitioner has established a reasonable likelihood of prevailing on either asserted ground for the reasons explained below.

1. Schön

Schön discloses “a method for assigning bus addresses for a data processing system having a plurality of stations and a control unit (master).” Ex. 1004, col. 1, ll. 4–6. The master “first transmits to the stations a command for address generation, whereupon each station generates for itself a random address from a preset value range.” *Id.* at col. 1, ll. 40–43, col. 2, ll. 57–65. The master then tests each address within the preset range to see if a station assigned itself that address. *Id.* at col. 1, ll. 44–47, col. 2, l. 65–col. 3, l. 1. If the master receives a reply from a station with a valid address, the master informs the station that the address has been accepted and the station sets an “address flag” in response. *Id.* at col. 1, ll. 47–51, 53–56, col. 3, ll. 1–6. If the reply has a transmission error, however, “this indicates to the master station that at least two stations have the same random address” and no acknowledgement is provided. *Id.* at col. 1, ll. 51–53, col. 3, ll. 7–10. “If at the end of an inquiry cycle only valid replies have been supplied by the stations, each station can be assigned a clear

address.” *Id.* at col. 3, ll. 11–13. Otherwise, “the method is repeated, but with the command for address generation only being reacted to by those stations that have not set the address flag for successful address assignment.” *Id.* at col. 3, ll. 13–16.

2. *I²C Spec*

I²C Spec specifies a standard for “a simple bi-directional 2-wire bus for efficient inter-IC control,” which the reference calls “the Inter IC or I²C-bus.” Ex. 1003, 4. I²C Spec describes communication over an I²C bus between a master (“[t]he device which initiates a transfer, generates clock signals and terminates a transfer”) and a slave (“[t]he device addressed by a master”). *Id.* at 7. I²C Spec describes addressing procedures for the master to communicate with slave devices. *Id.* at 15. One addressing procedure uses 7-bit addressing for the slave address. *Id.* In this procedure, the “slave address can be made-up of a fixed and a programmable part.” *Id.* “The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.” *Id.*

3. *Robb*

Robb discloses “printing methodologies for printing objects that may be positioned at defined and alternate locations within a printed page.” Ex. 1007 ¶ 1. Printer cartridge 12 includes toner reservoir 38 and system board 46 coupled to system board 20 of printing device 10 via data bus 56, which may include “an I2C (i.e., Inter-IC) bus.” *Id.* ¶¶ 20–21, Fig. 2.

4. Vernon

Vernon discloses a “protocol . . . for the round-robin distributed arbitration of access to a common resource, such as a bus, in a multiprocessor system or machine,” where “[t]he protocol assigns identity values to each agent, or processor, which are compared during each arbitration to determine which agent is awarded control of the bus.”

Ex. 1006, code (57). Figure 1 of Vernon is reproduced below.

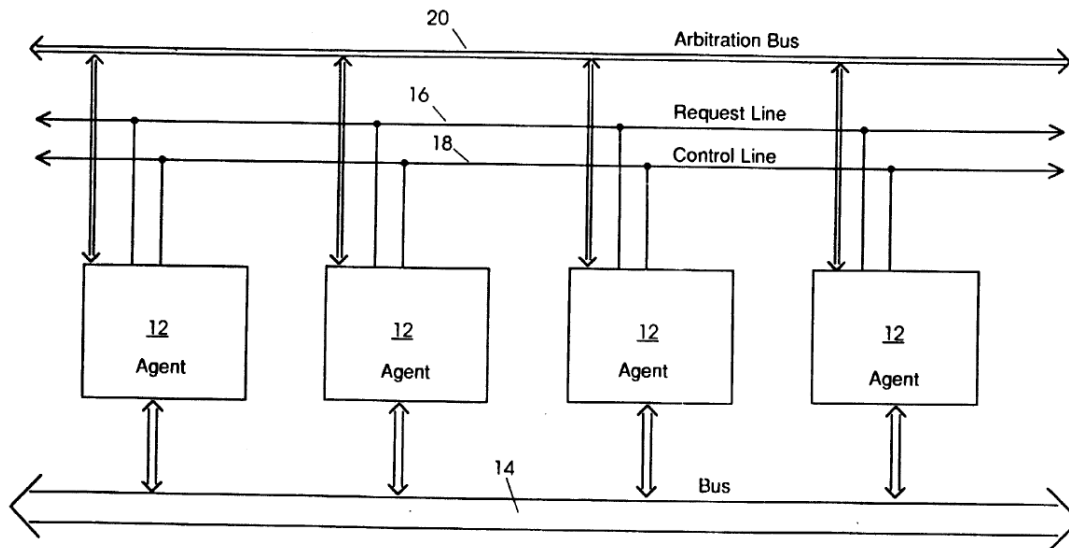


FIG. 1

Figure 1 depicts agents 12 competing for bus 14, with parallel arbitration bus 20, bus request line 16, and control lines 18 connected to each agent 12.

Id. at col. 5, ll. 18–29. Vernon’s arbitration protocol initially performs a “parallel contention arbiter” arbitration. *Id.* at col. 5, ll. 30–32. Each agent is assigned “a unique fixed k-bit arbitration number called its ‘identity.’”

Id. at col. 2, ll. 46–49. “An agent that wants control of the bus forces a wired-OR shared bus request line, and waits for a signal to start arbitration,” which may be “generated by the current bus master [or] a central timing controller.” *Id.* at col. 2, ll. 51–56. “At the start of an arbitration, the agent

applies its arbitration number to a separate parallel set of arbitration control lines provided on the bus for this purpose” and “monitors each of the arbitration lines, in parallel.” *Id.* at col. 2, ll. 51–60. “If the value carried by line *i* is ‘1,’ but the agent is applying a ‘0’ to it, then the agent removes the lower-order (*i*-1 to 0) bits of its identity. If line *i* drops back to ‘0,’ the agent reapplies the lower-order bits it removed before.” *Id.* at col. 2, ll. 60–64. Eventually “the lines carry the largest identity of all competing agents” and “[t]he agent whose arbitration number matches the winning number becomes the next bus master.” *Id.* at col. 3, ll. 3–8. Vernon notes that this process is fast but “inherently unfair, since an agent with a higher identity will always win an arbitration against an agent with a lower identity, and thus higher priority agents will disproportionately control the bus.” *Id.* at col. 3, ll. 10–15.

Vernon’s disclosed arbitration protocol then proceeds differently, resulting in an “improvement” to the “parallel contention arbiter” arbitration. *Id.* at col. 5, ll. 18–21, 32–33. “If the first arbitration is won by [an] agent with identity *j*, then in the next arbitration all agents with assigned identity values less than *j*, i.e. 1 through *j*-1, will be given priority over all agents having assigned identity values greater than or equal to [*j*], i.e. *j*. through *N*.” *Id.* at col. 2, l. 46–col. 3, l. 15, col. 5, ll. 30–38. In other words, the protocol grants “special status, for one arbitration,” to “agents which have lower assigned values than the winner of the prior arbitration” and distributes bus access fairly. *Id.* at col. 5, ll. 38–44.

Vernon describes an embodiment involving “one extra bit on the parallel arbitration bus 20” called the “round-robin bit.” *Id.* at col. 5, ll. 49–52. “Each agent records the identity of the winning agent, i.e. the agent that gained control of the bus, at the end of every arbitration,

excluding the round-robin priority bit.” *Id.* at col. 5, ll. 54–57. “An agent asserts the shared bus request line and competes in the next arbitration whenever it desires control of the bus.” *Id.* at col. 5, ll. 59–61. “When an agent competes in an arbitration, the agent sets its round-robin bit for its identity to ‘one’ if its static identity value is less than the recorded static identity value of the winner of the previous arbitration.” *Id.* at col. 5, ll. 61–65. Vernon further describes incorporating “priority service” into the disclosed arbitration protocol as follows:

Each agent’s identity consists of two dynamic bits and k lesser significant static bits. Thus $k+2$ lines are required in the parallel arbitration bus 20. The round-robin bit is the second most significant bit; the most significant bit is used for priority requests, and the remaining k lesser significant bits carry the agent’s unique static identity. All agents compete in each arbitration by setting the priority bit to “one” for a priority request, an agent circumvents the round robin order and gains control of the bus immediately. If more than one agent has a priority request, the agents follow the protocol to implement round-robin scheduling within the priority class.

Id. at col. 7, ll. 3–16.

5. Claim 1

Petitioner relies on Schön and Robb for all limitations of claim 1 other than one. Pet. 15–21. Petitioner argues that Robb teaches a “container for ink or toner” (i.e., printer cartridge 12) comprising a “reservoir for holding ink or toner” (i.e., toner reservoir 38) and “slave circuitry for communicating with an imaging device as a slave device when connected thereto.” *Id.* at 18 (citing Ex. 1007 ¶¶ 17, 20, 21, Figs. 1, 2). Petitioner argues that Schön teaches “slave circuitry” for communicating as a “slave device” and an “address generator” for generating plural addresses that can be changed in

response to a command from an imaging device, citing Schön's disclosure of the master transmitting a command for address generation and a station generating a random address in response. *Id.* at 19–20 (citing Ex. 1004, col. 1, ll. 39–42, col. 2, ll. 7–9, col. 3, ll. 11–16). Petitioner relies, in the alternative, on I²C Spec and Vernon as teaching a “slave address [that] includes a variable address bit portion and a fixed address bit portion,” as recited in claim 1. *Id.* at 20–21. We address each proposed combination in turn.

a) Combination of Schön, I²C Spec, and Robb

Petitioner argues that I²C Spec teaches a device address comprising seven bits, including four fixed (the claimed “fixed address bit portion”) and three programmable address bits (the claimed “variable address bit portion”). Pet. 20 (citing Ex. 1003, 15; Ex. 1002 ¶ 52). According to Petitioner, an ordinarily skilled artisan would have been motivated to combine Schön and I²C Spec because “Schön teaches methods for generating slave addresses, and the I²C Spec teaches various addressing formats for slave devices.” *Id.* at 16. Petitioner asserts that “[g]iven that the references are in the same field of endeavor and each teach the addressing of slave devices, a [person of ordinary skill in the art] would have found it obvious to combine their teachings.” *Id.* Petitioner also asserts that an ordinarily skilled artisan would have understood from Schön that “there is a natural need to utilize the addressing formats of [I²C Spec] to combine the stations or slaves of Schön into groups.” *Id.* at 21 (citing Ex. 1004, col. 2, ll. 31–34, 59–64; Ex. 1002, App. 1002-A, 2–9).

Patent Owner argues that Petitioner has failed to meet its burden in establishing that an ordinarily skilled artisan would have had reason to

combine Schön with I²C Spec. Prelim. Resp. 50–54. In particular, Patent Owner argues that Schön already discloses an address format, and neither Schön, I²C Spec, nor the Petition identifies any disadvantages with Schön’s address format that would have been improved by I²C Spec’s address format. *Id.* at 52. Patent Owner argues that Petitioner does not explain why an ordinarily skilled artisan would have replaced Schön’s exemplary 8-bit address format, which allows for up to 256 addresses, with I²C Spec’s 7-bit address format with a limited number of variable bits, allowing fewer addresses to be generated in response to an address generation command. *Id.* at 52–53. Dr. Folkins’s testimony supports Patent Owner’s arguments. *See* Ex. 2001 ¶¶ 101, 105–113. In particular, Dr. Folkins testifies that replacing Schön’s addressing scheme with I²C Spec’s addressing would limit the flexibility of Schön’s addressing. *Id.* ¶¶ 105–107. Dr. Folkins further testifies that I²C Spec’s addressing scheme would have caused inefficiencies in Schön’s system because a smaller pool of addresses would lead to more duplicate addresses, causing additional cycles of address generation. *Id.* ¶¶ 108–111.

We credit Dr. Folkins’s uncontroverted testimony. We recognize that, according to our rules, we “will take into account a patent owner preliminary response where such a response is filed, including any testimonial evidence, but a genuine issue of material fact created by such testimonial evidence will be viewed in the light most favorable to the petitioner solely for purposes of deciding whether to institute an *inter partes* review.” 37 C.F.R. § 42.108(c). However, in this case, Dr. Folkins’s testimony does not implicate a genuine issue of material fact. Petitioner does not provide *any* argument or cite to *any* testimony regarding the advantages or disadvantages of using I²C Spec’s addressing scheme in place of Schön’s. *See* Pet. 15–21. Petitioner merely

asserts, without further explanation, that Schön teaches “generating slave addresses,” I²C Spec teaches one “addressing format[,],” and a person of ordinary skill in the art would have been motivated to use the latter. *Id.* at 16. Dr. Direen’s testimony regarding combining the teachings of Schön and I²C Spec also makes no mention of advantages or disadvantages of replacing Schön’s addressing scheme with I²C Spec’s addressing scheme. *See* Ex. 1002, App. 1002-A, 7 (concluding that “[i]t would be natural for a [person of ordinary skill in the art] to combine the teaching of the I²C standard with [Schön’s] teachings as they both relate to similar computer bus systems,” without addressing advantages or disadvantages of the addressing schemes).

Further, to the extent Petitioner argues that an ordinarily skilled artisan would have found it obvious to combine Schön and I²C Spec simply because both teach addressing of slave devices, the fact that two references have similar disclosures, without more, is insufficient to establish a reason to combine their teachings. *See* Pet. 16; *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9 at 10–11 (PTAB Oct. 16, 2018) (informative) (“Mere compatibility of the references is . . . not sufficient.”); *see also Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (unpublished) (holding that “a broad characterization of [two references] as both falling within the same alleged field,” without more, was not “a sufficient rationale to support an obviousness conclusion,” as “[s]uch short-cut logic would lead to the conclusion that any and all combinations of elements known in th[e] broad field would automatically be obvious, without the need for any further analysis”); *Microsoft Corp. v. Enfish, LLC*, 662 F. App’x 981, 990 (Fed. Cir. 2016) (unpublished) (holding that the fact that two references “were directed to the same art or same

techniques” was “inadequate to show persuasively that a relevant skilled artisan would have been motivated to combine the references”).

Petitioner has not explained sufficiently how I²C Spec’s addressing scheme would have been combined with the teachings of Schön or why an ordinarily skilled artisan would have made the combination. Petitioner instead makes the conclusory assertion that a person of ordinary skill in the art would have combined the references, without sufficient explanation regarding how the combination would work or why an ordinarily skilled artisan would have made the combination. Thus, Petitioner has not articulated sufficient rationale for the replacement of Schön’s addressing scheme with I²C Spec’s addressing, which is the proposed combination of teachings of these references.⁴ Accordingly, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claim 1 is unpatentable over Schön, I²C Spec, and Robb.

b) Combination of Schön, Vernon, and Robb

Petitioner argues that Vernon teaches a “slave address [that] includes a variable address bit portion and a fixed address bit portion.” Pet. 20 (citing Ex. 1006, col. 7, ll. 5–6; Ex. 1002 ¶ 62). Petitioner identifies Vernon’s “two dynamic bits” used for priority service as the alleged “variable address bit portion” and Vernon’s “k lesser significant static bits” as the alleged

⁴ Patent Owner makes a number of other arguments in its Preliminary Response, including that Petitioner has not shown sufficiently that I²C Spec and other asserted references are prior art printed publications under 35 U.S.C. § 102(b). See Prelim. Resp. 20–25, 28–35, 41–46, 49–50, 54–56, 59–60. We need not reach these issues, however, because Petitioner has not shown a reasonable likelihood of prevailing on its asserted grounds for the reasons explained herein.

“fixed address bit portion.” *Id.* Patent Owner argues that Vernon does not teach a “variable address bit portion” of a “slave address.” Prelim. Resp. 35–37. On the record presented, we agree with Patent Owner.

As explained above, each agent in Vernon has a fixed address unique to that agent that is used to communicate with the agent over the data bus. *See* Ex. 1006, col. 1, ll. 47–50 (“When an agent (a device, e.g. a processor) wishes to communicate with another agent, the first agent sends signals that cause the second agent to respond. These signals are collectively called the address or identity.”), col. 2, ll. 46–49 (describing “assigning each agent a unique fixed k-bit arbitration number called its ‘identity’”), col. 5, ll. 29–30 (“[The disclosed] arbitration protocol makes use of fixed assigned identity values for each agent.”). The disclosed arbitration protocol involves communications over separate lines (i.e., parallel arbitration bus 20, bus request line 16, and control lines 18) to give a particular agent control over bus 14. *Id.* at col. 2, l. 46–col. 3, l. 15, col. 5, l. 18–col. 6, l. 7. Vernon implements “priority service” where the agent transmits an identity value on parallel arbitration bus 20 (not bus 14) consisting of its address (i.e., the agent’s “unique static identity” carried in the “k lesser significant bits”) and two flags set by the agent to implement the protocol: (1) the “round-robin” bit, the “second most significant bit,” set to 1 if the agent’s identity is less than the recorded identity of the previous arbitration winner, and (2) the “priority request” bit, the “most significant bit,” set to 1 if the agent has a high priority request and needs to gain control of the bus immediately. *Id.* at col. 5, ll. 49–65, col. 7, ll. 3–10.

Neither bit, however, is a portion of an “address” for the agent. It is clear from the language of the claims that an “address” is the mechanism by which the container is *addressed*. Claim 1 recites that the container

comprises an “address generator” coupled to the slave circuitry that generates “plural addresses so that the slave address associated with the container can be changed.” In response to a command from the imaging device, the slave circuitry controls the address generator to change the slave address “of the container.”⁵ This reading is consistent with the Specification. *See, e.g.*, Ex. 1001, col. 1, ll. 34–50 (disclosing that “slave devices are uniquely identified with respective addresses” and “[w]hen the master device initiates communications with a specific slave device, the address of the slave device is transmitted with a command on the bus during the initiation of the communication”).

By contrast, in Vernon, the round-robin bit and priority request bit are used to implement the arbitration protocol via communications over the arbitration bus. They are not used in any respect for communicating with the agent over the data bus. Instead, the agent has a unique fixed “identity” that is used for that purpose. Indeed, the two dynamic bits are not even retained once an arbitration is complete; only the fixed “identity” of the winning agent is retained by each agent. *See* Ex. 1006, col. 5, ll. 54–59. We are persuaded by Patent Owner that the two dynamic bits in Vernon identified by Petitioner as a “variable address bit portion” of a “slave address” are “unrelated to, and do not convey, an address” as recited in claim 1. *See* Prelim. Resp. 35–37.

⁵ Independent claims 10 and 15 similarly recite a replaceable unit comprising an “address generator” associated with slave circuitry that generates “plural addresses so that the address of the replaceable unit can be changed,” where in response to a command from a printing apparatus, the slave circuitry controls the address generator to change the address “of the replaceable unit.”

Petitioner has not shown sufficiently that the combination of Schön, Vernon, and Robb teaches a “variable address bit portion” of a “slave address” as recited in claim 1. Accordingly, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claim 1 is unpatentable over Schön, Vernon, and Robb.

6. *Claims 2, 3, 9 and 11*

Claims 2, 3, and 9 depend from claim 1. Claim 11 depends from claim 10, but recites the same “variable” and “fixed” address bit portions as claim 1. Petitioner makes the same arguments regarding I²C Spec and Vernon. *See* Pet. 20, 26. We find those arguments unpersuasive for the reasons explained above. Accordingly, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claims 2, 3, 9, and 11 are unpatentable over Schön, I²C Spec, and Robb, or over Schön, Vernon, and Robb.

7. *Claim 10*

In its Petition, Petitioner states that it is asserting a ground of unpatentability under 35 U.S.C. § 103(a) based on the combination of “Schön, I²C Spec or Vernon, and Robb.” Pet. 3, 15. In addressing the limitations of claim 10, however, Petitioner only cites Schön and Robb; Petitioner never cites I²C Spec or Vernon in its arguments regarding claim 10. *Id.* at 23–25; *see* Ex. 1002, App. 1002-A, 25 (Dr. Direen opining that “Schön in light of Robb render[s claim 10] obvious”). A petition for *inter partes* review must “identif[y], in writing and with particularity, each claim challenged [and] the grounds on which the challenge to each claim is based.” 35 U.S.C. § 312(a)(3); *see Harmonic Inc. v. Avid Tech., Inc.*,

815 F.3d 1356, 1363 (Fed. Cir. 2016) (“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.”). It is unclear whether Petitioner contends that claim 10 would have been obvious based on the combination of Schön and Robb with I²C Spec or Vernon, or based only on the combination of Schön and Robb. To the extent Petitioner is asserting the former, Petitioner has not established a reasonable likelihood of prevailing for the reasons explained above. *See supra* Section II.D.5. To the extent Petitioner is asserting the latter, we address Petitioner’s arguments below and reject the ground as to claim 10 under 35 U.S.C. § 325(d). *See infra* Section II.H.

E. Obviousness Grounds Based on Schön, I²C Spec, Robb, Maxfield, Kerl, Golomb, and Mano, and Schön, Vernon, Robb, Maxfield, Kerl, Golomb, and Mano

Petitioner contends that claims 4–8 and 12–15 are unpatentable over Schön, I²C Spec, Robb, Maxfield, Kerl, Golomb, and Mano, and over Schön, Vernon, Robb, Maxfield, Kerl, Golomb, and Mano, under 35 U.S.C. § 103(a), and Patent Owner makes various arguments in response. *See* Pet. 26–35; Prelim. Resp. 20–28, 41–48, 51–56, 60–65.

Claims 4–8 depend, directly or indirectly, from claim 1. Petitioner does not rely on any of the Pseudorandom Number Generator References as teaching a slave address with “variable” and “fixed” address bit portions, and thus has not shown a reasonable likelihood of prevailing on either ground as to claims 4–8 for the reasons explained above regarding parent claim 1. *See supra* Section II.D.5.

Claims 12 and 15 recite that “the address generator includes a shift register and a non-volatile memory for storing a default address, the default address used to set the shift register with a start address defined by the default address” (the “default address” limitation). Petitioner makes the same arguments regarding the default address limitation for each claim, and we refer to those regarding independent claim 15 for convenience. See Pet. 31–32, 35. Claims 13 and 14 depend from claim 12.

Petitioner asserts that “using a Linear Feedback Shift Register (‘LFSR’) is a common method for implementing a pseudorandom number generator,” pointing to Maxfield as one example.⁶ *Id.* at 35 (citing Ex. 1011, 398 (“[T]he sequence of values generated by a software implementation of a maximal-length LFSR provides a reasonably good pseudo-random source, but is somewhat more expensive in terms of processing requirements.”)). Petitioner argues that it is “well-known to ‘seed’ a pseudorandom number generator with a starting value” and it would have been “obvious to use a non-volatile memory” to store such a value because “that is the only way to persist such information.” *Id.* Thus, according to Petitioner, it would have been “obvious to utilize the LFSR of Maxfield as part of the random number generator of Schön to achieve the limitations of the claim.” *Id.*

Petitioner’s arguments, however, do not address the language of the default address limitation. Claims 12 and 15 require a shift register and non-volatile memory that stores a “default address,” which is “used to set the shift register with a start address defined by the default address.” Petitioner points to Maxfield’s disclosure of a seed value input to a pseudorandom

⁶ Although Petitioner’s asserted ground includes all of the Pseudorandom Number Generator References, Petitioner only cites Maxfield in addressing the default address limitation in the Petition. Pet. 35.

number generator to generate a pseudorandom number, but never argues that Maxfield teaches a default or start “address” or explains how such a seed value could be considered a default or start “address.” *See id.* Indeed, the terms “default address” and “start address” do not appear in Petitioner’s analysis of the limitation. *See id.*

Further, as explained above, an “address” is the mechanism by which the replaceable unit is *addressed*. *See supra* Section II.D.5.b. Claims 12 and 15 both require that the replaceable unit comprise an “address generator” associated with the slave circuitry that generates “plural addresses so that the address of the replaceable unit can be changed.” In response to a command from the printing apparatus, the slave circuitry controls the address generator to “chang[e] the address of the replaceable unit.” The non-volatile memory of the address generator stores a “default address used to set the shift register with a start address defined by the default address.” Thus, the replaceable unit operates with its own “address,” which can start with a “default address” and change over time. This reading is consistent with the Specification. *See, e.g.,* Ex. 1001, col. 6, ll. 38–48 (disclosing that a “default address” is read from the non-volatile memory and “slave device 14 will then operate thereafter with the default address until a change of address is requested and carried out”), col. 8, ll. 56–63 (noting that after a power loss, “[s]ince the slave device 14 has lost its address, it can neither accept routine commands from the master device 12, nor respond thereto,” and describing a special command accepted by slave device 14 to reestablish a “viable address” after power is lost).

Petitioner does not argue that, or explain how, Maxfield’s seed value constitutes a “default address.” *See* Pet. 35. Rather, as described in the reference, it appears that the seed value used to initialize the LFSR can be

any value other than all zeros or all ones (depending on the type of LFSR).

See Ex. 1011, 386. Maxfield explains:

One quirk with an XOR-based LFSR is that, if it happens to find itself in the all 0s value, it will happily continue to shift all 0s indefinitely (similarly for an XNOR-based LFSR and the all 1s value). This is of particular concern when power is first applied to the circuit. Each register bit can randomly initialize containing either a logic 0 or a logic 1, and the LFSR can therefore “wake up” containing its “forbidden” value. For this reason, it is necessary to initialize an LFSR with a *seed* value.

Id. Thus, for an XOR-based LFSR, for example, the LFSR will be able to generate a sequence of pseudorandom numbers as long as it is initialized with any non-zero value. See *id.*; Prelim. Resp. 48.

Nor does Dr. Direen’s testimony provide adequate support for Petitioner’s position. Petitioner cites portions of his declaration describing how pseudorandom number generators work in general and their use in the Specification of the ’657 patent, Kerl, Maxfield, and Golomb, but those portions again do not address the particular language of the default address limitation. See Pet. 35 (citing Ex. 1002 ¶¶ 33, 38, 41). Petitioner further cites the claim chart attached to the declaration, but Dr. Direen there merely states that setting an initial value for a LFSR is the “same” as defining an initial address, without further explanation of why that would be the case. See *id.* (citing Ex. 1002, App. 1002-A, 35–36).

Petitioner has not made a sufficient showing that the asserted references, alone or in combination, teach the default address limitation. Accordingly, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claims 12–15 are unpatentable over Schön, I²C Spec, Robb, Maxfield, Kerl, Golomb, and Mano, or over Schön, Vernon, Robb, Maxfield, Kerl, Golomb, and Mano.

*F. Obviousness Grounds Based on Mayer, I²C Spec, and Robb,
and Mayer, Vernon, and Robb*

Petitioner contends that claims 1–3 and 9–11 are unpatentable over Mayer, I²C Spec, and Robb, and over Mayer, Vernon, and Robb, under 35 U.S.C. § 103(a), and Patent Owner makes various arguments in response. *See* Pet. 35–47; Prelim. Resp. 20–46, 56–65.

1. Mayer

Mayer discloses a method for automatic identification code generation in a data processing system having a bus, plurality of network devices, and bus master “used to control the flow [of] information between network devices connected to the bus.” Ex. 1005, col. 1, ll. 58–62, col. 2, ll. 45–51. Each network device includes a number generator for generating its own unique identification code, and “must register with the bus master in order to communicate over the bus.” *Id.* at col. 2, ll. 51–56. The bus master begins the identification code generation procedure by switching all network devices into “active mode” and sending a request for an identification code to each network device. *Id.* at col. 2, l. 57–col. 3, l. 1. In response to the bus master’s request, each network device sends its identification code to the bus master. *Id.* at col. 2, ll. 5–10. The bus master saves the received identification codes in an identification code table. *Id.* at col. 2, ll. 52–54. After the process completes, “the bus master compares the number of received identification codes with the number of devices connected to the bus.” *Id.* at col. 3, ll. 29–31. “If each network device has a unique identification code, then the number of transmitted identification codes corresponds to the number of devices connected to the bus” and the process is complete. *Id.* at col. 3, ll. 31–34. If the number of received identification

codes is smaller than the number of devices connected to the bus, however, there are at least two devices with the same identification code. *Id.* at col. 3, ll. 35–41. In that case, “the bus master requests all of the network devices to generate new identification codes and replace the existing identification codes with the new ones.” *Id.* at col. 3, ll. 44–54.

2. Claim 1

Petitioner relies on Mayer and Robb for the majority of the limitations of claim 1. Pet. 35–41. For example, Petitioner argues that Robb teaches a “container for ink or toner” (i.e., printer cartridge 12) comprising a “reservoir for holding ink or toner” (i.e., toner reservoir 38) and “slave circuitry for communicating with an imaging device as a slave device when connected thereto.” *Id.* at 37–38 (citing Ex. 1007 ¶¶ 17, 20, 21, Figs. 1, 2). Petitioner argues that Mayer teaches “slave circuitry” for communicating as a “slave device” and an “address generator” for generating plural addresses that can be changed in response to a command from an imaging device, citing Mayer’s disclosure of the bus master requesting all of the network devices to generate new identification codes and the devices generating respective identification codes in response. *Id.* at 37–40 (citing Ex. 1005, col. 1, ll. 7–29, 63–67, col. 3, ll. 42–46, col. 4, ll. 55–61). Petitioner relies, in the alternative, on I²C Spec and Vernon as teaching a “slave address [that] includes a variable address bit portion and a fixed address bit portion,” as recited in claim 1. *Id.* at 40–41. We address each proposed combination in turn.

a) *Combination of Mayer, I²C Spec, and Robb*

Petitioner argues that I²C Spec teaches a device address comprising seven bits, including four fixed (the claimed “fixed address bit portion”) and three programmable address bits (the claimed “variable address bit portion”). Pet. 40 (citing Ex. 1003, 15; Ex. 1002 ¶ 52). According to Petitioner, an ordinarily skilled artisan would have been motivated to combine Mayer and I²C Spec because Mayer teaches methods for “assigning addresses to devices on a shared bus” and I²C Spec is “the ‘de facto world standard’ for shared bus addressing and communication.” *Id.* at 35–36 (citing Ex. 1003, 3). Petitioner asserts that “[g]iven that the references are in the same field of endeavor and each teach the addressing of slave devices, a [person of ordinary skill in the art] would have found it obvious to combine their teachings.” *Id.* at 36.

Petitioner also asserts, without citation, that “I²C Spec defines the specification on which Mayer is built.” *Id.* According to Petitioner, “[g]iven that I²C Spec discloses address formats, a [person of ordinary skill in the art] would have been motivated to combine Mayer and [I²C Spec] as Mayer provides additional disclosure on device addressing techniques.” *Id.* (citing Ex. 1002, App. 1002-B, 7–8). Petitioner also asserts that “Mayer discusses the need for different addressing techniques, for instance assigning a unique session code to each device, once each device has received a unique slave address.” *Id.* at 40–41 (citing Ex. 1005, 3:55–61).

Patent Owner argues that Petitioner has failed to meet its burden in establishing that an ordinarily skilled artisan would have had reason to combine Mayer with I²C Spec. Prelim. Resp. 56–58. In particular, Patent Owner argues that neither Mayer, I²C Spec, nor the Petition identifies any disadvantages with Mayer’s existing address format that would have been

improved by the 7-bit format from I²C Spec. *Id.* at 56–57. Patent Owner argues that Petitioner does not explain why an ordinarily skilled artisan would have used I²C Spec’s 7-bit address format with a limited number of variable bits, which allows for fewer addresses to be modified in response to an address generation command, again relying on supporting testimony from Dr. Folkins. *Id.* at 57 (citing Ex. 2001 ¶¶ 163–170).

On this record, and for reasons similar to those addressed above regarding Schön and I²C Spec, we agree that Petitioner has failed to show that an ordinarily skilled artisan would have been motivated to combine the references as proposed. *See supra* Section II.D.5.a. Petitioner has not articulated sufficient rationale for the replacement of Mayer’s addressing scheme with I²C Spec’s addressing. Petitioner has not explained sufficiently how the I²C Spec addressing scheme would have been combined with the teachings of Mayer or why an ordinarily skilled artisan would have made the combination. Petitioner instead makes the conclusory assertion that a person of ordinary skill in the art would have combined the references, without sufficient explanation regarding how the combination would work or why an ordinarily skilled artisan would have made the combination.

Moreover, the disclosure of Mayer contradicts the basis for Petitioner’s proposed combination. Mayer teaches the importance of a large range of numbers for potential addresses generated by the network device number generator. *See* Ex. 1005, col. 4, l. 55–col. 5, l. 14; *see* Ex. 2001 ¶¶ 168–169. Mayer’s exemplary number generator uses sixteen digit numbers. Ex. 1005, col. 5, ll. 3–5. Mayer specifically notes that the chance of assigning the same identification code would be “exceedingly small for any small or medium sized network” if a number generator of this size were used. *Id.* at col. 5, ll. 5–9. Dr. Folkins testifies that the penalty for duplicate

addresses in Mayer is particularly severe because the entire addressing process is repeated until no duplicates occur. *See* Ex. 2001 ¶¶ 167–170.

This penalty would be a significant disadvantage to using I²C Spec’s addressing scheme in place of Mayer’s according to Dr. Folkins. *Id.*

¶¶ 169–170 (opining that I²C Spec “provides precisely the opposite effect as what Mayer’s system needs,” where the use of I²C Spec’s address format “would have created more address conflicts, more repetitive executions of the address discovery/generation process, and thus slower discovery/generation of slave device addresses”). We credit this uncontroverted testimony, which is consistent with the disclosure of Mayer and I²C Spec.

Again, we recognize that, according to our rules, we “will take into account a patent owner preliminary response where such a response is filed, including any testimonial evidence, but a genuine issue of material fact created by such testimonial evidence will be viewed in the light most favorable to the petitioner solely for purposes of deciding whether to institute an *inter partes* review.” 37 C.F.R. § 42.108(c). However, in this case, Dr. Folkins’s testimony does not implicate a genuine issue of material fact because Petitioner does not provide *any* argument or cite to *any* testimony regarding the advantages or disadvantages of using I²C Spec’s addressing scheme in place of Mayer’s. *See* Pet. 35–41. Petitioner merely asserts, without further explanation, that Mayer teaches “generating device . . . addresses,” I²C Spec teaches one “address format[,],” and a person of ordinary skill in the art would have been motivated to use the latter. *Id.* at 36. Dr. Direen’s testimony makes no mention of advantages or disadvantages of replacing Mayer’s addressing scheme with I²C Spec’s addressing scheme. *See* Ex. 1002, App. 1002-B, 6 (opining that a person of

ordinary skill in the art would have been “motivated to combine the teaching of Mayer with the I²C Standard as they both deal with similar master/slave bus systems and both systems require the slave devices to have unique addresses,” and “[i]t would be natural for a [person of ordinary skill in the art] to combine the teaching of the I²C standard with [Mayer’s] teachings as they both relate to similar computer bus systems,” without addressing advantages or disadvantages of the addressing schemes).

Petitioner has not articulated sufficient rationale for the replacement of Mayer’s addressing scheme with I²C Spec’s addressing, which is the proposed combination of teachings of these references. Accordingly, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claim 1 is unpatentable over Mayer, I²C Spec, and Robb.

b) Combination of Mayer, Vernon, and Robb

Petitioner’s arguments that Vernon teaches a slave address with “variable” and “fixed” address bit portions, as recited in claim 1, are identical to those addressed above regarding the combination of Schön, Vernon, and Robb. *Compare* Pet. 20–21, *with id.* at 40–41. Accordingly, for the reasons explained above, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claim 1 is unpatentable over Mayer, Vernon, and Robb. *See supra* Section II.D.5.b.

3. Claims 2, 3, 9, and 11

Claims 2, 3, and 9 depend from claim 1. Claim 11 depends from claim 10, but recites the same “variable” and “fixed” address bit portions as claim 1. Petitioner makes the same arguments regarding I²C Spec and Vernon. *See* Pet. 40–41, 46–47. These arguments are unpersuasive for the

reasons explained above. Accordingly, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claims 2, 3, 9, and 11 are unpatentable over Mayer, I²C Spec, and Robb, or over Mayer, Vernon, and Robb.

4. *Claim 10*

In its Petition, Petitioner states that it is asserting a ground of unpatentability under 35 U.S.C. § 103(a) based on the combination of “Mayer, I²C Spec or Vernon, and Robb.” Pet. 3–4, 35. In addressing the limitations of claim 10, however, Petitioner only cites Mayer and Robb; Petitioner never cites I²C Spec or Vernon in its arguments regarding claim 10. *Id.* at 43–46; *see* Ex. 1002, App. 1002-B, 22 (Dr. Direen opining that “Mayer in light of Robb renders [claim 10] obvious”). Similar to the asserted grounds based in part on Schön, it is unclear from the Petition whether Petitioner contends that claim 10 would have been obvious based on the combination of Mayer and Robb with I²C Spec or Vernon, or based only on the combination of Mayer and Robb. *See supra* Section II.D.7. To the extent Petitioner is asserting the former, Petitioner has not established a reasonable likelihood of prevailing for the reasons explained above. *See supra* Section II.F.2. To the extent Petitioner is asserting the latter, we address Petitioner’s arguments below and reject the ground as to claim 10 under 35 U.S.C. § 325(d). *See infra* Section II.H.

G. Obviousness Grounds Based on Mayer, I²C Spec, Robb, Maxfield, Kerl, Golomb, and Mano, and Mayer, Vernon, Robb, Maxfield, Kerl, Golomb, and Mano

Petitioner contends that claims 4–8 and 12–15 are unpatentable over Mayer, I²C Spec, Robb, Maxfield, Kerl, Golomb, and Mano, and over Mayer, Vernon, Robb, Maxfield, Kerl, Golomb, and Mano, under 35 U.S.C. § 103(a), and Patent Owner makes various arguments in response. *See* Pet. 47–56; Prelim. Resp. 20–28, 41–50, 56–65.

Claims 4–8 depend, directly or indirectly, from claim 1. Petitioner does not rely on any of the Pseudorandom Number Generator References as teaching a slave address with “variable” and “fixed” address bit portions, and thus has not shown a reasonable likelihood of prevailing on either ground as to claims 4–8 for the reasons explained above regarding parent claim 1. *See supra* Section II.F.2.

Petitioner’s analysis regarding the default address limitation of claims 12 and 15 is identical to its analysis for the previously addressed grounds. *Compare* Pet. 31–32, 35, *with id.* at 51, 55–56. Petitioner has not shown a reasonable likelihood of prevailing as to claims 12 and 15, or claims 13 and 14, which depend from claim 12, for the reasons explained above. *See supra* Section II.E.

H. Claim 10

Patent Owner argues that the Petition as a whole should be denied under 35 U.S.C. § 325(d) because Schön and Robb were considered and applied by the examiner in claim rejections during prosecution of the parent

of the '657 patent, U.S. Patent No. 8,225,021 B2 (“the '021 patent”),⁷ and Mayer is cumulative of Schön. Prelim. Resp. 60–64. As explained above, it is unclear what specific combination(s) of references Petitioner is asserting in challenging claim 10, given Petitioner’s use of “I²C Spec or Vernon” in the Petition and the fact that Petitioner never refers to I²C Spec or Vernon in its arguments regarding the limitations of claim 10. See Pet. 3–4, 15, 23–25, 35, 43–46 (emphasis added); *supra* Sections II.D.7, II.F.4. To the extent Petitioner is asserting grounds for claim 10 under 35 U.S.C. § 103(a) based on the combination of Schön and Robb or based on the combination of Mayer and Robb, under the particular factual circumstances of this case, we agree with Patent Owner’s arguments as to claim 10.⁸

Institution of *inter partes* review is discretionary. *Harmonic*, 815 F.3d at 1367. Pursuant to 35 U.S.C. § 325(d), in determining whether to

⁷ U.S. Patent Application No. 13/550,579, which issued as the '657 patent, is a continuation of U.S. Patent Application No. 12/474,052, which issued as the '021 patent. Petitioner challenges claims of the '021 patent in Case IPR2019-01389.

⁸ See, e.g., *DynaEnergetics US, Inc. v. GEODynamics, Inc.*, PGR2018-00065, Paper 8 (PTAB Nov. 15, 2018) (denying institution, finding that the petitioner had failed to show that claims were more likely than not unpatentable based on certain grounds and exercising discretion to deny review as to other grounds under 35 U.S.C. § 325(d)); *Nikon Corp. v. Carl Zeiss AG*, IPR2018-00686, Paper 7 (PTAB Sept. 27, 2018) (denying institution, finding that the petitioner had failed to show a reasonable likelihood of prevailing as to certain grounds and exercising discretion to deny review as to other grounds under 35 U.S.C. § 325(d)); *SMR Auto. Sys. USA, Inc. v. Magna Mirrors of Am., Inc.*, IPR2018-00931, Paper 7 (PTAB Sept. 14, 2018) (same); *Pfizer, Inc. v. Genentech, Inc.*, IPR2018-00373, Paper 12 (PTAB Aug. 2, 2018) (same); *Initiative for Medicines, Access & Knowledge (I-MAK), Inc. v. Gilead Pharmasset LLC*, IPR2018-00125, Paper 9 (May 24, 2018) (same).

institute an *inter partes* review, “the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”

In evaluating whether to exercise our discretion when the same or substantially the same prior art or arguments previously were presented to the Office under section 325(d), we have weighed some common *non-exclusive* factors, such as: (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph) (“*Becton, Dickinson*”).

We begin with factors (a) and (b). During prosecution of the parent ’021 patent, the examiner rejected certain claims as anticipated by Schön under 35 U.S.C. § 102(b), rejected other claims as unpatentable over Schön and Robb under 35 U.S.C. § 103(a), and indicated that other claims would be allowable if rewritten in independent form. Ex. 1015 (Office Action dated June 7, 2011).⁹ Similar to claim 10, the claims rejected based on the

⁹ Petitioner filed copies of the prosecution histories of the ’021 and ’657 patents as Exhibits 1008 and 1019, respectively, but did not include page numbers as required by 37 C.F.R. § 42.63(d)(2)(i). Petitioner also filed certain materials from the prosecution history of the ’021 patent as

combination of Schön and Robb (e.g., original claim 18) recited a “replaceable container for containing a material that is deposited on [a] print medium,” “data bus,” “master device,” and “at least one slave device . . . identified by a unique address” having “means for generating addresses for said slave device” so that the device “can periodically be identified by a new address,” where the master device “periodically command[s] said slave device to change its address.” Ex. 1008 (claims filed May 28, 2009). The applicants subsequently amended the claims and submitted a Request for Continued Examination and Information Disclosure Statement with an international search report, and the examiner allowed the pending claims. See Ex. 1008 (materials dated October 7, 2011, November 1, 2011, February 1, 2012, and March 14, 2012). The same examiner again considered Schön and Robb during prosecution of the ’657 patent and allowed the pending claims. See Ex. 1001, code (56); Ex. 1019 (Notice of Allowability dated October 22, 2012); Pet. 6–8 (describing the prosecution histories of the ’021 and ’657 patents).

We also agree with Patent Owner that, as applied by Petitioner to claim 10, Mayer is cumulative to Schön, the disclosure of which was considered and applied by the examiner in a rejection during prosecution of the parent ’021 patent. See Prelim. Resp. 62–63. Both references teach master and slave devices on a bus, the master device sending a command to the slave device to generate an address, the slave device generating its own address in response, and the master device discovering the addresses generated by the slave devices. See *id.* at 62. Importantly, Petitioner relies

Exhibits 1015 and 1016. Where necessary, we refer to material in the prosecution histories by date.

on both Schön and Mayer as teaching the same limitations of claim 10, namely “slave circuitry” for communicating with another device as a “slave device” and “an address generator associated with the slave circuitry, the address generator generating plural addresses so that the address of the replaceable unit can be changed,” wherein “the slave circuitry is responsive to a command from the printing apparatus for changing the address of the replaceable unit, and controls the address generator for changing the address thereof.” See Pet. 24–25, 43–46. Petitioner’s asserted reasons to combine Schön with Robb likewise are nearly identical to those for combining Mayer with Robb. Compare *id.* at 17–18, with *id.* at 37. The testimony of Dr. Direen regarding both combinations is similar as well. See Ex. 1002 ¶¶ 72–81; compare *id.*, App. 1002-A, 20–25, with *id.*, App. 1002-B, 18–22. Factors (a) and (b) weigh in favor of denying institution of review as to claim 10.

Factor (c), “the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection,” also weighs in favor of denial. See *Becton, Dickinson*, Paper 8 at 17. Schön and Robb were evaluated during prosecution of the parent ’021 patent and used in combination as the basis for an obviousness rejection, just as Petitioner asserts in the Petition.

The remaining factors (d), (e), and (f), “the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art,” “whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art,” and “the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments,” weigh in favor of denial as well. See *id.* at 17–18.

Many of the arguments made by Petitioner in support of its contention that Schön and Robb teach the limitations of claim 10 are very similar to how the examiner found similar limitations taught by the references during prosecution of the '021 patent. *See* Pet. 23–25, 43–44; Ex. 1015, 2–5. Indeed, Petitioner expressly relies on the examiner's findings regarding Schön and Robb in the Petition. *See, e.g.*, Pet. 11, 17–18, 22, 37 (arguing that the examiner “properly” relied on Schön and Robb for certain limitations). With respect to claim 10 in particular, Petitioner points to no particular error in the examiner's analysis, or any other evidence or facts, that would warrant reconsideration of the prior art disclosures already considered by the examiner. Based on the parties' arguments and particular facts of this proceeding, and weighing the factors listed above, we conclude that it is appropriate to exercise our discretion to deny institution of review as to claim 10 under 35 U.S.C. § 325(d).

III. CONCLUSION

Based on the arguments presented in the Petition, we conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the '657 patent challenged in the Petition. Further, to the extent Petitioner is asserting a ground of unpatentability for claim 10 based solely on Schön and Robb or based solely on Mayer and Robb, taking into account the factors set forth in *Becton, Dickinson*, we find that the evidence weighs in favor of exercising our discretion and denying institution of review as to such ground(s) under 35 U.S.C. § 325(d). Therefore, we do not institute an *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied and no *inter partes* review is instituted.

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