

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIVERSAL IMAGING INDUSTRIES, LLC,
Petitioner,

v.

LEXMARK INTERNATIONAL, INC.,
Patent Owner.

IPR2019-01378
Patent 9,245,591 B2

Before JUSTIN T. ARBES, DAVID C. McKONE, and
MATTHEW J. McNEILL, *Administrative Patent Judges*.

McKONE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Universal Imaging Industries, LLC (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–16 of U.S. Patent No. 9,245,591 B2 (Ex. 1001, “the ’591 patent”). Pet. 1. Lexmark International, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. See 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2019). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Under the circumstances of this case, for the reasons explained below, we decline to institute *inter partes* review of the challenged claims of the ’591 patent.

B. *Related Matters*

The parties indicate that Patent Owner has asserted the ’591 patent against Petitioner in *Lexmark International, Inc. v. Universal Imaging Industries, LLC*, 8:18-cv-01047-EAK-AEP (M.D. Fla.). Pet. 1; Paper 4, 3. Petitioner also has filed several petitions for *inter partes* review of related patents of Patent Owner. Pet. 1; Paper 4, 3–4.

C. *The ’591 Patent*

The ’591 patent relates to an addressing scheme for non-volatile memory in modules such as printer ink/toner cartridges. Ex. 1001, 1:34–37,

4:19–24. One example is described with reference to Figure 1C, reproduced below:

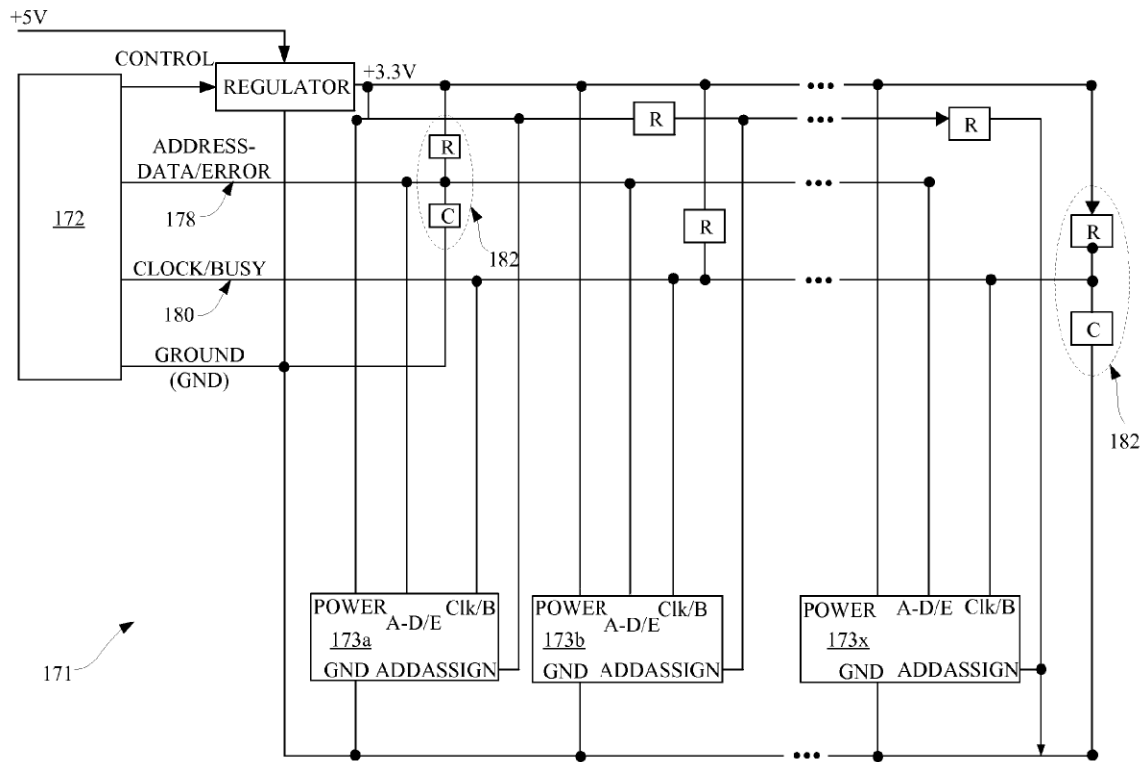


FIG. 1C

Figure 1 C is a schematic of electrical interface 171 between controlling computer system 172 and non-volatile memory modules 173a–173x. *Id.* at 3:27–28, 8:24–30. Electrical interface 171 encodes a binary clock with values 0 and 1 and a busy status on Clock/Busy channel 180; and binary data transmission values of 0 and 1 and error status information on Address-Data/Error channel 178. *Id.* at 8:37–42.

Controlling computer system 172 and memory modules 173a–173x can communicate bi-directionally using Clock/Busy channel 180 by using three voltage levels. Specifically, the maximum voltage of Clock/Busy channel 180 can be clamped at an intermediate voltage, for example by shorting Clock/Busy channel 180 to ground through a Zener diode, when at

least one of memory modules 173a–173x reports a busy condition. *Id.* at 9:2–9. The three voltage levels allow the following three communication conditions:

- 1) When Clock/Busy channel 180 is at a low voltage, it encodes a logical 0 clock state independent of whether any of memory modules 173a–173x are reporting a busy condition. *Id.* at 8:60–63;
- 2) When Clock/Busy channel 180 is at an intermediate voltage level, it encodes a logical 1 clock state and indicates that at least one of memory modules 173a–173x is reporting a busy condition. *Id.* at 8:63–66;
- 3) When Clock/Busy channel 180 is at a high voltage level, it encodes a logical 1 clock state and indicates that none of memory modules 173a–173x is reporting a busy state. *Id.* at 8:66–9:2.

The '591 patent describes a similar three-voltage-level scheme for communicating over Address-Data/Error channel 178. *Id.* at 8:43–60.

Claim 1, reproduced below, is illustrative of the invention:

1. A memory module, comprising:
a plurality of memory cells; and
a plurality of signal lines for communicating with a processing device, the memory module configured such that upon encountering a first condition while processing a command received by the memory module, the memory module limits a voltage on a first signal line of the plurality of signal lines to be no more than an intermediate voltage greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding to a binary one state for a period of time for indicating an occurrence of the first condition,

wherein the memory module is configured to receive a first signal on the first signal line, and during the period of time the memory module limits a voltage on the first signal line to be no greater than the intermediate voltage, a voltage level on the first signal line corresponding to the binary zero state is interpreted by the memory module as a binary zero state of the first signal and the intermediate voltage on the first signal line is interpreted by the memory module as a binary one state of the first signal such that during the period of time, the memory module receives the first signal on the first signal line while at the same time the memory module communicates the occurrence of the first condition on the first signal line to the processing device,

wherein the first signal comprises a clock signal and the first condition comprises a busy condition.

D. Evidence

Petitioner relies on the references listed below.

Reference		Date	Exhibit No.
Blood	US 3,993,867	issued Nov. 23, 1976	1003
I ² C Spec	Phillips Semiconductors, <i>The I²C-Bus Specification</i> , V.2.1	Jan. 2000	1004
Bruce	US 5,822,251	issued Oct. 13, 1998	1005

Petitioner also relies on the Declaration of Harry Direen, Ph.D., P.E.
(Ex. 1002).

Patent Owner relies on the Declaration of Jeffrey J. Folkins, Ph.D.
(Ex. 2001).

E. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–16 on the ground of obviousness, under 35 U.S.C. § 103, over Blood, I²C Spec, and Bruce. Pet. 2–3.

II. ANALYSIS

A. Claim Construction

For petitions filed after November 13, 2018, we construe claims “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2019)¹; *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Both parties believe that no term requires construction to resolve the parties’ dispute. Pet. 4; Prelim. Resp. 10. Based on the record before us, we do not find it necessary to provide any express claim constructions. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

¹ On October 11, 2018, the USPTO revised its rules to harmonize the Board’s claim construction standard with that used in federal district court. Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (now codified at 37 C.F.R. pt. 42). This rule change applies to petitions filed on or after November 13, 2018. *Id.*

B. Obviousness of Claims 1–16 over Blood, I²C Spec, and Bruce

Petitioner contends that claims 1–16 would have been obvious over Blood, I²C Spec, and Bruce. Pet. 9–34. A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are “such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” We resolve the question of obviousness on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.² See *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Level of Skill in the Art

Petitioner, relying on Dr. Direen’s testimony, proposes that a person of ordinary skill in the art “would have a bachelor’s degree in electrical and/or computer engineering with training and one or more years of experience in embedded systems, including both hardware and embedded software design.” Pet. 4 (citing Ex. 1002 ¶¶ 25–28). Patent Owner, relying on Dr. Folkins’s testimony, proposes a different level of skill, namely, “a bachelor’s degree in electrical and/or computer engineering with one or more years of work experience in printer design, including hardware and/or

² The record does not include allegations or evidence of objective indicia of nonobviousness.

embedded software design for printer applications.” Prelim. Resp. 9 (citing Ex. 2001 ¶¶ 29–31).

The only meaningful difference we discern between the competing proposals is that Patent Owner more narrowly limits the work experience of a skilled artisan to printer design. The ’591 patent and the prior art (e.g., Blood) are not limited to printer design, however. Thus, we are not persuaded that the experience of a skilled artisan would have been limited to that field. Accordingly, on the record presented, we adopt Petitioner’s proposal. Nevertheless, Patent Owner “does not believe that the definition of a [person of ordinary skill in the art] will be dispositive of the outcome of this proceeding because Petitioner has not shown that the claims are anticipated or obvious to a [person of ordinary skill in the art] given either proposed level of skill.” Prelim. Resp. 9 (citing Ex. 2001 ¶¶ 32–33).

2. Scope and Content of the Prior Art

a) Overview of Blood

Blood relates to transmission of full duplex digital signals over a single line. Ex. 1003, Abs. Blood explains that the transmitter and receiver pair discussed therein “are used as generic expressions to denote many diverse systems and subsystem components, such as . . . memories, registers, central processing units and the like that function as a transmitter or receiver of digital signals. Likewise, a ‘transmission line’ is used as a generic expression to denote a single signal transmission path, such as a bus interconnecting the stations.” *Id.* at 2:23–32.

Figure 2, reproduced below, illustrates an example:

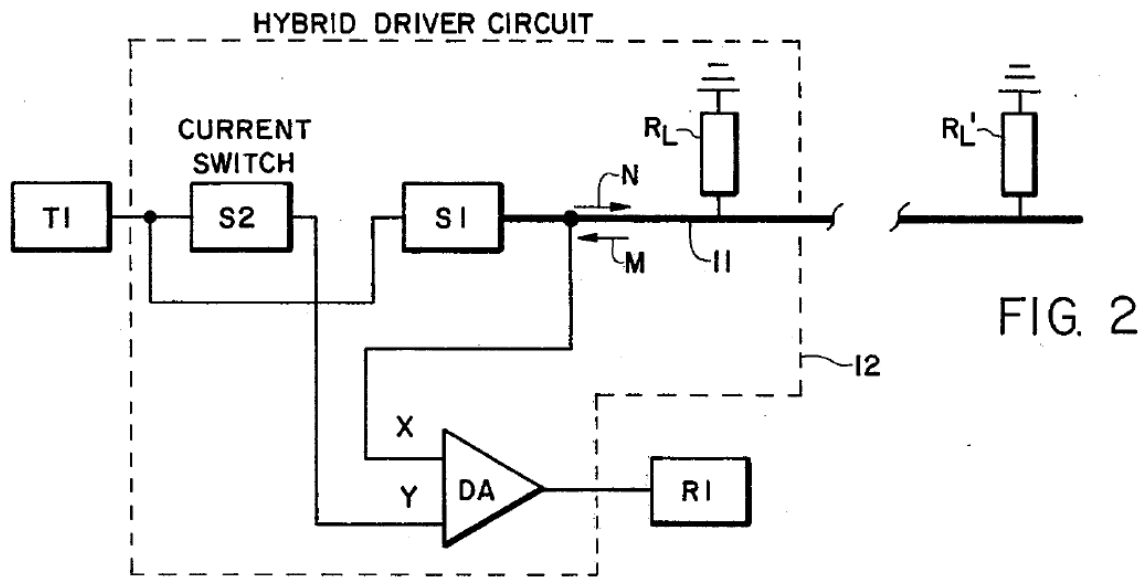


Figure 2 is a block diagram of a driver circuit. *Id.* at 2:6–7. Switching means S1 applies an outgoing signal from transmitter T1 to single signal line or bus 11 and to input X of differential amplifier DA, which is connected to receiver R1. *Id.* at 2:56–60. Second switch S2 derives an indicating signal representing the outgoing signal from transmitter T1 and applies it to input Y of differential amplifier DA. *Id.* at 2:61–64. Line 11 might include a signal transmitted by another transmitter T2. Differential amplifier DA compares inputs X and Y and, in essence, subtracts from the bus signal the signal transmitted by transmitter T1, allowing only the received signal from transmitter T2 to pass to receiver R1. *Id.* at 3:1–7.

Figure 3, reproduced below, illustrates these various signals:

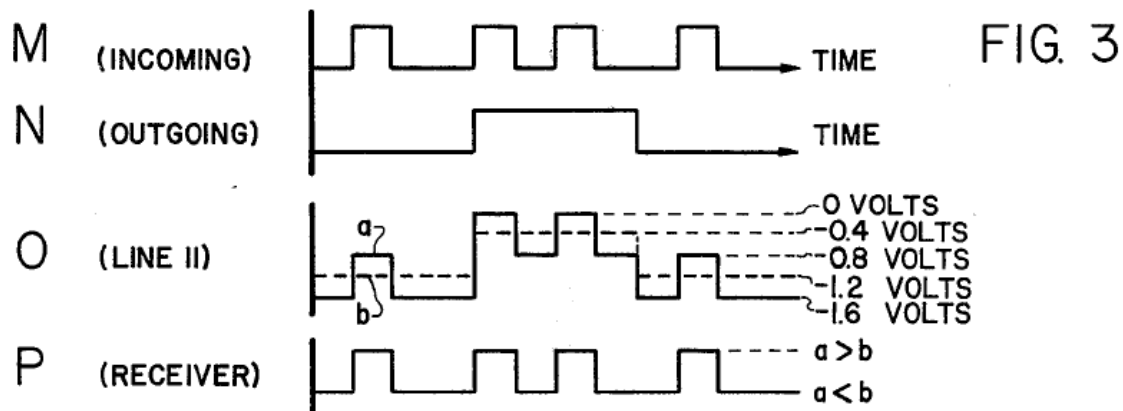


Figure 3 is a diagram showing signal waveforms at certain points in the circuitry of Figure 2 with respect to time. *Id.* at 2:8–10. Waveform M (Incoming) represents the incoming waveform from transmitter T2 and waveform N (Outgoing) represents the outgoing signal from transmitter T1. *Id.* at 3:16–22. The combined signal found on line 11 is shown in waveform O (Line 11). *Id.* at 3:35–47. “O is a composite or algebraic addition of the outgoing and incoming waveforms M and N shown in FIG. 3. This composite waveform appears in line 11 and is also applied to one of the inputs, x, of the differential amplifier.” *Id.* at 3:42–47. Differential amplifier DA compares signals *a* and *b* at inputs X and Y of differential amplifier DA, respectively, and generates the output shown in waveform P (Receiver), which is the same as the signal incoming from transmitter T2. *Id.* at 4:9–14. This output of differential amplifier DA, waveform P, is applied to receiver R1. *Id.* at 4:18–20.

Blood explains that when neither T1 nor T2 is transmitting, no current is present in line 11 and the transmission voltage at the line is zero volts. *Id.* at 5:44–48. When T1 or T2 is transmitting a digital signal, voltage potential at line 11 shifts between two levels. *Id.* at 5:49–52. “When both

transmitters send, then the voltage level at the transmission line 11 shifts between three levels, as illustrated in FIG. 3; O.” *Id.* at 5:52–55.

b) Overview of I²C Spec

I²C Spec specifies a standard for “a simple bi-directional 2-wire bus for efficient inter-IC control,” which I²C Spec calls “the Inter IC or I²C-bus.” Ex. 1004, 4. Dr. Direen testifies that “[a] person designing a product that includes an I²C [bus] will read and be familiar with the standard in order to properly make use of the I²C bus and protocols.” Ex. 1002 ¶ 52. I²C Spec describes communication over an I²C bus between a master (“The device which initiates a transfer, generates clock signals and terminates a transfer”) and a slave (“The device addressed by a master”). Ex. 1004, 7.

I²C Spec describes, *inter alia*, generation of clock signals on the I²C bus. Relevant to Petitioner’s allegations, “[b]us clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs.” *Id.* at 8. For example,

If a slave can’t receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the [serial clock line (SCL)] LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

Id. at 10.

c) Overview of Bruce

Bruce discloses a “flash-memory system” which is expandable. Ex. 1005, Abst. Bruce explains that “[a] busy signal is usually provided by

each flash-memory chip to indicate when the read, write, or erase operation has completed. The busy signal allows a local processor to continue with other tasks while the flash-memory integrated circuit chip performs the flash operation.” *Id.* at 1:66–2:3.

3. *Analysis of Claims 1–16*

Petitioner contends that both Blood and Bruce teach “[a] memory module, comprising: a plurality of memory cells,” as recited in claim 1. Pet. 10. Blood lists “memories” and “registers” as examples in which its transmission techniques could be used. Ex. 1003, 2:22–39. Bruce, in particular, describes its invention in the context of flash memories, such as those depicted in Figures 1 and 2. Ex. 1005, Abst., Figs. 1, 2. As to “a plurality of signal lines for communicating with a processing device,” as recited in claim 1, Petitioner cites to I²C Spec and Bruce. Pet. 10–11. I²C Spec shows communication via multiple signal lines (e.g., serial data line (SDA), serial clock line (SCL), and DLEN). Ex. 1004, 4, 18–19, Fig. 19. Bruce³ describes communicating command and address bytes from a controller to memory on a flash bus that has a plurality of shared lines. Ex. 1005, 2:57–60.

Petitioner contends that Blood and Bruce teach:

the memory module configured such that upon encountering a first condition while processing a command received by the memory module, the memory module limits a voltage on a first signal line of the plurality of signal lines to be no more than an intermediate voltage greater than voltage levels corresponding to a binary zero state and less than voltage levels corresponding

³ Petitioner purports to cite to Blood, Exhibit 1003. However, the column and line numbers, as well as the text quoted in the Petition, are clearly from Bruce. We assume that the reference to Blood is a typographical error.

to a binary one state for a period of time for indicating an occurrence of the first condition,
as recited in claim 1. Pet. 11–12. Specifically, Petitioner contends that Blood describes full-duplex transmission on a signal line that corresponds to three transmission levels, one of those levels being an intermediate voltage between a low voltage level and a high voltage level. *Id.* at 11. As noted above (and shown in Blood’s Figure 3, reproduced above), Blood describes two transmitters transmitting on the same bus, where the bus carries signals that can be at a low level (when both transmitters transmit a “zero”), a middle level (when one transmitter transmits a “zero” and the other transmits a “one”), and a high level (when both transmitters transmit “ones”).
Ex. 1003, 3:16–4:20.

Petitioner cites to Bruce for a teaching that a flash memory transmits a busy signal to a controller to indicate when flash operation is in progress. Pet. 11 (citing Ex. 1005, 3:19–21). According to Petitioner, the “busy” state corresponds to the claimed “first condition while processing a command received by the memory module,” as recited in claim 1. *Id.* In Petitioner’s theory, Bruce’s busy signal would be at a low logic level. With that assumption, “[a] busy signal on the memory going low will cause the line 11 voltage to go to an intermediate voltage halfway between the high and low voltages on line 11 when the processor side of the line is in the high state.” *Id.* at 11–12. Thus, Petitioner argues, “[w]hen the processor side of the line is in the low state and the memory busy signal is in the low state, line 11 will be at the low voltage, which is less than the intermediate voltage.” *Id.* at 12.

Claim 1 further recites:

wherein the memory module is configured to receive a first signal on the first signal line, and during the period of time the memory module limits a voltage on the first signal line to be no

greater than the intermediate voltage, a voltage level on the first signal line corresponding to the binary zero state is interpreted by the memory module as a binary zero state of the first signal and the intermediate voltage on the first signal line is interpreted by the memory module as a binary one state of the first signal such that during the period of time, the memory module receives the first signal on the first signal line while at the same time the memory module communicates the occurrence of the first condition on the first signal line to the processing device.

Petitioner argues (Pet. 12–13) that Blood describes interpreting an intermediate value as a binary one state when one transmitter is transmitting a binary zero and the other is transmitting a binary one and interpreting a voltage level corresponding to a binary zero as a binary zero state when both transmitters are transmitting a binary zero. *Id.* (citing Ex. 1003, 5:44–49, 6:3–12, 6:28–30). In Petitioner’s view, Blood teaches that a transmitter can communicate a first condition on the first signal line (e.g., a memory transmitting a binary zero state on the bus) to a receiver (e.g., a processing device). *Id.* at 13–14.

Claim 1 further recites “wherein the first signal comprises a clock signal and the first condition comprises a busy signal.” Petitioner cites I²C Spec for a disclosure that, in a system compatible with the I²C standard, bus clock signals from a master can be altered by a slow-slave device that holds down the clock line, for example, when the slave cannot receive or transmit another complete byte of data until it has performed some other function. Pet. 14 (citing Ex. 1004, 8, 10). Petitioner argues that this shows that it was well-known for a device to send a busy condition in response to a signal on the clock line. *Id.*

Patent Owner contends that “the Petition fails to show that the memory module interpreting an intermediate value as a binary one enables

the memory module to simultaneously communicate a busy condition and receive clock information from the processing device.” Prelim. Resp. 43–44. According to Patent Owner, Blood merely provides a generic description of duplexing between two stations, saying nothing of clock or busy signals, and the Petition improperly assumes a hypothetical scenario in which one station shown in Blood is a memory module and the other is a processing device. *Id.* at 44.

Patent Owner further argues that Petitioner’s proposed combination would be inoperable and inconsistent with I²C Spec. *Id.* at 45. According to Patent Owner, the purpose of the clock-stretching feature described in I²C Spec is to stop the master from generating more clock signals until the slave releases the line. *Id.* Therefore, Patent Owner argues, I²C Spec does not teach signaling a busy condition while at the same time receiving clock signals from the master. *Id.* Dr. Folkins testifies that, “[b]ecause only one data bit may be transmitted per clock cycle, holding down the clock signal enables a slave device to limit the rate at which data is transmitted, which enables a slower device on the bus (e.g. what the I²C Specification refers to as a ‘slow-slave’ device) to ensure that data is not transmitted faster than it is received.” Ex. 2001 ¶ 88. According to Dr. Folkins, “because data bits may only be changed when the clock signal changes, this feature stops the master from transmitting additional data until the slave device releases the line.” *Id.* ¶ 89. Patent Owner argues that, because the purpose of holding the line low in I²C Spec is to prevent the clock line from going high until the line is released, continuing to receive clock signals would directly contradict the teachings of I²C Spec and the combination would be inoperable. Prelim. Resp. 45.

On the record presented, we are persuaded by Patent Owner. Petitioner's theory as to why a skilled artisan would have combined I²C Spec with Blood and Bruce is that the skilled artisan would have done so to follow an industry standard, I²C. According to Petitioner, "I²C Spec . . . deals with signaling on a shared bus, and is in fact the 'de facto world standard' for shared bus addressing and communication. As such, a [person of ordinary skill in the art] would also rely on the teachings of I²C Spec to implement memory chips communicating on an I²C bus." Pet. 9–10 (quoting Ex. 1004, 3). A combination that did not comply with this standard would undermine Petitioner's stated reason to combine I²C Spec with Blood and Bruce. As Dr. Direen testifies, "[m]anufacture[r]s who make integrated circuit devices such as a memory device that supports an I²C bus interface are expected to design the device such that the I²C interface conforms to the standard." Ex. 1002 ¶ 53.

Patent Owner has introduced credible evidence that Petitioner's proposed combination, in which both a busy signal and a clock signal are transmitted simultaneously on the same bus (from a memory and from a processing device, respectively) would have been at odds with I²C Spec. Prelim. Resp. 45 (citing Ex. 2001 ¶¶ 88–89, 178). As noted above, I²C Spec describes a slave holding the serial clock line (SCL) at a low level to force the master into a wait state when the slave cannot process more data. Ex. 1004, 10. "Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL." *Id.* Thus, as Dr. Folkins testifies, "because data bits may only be changed when the clock signal changes, this feature stops the master from transmitting additional data until the slave device releases the line." Ex. 2001 ¶ 89.

In Petitioner’s proposed combination, however, a processor (corresponding to a master in I²C Spec) would continue to send a clock signal when a memory device on the bus (corresponding to a slave in I²C Spec) sends a busy signal. Pet. 11–14; Ex. 1002, A5–A8.⁴ As Dr. Direen testifies, in Petitioner’s combination, the “memory module will receive the processing device’s clock signal (binary 1s and 0s) no matter what the state of the memory module’s busy signal.” Ex. 1002, A8. This is inconsistent with I²C Spec, in which a signal from the slave holding down the bus temporarily disables the clock from the master such that no data is written to the slave while the slave is holding the line down. Ex. 1004, 8, 10. Dr. Folkins testifies that “the purpose of holding the line low in both cases [(examples of I²C Spec pages 8 and 10)] is to prevent further transmission of data until the line is released.” Ex. 2001 ¶ 90. According to Dr. Folkins, “allowing a master device to continue to transmit clock signals at an intermediate voltage while the line is being held low would defeat the purpose of the clock-stretching features taught by the I²C Specification.” *Id.* We credit this uncontroverted testimony.

We recognize that, according to our Rules, we “will take into account a patent owner preliminary response where such a response is filed, including any testimonial evidence, *but a genuine issue of material fact created by such testimonial evidence will be viewed in the light most favorable to the petitioner solely for purposes of deciding whether to institute an inter partes review.*” 37 C.F.R. § 42.108(c) (emphasis added). In this case, Dr. Folkins’s testimony does not implicate a genuine issue of

⁴ Here, we cite to the claim chart appendix to Dr. Direen’s Declaration, which is labeled 1002-A. A5–A8 refers to pages 5–8 of the claim chart.

material fact. Petitioner (Pet. 14) simply cites to the disclosure of I²C Spec (Ex. 1004, 8, 10). The disclosure in I²C Spec discussed above is consistent with Dr. Folkins's testimony (Ex. 2001 ¶¶ 88–90). Petitioner does not cite to expert testimony that would contradict Dr. Folkins or, indeed, support its own arguments. Pet. 14.

Moreover, Dr. Direen's testimony would not support Petitioner's position even if cited. Rather, Dr. Direen does not testify that "wherein the first signal comprises a clock signal and the first condition comprises a busy signal," as recited in claim 1, is taught by I²C Spec, as argued by Petitioner (Pet. 14). Rather, it is Dr. Direen's opinion that Blood, by itself, teaches this limitation. Ex. 1002, A9. According to Dr. Direen,

[b]ased upon Blood's teaching, a [person of ordinary skill in the art] faced with establishing communication lines between a processing device and a memory device has all the tools he/she needs to apply the teaching. It then simply becomes an ordinary design choice as to which memory interface signals to combine onto single lines, thereby reducing the number of connections between the processing device and the memory device. The choice is somewhat arbitrary. With Blood teaching at hand, it is well within a [person of ordinary skill in the art]'s skill set to choose to combine the clock and busy signals onto a common signal line.

Id. Here, Dr. Direen's theory is different from that of Petitioner. Indeed, it is unclear whether Dr. Direen relies on I²C Spec at all in his application of the prior art to claim 1. *See id.* at A2–A9. The only reference to I²C is at page A4, which does not appear to be a citation to I²C Spec. *Id.* at A4 ("I2C is a common interface for memory modules. The I2C interface makes use of an address-data signal line and a clock signal line. It is clear to a [person of ordinary skill in the art] reviewing Figure 1 of the '591 [patent] that an I2C bus is being used."). It appears that Dr. Direen has a different theory of

obviousness, involving a different combination of references (Blood and Bruce only) than that advanced by Petitioner. Thus, Dr. Direen does not support Petitioner's position and does not supply a genuine issue of material fact to resolve in a trial.

The evidence in the record suggests that Petitioner's proposed combination would result in a system that does not comply with the standard set forth in I²C Spec. Petitioner's only stated reason for combining I²C Spec with Blood and Bruce is that a skilled artisan would do so to comply with the I²C standard specified in I²C Spec. Pet. 9–10. Thus, the evidence, namely the disclosure of I²C Spec and Dr. Folkins's testimony regarding that disclosure, undermines Petitioner's stated reason to combine I²C Spec with Blood and Bruce. Ex. 1004, 8, 10; Ex. 2001 ¶¶ 88–90. “An inference of nonobviousness is especially strong where the prior art's teachings undermine the very reason being proffered as to why a person of ordinary skill would have combined the known elements.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1326 (Fed. Cir. 2009). In light of the uncontroverted evidence that undermines Petitioner's stated reason to combine the references, Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claim 1 would have been obvious over Blood, I²C Spec, and Bruce.

Claims 2–6 depend from claim 1. Petitioner's additional arguments and evidence regarding these dependent claims do not cure the above-noted deficiency in Petitioner's showing for claim 1. Pet. 15–17. Accordingly, Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 2–6 would have been obvious over Blood, I²C Spec, and Bruce.

Independent claim 7 recites “the apparatus receives a clock signal on the first signal line, and the at least one condition comprises a busy status condition . . . and . . . wherein . . . the memory module receives the clock signal on the first signal line while at the same time the memory module communicates the occurrence of the busy status condition on the first signal line to a processing device.” Similarly, independent claim 11 recites “a first signal line for receiving, by the memory device, clock information” wherein “the memory device receives the clock information on the first signal line while at the same time the memory device communicates the busy condition on the first signal line to the processing device.” Petitioner’s arguments for these limitations appear to be substantially the same as those detailed above for claim 1, “wherein the first signal comprises a clock signal and the first condition comprises a busy signal.” Pet. 18 (citing Ex. 1004, 8, 10), 21–22 (same), 27 (same), 30–32. Dr. Direen’s opinion for each of claims 7 and 11 is that, in his proposed combination, the “memory module will receive the processing device’s clock signal (binary 1s and 0s) no matter what the state of the memory module’s busy signal.” Ex. 1002, A31 (claim 7), A48 (for claim 11, “the memory device receives the clock signal while at the same time the memory device communicates the busy condition on the first signal line to a processing device”). For the same reasons as given for claim 1, Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 7 and 11 would have been obvious over Blood, I²C Spec, and Bruce.

Claims 8–10 depend from claim 7 and claims 12–16 depend from claim 11. Petitioner’s additional arguments and evidence regarding these dependent claims do not cure the above-noted deficiency in Petitioner’s showing for claim 1. Pet. 24–26, 32–34. Accordingly, Petitioner has not

demonstrated a reasonable likelihood that it would prevail in showing that claims 8–10 and 12–16 would have been obvious over Blood, I²C Spec, and Bruce.

III. CONCLUSION

Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that claims 1–16 would have been obvious over Blood, I²C Spec, and Bruce.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied* as to the challenged claims of the '591 patent, and no *inter partes* review is instituted.

IPR2019-01378
Patent 9,245,591 B2

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