

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIVERSAL IMAGING INDUSTRIES, LLC,
Petitioner,

v.

LEXMARK INTERNATIONAL, INC.,
Patent Owner.

IPR2019-01383
Patent 8,850,079 B2

Before JUSTIN T. ARBES, DAVID C. McKONE, and
GREGG I. ANDERSON, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Petitioner Universal Imaging Industries, LLC, filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–22 of U.S. Patent No. 8,850,079 B2 (Ex. 1001, “the ’079 patent”) pursuant to 35 U.S.C. § 311(a). Patent Owner Lexmark International, Inc., filed a

Preliminary Response (Paper 6, “Prelim. Resp.”) pursuant to 35 U.S.C. § 313. Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons that follow, we do not institute an *inter partes* review.

B. Related Matters

The parties indicate that the ’079 patent is the subject of the following district court case: *Lexmark International, Inc. v. Universal Imaging Industries, LLC*, Case No. 8:18-cv-01047-EAK-AEP (M.D. Fla.). *See* Pet. 1; Paper 3, 2–3. Petitioner has filed petitions challenging other patents also asserted in the district court case in Cases IPR2019-01368, IPR2019-01369, IPR2019-01378, IPR2019-01380, IPR2019-01381, IPR2019-01385, IPR2019-01387, IPR2019-01388, and IPR2019-01389.

C. The ’079 Patent

The ’079 patent relates to “addressing schemes, and, more particularly, to dynamically changing addresses of components in an imaging device to provide enhanced security.” Ex. 1001, col. 1, ll. 32–35. The ’079 patent describes known techniques for communication between a bus master and uniquely addressed components over a “shared bus system” using, for example, the “Inter-Integrated Circuit (I²C) protocol.” *Id.* at col. 1, ll. 37–45. The bus master communicates with a specific component by transmitting a command on the bus with the address of the desired component. *Id.* at col. 1, ll. 45–48. All of the components on the bus

receive the command, but only the component with a matching address acknowledges it and begins two-way communication with the bus master. *Id.* at col. 1, ll. 48–52. This technique was not secure, however, because an unauthorized component connected to the bus could communicate simply by obtaining and using an active address. *Id.* at col. 1, ll. 53–67.

The '079 patent describes known ways of enhancing security where “the bus master periodically requests an authorized component to change its address . . . without transmitting a new address [to the authorized component] and without the component transmitting its new address to the bus master.” *Id.* at col. 2, ll. 1–11. Rather, the bus master and component both run the same “address change algorithm” to determine a new address. *Id.* at col. 2, ll. 5–15. According to the '079 patent, this approach also had security problems because “authorized components may need to reset their respective addresses to a default address after installation or during power-up” and “[i]f authorized components utilize pseudorandom address generators, the generated pseudorandom sequences of addresses may be deterministic and reproducible such that the same series of addresses is generated after every instance of a reset or power-up.” *Id.* at col. 2, ll. 16–24. “As a result, when authorized components have an invariable starting address, i.e. the default address, an attacker device may easily learn the progression of addresses of the authorized component.” *Id.* at col. 2, ll. 24–27. The '079 patent seeks to further improve security by changing the address of an authorized component to a variable, rather than predetermined, address “on reset in order to prevent [a] recurring series of address changes after every reset and to keep an unauthorized component using a copied set of address changes from communicating with the bus master and acting as a clone of an authorized component.” *Id.* at col. 2, ll. 31–37.

Figure 2 of the '079 patent is reproduced below.

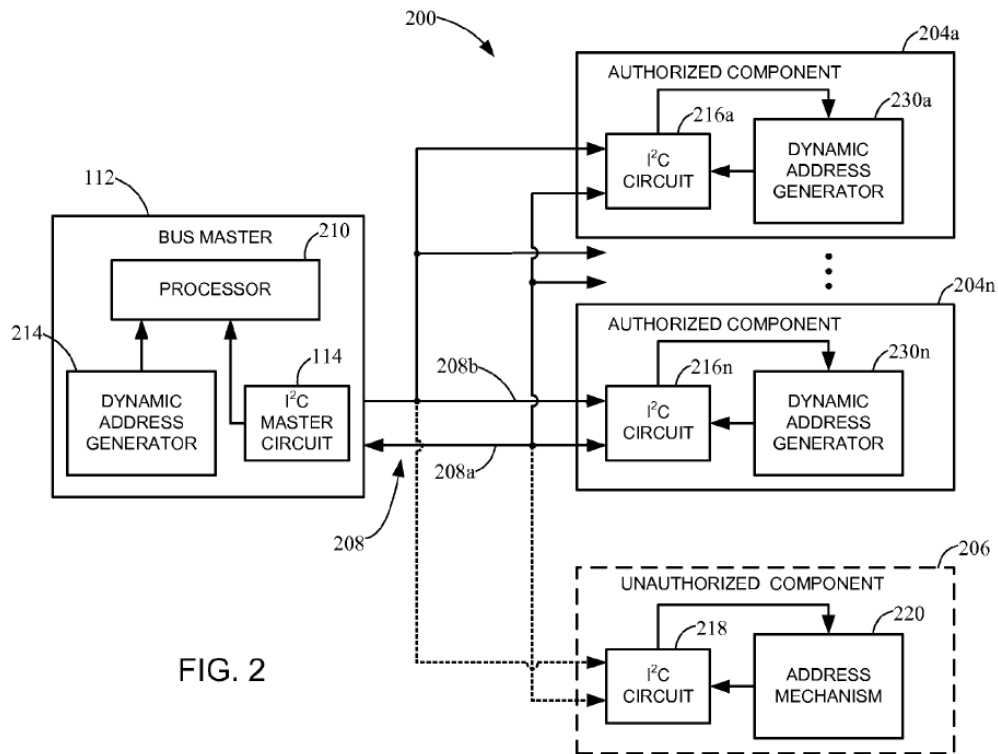


FIG. 2

Figure 2 depicts shared bus system 200 comprising bus master 112 connected via shared bus 208 to authorized components 204a–204n and unauthorized component 206. *Id.* at col. 5, ll. 13–45. Each component 204 includes dynamic address generator 230 for “dynamically changing its respective address upon request by bus master 112.” *Id.* at col. 5, ll. 46–50. Dynamic address generator 230 may be “a pseudorandom address generator that generates addresses according to a predefined algorithm” that is also known to bus master 112. *Id.* at col. 5, ll. 50–63.

Upon reset, controller 102 of imaging device 100 (shown in Figure 1) determines a “characterization value associated with a consumable,” such as a “parameter derived from sensor measurements” like “ink/toner level in . . . a tank.” *Id.* at col. 6, ll. 30–44, Fig. 4 (blocks 400 and 402). Controller 102 then calculates “a number of address changes . . . based upon the characterization value.” *Id.* at col. 6, ll. 45–46, Fig. 4 (block 404). Bus

master 112 requests authorized component 204 to change its address by transmitting a “change address command,” authorized component 204 “executes its address change algorithm in order to generate a new address,” authorized component 204 sends an acknowledgement to bus master 112, and bus master 112 executes the same algorithm to “predict the new address.” *Id.* at col. 7, l. 31–col. 8, l. 3, Fig. 4 (blocks 406–412). Controller 102 “determine[s] whether or not the number of address change operations performed is equal to the calculated number of address changes.” *Id.* at col. 8, ll. 4–6, Fig. 4 (block 414). If so, “the last address generated by the series of address change operations is set as the new address of authorized component 204.” *Id.* at col. 8, ll. 6–9, Fig. 4 (block 416). If not, the process is repeated until the calculated number of address changes is reached. *Id.* at col. 8, ll. 9–16, Fig. 4 (blocks 406–414). According to the ’079 patent,

[u]nauthorized component 206, which may have a fixed series of addresses copied from an authorized component, may not be able to change its address a number of times as requested by bus master 112. As a result, the series of addresses configured in address mechanism 220 of unauthorized component 206 may no longer correspond to the new set addresses required by bus master 112 in order for unauthorized component 206 to properly access shared bus 208 and communicate with bus master 112. Unauthorized component 206 may then be detected as a clone, counterfeit or otherwise unauthorized component, and appropriate actions may be taken.

Id. at col. 8, ll. 30–41.

D. Illustrative Claims

Claims 1 and 7 of the ’079 patent recite:

1. A method of setting an address of a component, comprising:

receiving, from a master by component circuitry associated with the component, a series of a plurality of address change requests;

in response to each address change request received, generating, by the component circuitry, a new component address, each new component address generated including a pseudorandom address value, and sending, by the component circuitry, an acknowledgement to the master, each acknowledgement being sent prior to a next address change request of the plurality of address change requests being received by the component circuitry; and

using, by the component circuitry, a last one of the new component addresses generated as the component address for at least one subsequent communication with the master.

7. Component circuitry, comprising:

an interface for coupling to a master over a shared bus; and

a dynamic address generator coupled to the interface for generating a component address, wherein substantially immediately following a predetermined event and in a continual series of a plurality of address change requests received by the interface and corresponding acknowledgements sent thereby in reply, for each address change request received the dynamic address generator generates a new component address, wherein the component circuitry uses a last one of the new component addresses generated as the component address for one or more subsequent communications with the master.

E. Evidence

Petitioner relies on the following prior art:

U.S. Patent No. 7,506,086 B2, issued Mar. 17, 2009 (Ex. 1007, “Mayer”);

U.S. Patent No. 5,995,774, issued Nov. 30, 1999 (Ex. 1005, “Applegate”);

U.S. Patent No. 5,708,831, issued Jan. 13, 1998 (Ex. 1004, “Schön”);

U.S. Patent Application Publication No. 2010/0306431 A1, published Dec. 2, 2010 (Ex. 1006, “Adkins”); and

The I²C-Bus Specification, version 2.1, Jan. 2000 (Ex. 1003, “I²C Spec”).

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–22 of the ’079 patent are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–5, 7, 8, 10–13, 15, 17, 18, 20–22	103(a) ¹	Mayer, I ² C Spec
6, 9, 14, 16, 19	103(a)	Mayer, I ² C Spec, Applegate
1–5, 7, 8, 10–13, 15, 17, 18, 20–22	103(a)	Schön, I ² C Spec
6, 9, 14, 16, 19	103(a)	Schön, I ² C Spec, Applegate
1–22	103(a)	Adkins

II. ANALYSIS

A. Legal Standards

A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). The

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. § 103. Because the challenged claims of the ’079 patent have an effective filing date before the effective date of the applicable AIA amendment, we refer to the pre-AIA version of 35 U.S.C. § 103. *See* Ex. 1001, codes (22), (63).

question of obviousness is resolved on the basis of underlying factual determinations, including “the scope and content of the prior art”; “differences between the prior art and the claims at issue”; and “the level of ordinary skill in the pertinent art.”² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. An obviousness determination requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418 (for an obviousness analysis, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does”). “Although the *KSR* test is flexible, the Board ‘must still be careful not to allow hindsight reconstruction of references . . . without any explanation as to *how* or *why* the references would be combined to produce the claimed invention.’” *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016) (citation omitted). Further, an assertion of obviousness “cannot be sustained by mere conclusory statements; instead, there must be some

² Additionally, secondary considerations, such as “commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy.” *Graham*, 383 U.S. at 17–18. Neither party, however, has presented any such evidence for us to consider.

articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); accord *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (stating that ““conclusory statements”” amount to an “insufficient articulation[] of motivation to combine”; “instead, the finding must be supported by a ‘reasoned explanation’” (citation omitted)); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”).

B. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art at the time of the ’079 patent would have had “a bachelor’s degree in electrical and/or computer engineering with training and one or more years of experience in embedded systems including both hardware and embedded software design,” as well as “a working understanding of communication on an electronics bus.” Pet. 13 (citing Ex. 1002 ¶¶ 26–29). Patent Owner argues that an ordinarily skilled artisan would have had “a bachelor’s degree in electrical and/or computer engineering with one or more years of work experience in printer design, including hardware and/or embedded software design for printer applications.” Prelim. Resp. 9 (citing Ex. 2001 ¶¶ 29–33). The parties’ proposed definitions differ in that Petitioner’s definition requires experience with “embedded systems” and “communication on an electronics bus,” whereas Patent Owner’s definition more specifically requires experience with “printer design.” The Specification of the ’079 patent states

that the disclosure relates generally to “addressing schemes” and describes “shared bus system[s]” as the related art. Ex. 1001, col. 1, l. 31–col. 2, l. 37. Independent claims 1, 7, 12, and 17 of the ’079 patent similarly each recite a “component” or “component circuitry” receiving plural “address change requests” and using a particular address for subsequent communication with a “master,” without limiting the “component” to a printer component. Based on the record presented, including our review of the ’079 patent and the types of problems and solutions described in the ’079 patent and cited prior art, we agree with and apply Petitioner’s proposed definition of the level of ordinary skill in the art for purposes of this Decision.

C. Claim Interpretation

We interpret the challenged claims

using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019). Neither party proposes any interpretations for the challenged claims. *See* Pet. 13; Prelim. Resp. 9. We have reviewed the parties’ papers and conclude that no term requires interpretation to determine whether to institute an *inter partes* review in this proceeding. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“Because we need only construe terms that are in controversy, and only to the extent necessary to resolve the controversy, we need not construe [a particular claim limitation] where the construction is

not material to the . . . dispute.” (internal quotation marks and citations omitted)).

D. Obviousness Ground Based on Adkins

Petitioner contends that claims 1–22 are unpatentable over Adkins under 35 U.S.C. § 103(a), citing the testimony of Harry Direen, Ph.D., P.E., as support. Pet. 42–60 (citing Ex. 1002). Patent Owner makes various arguments in response, citing the testimony of Jeffrey J. Folkins, Ph.D., as support. Prelim. Resp. 20–26, 59–66 (citing Ex. 2001).

1. Adkins

Adkins discloses a communication system having a master device in communication with uniquely addressed slave devices, such as, for example, a printer controller in communication with a replaceable printer cartridge over a shared bus. Ex. 1006, code (57), ¶¶ 44–46. Adkins seeks to improve security by “periodically chang[ing] the slave device addresses to increase the difficulty for an imposter to communicate with the master device” and “request[ing] that a slave device change its address, but prevent[ing] the slave device from communicat[ing] the new address to the master device, thereby reducing the chances of an imposter learning the new address.”

Id. ¶ 8.

Figure 1 of Adkins is reproduced below.

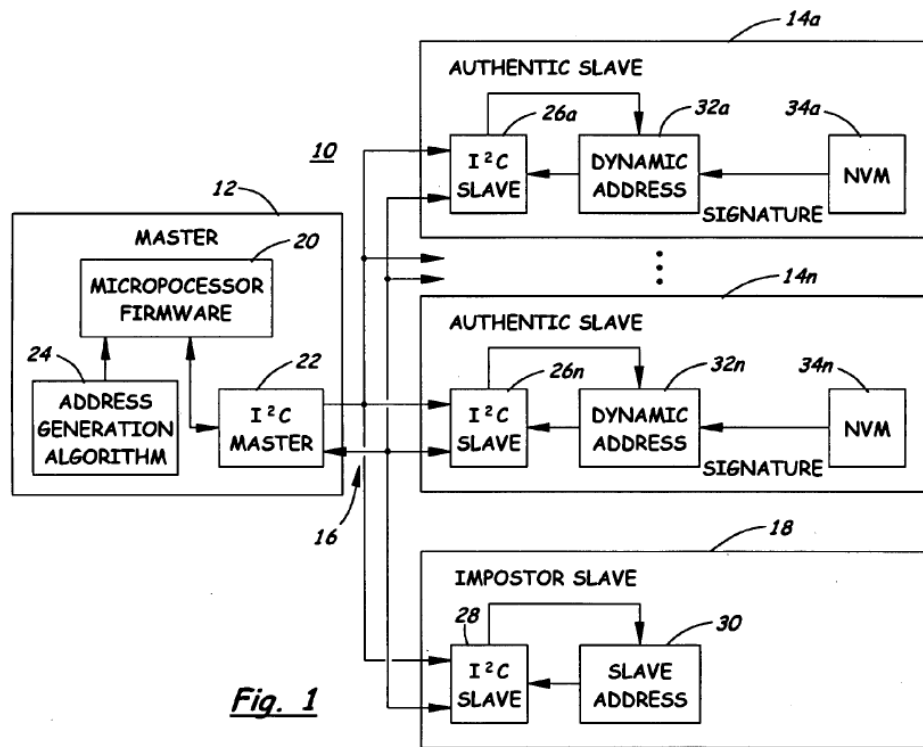


Figure 1 depicts shared bus system 10 comprising master device 12 connected via shared bus 16 to slave devices 14a–14n and imposter slave device 18. *Id.* ¶ 26. Each slave device 14 includes non-volatile memory 34 for storing a default slave address and signature code, and dynamic address generator 32 for changing its address upon request by master device 12. *Id.* ¶¶ 31–32. Dynamic address generator 32 may be “a pseudorandom address generator that generates addresses according to a predefined algorithm” that is also known to master device 12. *Id.* ¶ 31.

“[T]he slave addresses of the shared bus system 10 are periodically changed to thereby thwart attempts by imposters to gain access to the system.” *Id.* ¶ 29. “[M]aster device 12 does not dictate to the slave device 14 what new address should be used, only that the slave device 14 should assign to itself a new address.” *Id.* ¶ 31. Adkins discloses that master device 12 transmits

a “change address” command on the shared bus 16 in a conventional manner. When the slave device, for example slave device 14a, receives the command and the old slave address matches the address currently provided by the dynamic address generator 32a, then the command is processed by the I²C circuit 26a. When decoded, the address change command causes the dynamic address generator 32a to be incremented, whereupon a new random address is generated and self-assigned to the slave device 14a. The request is acknowledged by the slave device 14a to the master device 12, whereupon the master device 12 determines or predicts the newly assigned address by use of the algorithm stored in the memory 24. Thus, both the master device 12 and the slave device 14a are updated as to the new slave address without transmitting the same on the shared bus 16 to the master device 12. All subsequent transmissions by the master device 12 to the slave device 14a will be by way of the newly-assigned address.

Id. ¶ 32.

Adkins further discloses that “[i]n the event that the system 10 or a slave device 14 loses power, then the slave address can be reconstructed using the non-volatile memory 34.” *Id.* ¶¶ 33–34. Master device 12 issues a “soft reset” command to slave device 14, which reads non-volatile memory 34 and “retrieve[s] both a default address and a signature code to be loaded into the linear feedback shift register, or other apparatus functioning as the pseudorandom generator.” *Id.* ¶ 33, 41–42, Fig. 7 (block 88). “[S]lave device 14 will then operate thereafter with the default address until a change of address is requested and carried out.” *Id.* ¶¶ 33, 42 (“The master device 12 can communicate to the slave device 14 using the default address or general call address until an address change command is issued. At some time later, the master device 12 sends an address change command . . .”), Fig. 7 (blocks 90 and 92).

2. *Analysis*

Adkins is the patent application publication of U.S. Patent Application No. 12/474,052 (“the Adkins application”), which issued as U.S. Patent No. 8,225,021 B2 (“the ’021 patent”).³ Patent Owner argues that we should exercise our discretion to deny the Petition as to Adkins because the Adkins application and the ’021 patent that issued from it are listed on the face of the ’079 patent, cross-referenced in the ’079 patent, and discussed in the Background section of the ’079 patent. Prelim. Resp. 16, 59–60 (citing Ex. 1001, code (56)); *see* Ex. 1001, col. 1, ll. 15–18 (“This application is related to U.S. patent application Ser. No. 12/474,052, filed on May 28, 2009, entitled, ‘Dynamic Address Change for Slave Devices on a Shared Bus,’ and assigned to the assignee of the present application.”), col. 2, ll. 1–30. Patent Owner also points out that Adkins and the ’079 patent were examined by the same Examiner. Prelim. Resp. 60. Petitioner argues that “Adkins was not cited during prosecution of the ’079 Patent.” Pet. 15.

Institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech, Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he [Office] is permitted, but never compelled, to institute an [*inter partes* review] proceeding.”); 35 U.S.C. § 314(a) (“The Director *may not* authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” (emphasis added)). Pursuant to 35 U.S.C.

³ The ’021 patent was challenged by Petitioner in Case IPR2019-01389, in which institution was denied.

§ 325(d), in determining whether to institute an *inter partes* review, “the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”

In evaluating whether to exercise our discretion when the same or substantially the same prior art or arguments previously were presented to the Office under section 325(d), we have weighed some common *non-exclusive* factors, such as: (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph) (“*Becton, Dickinson*”).

As to *Becton, Dickinson* factor (a), Petitioner argues that “Adkins is not identified on the face of the ‘079 Patent as having been considered by the Examiner, nor is there an Information Disclosure Statement identifying Adkins for the Examiner’s consideration.” Pet. 42. Adkins, however, is the patent application publication of the Adkins application, which is specifically referenced as “related” in the ‘079 patent. *See* Ex. 1001, col. 1, ll. 15–18; Pet. 1 (“The ‘079 Patent identifies itself as being related to the ‘021 Patent.”). Further, the ‘021 patent, which issued from the Adkins application and has the same written description as Adkins, was cited in an

Information Disclosure Statement (IDS) during prosecution and appears on the face of the '079 patent. *See* Ex. 1001, code (56); Ex. 1011 (IDS dated November 4, 2013, and Examiner signature indicating that “all references [were] considered” dated January 10, 2014).⁴ Thus, the Adkins application was referenced in the '079 patent and the '021 patent was cited during prosecution, so there is no material difference between Adkins and the prior art involved during examination. Given these facts, we need not further evaluate factor (b), whether Adkins is cumulative. Factors (a) and (b) weigh in favor of exercising our discretion.

As to factor (c), the extent to which Adkins was evaluated during prosecution of the '079 patent, Patent Owner states that the '021 patent “is listed on the face of the '079 Patent, was submitted in an information disclosure statement during the prosecution of the '079 Patent, and was considered by the same examiner that examined and allowed both the '021 and the '079 Patents.” Prelim. Resp. 59–60. Patent Owner acknowledges that the only substantive rejection during prosecution of the '079 patent was a rejection under 35 U.S.C. § 112, which the applicants overcame. *Id.* at 8–9 (citing Ex. 1011). Patent Owner, however, argues that the '079 patent references the Adkins application as a related application and discusses Adkins in its Background section. *Id.* at 60–61 (citing Ex. 1001, col. 2, ll. 16–30). Petitioner’s only argument pertinent to our analysis is that “Adkins was not cited during prosecution of the '079 Patent.” Pet. 15.

⁴ Petitioner filed a copy of the prosecution history of the '079 patent as Exhibit 1011, but did not include page numbers as required by 37 C.F.R. § 42.63(d)(2)(i). Accordingly, where necessary, we refer to material in the prosecution history by date.

As explained above, although Adkins (a patent application publication) was not cited, the corresponding Adkins application and issued '021 patent clearly were identified to the Examiner during prosecution. Further, although the Examiner did not reject any claims of the '079 patent based on Adkins, that is not the end of our analysis. As Patent Owner argues, the Examiner was familiar with the substance of Adkins because the same Examiner examined both the '021 patent and the '079 patent.⁵ Prelim. Resp. 16, 59–60. Patent Owner also notes that the '079 patent expressly identifies the Adkins application, which published as Adkins, as related to the '079 patent. *Id.* at 60; Ex. 1001, col. 1, ll. 15–18. Because the Examiner was already familiar with the substance of Adkins, and Patent Owner expressly called the Adkins application to the attention of the Examiner in the Specification, stating that it is “related” to the application being prosecuted, it is reasonable to assume that the Examiner considered the substance of Adkins when examining the '079 patent, despite the lack of an express claim rejection over Adkins. Factor (c), thus, favors exercise of our discretion.

Factor (d), the extent to which the arguments in this proceeding overlap those made during prosecution, also weighs in favor of exercising our discretion. To be sure, because the Examiner did not reject the claims of the '079 patent over Adkins, Patent Owner did not present arguments related to Adkins in an office action response. *See* Ex. 1011 (Office Action dated January 15, 2014). As Patent Owner notes, however, the Background

⁵ The Adkins application was prosecuted from May 28, 2009, to July 17, 2012. The parent application of the '079 patent, U.S. Patent Application No. 13/218,658, was prosecuted before the same Examiner from August 26, 2011, to December 31, 2013. *See* Ex. 1001, code (63).

section of the '079 patent discusses differences between Adkins and the invention of the '079 patent. Prelim. Resp. 60–61 (citing Ex. 1001, col. 2, ll. 16–30). Although this passage from the Specification does not expressly cite Adkins, the subject matter described in the '079 patent's Background appears to correspond to that described in Adkins. *Compare* Ex. 1001, col. 2, ll. 1–30 (describing a prior art system in which a bus master transmits an address change command to a component without transmitting the new address; the component runs a pseudorandom address generator algorithm to change its address without transmitting the new address to the bus master; and the bus master runs the same address change algorithm to predict the new address), *with* Ex. 1006 ¶¶ 27–32 (same). The '079 patent identifies alleged shortcomings of Adkins's technique (“[W]hen authorized components have an invariable starting address, i.e. the default address, an attacker device may easily learn the progression of addresses of the authorized component. An unauthorized component may then be installed to replace the authorized component and act as a clone which can correctly respond with the same series of addresses as the authorized component.”) and introduces its invention as a solution to address these shortcomings (“[T]here is a need to further enhance security by setting the address of an authorized component to a variable address on reset in order to prevent [a] recurring series of address changes after every reset and to keep an unauthorized component using a copied set of address changes from communicating with the bus master and acting as a clone of an authorized component.”). Ex. 1001, col. 2, ll. 16–37. Patent Owner reiterates these alleged distinctions in its Preliminary Response, at pages 60–62.

Although not in response to an office action, this discussion in the '079 patent's Background is a set of arguments in favor of patentability that

attempt to distinguish the '079 patent's invention from the same prior art asserted in this proceeding. It is reasonable to assume that the Examiner read the Specification and understood these statements as part of examining the '079 patent. *See, e.g.*, MPEP §§ 608.01(c) (9th ed., Mar. 2014) (“The Background of the Invention may include the following parts: . . . Description of the related art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A paragraph(s) describing to the extent practical the state of the prior art or other information disclosed known to the applicant, including references to specific prior art or other information where appropriate. Where applicable, the problems involved in the prior art or other information disclosed which are solved by the applicant's invention should be indicated.”), 2129 (guidance for an examiner's consideration of admissions of prior art in the specification). Accordingly, factor (d) favors exercise of our discretion under § 325(d).

Factor (e) asks whether Petitioner points to error in the Examiner's evaluation of Adkins. Much of Petitioner's analysis consists of conclusory statements followed by citations to Adkins that do not appear to support those statements. For example, in alleging the obviousness of claim 7 over Adkins, Petitioner argues that “Adkins discloses substantially immediately following a predetermined event and in a continual series of a plurality of address change requests received, generating a new address using the dynamic address generator,” and quotes, without further explanation, from paragraph 32 of Adkins. Pet. 47–48. Here, Adkins describes a master device that “periodically request[s] that a slave device 14 change its address.” Ex. 1006 ¶ 32. However, Petitioner does not identify a “predetermined event” in the discussion in paragraph 32 of Adkins or explain how a continual series of a plurality of address change requests

occurs “substantially immediately following” such an event. Pet. 47–48. From Petitioner’s presentation, we cannot say that the Examiner clearly erred in allowing the claims of the ’079 patent. At this stage of the proceeding, factor (e) weighs in favor of denial or is, at most, neutral.

Relevant to factor (f), Petitioner offers the testimony of Dr. Direen, which was not available to the Examiner. However, Dr. Direen’s testimony is entitled to little weight because it consists primarily of quotations from Adkins, many of which are not cited in the Petition, and an unsupported inherency theory that is not argued in the Petition. *See, e.g.*, Ex. 1002, App. 1002-C, 11–16 (testimony for claim 7). *See* 37 C.F.R. §§ 42.6(a)(3) (“Arguments must not be incorporated by reference from one document into another document.”), 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). Thus, Dr. Direen’s testimony does not provide persuasive evidentiary support for Petitioner’s arguments regarding Adkins. This factor is, at most, neutral.

Weighing each of the factors, we conclude that the circumstances of this case, on the record presented, warrant exercise of our discretion to deny institution based on § 325(d). Patent Owner identified the Adkins application as “related” to the ’079 patent, made statements in the Specification attempting to distinguish the ’079 patent’s invention from Adkins, and cited the ’021 patent in an IDS. Further, the Examiner already was familiar with Adkins given that the same Examiner examined both the ’021 patent and the ’079 patent. We infer from these circumstances that the Examiner considered the substance of Adkins and Patent Owner’s statements regarding the disclosure of Adkins and problems with its approach, despite the lack of an express rejection over Adkins. Petitioner

has not presented a convincing case that the Examiner erred in allowing the claims of the '079 patent and Dr. Direen's testimony does not provide persuasive support for Petitioner's arguments.

As we explain in detail below, Petitioner has not demonstrated a reasonable likelihood of prevailing on its other asserted grounds of unpatentability. Because each of Petitioner's grounds should be denied, either for an inadequate showing on the merits or pursuant to our discretion under § 325(d), we exercise our discretion to deny the Petition under §§ 314(a) and 325(d).

E. Obviousness Ground Based on Mayer and I²C Spec

Petitioner contends that claims 1–5, 7, 8, 10–13, 15, 17, 18, and 20–22 are unpatentable over Mayer and I²C Spec under 35 U.S.C. § 103(a), and Patent Owner makes various arguments in response. *See* Pet. 18–29; Prelim. Resp. 20–34, 37–40, 42–57.

1. Mayer

Mayer discloses a method for automatic identification code generation in a data processing system having a bus, plurality of network devices, and bus master “used to control the flow [of] information between network devices connected to the bus.” Ex. 1007, col. 1, ll. 58–62, col. 2, ll. 45–51. Each network device includes a number generator for generating its own unique identification code, and “must register with the bus master in order to communicate over the bus.” *Id.* at col. 2, ll. 51–56. The bus master begins the identification code generation procedure by switching all network devices into “active mode” and sending a request for an identification code to each network device. *Id.* at col. 2, l. 57–col. 3, l. 1. In response to the bus

master's request, each network device sends its identification code to the bus master. *Id.* at col. 3, ll. 5–10. The bus master saves the received identification codes in an identification code table. *Id.* at col. 2, ll. 52–54. After the process completes, “the bus master compares the number of received identification codes with the number of devices connected to the bus.” *Id.* at col. 3, ll. 29–31. “If each network device has a unique identification code, then the number of transmitted identification codes corresponds to the number of devices connected to the bus” and the process is complete. *Id.* at col. 3, ll. 31–34. If the number of received identification codes is smaller than the number of devices connected to the bus, however, there are at least two devices with the same identification code. *Id.* at col. 3, ll. 35–41. In that case, “the bus master requests all of the network devices to generate new identification codes and replace the existing identification codes with the new ones.” *Id.* at col. 3, ll. 44–54.

2. I²C Spec

I²C Spec specifies a standard for “a simple bi-directional 2-wire bus for efficient inter-IC control,” which the reference calls “the Inter IC or I²C-bus.” Ex. 1003, 4. I²C Spec describes communication over an I²C bus between a master (“[t]he device which initiates a transfer, generates clock signals and terminates a transfer”) and a slave (“[t]he device addressed by a master”). *Id.* at 7. I²C Spec describes addressing procedures for the master to communicate with slave devices. *Id.* at 15. One addressing procedure uses the first seven bits of the first byte of a message for the slave address. *Id.* at 13, 15. In this procedure, the “slave address can be made-up of a fixed and a programmable part.” *Id.* at 15. “The number of programmable address bits of a device depends on the number of pins available. For

example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.” *Id.* “The exception is the ‘general call’ address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

However, devices can be made to ignore this address.” *Id.* at 15. “The second byte of the general call address then defines the action to be taken.”

Id. I²C Spec describes the following as the second byte:

00000110 (H‘06’). Reset and write programmable part of slave address by hardware. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. . . .

00000100 (H‘04’). Write programmable part of slave address by hardware. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The device will not reset.

Id. at 16.

3. Analysis

a) “Substantially Immediately Following a Predetermined Event”: *Independent Claims 7, 12, and 17*

Petitioner argues independent claims 1, 7, 12, and 17 together in its Petition. Pet. 18–25. With respect to claim 7, Petitioner argues that Mayer teaches “component circuitry” associated with a component, Mayer and I²C Spec both teach receiving from a master a “series of a plurality of address change requests,” and Mayer teaches using a “last one of . . . new component addresses generated as the component address for one or more subsequent communications with the master.” *Id.* at 20–21, 24–25. Claim 7 also recites a “dynamic address generator” wherein “substantially

immediately following a predetermined event and in a continual series of a plurality of address change requests received by the interface and corresponding acknowledgements sent thereby in reply, for each address change request received the dynamic address generator generates a new component address.” Petitioner includes allegations directed to a portion of the claim language, namely “in a continual series of a plurality of address change requests received by the interface and corresponding acknowledgements sent thereby in reply, for each address change request received the dynamic address generator generates a new component address,” arguing that Mayer teaches the limitations and I²C Spec also teaches receiving a “series of a plurality of address change requests” and “sending an acknowledgement.” *Id.* at 20–24.

Patent Owner responds that Petitioner fails to account for the claim limitation that the plurality of address change requests occurs “substantially immediately following a predetermined event.”⁶ Prelim. Resp. 42. We agree. In its analysis of claim 7, Petitioner does not identify any “event” at all or explain how such an event would be “predetermined” or why the alleged address change requests in Mayer or I²C Spec would occur “substantially immediately following” such an event. *See* Pet. 21–24. Indeed, the “substantially immediately following a predetermined event” claim language does not even appear in Petitioner’s arguments. *See id.*

⁶ Patent Owner makes a number of other arguments regarding the asserted combinations with I²C Spec in its Preliminary Response, including that Petitioner has not shown sufficiently that I²C Spec is a prior art printed publication under 35 U.S.C. § 102(b). *See* Prelim. Resp. 26–30, 36–37, 43–48. We need not reach these issues, however, because Petitioner has not shown a reasonable likelihood of prevailing on the asserted grounds for the reasons explained herein.

Although Petitioner does not identify a “predetermined event” in its Petition, Dr. Direen appears to opine that a “power-on reset process” would trigger the plurality of address change requests. Ex. 1002, App. 1002-A, 14. Dr. Direen states that “[i]t is well understood in the electronic industry and by [persons of ordinary skill in the art] that complex devices such as a microprocessor or I2C slave device will go through a power-on reset process to ensure internal states are at known states. This is inherent device operation.” *Id.* Dr. Direen, however, cites no support for this opinion and does not explain in any detail what a power-on reset process would entail or why a plurality of address change requests in either Mayer or I²C Spec would occur “substantially immediately following” a power-on reset process. *See id.* Moreover, to the extent Dr. Direen bases his opinion on inherency, Petitioner does not assert that theory in its Petition.⁷ *See* Pet. 21–24. Petitioner has not shown sufficiently that Mayer and I²C Spec teach a “dynamic address generator” wherein “substantially immediately following a predetermined event and in a continual series of a plurality of address change requests received by the interface and corresponding acknowledgements sent thereby in reply, for each address change request received the dynamic address generator generates a new component address,” as recited in claim 7.

Independent claims 12 and 17 recite limitations similar to those of claim 7. Claim 12 recites a “dynamic address generator” wherein “substantially immediately following a predetermined event, the interface

⁷ As Patent Owner correctly points out, Dr. Direen’s opinions on how the challenged claims allegedly are unpatentable differ from the grounds asserted in the Petition. *See* Prelim. Resp. 21–22; *compare* Pet. 3 with Ex. 1002 ¶ 69.

circuit receives a plurality of address change requests in succession from the master and, in response to each address change request received, the dynamic address generator generates a new component address and the interface circuit sends to the master an acknowledgement.” Claim 17 recites a “dynamic address generator” wherein “substantially immediately following a predetermined event, the component circuitry performs in succession a plurality of sets of operations, each set of operations comprising receiving by the interface an address change request from the master and generating a new component address by the dynamic address generator in response.” Petitioner argues the independent claims together and, as explained above, fails to identify any “predetermined event” or explain how the alleged plurality of address change requests or operations would occur “substantially immediately following” such an event. *See id.* Dr. Direen’s testimony is identical to his testimony regarding claim 7. *See* Ex. 1002, App. 1002-A, 14, 23, 33. Petitioner, therefore, has not made a sufficient showing as to claims 12 and 17 either.

Because Petitioner has not shown sufficiently that the references teach the “predetermined event” limitations of independent claims 7, 12, and 17,⁸ Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 7, 12, and 17, or claims 8, 10, 11, 13, 15, 18, and 20–22 depending therefrom, are unpatentable over Mayer and I²C Spec.

⁸ Claim 1 recites receiving from a master “a series of a plurality of address change requests,” but unlike independent claims 7, 12, and 17, does not recite that the requests are received “substantially immediately following a predetermined event.”

b) Reason to Combine: Independent Claims 1, 7, 12, and 17

As explained above, Petitioner argues independent claims 1, 7, 12, and 17 together in its Petition. Pet. 18–25. With respect to claim 1, Petitioner argues that Mayer teaches “component circuitry” associated with a component and using a “last one of . . . new component addresses generated as the component address for at least one subsequent communication with the master.” *Id.* at 19, 24–25. Claim 1 further recites component circuitry receiving “a series of a plurality of address change requests.” Petitioner argues that Mayer teaches the limitation, citing Mayer’s disclosure that “if a first pass of generating a set of network device addresses does not produce a unique set of addresses across all the network (slave) devices, then the master will request the network devices to generate new identification codes.” *Id.* at 20–21 (citing Ex. 1007, col. 3, ll. 42–44). Petitioner further states that “I²C Spec additionally discloses receiving, from a master by component circuitry associated with the component, a series of a plurality of address change requests.” *Id.* at 21. As support, Petitioner cites page 16 of I²C Spec, which describes two different options as the second byte of the general call address (H‘06’ and H‘04’), as well as Dr. Direen’s testimony, where he states:

The I2C Standard discloses two different commands (00000110 (H‘06’) and 00000100 (H‘04’), . . . pg. 16) for causing slave devices to set the programmable portion of their address. . . .

All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence.

The two-byte sequence is the general call address (0000 000) combined with the command: 00000110 (H‘06’) or 00000100 (H‘04’).

See Ex. 1002, App. 1002-A, 3 (emphasis omitted); Ex. 1003, 16. Finally, claim 1 recites:

in response to each address change request received, generating, by the component circuitry, a new component address, each new component address generated including a pseudorandom address value, and sending, by the component circuitry, an acknowledgement to the master, each acknowledgement being sent prior to a next address change request of the plurality of address change requests being received by the component circuitry.

Petitioner argues that Mayer teaches the limitation and “I²C Spec further discloses sending an acknowledgement,” citing I²C Spec’s disclosure that “[d]ata transfer with acknowledge is obligatory.” Pet. 21–24 (quoting Ex. 1003, 10).

As to the combination of Mayer and I²C Spec, Petitioner argues that Mayer is “directed to assigning addresses to devices on a shared bus” and I²C Spec is “the ‘de facto world standard’ for shared bus addressing and communication.” *Id.* at 18 (citing Ex. 1003, 3; Ex. 1007, code (57)).

According to Petitioner, “[g]iven that the references are in the same field of endeavor and teach the addressing of slave devices, a [person of ordinary skill in the art] would have found it obvious to combine their teachings.” *Id.* Petitioner also asserts, without citation, that “I²C Spec defines the specification on which Mayer is built.” *Id.* at 19. Petitioner argues that a person of ordinary skill in the art “would have been motivated to combine Mayer and [I²C Spec]” because I²C Spec teaches “address formats” and Mayer “provides additional disclosure on device addressing techniques.” *Id.* (citing Ex. 1002, App. 1002-A).

As an initial matter, it is unclear what combination of the two references Petitioner is asserting. Petitioner does not clearly identify a

modification that a person of ordinary skill in the art would have made to Mayer's process based on the teachings of I²C Spec. Petitioner appears to be arguing that a person of ordinary skill in the art would have implemented I²C Spec's two different variations of the general call address (H'06' and H'04'), which both instruct the slave devices to change the "programmable" parts of their addresses (i.e., in the format of I²C Spec, with a "fixed" and "programmable" part), in Mayer's process as "a series of a plurality of address change requests."⁹ *See id.* at 19–21; Prelim. Resp. 51–52; Ex. 1002, App. 1002-A, 3; Ex. 1003, 15–16.

We agree with Patent Owner that Petitioner's reasoning with respect to the combination of Mayer and I²C Spec is insufficient. *See* Prelim. Resp. 24–26, 48–52. First, the fact that the references are in the "same field of endeavor" and have similar disclosures (e.g., communication with addressed devices over a shared bus) does not explain why a person of ordinary skill in the art would have had reason to incorporate any particular aspect of I²C Spec into the process of Mayer. *See* Pet. 18–19. At most, it is merely a starting point to the obviousness analysis and helps show that the references are sufficiently similar that a person of ordinary skill in the art could have combined their teachings, not that such an individual would have done so to achieve the method having the steps set forth in the claim. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have*

⁹ Unlike the asserted ground based on Schön and I²C Spec, discussed below, Petitioner does not appear to be arguing that a person of ordinary skill in the art would have added to Mayer's process an acknowledgement for each address change request, as Petitioner's position is that Mayer already teaches such an acknowledgement. *See* Pet. 21–24; *infra* Section II.F.2.b.

been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9 at 10–11 (PTAB Oct. 16, 2018) (informative) (“Mere compatibility of the references is . . . not sufficient.”); *see also Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (unpublished) (holding that “a broad characterization of [two references] as both falling within the same alleged field,” without more, was not “a sufficient rationale to support an obviousness conclusion,” as “[s]uch short-cut logic would lead to the conclusion that any and all combinations of elements known in th[e] broad field would automatically be obvious, without the need for any further analysis”); *Microsoft Corp. v. Enfish, LLC*, 662 F. App’x 981, 990 (Fed. Cir. 2016) (unpublished) (holding that the fact that two references “were directed to the same art or same techniques” was “inadequate to show persuasively that a relevant skilled artisan would have been motivated to combine the references”).

Second, Petitioner’s asserted reason to combine is premised on Mayer’s teaching of a network device generating an identification code for itself and I²C Spec’s teaching of one “format[]” for a slave device address. *See* Pet. 18–19. Petitioner, however, does not explain how I²C Spec’s formatting relates to the combination being proposed, namely using the two general call address variations in Mayer’s process. Petitioner does not explain in any detail why a person of ordinary skill in the art would have been motivated to modify Mayer’s process to have the bus master send either of the two general call address variations from I²C Spec (rather than the request to generate new identification codes when the number of received identification codes is smaller than the number of devices connected to the bus, as described in Mayer) as an address change request.

Petitioner, for example, does not explain why doing so, based on the teachings of I²C Spec, would have been considered an improvement or advancement to the functionality of Mayer. Nor does Petitioner explain how I²C Spec's general call address variations would have been combined with the teachings of Mayer. Petitioner's conclusory assertions in the Petition are insufficient to show a reason to combine Mayer and I²C Spec.

Third, we agree with Patent Owner that Dr. Direen's testimony also is conclusory and does not provide sufficient explanation as to why or how a person of ordinary skill in the art would have combined the references' teachings. *See* Prelim. Resp. 24–26, 48–49; Ex. 1002 ¶ 63, App. 1002-A, 2–6. Dr. Direen opines, without further explanation, that “[i]n that Mayer discloses a master slave data communications system, a [person of ordinary skill in the art] would be motivated to combine [the] teaching of the I²C bus with Mayer's teachings.” Ex. 1002, App. 1002-A, 2. Dr. Direen further states that because Mayer's system uses a “clocked bus with a wired OR data line,” which is “similar to the very common I²C bus,” “a [person of ordinary skill in the art] would be motivated to combine the teaching of Mayer with the I²C Standard as they both deal with similar master/slave bus systems and both systems require the slave devices to have unique addresses.” *Id.* at 2–3. Again, the fact that the references have some common teachings is not sufficient to establish a reason to combine their teachings to achieve the method set forth in the claim. Dr. Direen also identifies I²C Spec's two different variations of the general call address (H'06' and H'04'). *Id.* at 3. The mere existence of that teaching, however, does not support a conclusion that a person of ordinary skill in the art would have had reason to modify Mayer's process to use the general call address

variations as “a series of a plurality of address change requests” in the manner recited in the claim.

Petitioner has not set forth a sufficient rationale for combining the teachings of Mayer and I²C Spec in reaching a conclusion of obviousness as to claim 1. Independent claims 7, 12, and 17 recite limitations similar to those of claim 1, including a plurality of “address change request[s]” as either a “continual series” or “in succession.” Petitioner asserts the same alleged reasons to combine for all of the challenged claims. *See* Pet. 18–19. Accordingly, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that independent claims 1, 7, 12, and 17, or claims 2–5, 8, 10, 11, 13, 15, 18, and 20–22 depending therefrom, are unpatentable over Mayer and I²C Spec.

F. Obviousness Ground Based on Schön and I²C Spec

Petitioner contends that claims 1–5, 7, 8, 10–13, 15, 17, 18, and 20–22 are unpatentable over Schön and I²C Spec under 35 U.S.C. § 103(a), and Patent Owner makes various arguments in response. *See* Pet. 30–40; Prelim. Resp. 20–32, 34–38, 40–49, 57–58.

1. Schön

Schön discloses “a method for assigning bus addresses for a data processing system having a plurality of stations and a control unit (master).” Ex. 1004, col. 1, ll. 4–6. The master “first transmits to the stations a command for address generation, whereupon each station generates for itself a random address from a preset value range.” *Id.* at col. 1, ll. 40–43, col. 2, ll. 57–65. The master then tests each address within the preset range to see if a station assigned itself that address. *Id.* at col. 1, ll. 44–47, col. 2,

l. 65–col. 3, l. 1. If the master receives a reply from a station with a valid address, the master informs the station that the address has been accepted and the station sets an “address flag” in response. *Id.* at col. 1, ll. 47–51, 53–56, col. 3, ll. 1–6. If the reply has a transmission error, however, “this indicates to the master station that at least two stations have the same random address” and no acknowledgement is provided. *Id.* at col. 1, ll. 51–53, col. 3, ll. 7–10. “If at the end of an inquiry cycle only valid replies have been supplied by the stations, each station can be assigned a clear address.” *Id.* at col. 3, ll. 11–13. Otherwise, “the method is repeated, but with the command for address generation only being reacted to by those stations that have not set the address flag for successful address assignment.” *Id.* at col. 3, ll. 13–16.

2. Analysis

a) “*Substantially Immediately Following a Predetermined Event*”: *Independent Claims 7, 12, and 17*

Petitioner argues independent claims 1, 7, 12, and 17 together in its Petition. Pet. 30–36. With respect to claim 7, Petitioner argues that Schön and I²C Spec both teach certain limitations, such as “component circuitry” associated with a component and using a “last one of . . . new component addresses generated as the component address for one or more subsequent communications with the master.” *Id.* at 31, 35–36. Claim 7 also recites a “dynamic address generator” wherein “substantially immediately following a predetermined event and in a continual series of a plurality of address change requests received by the interface and corresponding acknowledgements sent thereby in reply, for each address change request received the dynamic address generator generates a new component

address.” Petitioner argues that Schön teaches a “plurality of address change commands,” citing Schön’s description of its method being “repeated” if at least two stations generated the same address, and I²C Spec also teaches a “plurality of address change requests.” *Id.* at 32–33 (citing Ex. 1004, col. 3, ll. 14–16; Ex. 1003, 16). Petitioner further contends that Schön teaches component circuitry generating a new component address using a pseudorandom number generator. *Id.* at 34–35 (citing Ex. 1004, col. 1, ll. 39–43). Petitioner relies on I²C Spec as allegedly teaching sending “acknowledgement[s].” *Id.* at 35 (citing Ex. 1003, 10–11).

Patent Owner responds that Petitioner fails to account for the claim limitation that the plurality of address change requests occurs “substantially immediately following a predetermined event.” Prelim. Resp. 42. We agree. In its analysis of claim 7, Petitioner does not identify any “event” at all or explain how such an event would be “predetermined” or why the alleged address change requests in Schön or I²C Spec would occur “substantially immediately following” such an event. *See* Pet. 31–36. Indeed, the “substantially immediately following a predetermined event” claim language does not even appear in Petitioner’s arguments. *See id.*

Nor does Dr. Direen’s testimony support the Petition. Dr. Direen states that “[i]t is well understood in the electronic industry and by [persons of ordinary skill in the art] that complex devices such as a microprocessor or I2C slave device will go through a power-on reset process to ensure internal states are at known states. This is inherent device operation.” Ex. 1002, App. 1002-B, 15. Dr. Direen, however, cites no support for this opinion and does not explain in any detail what a power-on reset process would entail or why a plurality of address change requests in either Schön or I²C Spec would occur “substantially immediately following” a power-on reset

process. *See id.* Moreover, to the extent Dr. Direen bases his opinion on inherency, Petitioner does not assert that theory in its Petition. *See* Pet. 31–36. Petitioner has not shown sufficiently that Schön and I²C Spec teach a “dynamic address generator” wherein “substantially immediately following a predetermined event and in a continual series of a plurality of address change requests received by the interface and corresponding acknowledgements sent thereby in reply, for each address change request received the dynamic address generator generates a new component address,” as recited in claim 7.

Independent claims 12 and 17 recite limitations similar to those of claim 7. Petitioner argues the independent claims together and, as explained above, fails to identify any “predetermined event” or explain how the alleged plurality of address change requests or operations would occur “substantially immediately following” such an event. *See id.* at 31–36. Dr. Direen’s testimony is identical to his testimony regarding claim 7. *See* Ex. 1002, App. 1002-B, 15, 26, 36. Petitioner, therefore, has not made a sufficient showing as to claims 12 and 17 either.

Because Petitioner has not shown sufficiently that the references teach the “predetermined event” limitations of independent claims 7, 12, and 17, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 7, 12, and 17, or claims 8, 10, 11, 13, 15, 18, and 20–22 depending therefrom, are unpatentable over Schön and I²C Spec.

b) Reason to Combine: Independent Claims 1, 7, 12, and 17

As explained above, Petitioner argues independent claims 1, 7, 12, and 17 together in its Petition. Pet. 30–36. With respect to claim 1, Petitioner argues that Schön and I²C Spec both teach, for example,

“component circuitry” associated with a component and using a “last one of . . . new component addresses generated as the component address for at least one subsequent communication with the master.” *Id.* at 31, 35–36.

Claim 1 further recites component circuitry receiving “a series of a plurality of address change requests.” Petitioner argues that Schön teaches a “plurality of address change commands” and “I²C Spec additionally discloses receiving, from a master by component circuitry associated with the component, a series of a plurality of address change requests,” specifically “two different commands for the master to cause slave devices to set their addresses,” again relying on page 16 of I²C Spec and Dr. Direen’s testimony. *Id.* at 32–33 (citing Ex. 1003, 16; Ex. 1002, App. 1002-A, 2–6). Claim 1 also recites (with numeric labels added):

in response to each address change request received, [1] generating, by the component circuitry, a new component address, each new component address generated including a pseudorandom address value, and [2] sending, by the component circuitry, an acknowledgement to the master, each acknowledgement being sent prior to a next address change request of the plurality of address change requests being received by the component circuitry.

Although not entirely clear from the Petition, Petitioner appears to rely on a combination of both references for this limitation. *See id.* at 33–35.

Petitioner contends that (1) Schön teaches a station receiving “address change request[s]” and in response to each request generating a new random address, and (2) I²C Spec teaches sending an “acknowledgement” to the master. *Id.* (citing Ex. 1004, col. 1, ll. 39–43, col. 2, ll. 7–9, col. 3, ll. 11–16; Ex. 1003, 10–11).

As to the combination of Schön and I²C Spec, Petitioner argues that Schön teaches a “method of assigning addresses on a shared bus” and

I²C Spec is “the ‘de facto world standard’ for shared bus addressing and communication.” *Id.* at 30–31 (citing Ex. 1003, 3). According to Petitioner, “[g]iven that the references are in the same field of endeavor and both teach the addressing of slave devices, a [person of ordinary skill in the art] would have found it obvious to combine their teachings.” *Id.* Petitioner further states that a person of ordinary skill in the art “would have been motivated to combine Schön and the I²C Spec as Schön teaches methods for generating slave addresses, and the I²C Spec teaches various addressing formats for slave devices.” *Id.* at 31 (citing Ex. 1004, col. 1, ll. 39–43; Ex. 1003, 15); *see* Ex. 1002 ¶ 66.

We agree with Patent Owner that Petitioner’s reasoning with respect to the combination of Schön and I²C Spec is insufficient. *See* Prelim. Resp. 24–26, 40–41, 48–51, 57–58. First, the fact that the references are in the “same field of endeavor” and have similar disclosures (e.g., communication with addressed devices over a shared bus) does not explain why a person of ordinary skill in the art would have had reason to incorporate any particular aspect of I²C Spec into the process of Schön. *See* Pet. 30–31.

Second, Petitioner’s asserted reason to combine is premised on Schön’s teaching of a station generating a random address for itself and I²C Spec’s teaching of one “format[]” for such an address. *See id.* To the extent Petitioner’s proposed combination involves using the general call address variations of I²C Spec in Schön’s process, we are not persuaded for the reasons explained above. *See supra* Section II.E.3.b. To the extent the combination is adding an acknowledgement to Schön’s process, that does not appear to have anything to do with the format of the station’s address. *See* Pet. 30–31. Petitioner does not explain in any detail why a person of ordinary skill in the art would have been motivated to modify Schön’s

process to have the station send an acknowledgement to the master for “each” address change request at the particular time recited in claim 1, namely “prior to a next address change request of the plurality of address change requests being received by the component circuitry.” Petitioner, for example, does not explain why doing so, based on the teachings of I²C Spec, would have been considered an improvement or advancement to the functionality of Schön.

Third, we agree with Patent Owner that a person of ordinary skill in the art would have found an acknowledgement at the recited time in Schön to be superfluous, given Schön’s sequence of operations. *See* Prelim. Resp. 41, 58. Schön describes the master station transmitting a “command for address generation” to all stations. Ex. 1004, col. 2, ll. 58–63. The stations then generate new addresses for themselves from a predetermined range, but do not send any acknowledgement to the master station. *Id.* at col. 2, ll. 63–65. The master station polls all of the possible addresses, starting at the lowest numbered address, to determine if any station generated each address, and a station responds to *that* message if it is the device with the respective address. *Id.* at col. 2, l. 65–col. 3, l. 1. If the reply for a particular address has a transmission error, the master station knows that at least two stations generated the same address and the method needs to be repeated. *Id.* at col. 3, ll. 7–16. Adding an acknowledgement from a station to the master station in response to the address generation command would be unnecessary because the master station later polls all of the available addresses and receives replies in sequence from stations that assigned themselves those addresses. *See* Prelim. Resp. 58. Nor does Petitioner provide any justification for substituting Schön’s existing polling replies from the individual stations for an acknowledgement in response to the

initial address generation command. Petitioner's conclusory assertions in the Petition are insufficient to show a reason to combine Schön and I²C Spec.

Fourth, Dr. Direen's testimony is conclusory and does not provide any additional explanation as to why or how a person of ordinary skill in the art would have combined the references' teachings in the manner asserted in the Petition. *See* Ex. 1002 ¶ 66, App. 1002-B, 2–6. Dr. Direen opines, without further explanation, that “[i]n that Schön discloses a master slave data communications system, a [person of ordinary skill in the art] would be motivated to combine [the] teaching of the I²C bus with Schön's teachings.” *Id.*, App. 1002-B, at 2–3. Again, the fact that the references have some common teachings is not sufficient to establish a reason to combine their teachings to achieve the method set forth in the claim. Dr. Direen also testifies that I²C Spec teaches the recited “acknowledgment” and a person of ordinary skill in the art “understands that message acknowledgements are very common in communication systems and protocols.” *Id.* at 5. This does not support a conclusion, however, that a person of ordinary skill in the art would have had reason to modify Schön's process to send an acknowledgement to the master for “each” address change request at the particular time recited in claim 1, namely “prior to a next address change request of the plurality of address change requests being received by the component circuitry.”

Petitioner has not set forth a sufficient rationale for combining the teachings of Schön and I²C Spec in reaching a conclusion of obviousness as to claim 1. Independent claims 7, 12, and 17 recite limitations similar to those of claim 1, including the recited “acknowledgement[s]” from the component circuitry to the master. Petitioner asserts the same alleged

reasons to combine for all of the challenged claims. *See* Pet. 30–31.

Accordingly, Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that independent claims 1, 7, 12, and 17, or claims 2–5, 8, 10, 11, 13, 15, 18, and 20–22 depending therefrom, are unpatentable over Schön and I²C Spec.

G. Obviousness Grounds Based on Schön, I²C Spec, and Applegate, and Mayer, I²C Spec, and Applegate

Petitioner contends that claims 6, 9, 14, 16, and 19 are unpatentable over Schön, I²C Spec, and Applegate, and Mayer, I²C Spec, and Applegate, under 35 U.S.C. § 103(a), and Patent Owner makes various arguments in response. *See* Pet. 29–30, 40–41; Prelim. Resp. 20–30, 66. Claims 6, 9, 14, and 19, which depend from claims 1, 7, 12, and 17, respectively, recite that “the component circuitry is connectable to a tank containing toner or ink.” Claim 16, which depends from claim 12, recites that “the component circuitry is connected to a tank containing toner or ink.” Petitioner only relies on Applegate as teaching these additional limitations, not for any teaching regarding a predetermined event, plural address change requests, or acknowledgements. *See* Pet. 29–30, 40–41. Accordingly, for the reasons explained above regarding independent claims 1, 7, 12, and 17, Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claims 6, 9, 14, 16, and 19 are unpatentable over Schön, I²C Spec, and Applegate, or Mayer, I²C Spec, and Applegate. *See supra* Sections II.E.3, II.F.2.

III. CONCLUSION

Based on the arguments presented in the Petition, we conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the '079 patent challenged in the Petition. With respect to Petitioner's asserted ground of unpatentability based on Adkins, taking into account the factors set forth in *Becton, Dickinson*, we find that the evidence weighs in favor of exercising our discretion and denying institution of review as to the ground under 35 U.S.C. § 325(d). Therefore, we do not institute an *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied and no *inter partes* review is instituted.

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Patent 8,850,079 B2

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