

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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ADVANCED MICRO DEVICES, INC.,  
Petitioner,

v.

AQUILA INNOVATIONS, INC.,  
Patent Owner.

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IPR2019-01525  
Patent 6,239,614 B1

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Before SALLY C. MEDLEY, DENISE M. POTHIER, and  
AMBER L. HAGY, *Administrative Patent Judges*.

HAGY, *Administrative Patent Judge*.

DECISION  
Final Written Decision  
Determining All Challenged Claims Unpatentable  
*35 U.S.C. § 318(a)*

## I. INTRODUCTION

Advanced Micro Devices, Inc. (“Petitioner”)<sup>1</sup> filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 1–5 (the “challenged claims”) of U.S. Patent 6,239,614 B1 (Ex. 1001, the “’614 patent”). Aquila Innovations, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 9, “Prelim. Resp.”). With authorization from the Board, Petitioner filed a Reply (Paper 10, “Reply”), and Patent Owner filed a Sur-reply (Paper 11, “Sur-reply”). Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review of all challenged claims on all grounds presented in the Petition. Paper 12 (“Institution Decision” or “Dec.”). Patent Owner filed a Patent Owner Response (Paper 18, “PO Resp.”), Petitioner filed a Reply (Paper 21, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 33, “PO Sur-reply”).

On December 11, 2020, we conducted an oral hearing. A copy of the transcript (Paper 38, “Tr.”) is included in the record.

We have jurisdiction under 35 U.S.C. § 6(b). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–5 of the ’614 patent are unpatentable. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a).

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<sup>1</sup> Petitioner identifies itself and ATI Technologies ULC as the real parties-in-interest. Pet. 4.

## II. BACKGROUND

### *A. Related Proceedings*

Petitioner states the '614 patent has been asserted by Patent Owner in *Aquila Innovations Inc. v. Advanced Micro Devices, Inc.*, No. 1:18-cv-00554-LY, filed July 2, 2018, pending in the Western District of Texas. Pet. 4; *see also* Paper 5, 2.

### *B. The '614 Patent*

The '614 patent was filed on April 1, 1999, and claims priority to a Japanese application filed on January 14, 1999. Ex. 1001, codes (22), (30). The '614 patent relates to a layout for a semiconductor integrated circuit device, including multi-threshold complementary metal oxide semiconductor (“MTCMOS”) transistors, which is capable of operating at a lower power supply voltage when active and with reduced leakage current during standby. *Id.* at code (57), 1:7–12. The '614 patent also relates to the use of MOS decoupling capacitors to reduce voltage variations and time delays in MTCMOS devices. *Id.* at code (57), 4:59–5:9.

The '614 patent describes the desirability of operating integrated circuit devices with a low threshold voltage to reduce power consumption. *Id.* at 1:14–21. Lowering the threshold voltage, however, increases leakage current of the MOS transistor during standby. *Id.* at 1:21–26. The '614 patent describes a type of transistor—the MTCMOS transistor—that was known to address this problem. *Id.* at 1:26–32. The MTCMOS transistor is comprised of MOS transistors having a low threshold voltage, which allow reduced power consumption while maintaining operating speed, and standby power control MOS transistors each having a high threshold voltage, which reduce leakage current during standby. *Id.* at 1:33–41.

The '614 patent states that the conventional layout for MTCMOS devices adopted “a standard cell system in which layout design is performed in units of a latch circuit such as a flip-flop circuit comprised of an inverter circuit, a master circuit and a slave circuit, and a logic circuit.” *Id.* at 1:50–55. The '614 patent further notes that “[t]he layout design based on such a standard cell system has a problem in that since it is performed in respective circuit units, the period required to manufacture the MTCMOS becomes long.” *Id.* at 1:55–58. The '614 patent purports to address this problem by “implement[ing] the layout of a semiconductor integrated circuit device by a gate array system, thereby shortening a manufacturing period thereof as compared with the conventional standard cell system.” *Id.* at 2:1–7.

Figure 1 of the '614 patent, reproduced below, illustrates the layout of MTCMOS transistors in a gate array:

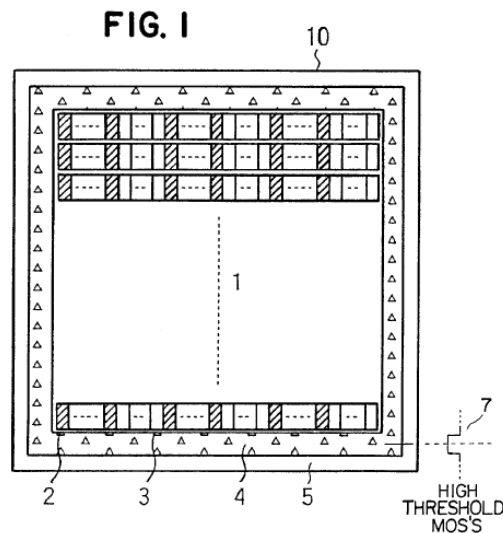


Figure 1 of the '614 patent, reproduced above, is a layout showing an embodiment of the claimed invention. *Id.* at 2:49–50. In particular, Figure 1 illustrates unit cell array 1, in which unit cells 2 with low-threshold MOSFETs are arranged in columns alternating with columns of unit cells 3

with high-threshold MOSFETs. *Id.* at 3:7–16. Power switch 4 is placed around the unit cell array 1, and input/output circuits 5 are disposed there around. *Id.* at 3:16–19. Power switch 4 comprises a PMOS (p-channel metal oxide semiconductor) transistor and an NMOS (n-channel metal oxide semiconductor) transistor, each of which is a MOS transistor 7 that has a high threshold voltage for cutting off leakage current during standby. *Id.* at 3:19–22.

Figure 3 of the '614 patent, shown below, illustrates the unit cells in a MTCMOS integrated circuit device.

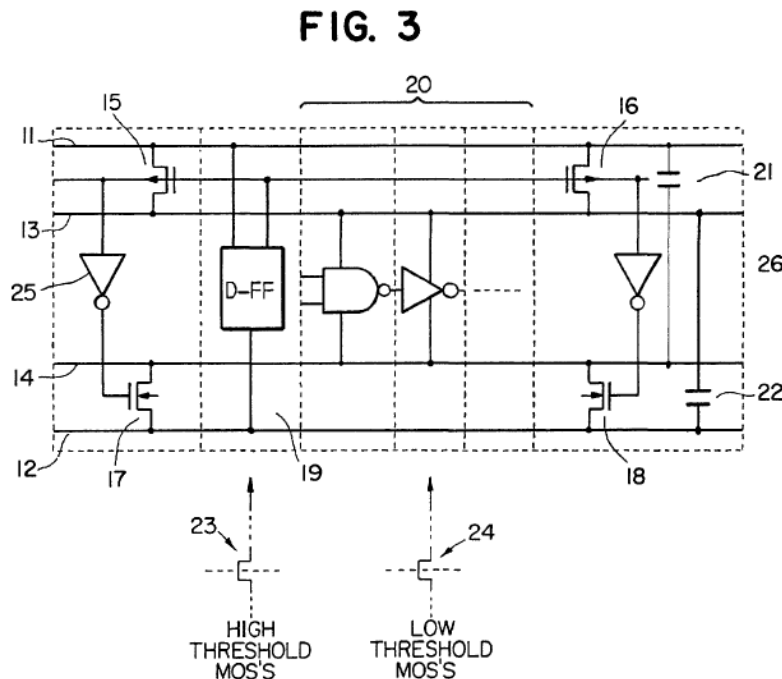


Figure 3 of the '614 patent, reproduced above, is a circuit diagram depicting one example of the unit cells shown in Figure 1 according to the claimed invention. *Id.* at 2:54–56. In particular, the MTCMOS device comprises (1) unit cells having low threshold voltage MOS transistors to form logic cells 20 connecting between two virtual power supply lines 13 and 14,

(2) unit cells having high threshold voltage MOS transistors to form the DFF (D flip flop) cell connecting between two power supply lines 11 and 12, and  
(3) high threshold PMOS and NMOS transistors 15, 16, 17, 18 to form the power switch. *Id.* at 3:7–45.

As also shown above in Figure 3, the MTCMOS includes capacitors 21 and 22 formed between power supply lines and virtual power supply lines. *Id.* at 3:36–39. With these capacitors, according to the '614 patent, the MTCMOS is described as “capable of restraining variations in the values of voltages applied to a virtual power supply line and a virtual ground line and reducing a delay time when switching is done between logic circuits provided within an MTCMOS.” *Id.* at 2:6–13.

### *C. Illustrative Claims*

Of the contested claims, claims 1 and 4 are independent, claims 2 and 3 depend from claim 1, and claim 5 depends from claim 4. Claims 1 and 4, reproduced below, illustrate the claimed subject matter:

1. A semiconductor integrated circuit device, comprising:
  - a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage;
  - a plurality of second unit cells each including a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage;
  - a unit cell array comprised of said first and second unit cells laid in array form;
  - a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage; and

a plurality of input/output circuits disposed around said unit cell array.

4. A semiconductor integrated circuit device comprising:
  - a first power supply line supplied with a first power supply potential level;
  - a second power supply line supplied with a second power supply potential level;
  - a first virtual power supply line;
  - a second virtual power supply line;
  - a latch circuit connected between said first and second power supply lines;
  - a logic circuit connected between said first power supply line and said second virtual power supply line;
  - a first capacitor connected between said first power supply line and said second virtual power supply line; and
  - a second capacitor connected between said second power supply line and said first virtual power supply line;wherein said latch circuit, said logic circuit and said first and second capacitors are constructed by connecting MOS transistors placed within unit cells in array form.

*D. Instituted Grounds of Unpatentability*

We instituted *inter partes* review of all challenged claims based on all grounds of unpatentability asserted in the Petition, which are as follows:

| Claims Challenged | 35 U.S.C. §         | References/Basis                          |
|-------------------|---------------------|-------------------------------------------|
| 1–3               | 103(a) <sup>2</sup> | Urano, <sup>3</sup> Mutoh021 <sup>4</sup> |
| 1–3               | 103(a)              | Mutoh, <sup>5</sup> Mutoh021              |
| 4, 5              | 103(a)              | Douseki, <sup>6</sup> Ramus <sup>7</sup>  |

Dec. 8, 50; Pet. 4–6.

III. DISCUSSION

*A. Principles of Law*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

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<sup>2</sup> The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended several provisions of 35 U.S.C., including § 103. Because the ’614 patent has an effective filing date prior to the effective date of the applicable AIA amendments, we refer herein to the pre-AIA version of § 103.

<sup>3</sup> Urano, Japanese Pat. App. H10–125878, published May 5, 1988 (Ex. 1008, “Urano”) (English translation).

<sup>4</sup> Mutoh et al., Japanese Pat. App. H08-018021A, published Jan. 19, 1996 (Ex. 1013, “Mutoh021”) (English translation).

<sup>5</sup> S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, J. Yamada, “1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS,” IEEE J. SSC, vol. 30, no. 8, pp. 847–854 (Aug. 1995) (Ex. 1005, “Mutoh”).

<sup>6</sup> Douseki et al., U.S. Pat. No. 5,486,774, filed Nov. 2, 1994, issued Jan. 23, 1996 (Ex. 1010, “Douseki”).

<sup>7</sup> Ramus et al., U.S. Pat. No. 5,631,492, filed Apr. 15, 1996, issued May 20, 1997 (Ex. 1011, “Ramus”).

the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.<sup>8</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

#### *B. Level of Ordinary Skill in the Art*

Relying on the testimony of Douglas R. Holberg, Ph.D. (Ex. 1003, “Holberg Declaration”), Petitioner describes the level of ordinary skill as follows:

A person of ordinary skill in the art (“POSA”) at the time of the claimed invention would have a B.S. degree in Electrical

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<sup>8</sup> The parties do not direct our attention to any objective evidence of nonobviousness.

Engineering or an equivalent field, as well as at least 3–5 years of academic or industry experience in semiconductor integrated circuit field, or comparable industry experience.

Pet. 14–15 (citing Ex. 1003 ¶ 26). Patent Owner does not propose an alternative assessment. Ex. 2002 ¶ 57.

Having reviewed the arguments and evidence in the full record, we adopt Petitioner’s definition above, as we did initially in the Institution Decision, as it is consistent with the ’614 patent and the asserted prior art.

### *C. Claim Construction*

In interpreting the claims of the ’614 patent, we “us[e] the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” *See* 37 C.F.R. § 42.100(b) (2019). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005).

#### *1. “unit cells”*

Petitioner proposes we construe the term “unit cells,” recited in independent claims 1 and 4, as “semiconductor integrated circuits implemented by a gate array system, cannot be a conventional standard cell.” Pet. 16.

As support for this construction, Petitioner first notes that the term “unit cells” is not a term of art, nor is it defined in the ’614 specification. *Id.* Petitioner asserts, however, that the ’614 patent consistently distinguishes the claimed invention, which is implemented “by a gate array system,” from conventional MTCMOS circuits that “implemented a standard cell system.”

*Id.* at 17 (citing Ex. 1001, 1:51–58, 2:3–7). For example, according to Petitioner, “[t]he ’614 patent explains that ‘for achieving the’ objective of a MTCMOS gate array system, ‘unit cells each including PMOS transistors and NMOS transistors’ are used in an array format instead of standard cells.” *Id.* (citing Ex. 1001, 2:14–26). Relying on the testimony of Dr. Holberg, Petitioner further asserts “gate arrays and standard cells are two distinct ways of designing and fabricating semiconductor circuits,” and the ordinarily skilled artisan “reading the specification would understand that ‘unit cells’ as recited in claims 1 and 4 are semiconductor integrated circuits implemented by a gate array system, and that they cannot be a conventional standard cell.” *Id.* at 18 (citing Ex. 1003 ¶¶ 74–78).

Patent Owner first “submits that it is not necessary for the Board to construe any of the terms proposed by Petitioner.” PO Resp. 9.<sup>9</sup> Patent Owner then criticizes Petitioner’s proposed construction as “a transparent and improper effort to import a limitation from the specification into the claims.” PO Resp. 11. Patent Owner acknowledges that the Specification depicts the unit cells in a gate array configuration, but asserts “[w]hen the specification describes a single embodiment to enable the invention, this court will not limit broader claim language to that single application ‘unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.’” *Id.* at 12 (quoting *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1288 (Fed. Cir. 2009)). Patent Owner asserts the Specification does not include such “words

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<sup>9</sup> Patent Owner also acknowledged at the oral hearing that “[w]e don’t think that the dispute turns on any of the constructions.” Tr. 17:12–13.

or expressions of manifest exclusion or restriction,” but instead describes the examples in permissive language, stating that the “layout of the MTCMOS 10 *can* be implemented in accordance with a gate array system,” without requiring that it “*must* be implemented” with a gate array. *Id.* (emphases added) (citing Ex. 1001, 3:51–54).

Patent Owner then proposes, “to the extent that a construction is necessary” (*id.* at 9), the Board should adopt the same construction Patent Owner proposed in the co-pending district court proceeding; namely, “unit cells” should be construed as “logic elements of which a unit cell array is comprised.” *See id.* at 12. Petitioner anticipated this proposal in its Petition, and criticized it on the grounds that it “fails to provide clarity to the term, is inaccurate, and fails to account for the specification’s distinction between unit cells and standard cells.” Pet. 18.<sup>10</sup>

We determine that the parties’ dispute over whether “unit cells” are limited to those implemented by a gate array system, to the exclusion of standard cells, is not material to our decision herein. As Petitioner tacitly acknowledges, Petitioner’s proposed construction is actually *narrower* than the one Patent Owner proposes. *See* Pet. 18. As our reviewing court has held, “only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.” *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017

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<sup>10</sup> The parties’ constructions as proposed in the district court are not part of the record before us, aside from the parties’ representations. We further note, based on available public records, that the district court has not issued a claim construction ruling and stayed the action in June 2020.

(Fed. Cir. 2017) (citing *Vivid Technologies* in the context of an *inter partes* review).

Therefore, we determine, as we did in the Institution Decision, that the term “unit cells” includes “logic elements of which a unit cell array is comprised,” and we maintain that construction for purposes of this Final Written Decision. We need not determine whether the proper construction of this term excludes conventional standard cells, as Petitioner contends.

## 2. “unit cell array”

Claim 1 recites “a unit cell array comprised of said first and second unit cells laid in array form.” Petitioner proposes we construe “unit cell array” as “a plurality of said first and second unit cells laid in a regular arrangement or pattern.” Pet. 19. As support for this construction, Petitioner relies on a dictionary definition of “array” as meaning “a **regular** and imposing group or **arrangement**.” *Id.* (citing Merriam-Webster’s Collegiate Dictionary (10th ed. 2001) (Ex. 1037, 64)).

Patent Owner criticizes Petitioner’s proposed construction as based on a “selectively edited non-technical dictionary” and as failing to state “that this definition is consistent with how a person of ordinary skill in the art would understand the term, or explain why resort to extrinsic evidence is necessary.” PO Resp. 13. In challenging Petitioner’s proposed construction, Patent Owner apparently takes issue with Petitioner’s inclusion of a “regular arrangement or pattern.” Patent Owner proposes instead that “unit cell array” be construed as “an arrangement of first and second unit cells, *not necessarily in a regular arrangement or pattern*.” *See id.* (emphasis added).

We determine that Petitioner’s proposed construction is supported by the Specification, which describes a “unit cell array” as “comprised of the

first and second unit cells laid in array form.” Ex. 1001 at 2:21–23. The Specification further refers to Figure 1 (reproduced below) as depicting unit cells 2 and 3 being “laid in array form” (*id.* at 3:17).

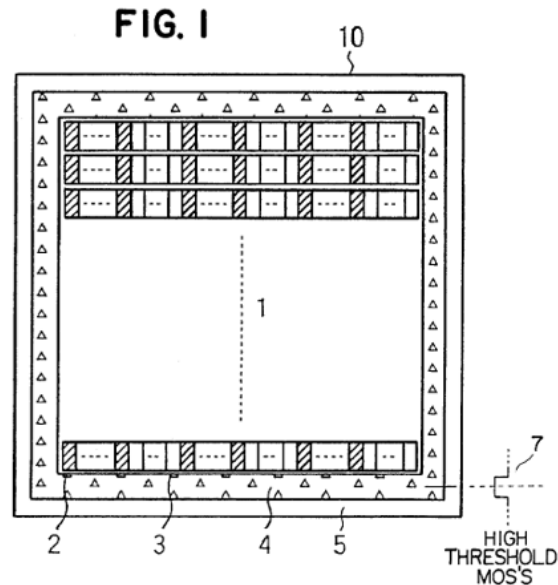


Figure 1 of the '614 patent, reproduced above, depicts a layout of an embodiment of the claimed invention. *Id.* at 2:49–50. Figure 1 shows an arrangement of unit cells 2 and 3 in a regular pattern consisting of repeating rows and columns. The '614 patent does not depict or describe any other arrangement of the unit cells or otherwise define “unit cell array.”

We determine Petitioner’s proposed construction of “unit cell array” is consistent with the Specification and is supported by Petitioner’s proffered dictionary definition, which is informative of the ordinary meaning of the term “array.” *See Phillips*, 415 F.3d at 1314 (noting that “[i]n some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words”). Patent Owner’s proposed

construction, on the other hand, is actually broader than Petitioner's proposal, as it does not exclude a "regular arrangement or pattern." PO Resp. 13.

For purposes of resolving the issues presented in the Petition, we need not determine whether a "unit cell array" *requires* a "regular arrangement or pattern," as the parties agree it *includes* such an arrangement. Therefore, as we did in our Institution Decision, we determine the term "unit cell array" includes "a plurality of said first and second unit cells laid in a regular arrangement or pattern," as proposed by Petitioner, and we maintain that construction for purposes of this Final Written Decision.

### 3. Other Terms

Petitioner also provides constructions for several other terms: "power switch," "power switch disposed around said unit cell array," "plurality of input/output circuits," and "parts of said power switch are disposed within said unit cell array." Pet. 19–24. Patent Owner points out perceived flaws in Petitioner's constructions. PO Resp. 13–16. For example, Patent Owner contends "power switch" requires no construction, but should not be limited to being implemented only with PMOS or NMOS transistors. *Id.* at 14. Patent Owner also contends Petitioner's construction of "disposed around" should not be construed as "encircle," but instead as "located on all sides." *Id.* at 15. Patent Owner also contends "parts of said power switch disposed within said unit cell array" may include, but need not be limited to, third MOS transistors. *Id.* at 16. Thus, as to each term, Patent Owner takes issue with Petitioner's proposed constructions as being *too narrow*. Patent Owner does not, however, point out how any of the parties' claim construction disputes are material to this proceeding, and in fact acknowledged at oral

argument that the parties' disputes do not turn on claim construction.

*See* Tr. 17:12–13.

For purposes of this Final Written Decision, we determine that we need not provide an express construction for any other terms in the '614 patent. *See Nidec Motor Corp.*, 868 F.3d at 1017.

*D. Ground 1: Obviousness of Claims 1–3 Over Urano and Mutoh021*

*1. Overview of Urano (Ex. 1008)*

Urano is a Japanese Unexamined Patent Application that was published on May 5, 1998; accordingly, it is prior art under 35 U.S.C. § 102(a). Pet. 6. Patent Owner does not dispute the prior-art status of Urano.

Urano describes a semiconductor integrated circuit device, and specifically, a cell array that includes a MTCMOS circuit to achieve low voltage and high-speed operation. Ex. 1008, code (57). Urano's integrated circuit device includes an array of "basic cells" to utilize logic functions, where the cells include components of an MTCMOS circuit having high-speed and low-voltage output. *Id.* ¶¶ 1, 29. Urano also teaches that a plurality of low-threshold MOSFETs can be provided along with high-threshold MOSFETs to form different types of basic cells used in a cell array. *Id.* ¶¶ 30, 38.

Figure 25 of Urano, reproduced below, illustrates a layout of cells in a gate array format.

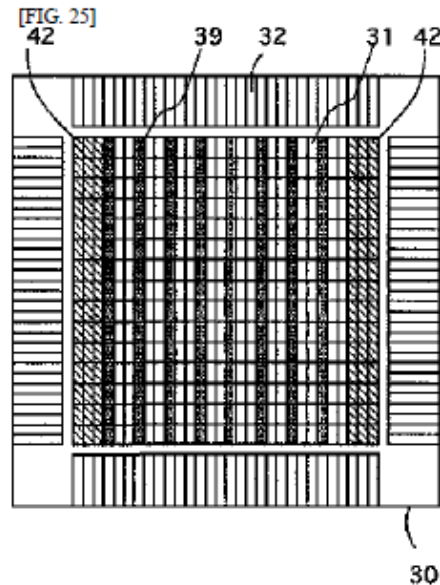


Figure 25 of Urano, reproduced above, is a “diagram for a gate array” according to Urano’s invention. *Id.* ¶ 101. As shown in Figure 25, the gate array includes multiple first basic cells 31 having low-threshold MOSFETs, multiple second basic cells 39 having high-threshold MOSFETs, and multiple third basic cells 42 with high-threshold MOSFETs used as power switch cells. *Id.* ¶¶ 62, 75, 82, 85–87. Urano states “first basic cells 31 and second basic cells 39 are laid out on the chip 30, repeated in units of specific numbers of cells, and third basic cells 42 are arranged on the periphery thereof.” *Id.* ¶ 85.

## 2. Overview of Mutoh021 (Ex. 1013)

Mutoh021 is an Unexamined Japanese Application published on January 19, 1996, more than one year before the priority date of the ’614 patent; accordingly, it is prior art under 35 U.S.C. § 102(b). Ex. 1013; Pet. 6. Patent Owner does not dispute the prior-art status of Mutoh021.

Mutoh021 discloses a MTCMOS IC device configured in a gate array and, more specifically, a gate array-type IC compatible with CMOS circuits

for low-voltage / high-speed operation, composed of a high threshold voltage transistor and a low threshold voltage transistor. Ex. 1013 ¶ 1.

Mutoh021 teaches various layouts in which the high-threshold power switch transistors are located at different regions of the gate array. For example, Mutoh021 states that “a group of logic circuits is formed in the first basic cell, and a power supply control circuit is formed in the second basic cell to control the supply of power to the group of logic circuits,” with “the second basic cell being arranged adjacent to the cell array composed of the first basic cell, at any end vertically or horizontally, at both ends horizontally, at both ends vertically, at all ends vertically and horizontally, or inside [the cell array composed of] the first basic cell.” *Id.* ¶¶ 15–16. Examples of the various layouts are selectively illustrated in Figures 1 and 68 of Mutoh021.

Figure 1 of Mutoh21, reproduced below, illustrates a first layout of the gate array.

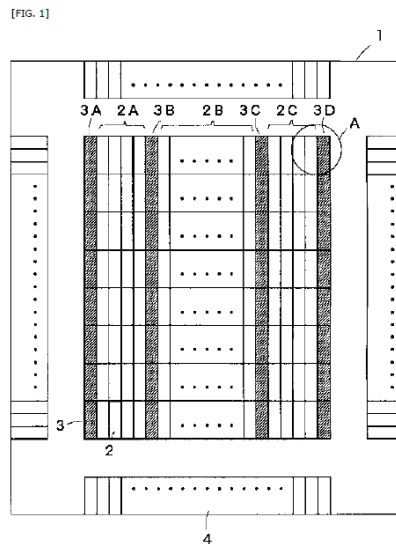
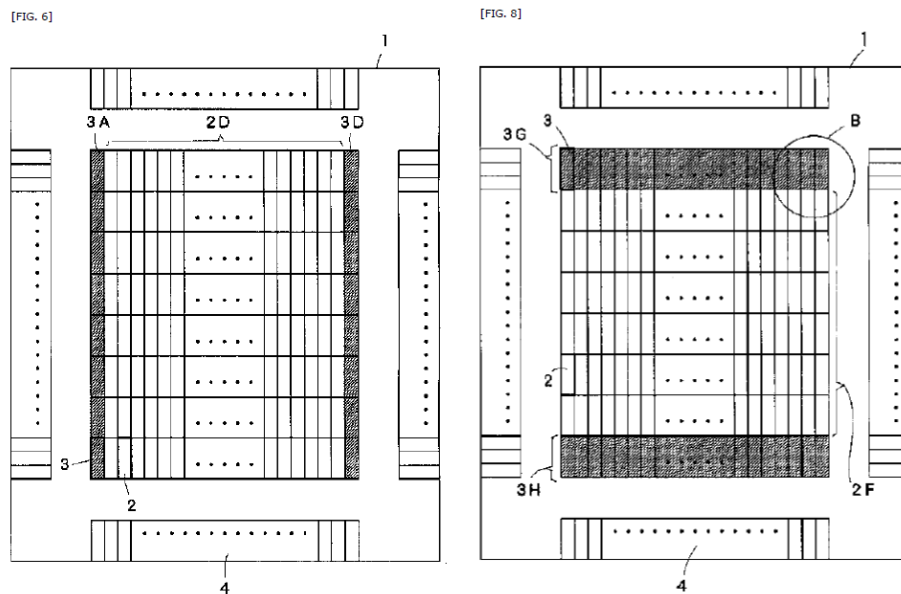


Figure 1 of Mutoh21, reproduced above, is a schematic diagram of LSI chip 1 with a gate array integrated circuit. *Id.* ¶ 19. The array includes first basic

cells 2 arranged in “matrix fashion” to form cell arrays 1A, 2B, and 2C.

*Id.* ¶¶ 3, 19. In each of cell arrays 2A, 2B, and 2C, cell columns (cell arrays) 3A, 3B, 3C, and 3D consisting of second basic cells 3 are arranged next to each other. *Id.* ¶ 19. Input / output cells 4 are located at the periphery of the cell array to form an interface with outside components. *Id.* A power supply control circuit is formed in the second basic cell to control the supply of power to the group of logic circuits. *Id.* ¶ 16. The cell array composed of the second basic cell may be “arranged adjacent to the cell array composed of the first basic cell, at any end vertically or horizontally, at both ends horizontally, at both ends vertically, at all ends vertically and horizontally, or inside the first basic cell.” *Id.* ¶ 15.

Figures 6 and 8 of Mutoh021, reproduced below, illustrate second and third layouts of the gate array, respectively.



Figures 6 and 8 of Mutoh021, reproduced above, depict circuit diagrams of different embodiments of the gate array. *Id.* ¶¶ 27, 30. In the second layout, shown in Figure 6 (above left), second basic cells 3A, 3D are located on the

left and right ends. *Id.* ¶ 27. In the third layout, shown in Figure 8 (above right), second basic cells 3A, 3D are located on the upper and lower ends. *Id.* ¶ 30.

### 3. Analysis

In Ground 1, Petitioner contends claims 1–3 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Urano and Mutoh021. Pet. 34–59. We are persuaded Petitioner has established, by a preponderance of the evidence, that claims 1–3 are unpatentable on this ground.

#### a. Claim 1: “semiconductor integrated circuit device” (preamble)

Without conceding that the preamble is limiting, Petitioner presents evidence that Urano discloses a semiconductor integrated circuit device comprising a gate array of transistors arranged on a chip. Pet. 41 (citing Ex. 1008 ¶ 1). Patent Owner does not dispute Petitioner’s contentions pertaining to the preamble of claim 1.

Regardless of whether the preamble is limiting, we find Urano teaches the subject matter of the preamble of claim 1. In particular, Urano discloses a gate array that includes MTCMOS circuits, which are semiconductor integrated circuit devices. *See, e.g.*, Ex. 1008 ¶¶ 6–8 (describing gate arrays as including logic circuits in semiconductor integrated circuits).

*b. Claim 1: “a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage”*

*“a plurality of second unit cells each including a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage”*

Petitioner presents evidence that Urano discloses a plurality of first unit cells (e.g., first basic cells 31), each including a plurality of first MOS transistors (e.g., Q1–Q4) having a first threshold voltage (e.g., low).

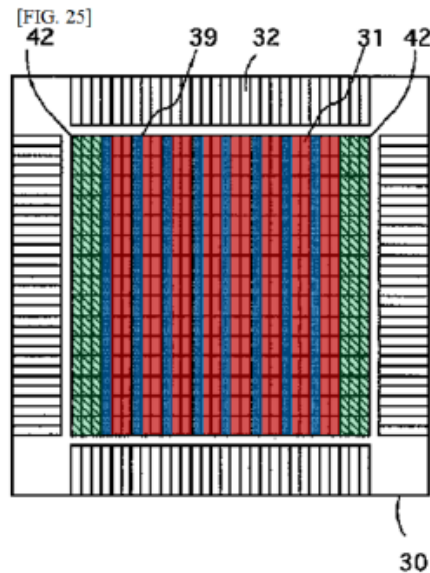
Pet. 42–44 (citing Ex. 1008 ¶ 85, Fig. 25). Petitioner also presents evidence that Urano discloses a plurality of second unit cells (e.g., basic cells 39) that each include MOS transistors (e.g., Q6, Q8) with a second threshold voltage (e.g., high). *Id.* at 45–46.

Patent Owner does not address Petitioner’s arguments or evidence regarding “unit cells.” Rather, as discussed below, Patent Owner’s challenge to Petitioner’s arguments and evidence in Ground 1 is directed to Petitioner’s combination of the Urano and Mutoh021 references regarding the “disposed around” limitations of claim 1. *Infra* Section III.D.3.f.

Petitioner’s arguments and un rebutted evidence are persuasive. Based on those arguments and evidence, we find Petitioner has proven, by a preponderance of the evidence, that Urano discloses “a plurality of first unit cells each including a plurality of first MOS transistors, each of the first MOS transistors having a first threshold voltage,” and “a plurality of second unit cells each including a plurality of second MOS transistors, each of the second MOS transistors having a second threshold voltage,” as recited in claim 1.

*c. Claim 1: “a unit cell array comprised of said first and second unit cells laid in array form”*

Petitioner presents evidence that Urano discloses a unit cell array comprised of said first and second unit cells (e.g., first basic cells 31 and 39) laid in array form. Pet. 42, 45, 48. Urano states “FIG. 25 is a diagram showing a gate array according to a fourth embodiment,” in which “first basic cells 31 and second basic cells 39 are laid out on the chip 30, repeated in units of specific numbers of cells, and third basic cells 42 are arranged on the periphery thereof.” Ex. 1008 ¶ 85; Pet. 48. Petitioner asserts Figure 25 of Urano, reproduced below as annotated by Petitioner (Pet. 49), illustrates first basic cells 31 and second basic cells 39 laid in a regular arrangement pattern forming an array:



EX1008, Fig. 25 (annotated).

Figure 25 of Urano, reproduced above as annotated by Petitioner, illustrates one layout of a cell array with multiple first basic cells (31) having low-threshold MOSFETs (annotated red), multiple second basic cells (39) having

high-threshold MOSFETs (annotated blue), and multiple third basic cells (42) used as power switch cells with high-threshold MOSFETs (annotated green). *Id.* (citing Ex. 1008 ¶¶ 62, 75, 82, 85–87).

Patent Owner does not address Petitioner’s arguments and evidence as to this limitation, aside from asserting that Petitioner’s construction of “unit cell array” is too narrow. *See* PO Resp. 12–13. As noted above (*supra* Section III.C.2), we disagree with Patent Owner’s construction. Even if we agreed that Petitioner’s proposed construction were too narrow and that a broader construction should be adopted, Petitioner’s showing that this limitation is disclosed by Urano would not be defeated but would, if anything, be stronger.

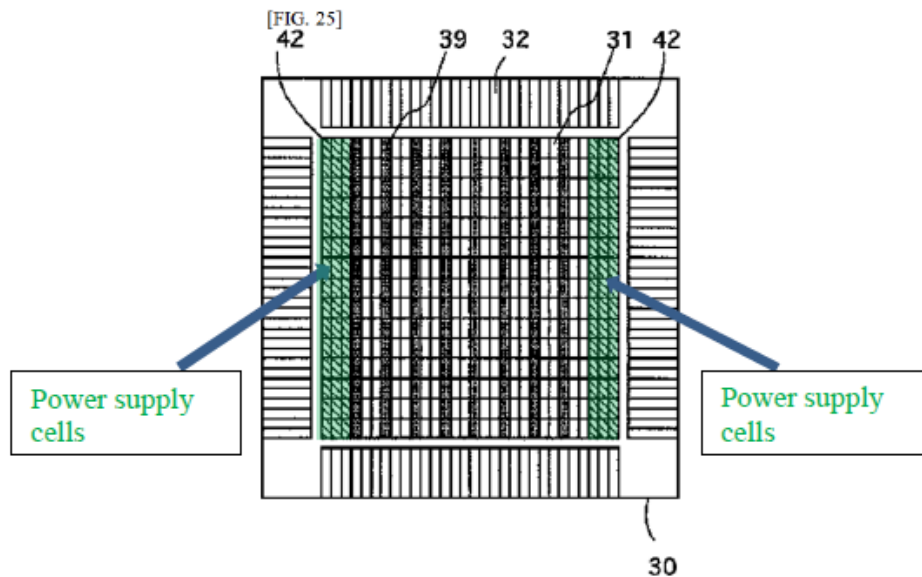
Based on Petitioner’s arguments and unrebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Urano discloses “a unit cell array comprised of said first and second unit cells laid in array form,” as recited in claim 1.

*d. Claim 1: “a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage”*

Petitioner presents evidence that Urano discloses a power switch (e.g., power supply cells 43 structured using third basic cells 42) disposed around said unit cell array and comprised of a plurality of third MOS transistors (e.g., p-channel MOS transistors Q13–Q14 and n-channel MOS transistors Q15–Q16), each of the third MOS transistors (e.g., Q13–Q16) having the second threshold voltage (e.g., high). Pet. 49–50 (citing Ex. 1008 ¶¶ 65–69, 78–80, 86–88, 93). Petitioner also presents evidence that Urano teaches

the power supply cells having the high threshold MOSFETs Q13-Q16 are disposed about the periphery of the cell array— “[the] first basic cells 31 and [the] second basic cells 39 are laid out on the chip 30, repeated in units of specific numbers of cells, and [the] **third basic cells 42 are arranged on the periphery thereof.**”

Pet. 51 (quoting Ex. 1008 ¶ 85). Figure 25 of Urano, reproduced below as annotated by Petitioner (Pet. 52), illustrates an arrangement of the power supply cells:

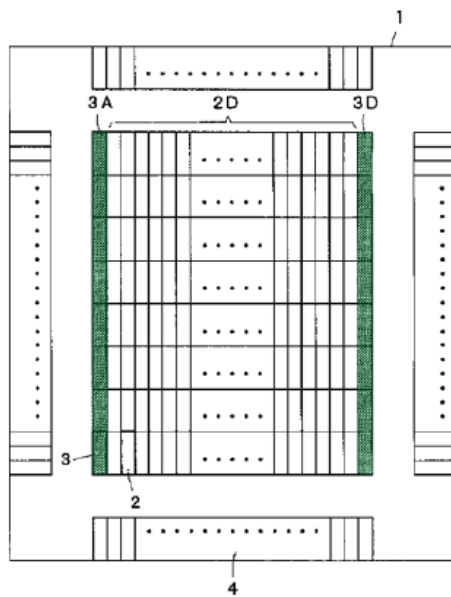


EX1008, Fig. 25 (annotated).

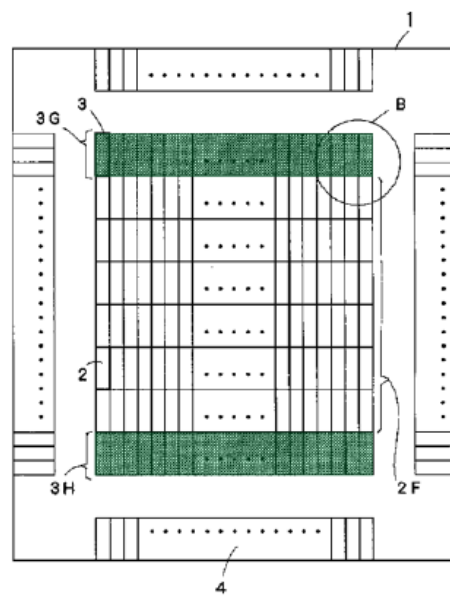
Figure 25 of Urano, reproduced above as annotated by Petitioner, shows power supply cells (third basic cells 42 (annotated green)) “arranged on the periphery” of the array of first and second basic cells (31, 39). Ex. 1008 ¶ 85.

Petitioner acknowledges Urano does not explicitly teach the third MOS transistors (e.g., p-channel MOS transistors Q13–Q14 and n-channel MOS transistors Q15–Q16) *disposed around* the unit cell array, but argues

that Mutoh021 discloses power switch MOSFETs of an MTCMOS circuit disposed around a unit cell array. Pet. 52. In particular, Petitioner presents evidence that Mutoh021 teaches second basic cells 3 having high threshold voltage PMOS and NMOS that are used as a power switch circuit to control the power supply to the logic circuits. *Id.* at 53 (citing Ex. 1013 ¶¶ 15–16, 33; Ex. 1003 ¶ 144). Figures 6 and 8 of Mutoh021, reproduced below as annotated by Petitioner (Pet. 54), illustrate two layouts of the second basic cells.



EX1013, Fig. 6 (annotated).



EX1013, Fig. 8 (annotated).

Figure 6 of Mutoh021, reproduced above as annotated by Petitioner, shows a circuit diagram of a chip, on which second basic cells 3 are located on the entire left and right vertical ends 3A and 3D (annotated green). Ex. 1013, Fig. 6, ¶ 27. Figure 8 of Mutoh021, reproduced above as annotated by Petitioner, shows a circuit diagram of a chip, on which second basic cells 3 are located on the entire upper and lower horizontal ends 3G and 3H (annotated green). Pet. 54; Ex. 1013 ¶ 30.

Petitioner presents evidence that Mutoh021 also discloses that second basic cells 3 (equivalent to third basic cells 42 of Urano) can be located around *all sides* of the gate array, although this configuration is not illustrated in the figures. Pet. 54. Specifically, Mutoh021 states “the second basic cell [can be] arranged adjacent to the cell array composed of the first basic cell, at any end vertically or horizontally, at both ends horizontally, at both ends vertically, *at all ends vertically and horizontally*, or inside [the cell array composed of] the first basic cell.” Ex. 1013 ¶ 15 (emphasis added); Pet. 54. Petitioner further argues “a POSA would have been motivated to place the power supply cells 42 of Urano around the cell array as disclosed in Mutoh021.” Pet. 55.

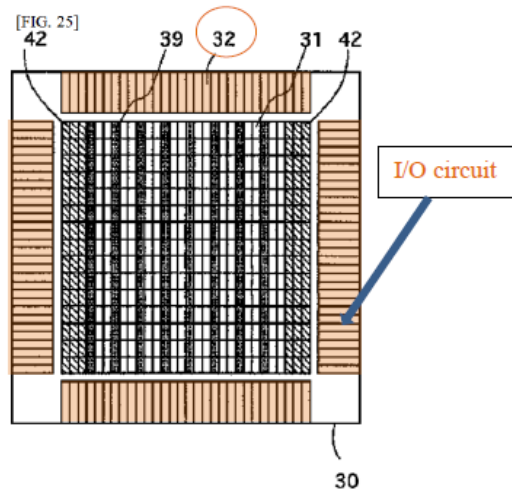
Aside from challenging Petitioner’s constructions of “unit cell” and “unit cell array,” as discussed above (*see* Section III.C), Patent Owner does not otherwise challenge Petitioner’s arguments or evidence as to Urano’s disclosure regarding this limitation, nor does it challenge Petitioner’s arguments or evidence that Mutoh021 discloses second basic cells disposed around the cell array. Patent Owner does, however, argue that Petitioner has failed to provide evidence supporting a motivation for the ordinarily skilled artisan to have combined the teachings of Urano and Mutoh021. PO Resp. 19–35. This argument is addressed, below, in conjunction with our discussion of Petitioner’s arguments and evidence of a motivation to combine.

Based on Petitioner’s arguments and un rebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has demonstrated by a preponderance of the evidence that the combination of Urano and Mutoh021 discloses “a power switch disposed

around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage,” as recited in claim 1. Our findings regarding a motivation to combine the teachings of Urano and Mutoh021 are discussed below in Section III.D.f.

*e. Claim 1: “a plurality of input/output circuits disposed around said unit cell array”*

Petitioner presents evidence that Urano discloses “first basic cells 31 are arranged, in the form of an array, on the chip 30, with **input/output buffer cells 32 at the four edges thereof**. These input/output buffer cells 32, as with the basic cells, are structured from MOS transistors, where logic gates are structured through interconnections, to function as input buffers or output buffers.” Pet. 55 (quoting Ex. 1008 ¶ 61). Figure 25 of Urano, reproduced below as annotated by Petitioner (Pet. 56), illustrates input/output buffer cells 32 encircling the basic cells.



EX1008, Fig. 25 (annotated).

Figure 25 of Urano, reproduced above as annotated by Petitioner, is a diagram showing “a gate array,” with input/output buffer cells 32 (annotated

in orange) encircling the array of basic cells 31, 39. Pet. 56; Ex. 1008 ¶¶ 61, 74. Although Petitioner prefaces its discussion of this limitation by referring to the *combined* teachings of Urano and Mutoh021, Petitioner discusses only Urano’s teachings. See Pet. 55–56.

Aside from challenging Petitioner’s constructions of “unit cell” and “unit cell array” (see Section III.C), Patent Owner does not otherwise challenge Petitioner’s arguments or evidence as to this limitation.

Based on Petitioner’s arguments and un rebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has demonstrated by a preponderance of the evidence that Urano discloses “a plurality of input/output circuits disposed around said unit cell array,” as recited in claim 1.

*f. Claim 1: Motivation and Rationale To Combine*

As discussed above, Petitioner relies primarily on Urano as disclosing the limitations of claim 1, but acknowledges Urano does not disclose a power switch “disposed around”<sup>11</sup> the array, for which Petitioner relies on Mutoh021 in combination with Urano. Pet. 52. Petitioner argues the ordinarily skilled artisan would have been motivated to combine Mutoh021’s teaching “of placing power switch MOSFETs that encircle a unit cell array with the unit cell array of Urano” to obtain the alleged

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<sup>11</sup> As noted *supra* Section III.C.3., Patent Owner contends “disposed around” should not be construed as “encircle,” as Petitioner proposes, but instead as “located on all sides.” PO Resp. 15; *see also* Pet. 21. Patent Owner does not explain the difference between the parties’ proposals. As also noted above, we determine this dispute is not material to our decision herein.

invention claimed in the '614 patent. *Id.* at 34–35. In particular, Petitioner presents arguments and evidence that: (1) Urano and Mutoh021 are directed to the same field (“circuits based on the same MTCMOS configuration and same cell-based gate array architecture”) (*id.* at 35); (2) Urano discloses power switch cells “on the periphery” of the cell array (*id.* at 35 (citing Ex. 1008 ¶¶ 87, 85)); (3) Mutoh021 discloses power switch cells “very similar to Urano’s” that can be positioned “at all ends vertically and horizontally” (*id.* at 36–37 (citing Ex. 1013 ¶¶ 15, 16, 31)); (4) “modify[ing] the layout in Urano based on the explicit teachings of Mutoh021 to arrange the power switch cells to all four ends to encircle the cell array” would provide advantages of “circuit design efficiencies, such as reducing wiring complexity, reducing resistance between components (*i.e.*, parasitics), decreasing response time of circuit components, and increased layout pattern density to achieve the low voltage, high-speed operation of Urano” (*id.* at 40 (citing Ex. 1003 ¶ 126)); and (5) an ordinarily skilled artisan would have “readily understood how to combine [the teachings of Urano and Mutoh021] using known layout design techniques” (*id.* at 38–41 (citing Ex. 1003 ¶¶ 126–128)).

Relying on the testimony of Dr. Holberg, Petitioner contends an ordinarily skilled artisan “would have been motivated to place the power switch cells of Urano on all four sides of the cell array or on all four sides of the cell array and within the cell array to achieve design efficiencies of reduced noise and voltage drops due to parasitic resistance.” *Id.* at 40–41 (citing Ex. 1003 ¶ 127). Further relying on the testimony of Dr. Holberg, Petitioner also contends the disclosed elements

would have been readily combined according to known methods to yield predictable results—reduced resistance between components—and there would have been a reasonable expectation of success because such a combination would have been applying a known technique—positioning power cells around the cell array or around and within the cell array—to a known device—a MTCMOS IC—and for a same purpose—operating under a same low voltage and suppressing the magnitude of the leakage current during standby.

*Id.* at 41 (citing Ex. 1003 ¶ 128).

Patent Owner challenges Petitioner’s assertions on several grounds. PO Resp. 21–35. In particular, Patent Owner argues Petitioner fails to show: (1) arranging power cells to encircle a unit cell array was an improvement over Urano’s “both ends vertically” arrangement (*id.* at 21–22); (2) the purported improvement was a known technique (*id.* at 22–24); (3) the ordinarily skilled artisan would have recognized such an improvement (*id.* at 24–30); and (4) Urano and Mutoh021 could be readily or predictably combined (*id.* at 30–33). Patent Owner also contends Petitioner’s proposed combination is above the level of ordinary skill in the art. *Id.* at 33–35. We address each of these contentions below.

*1) Petitioner’s Showing of Improving Urano with Mutoh021*

Patent Owner’s first three arguments are premised on alleged deficiencies in Petitioner’s showing that locating the power switch cells on all sides around a unit cell array (as taught by Mutoh021) would have improved Urano, by applying a known technique, and would have been recognized as such by the ordinarily skilled artisan. PO Resp. 21–30.

Patent Owner’s arguments are based, in part, on application of incorrect standards for determining obviousness. Patent Owner first argues

that Petitioner never explains “why Urano’s ‘both ends vertically’ arrangement is ready for improvement or performs any differently than Mutoh021’s purported ‘encircling’ arrangement.” PO Resp. 21. Patent Owner premises Petitioner’s purported failure on the notion that “[b]ecause *Urano does not disclose a problem*, a person of ordinary skill in the art would have had no reason to look to Mutoh021 for a solution.” *Id.* at 22 (emphasis added). The proper obviousness analysis, however, does not require prior art references to recognize or even suggest the problem that applicant attempted to solve. *See KSR*, 550 U.S. at 419–20 (“In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. . . . [A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.”); *see also Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (noting that a petitioner “does not need to show that there was a known problem with the prior art system in order to articulate the required rational underpinning for the proposed combination”).

The Supreme Court in *KSR* described many potential rationales that could make a modification or combination of prior art references obvious to the ordinarily skilled artisan. 550 U.S. at 417–22. In so doing, *KSR* overturned the approach previously used by the Federal Circuit requiring that some teaching, suggestion, or motivation be found in the prior art. 550 U.S. at 415. Instead, the Court explained that a rationale to combine could arise from “interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in

the art.” *Id.* at 418. For example, the Court posited that “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *Id.* at 417. Thus, for a technique’s use to be obvious in improving a device, the skilled artisan need only be able to recognize, based on her background knowledge, its potential to improve the device and be able to apply the technique.

Patent Owner argues against application of that principle here on the basis that “Mutoh021 does not disclose any advantage associated with an ‘at all ends vertically and horizontally’ arrangement,” and asserts that, therefore, an “encircle” arrangement was not a known technique that would improve Urano’s “both ends vertically” arrangement. PO Resp. 22. In that regard, Patent Owner faults Petitioner for “misleadingly manufactur[ing] an advantage that does not exist” by relying on paragraph 35 of Mutoh021 as disclosing that the “Effects of the Invention” may be attributable to Mutoh021’s “around or around and within” power switch cell arrangement. *Id.* at 23 (citing Pet. 37–38; Ex. 1013 ¶ 35). Patent Owner contends Mutoh021 “makes clear that the advantages the paragraph describes” are merely the result of arranging power switch cells “adjacent to the cell array” and are not specifically attributable to the “at all ends vertically and horizontally” arrangement. *Id.* Patent Owner continues: “According to Mutoh021, one of ordinary skill would just as easily realize its advantages by utilizing the ‘at both ends vertically’ arrangement Urano already practices, as it would from any of the other five arrangements Mutoh021 discloses.” *Id.*

Notably, in making this argument, Patent Owner implicitly acknowledges that “any” of the arrangements disclosed by Mutoh021 would result in the advantages described therein, tacitly conceding that Mutoh021 discloses several configurations, including the one relied upon by Petitioner, as effectively interchangeable. Patent Owner essentially faults Petitioner for failing to show that the “at all ends vertically *and* horizontally” arrangement is *superior* to the other “both ends vertically *or* horizontally” configurations described in Mutoh021 and similarly described in Urano. *See* PO Resp. 25–30; PO Sur-reply 11–15. But superiority is not the test for obviousness. Despite pointing to technical trade-offs between the various configurations (*see id.*), Patent Owner does not posit that the “at all ends vertically and horizontally” arrangement is necessarily inferior to any of the other disclosed arrangements. Even assuming that were the case, the Federal Circuit has explained that even if “better alternatives” exist, that “does not mean that an inferior combination is inapt for obviousness purposes.” *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012). We find Mutoh021’s effectively equating the power-switch configurations disclosed by Urano (at both ends vertically *or* horizontally) with a configuration of “at all ends vertically *and* horizontally” would have provided motivation for the ordinarily skilled artisan to have modified Urano accordingly.

Petitioner has presented additional evidence in support of the ordinarily skilled artisan choosing the “at all ends” power-switch configuration from among the options taught by Mutoh021. For example, Petitioner provides evidence that such configuration would provide benefits of “circuit design efficiencies, such as reducing wiring complexity, reducing resistance between components (*i.e.*, parasitics), decreasing response time of

circuit components, and increased layout pattern density to achieve the low voltage, high-speed operation of Urano.” Pet. 40 (citing Ex. 1003 ¶ 126). Petitioner’s expert, Dr. Holberg, provides testimony in support of this assertion. Ex. 1003 ¶¶ 125–128. In particular, Dr. Holberg notes that, at the time of the ’614 invention, one known advantage of power supply terminals disposed on all sides of the unit cell array would have been reduced resistance between components. *Id.* ¶ 127 (citing Ex. 1025, 295; Ex. 1017, 141); *see also* Pet. 41.

Patent Owner challenges Dr. Holberg’s testimony regarding known advantages as “generic” and as bearing “no relation to any specific combination of prior art elements.” PO Resp. 25. We disagree with this characterization. Dr. Holberg supports his testimony, for example, with the “Sato” article (Exhibit 1017), noting Sato confirms the ordinarily skilled artisan knew that power supply terminals “located on all four sides of the chip” were beneficial to “reduce the voltage drops in power busses caused by the maximum power supply current.” Ex. 1003 ¶ 127. Patent Owner acknowledges Dr. Holberg’s reliance on the Sato article, but asserts Dr. Holberg’s analysis is nevertheless lacking because Dr. Holberg does not state that Urano’s design suffers from the very flaw recognized in Sato as being aided by the encircling arrangement. PO Resp. 29. Patent Owner’s argument, however, presupposes that Petitioner must show the ordinarily skilled artisan would have made the combination only for the purpose recognized in Sato, which is contrary to the principles expressed by the Supreme Court in *KSR*. *See KSR*, 550 U.S. at 419–20 (noting that “any need or problem known in the field of endeavor at the time of invention and

addressed by the patent can provide a reason for combining the elements in the manner claimed”).

Patent Owner next argues that “adding more power cells to the horizontal ends of Urano” would result in a disadvantage of “increas[ing]” wiring complexity because it would require “new wiring running in a new direction.” PO Resp. 28. Patent Owner also argues this arrangement would result in another disadvantage—subtracting logic cells. *Id.* at 30. Patent Owner asserts these disadvantages show that the ordinarily skilled artisan would not have recognized Urano’s design would be improved by an arrangement of the power switch cells on all four sides instead of just two. *Id.*

Petitioner counters these contentions on several grounds. Petitioner first argues Patent Owner’s contentions are generic and unsupported. Pet. Reply 15. Petitioner further notes that the ’614 patent and Mutoh021 disclose the same level of detail regarding the placement of the power switch cells and posits that if the ordinarily skilled artisan would have appreciated the benefits of the “disposed around” arrangement of power switch cells from the disclosure of the ’614 patent, such artisan would also have appreciated similar benefits from the similar disclosure of Mutoh021.<sup>12</sup> *Id.*

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<sup>12</sup> We disagree with Patent Owner’s contention that this statement by Petitioner is a new argument in reply. *See* PO Sur-reply 7. Petitioners are not prohibited from relying on new evidence and arguments in a reply if the evidence and arguments are responsive to arguments made in a patent owner response. *See* 37 C.F.R. 42.23(b); Consolidated Trial Practice Guide, 73 (*available at* <https://www.uspto.gov/TrialPracticeGuideConsolidated>). Petitioner is not positing a new ground of unpatentability; rather, Petitioner is responding to Patent Owner’s contention that the ordinarily skilled artisan would not have understood benefits to power-switch cells disposed all

(citing Ex. 1047, 112:11–18) (Patent Owner’s expert acknowledging benefits to placing power switch around the unit cell array); *see also* Ex. 1047, 59:13–60:5 (Patent Owner’s expert acknowledging that the ’614 patent does not articulate the efficiency of design of a power switch disposed around the unit cell array, but asserting the ordinarily skilled artisan would have understood such benefits). As for the disadvantages alleged by Patent Owner to result from adding more power cells to Urano, Petitioner points to testimony by its expert contradicting those assertions. Pet. Reply 15 (citing Ex. 1048 ¶ 32 (stating that the ordinarily skilled artisan “would have instead understood that the extra supply cells are not redundant because they reduce the power supply feed resistance and thus provide a benefit. Cell utilization would also be unchanged by power switches at the periphery”))).

We find the ordinarily skilled artisan would have understood that power switch cells can be placed at any locations of the cell array, and that the ordinarily skilled artisan would have appreciated benefits to modifying Urano’s layout design to include power switch cells not just on two sides but on all four sides around the cell array, as described in Mutoh021. Not only does Mutoh021 effectively recognize that an all four sides arrangement is

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around the unit cell array based on what was then known in the art. *See* PO Resp. 21–22. We also disagree that Petitioner’s contention represents hindsight. *See* PO Sur-reply 7. It is not hindsight for Petitioner to identify prior-art disclosure in Mutoh021 commensurate to the teachings of the ’614 patent and to assert that the ordinarily skilled artisan would have understood the commensurate disclosures similarly; that is, if the artisan would have inherently understood certain undisclosed benefits from the ’614 patent’s “all sides” arrangement, it is logical the artisan would also have inherently understood the same benefits from the same arrangement disclosed in Mutoh021.

interchangeable with a two sides arrangement in achieving the benefits of Mutoh021's invention, as Patent Owner tacitly concedes (PO Resp. 23 (citing Ex. 1013 ¶ 35)), but Petitioner provides persuasive reasoning supporting advantages of such a design in Urano's configuration, including circuit design efficiencies as noted above. *See* Pet. 37–39.

Petitioner's contentions are supported by the testimony of Dr. Holberg, who provides persuasive explanation, as we also discuss above (*e.g.*, Ex. 1003 ¶¶ 120, 123–128). It is within our discretion to assign the appropriate weight to the expert testimony offered by the parties. *See, e.g., Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another “unless no reasonable trier of fact could have done so”); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004); (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.”). We give Dr. Holberg's testimony substantial weight because his testimony is consistent with the teachings of Urano and Mutoh021, as discussed above. We have reviewed Patent Owner's contrary arguments and evidence and given them due consideration, but we do not find that they rebut Petitioner's persuasive showing and evidence.

*2) Petitioner's Showing of Reasonable Expectation of Success*

Patent Owner's remaining two arguments are premised on alleged deficiencies in Petitioner's showing that the ordinarily skilled artisan would have understood how to combine the relevant teachings of Urano and Mutoh021—namely, Patent Owner contends that Petitioner has failed to show that Urano and Mutoh021 could be readily or predictably combined,

and further contends that, in fact, such combination would have been above the level of ordinary skill in the art. PO Resp. 30–35.

We disagree with Patent Owner’s contentions. Petitioner has provided evidence of a reasonable expectation of success in combining the teachings of Urano and Mutoh021 on the basis that such a combination would have been applying a known technique—positioning power cells around the cell array or around and within the cell array—to a known device—a MTCMOS integrated circuit (“IC”)—and for a same purpose—operating under a same low voltage and suppressing the magnitude of the leakage current during standby. *See* Pet. 34–41; Ex. 1003 ¶¶ 120, 123–128; Ex. 1048 ¶ 10; *see KSR*, 550 U.S. at 416 (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”). Petitioner’s contentions are supported by the testimony of Dr. Holberg, as well as by the teachings of Urano and Mutoh021, as discussed above, which describe analogous MTCMOS IC devices based on the same MTCMOS configuration and same cell-based gate array architecture. *See* Ex. 1003 ¶¶ 115–128; Ex. 1048 ¶ 12.

Patent Owner challenges Dr. Holberg’s testimony as “conclusory and factually unsupported,” asserting that Dr. Holberg’s testimony is deficient because it does not provide details on how the ordinarily skilled artisan would have rewired Urano to incorporate a power switch encircling the unit cell array. PO Resp. 32–33. Patent Owner proffers testimony of its expert, Dr. Przybylski, to the effect that “placement of cells in a base level cell array of a gate array is not ‘routine,’” but requires “many considerations related to power distribution, channel characteristics and metal utilization.” *Id.* at 32 (citing Ex. 2002 ¶ 108). Patent Owner then contends the ordinarily skilled

artisan “could not overcome these challenges by simply booting up design software.” *Id.*

Petitioner counters that “[n]one of the issues that [Patent Owner] raises are outside of the common aspects of circuit design that any POSA would regularly encounter and understand how to address.” Pet. Reply 21. Petitioner points to evidence, as cited in the Petition and confirmed by the testimony of Dr. Holberg, that “integrated circuit design, including the ‘first phase’ of arranging unit cells and the power switch cells, using standard computer-aided design (CAD) software for semiconductor IC circuit devices was well known” in the art at the time of the ’614 invention. *Id.* at 20 (citing Ex. 1025, xx; Ex. 1017, 142; Ex. 1005, 850; Ex. 1003 ¶¶ 44–46; Ex. 1048 ¶¶ 53–54). Petitioner further presents evidence that the ordinarily skilled artisan would have readily understood how to combine the teachings of Urano and Mutoh021 “using known layout design techniques.” *Id.* at 20–21. “For example, a POSA would have clearly understood how to adapt the layout design of an IC, such as an MTCMOS gate array, using well-known layout designs based on known design considerations to achieve a low-voltage, high-speed operation.” *Id.* at 21 (citing Ex. 1008 ¶ 29; Ex. 1025, xxi; Ex. 1048 ¶ 55).

We are persuaded by Petitioner’s arguments because they are supported by the cited evidence. On the other hand, we do not find the testimony of Patent Owner’s expert rebuts such arguments and evidence. Dr. Przybylski’s cited testimony does not contradict Dr. Holberg’s opinions as to the ability of the ordinarily skilled artisan to have made the proposed combination, but merely acknowledges the design constraints that would have had to be taken into consideration in placing power switch cells.

*See* Ex. 2002 ¶ 108. We find, based on Petitioner’s evidence and expert testimony, that the ordinarily skilled artisan would have been aware of such constraints and would have been able to address them effectively in combining the teachings of Urano and Mutoh021 to place a power switch disposed around a unit cell array, as claimed. In addition, as noted above, Patent Owner acknowledges that the advantages of Mutoh021 would have been achieved by any of the arrangements disclosed therein for the placement of the power switch cells (PO Resp. 23), essentially acknowledging that the arrangements are interchangeable. On the facts presented here, because an “at either end” power-switch arrangement (as in Urano) was known to be interchangeable with an “all sides” power-switch arrangement (as in Mutoh021), such evidence supports a finding that one of ordinary skill in the art would have had a reasonable expectation of success in modifying Urano’s power-switch arrangement in accordance with the teachings of Mutoh021.

Relatedly, Patent Owner argues that Petitioner’s proposed combination “requires a level of skill above the ordinary skill in the art.” PO Resp. 33 (citing *MobileMedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1167 (Fed. Cir. 2015) (noting that a proposed combination may not be obvious if making the combination would have been beyond the level of ordinary skill)). Although Patent Owner has not proposed a description of the level of ordinary skill in the art, Patent Owner nevertheless faults Petitioner for giving undue credit to the ordinarily skilled artisan within the definition proposed by Petitioner and adopted by the Board in the Institution Decision, stating “a person with a bachelor’s degree and three to five years of experience *would not necessarily* have had the level of skill needed to

appreciate the design considerations and tradeoffs underpinning Petitioner’s proposed combination sufficiently to make the combination work in practice.” *Id.* (emphasis added) (citing Ex. 2002 ¶ 123). Patent Owner bases this somewhat equivocal argument on the testimony of Dr. Przybylski, who opines that the design of a gate array requires “a great deal of detailed and manual design work of a highly skilled nature,” and further opines (also somewhat equivocally) that a person of ordinary skill according to the definition adopted by the Board “would *not necessarily* have had the level of skill needed to appreciate the design considerations and tradeoffs underpinning Petitioner’s proposed combination sufficiently to make the combination work in practice.” Ex. 2002 ¶ 127 (emphasis added). Dr. Przybylski bases this opinion on the assumption that such ordinarily skilled artisan would have “focused on logic design and implementation instead of circuit design and the interactions between semiconductor processes and the characteristics of the resulting integrated circuits,” and thus “would *not necessarily* have had any specific experience or insight into the many constraints and tradeoffs that drive gate array architecture, basic cell design and power distribution network design that are central to the first phase of the design process.” *Id.* (emphasis added).

We find that Patent Owner’s arguments and evidence do not rebut Petitioner’s showing. Notably absent from Patent Owner’s analysis is any description of the level of skill that would be required, beyond the definition adopted by the Board, to make the proposed combination. Instead, Patent Owner implicitly accepts the Board’s description of the ordinarily skilled artisan and then faults such artisan for “not necessarily” having sufficient skill to make the proposed combination. Not only is Patent Owner’s

argument equivocal, but it relies on assumptions inconsistent with the definition adopted by the Board. Specifically, our Institution Decision describes the ordinarily skilled artisan as having a “B.S. degree in Electrical Engineering” and “at least 3–5 years of academic or *industry experience in semiconductor integrated circuit field*, or comparable industry experience.” Dec. 9 (emphasis added). As noted above, Dr. Przybylski assumes for his opinion that the ordinarily skilled artisan would have focused on logic design and implementation “*instead of circuit design and the interactions between semiconductor processes and the characteristics of the resulting integrated circuits.*” Ex. 2003 ¶ 127 (emphasis added). But such focus is neither express nor implied in the Board’s description of the ordinarily skilled artisan, which refers broadly to experience in the “semiconductor integrated circuit field.” Neither Patent Owner nor Dr. Przybylski explain the basis for the assumption that the ordinarily skilled artisan would have focused on logic design and, accordingly, would “not necessarily” have had sufficient experience and skill in circuit design to combine the teachings of Urano and Mutoh021. See Ex. 2002 ¶ 127; PO Resp. 34–35.

On the other hand, we are persuaded by, and credit, the testimony of Dr. Holberg, who opines (with evidentiary support) that the ordinarily skilled artisan, within the definition adopted by the Board, would have understood “how to adapt the layout design of an IC, such as an MTCMOS gate array, using well-known layout designs based on known design considerations to achieve low voltage, high-speed operation.” Ex. 1003 ¶ 126; see also *id.* ¶¶ 120–126 (describing how the ordinarily skilled artisan would have applied his/her skills and experience to employ techniques

known in the art to result in the proposed combination) (citing, e.g., Ex. 1017, 1018, 1025, 1027).

Having considered the entirety of the trial record, we find that one of ordinary skill at the time of filing the '614 patent would have been motivated, and able, to combine the teachings of Urano and Mutoh021 to provide “a power switch disposed around said unit cell array and comprised of a plurality of third MOS transistors, each of the third MOS transistors having the second threshold voltage,” as recited in claim 1.

*g. Claims 2 and 3*

Claim 2 depends from claim 1, and adds to claim 1 “wherein said power switch is turned off during standby and turned on when taken active.” Ex. 1001, 6:63–65. Claim 3 depends from claim 2, and recites “wherein parts of said power switch are disposed within said unit cell array.” *Id.* at 6:65–67.

Petitioner persuasively maps the limitations of claim 2 to Urano’s disclosure. Pet. 56–57. In particular, Urano states that “[d]uring operation, the sleep control signal SL is at a low level. Through this, the high [I/O circuit] threshold value MOS transistors M15 and M16 are turned ON,” and “during sleep (when in standby), the sleep control signal is put to a high level, causing the high threshold value transistors M15 and M16 to turn OFF.” Ex. 1008 ¶¶ 12–13; Pet. 57. Thus, Urano teaches the third basic cells 42 used as power supply cells 43 include MOS transistors connected to a sleep control signal.

Patent Owner does not present separate arguments for claim 2.

We find Urano discloses “wherein said power switch is turned off during standby and turned on when taken active,” as recited in claim 2.

Petitioner relies on the combination of Urano and Mutoh021 as teaching the feature recited in claim 3. Pet. 57–58. In particular, Petitioner contends Mutoh021 teaches that the second basic cells 3—power supply cells forming the power switch—can be arranged at all ends vertically and horizontally of the cell array as well as within the cell array. *Id.* at 58–59 (citing Ex. 1013 ¶¶ 15, 31, Fig. 1). Invoking the arguments and reasoning supporting the combination of Urano and Mutoh021 for claim 1, and relying on the testimony of Dr. Holberg, Petitioner argues “it would have been obvious to a POSA to modify the layout of Urano based on the teachings of Mutoh021 to arrange the power switch cells to be located around and within the cell array,” as recited in claim 3. *Id.* at 59 (citing Ex. 1003 ¶ 156).

Patent Owner does not present separate arguments for claim 3.

We find the combination of Urano and Mutoh021 discloses “wherein parts of said power switch are disposed within said unit cell array,” as recited in claim 3, for the reasons expressed by Petitioner. For essentially the reasons noted above regarding claim 1, we also find one of ordinary skill, at the time of the filing of the ’614 patent, would have been motivated, and able, to combine the teachings of Urano and Mutoh021 to achieve the invention of claim 3.

*h. Conclusion regarding claims 1–3*

For all of the foregoing reasons, and after having analyzed the entirety of the record and assigning appropriate weight to the cited supporting evidence, we determine Petitioner has shown by a preponderance of the evidence that claims 1–3 are unpatentable over the combination of Urano and Mutoh021.

*E. Ground 2: Asserted Obviousness of Claims 1–3 over  
Mutoh and Mutoh021*

Petitioner presents Ground 2 as an alternative to Ground 1, and applies in Ground 2 Patent Owner’s construction of “unit cells,” in which the unit cells are not limited to “circuits implemented by a gate array system,” but may include “conventional standard cell[s].” *See* Pet. 59. For this combination, Petitioner relies on Mutoh instead of Urano.

Mutoh discloses a semiconductor IC device—a low power/high speed MTCMOS circuit—which combines MOSFETs with low and high threshold voltages in the same integrated circuit, and uses high-threshold MOSFETs as power switching transistors. Ex. 1005, 848. Petitioner maps the limitations of claim 1 to Mutoh’s disclosure similarly to Petitioner’s mapping of those limitations to Urano, with the exception that Mutoh’s disclosure is based on standard cells, as opposed to a gate array. Pet. 64–75. In particular, Petitioner asserts Mutoh discloses an integrated circuit device (an LSI, “Large Scale Integration”), having a plurality of first MOS transistors (first unit cells) with a low threshold voltage that are arranged in a standard cell array on a chip. *Id.* at 64–67 (citing Ex. 1005, code (57), 848, 850, and Figs. 3, 8 (logic cell)). Petitioner also asserts Mutoh discloses a plurality of second MOS transistors (second unit cells) with a high threshold voltage arranged in a standard cell array on a chip. *Id.* at 68–69 (citing Ex. 1005, 850, Fig. 8 (D flip-flop, or DFF)).

Petitioner maps the “power switch” and “input / output circuit” limitations to the combination of Mutoh and Mutoh021, in a manner similar to Petitioner’s mapping to the combination of Urano and Mutoh021. *See* Pet. 71–75 (citing Ex. 1005, 850, Fig. 8; Ex. 1013 ¶¶ 15, 16). In

particular, Petitioner notes Mutoh discloses power switches on two sides of the standard cell array (Pet. 71–72), whereas Mutoh021 teaches arranging the power switch comprising the second basic cells 3 around all ends vertically and horizontally to be located on all sides of the cell array, as noted *supra* in Section III.D.3.d (*id.* at 72–73). Petitioner also argues Mutoh discloses input/output pads arranged around the unit cell array (Pet. 73–74 (citing Mutoh Fig. 11)), but does not explicitly state that the input/output circuits are “disposed around the unit cell array.” *Id.* at 74. Petitioner contends “Mutoh021 also discloses that “[i]nput/output cell arrays 4 are arranged on the outer periphery to form an interface with outside components.” *Id.* (citing Ex. 1013 ¶ 19). Similar to its arguments for the combination of Urano and Mutoh021, Petitioner argues the ordinarily skilled artisan would have been motivated to combine the teachings of Urano and Mutoh021 to place the power switching MOSFETs and input/output cells of Mutoh on all sides of the unit cell array as disclosed in Mutoh021. Pet. 72, 75; *see also id.* at 59–64.

Patent Owner does not dispute that that the combined teachings of Mutoh and Mutoh021 disclose the claim limitations as Petitioner contends, but challenges Petitioner’s showing premised on an alleged deficient showing of a motivation to combine those references. PO Resp. 35–49. Patent Owner’s arguments are similar to those Patent Owner raises in Ground 1. *See id.*

We need not reach Petitioner’s alternative Ground 2. Petitioner conceded at oral argument that it presented Ground 2 as an “alternative” to Ground 1 and agreed that applying the Board’s construction of “unit cells” in our Institution Decision (not excluding standard cells), the Board need not

reach Ground 2. Tr. 28:12–21. We have applied the same construction of “unit cells” herein as we did in the Institution Decision. *Supra* Section III.C.1; *see* Dec. 13. We have also determined herein that Petitioner has shown by a preponderance of the evidence that claims 1–3 are unpatentable as obvious over Urano and Mutoh021. *Supra* Section III.D. In reaching that conclusion, we have rendered a final written decision on claims 1–3.

In final written decisions both before and after *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018), the Board has declined to reach grounds challenging claims that were already held unpatentable. *See, e.g., Sure-Fire Elec. Corp. v. Yongjiang Yin*, IPR2014-01448, Paper 56 at 25 (PTAB Feb. 22, 2016), *aff’d*, 702 F. App’x 981 (Fed. Cir. 2017); *SK Hynix Inc. v. Netlist, Inc.*, IPR2017-00692, Paper 25 at 40 (PTAB July 5, 2018). The Federal Circuit has acknowledged the Board’s discretion in this regard. *See Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, Nos. 2019-1594, -1604, -1605, 2020 WL 2071962, at \*4 (Fed. Cir. Apr. 30, 2020) (non-precedential) (recognizing that the “Board need not address issues that are not necessary to the resolution of the proceeding” and, thus, agreeing that the Board has “discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”).

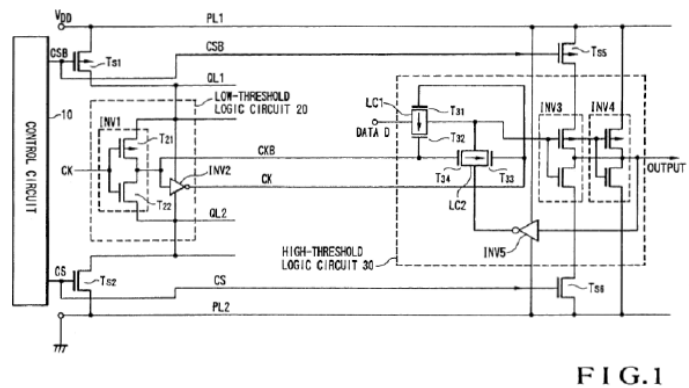
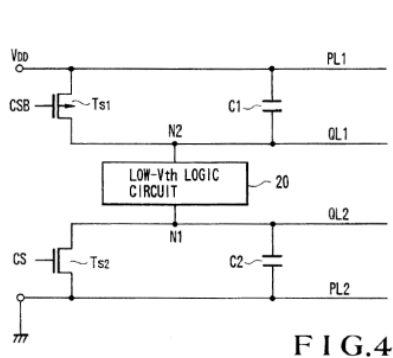
For the foregoing reasons, we determine that it is unnecessary for us to decide whether Petitioner has also shown by a preponderance of the evidence that claims 1–3 would have been obvious based on Mutoh and Mutoh021.

*F. Ground 3: Asserted Obviousness of Claims 4 and 5 over  
Douseki and Ramus*

*1. Overview of Douseki (Ex. 1010)*

Douseki is a U.S. Patent issued on January 23, 1996, more than a year before the priority date of the '614 patent. Ex. 1010, code (45); Pet. 7. Accordingly, Douseki is prior art under 35 U.S.C. § 102(b). Patent Owner does not dispute the prior-art status of Douseki.

Douseki is directed to a semiconductor integrated circuit including multi-threshold transistors and four power lines, and is based on a standard cell configuration. Ex. 1010, code (57), 10:16–40. Figures 1 and 4 of Douseki, reproduced below, illustrate the circuit of Douseki.



Figures 1 and 4 of Douseki, reproduced above, depict “a system diagram showing a logic circuit according to an embodiment of the present invention,” and “a system diagram showing a modification of the present invention,” respectively. Ex. 1010, 1:63–64, 2:5–6.

Douseki discloses a circuit comprising a pair of power source lines (PL1 and PL2 in Figure 4) and a pair of dummy power source lines (QL1 and QL2 in Figure 4). Ex. 1010, 2:39–52, 3:10–16, 5:33–53, Fig. 4. Douseki’s circuit includes a low-threshold logic circuit 20 (in Figure 4)

connected between the pair of dummy power source lines QL1 and QL2, and a high-threshold latch circuit 30 (in Figure 1) connected between the pair of power source lines PL1 and PL2. *Id.* Douseki also teaches a first capacitor C1 connected between power source PL1 and dummy power source line QL1, and a second capacitor C2 connected between power source PL2 and dummy power source line QL2, which are used to reduce power supply voltage variations. Ex. 1010, 5:33–43; Pet. 32–33.

*2. Overview of Ramus (Ex. 1011)*

Ramus is a U.S. Patent that issued on May 20, 1997, more than a year before the priority date of the '614 patent; thus, Ramus is prior art under 35 U.S.C. § 102(b). Ex. 1011, code (45); Pet. 7. Patent Owner does not dispute the prior-art status of Ramus.

Ramus is directed to a semiconductor integrated designed using standard cells. Ex. 1011, code (57). Ramus states that the standard cell array “usually has one or more empty spaces (54) wherein no circuitry is formed.” *Id.* Relying on the testimony of Dr. Holberg, Petitioner contends “Ramus teaches that ‘[t]hese empty spaces may be used to form capacitor standard cells which have capacitors (*see* Figs. 3 and 4) to both ground and power supply lines within the integrated circuit.’” Pet. 33 (quoting Ex. 1003 ¶ 203). Petitioner also argues that Ramus discloses an exemplary capacitor standard cell, shown in Figure 3 reproduced below.

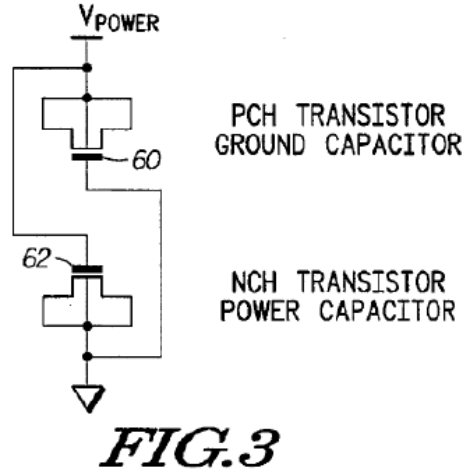


Figure 3 of Ramus, reproduced above, “illustrates, in a circuit schematic, a capacitor circuit standard cell used for reducing signal noise, the cell being in accordance with the present invention.” Ex. 1011, 2:29–31. According to Petitioner, “[a] capacitor standard cell includes both a P-channel transistor and an N-channel transistor,” and “[e]ach transistor is a MOS capacitor with source and drain and body nodes electrically connected together to a first voltage level, and the gate node connected to a second voltage level.” Pet. 33 (citing Ex. 1011, 4:34–5:27, Fig. 3; Ex. 1001 ¶ 204).

### 3. Analysis

Petitioner persuasively maps the limitations of claims 4 and 5 to the teachings of Douseki and Ramus. Pet. 80–92. In particular, Petitioner presents evidence that Douseki teaches “the use of decoupling capacitors between power supply lines to reduce voltage variations,” although Douseki “is silent on the type of decoupling capacitors implemented in its circuit.” Pet. 78 (citing Ex. 1010, 2:38–50, 5:33–53). Petitioner also presents evidence that “Ramus also teaches the use of decoupling capacitors between

power supply lines to reduce voltage variations.” *Id.* (citing Ex. 1011, Abstract).

Relying on the testimony of Dr. Holberg, Petitioner contends Ramus teaches using empty cells in the standard cell array wherein no circuitry is formed to form capacitors between power supply lines within the integrated circuit, and clearly introduces the motivation to do so: “[t]hese capacitors are used to reduce noise in the power and supply lines in a manner more useful/efficient than known methods. The capacitor standard cell taught herein is more useful/efficient due to the fact that the capacitance provided by these standard cells is distributed over the entire integrated circuit in small portions (i.e., standard cells are placed all over the integrated circuit (10)), and is placed close to the logic which is switching. It is the switching logic which is the root of a large portion of internal integrated circuit noise.”

*Id.* at 79 (Ex. 1003 ¶ 207). Further relying on the testimony of Dr. Holberg, Petitioner contends

a POSA would have been motivated to implement the decoupling capacitors in Douseki based on the teachings of Ramus to utilize transistors to form MOS capacitors to achieve this benefit articulated—the capacitors formed by the MOS transistors in the standard cells can be distributed over the entire integrated circuit in small portions, which can efficiently reduce internal integrated circuit noise and increase the voltage stability of each power line.

*Id.* (citing Ex. 1003 ¶ 208).

Petitioner also presents evidence that such modification of Douseki with Ramus would have been “routine” as a combination of known elements “according to known methods to yield predictable results,” and “there would have been a reasonable expectation of success, because such a combination would have been applying a known technique—MOS capacitors—to a

known device—a MTCMOS IC—and for a same purpose—reduce noise and voltage drops in the power supply lines.” *Id.* at 79–80 (citing Ex. 1003 ¶ 209). We find Petitioner’s arguments to be persuasive and to be supported by the cited evidence.

Patent Owner does not challenge Petitioner’s showing as to the individual teachings of the references, but argues Petitioner fails to establish a motivation to combine Douseki and Ramus. PO Resp. 50. In particular, Patent Owner argues Petitioner cannot establish a motivation “to combine Ramus’ teaching of MOS capacitors with the decoupling capacitors of Douseki,” as stated in the Petition (p. 78) because Douseki “never mentions ‘decoupling capacitors.’” PO Resp. 50. This contention is unavailing. Although Douseki may not describe capacitors C1 and C2 explicitly as “decoupling capacitors,” Petitioner presents persuasive evidence that those capacitors perform the function of decoupling capacitors to reduce variations between voltage lines. *See* Pet. 78 (citing Ex. 1010, 2:38–50, 5:33–53).

Patent Owner next argues that, even if Douseki does disclose decoupling capacitors, as Petitioner contends, then both Douseki and Ramus teach the use of decoupling capacitors, in which case the Petition is deficient in failing to explain why a person of skill in the art would have been motivated to combine two references that “disclose common functionality that would be redundant if present in the combination.” PO Resp. 51. Patent Owner’s argument appears to misapprehend Petitioner’s basis for the combination. Petitioner does not propose a circuit that includes both Douseki’s and Ramus’ decoupling capacitors. Rather, Petitioner notes that Douseki teaches decoupling capacitors, but is not specific as to the “type of decoupling capacitors.” Pet. 78. Petitioner then relies on Ramus as

disclosing capacitors comprised of MOS transistors, as recited in claims 4 and 5. *Id.* at 79–80. Thus, Petitioner’s argument introduces no redundancy.

Based on the arguments and evidence presented by Petitioner, we find that one of ordinary skill at the time of filing the ’614 patent would have been motivated, and able, to combine the teachings of Douseki and Ramus to achieve the invention recited in claims 4 and 5, in which MOS transistors are used as capacitors connected between power supply lines.

For all of the foregoing reasons, and after having analyzed the entirety of the record and assigning appropriate weight to the cited supporting evidence, we determine Petitioner has shown by a preponderance of the evidence that claims 4 and 5 are unpatentable over the combination of Douseki and Ramus.

*G. Patent Owner’s Constitutionality Challenges*

Patent Owner contends this proceeding should be terminated because the Board lacks constitutional power to issue a final written decision in this proceeding under the Appointments Clause of the U.S. Constitution. PO Resp. 51–52. In particular, Patent Owner contends “Administrative Patent Judges (APJs) remain unconstitutionally appointed.” *Id.* at 51. We decline to consider Patent Owner’s constitutional challenge as the issue has been addressed by the Federal Circuit in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320, 1328 (Fed. Cir. 2019), *cert. granted sub nom. United States v. Arthrex, Inc.*, 2020 WL 6037206 (Oct. 13, 2020). Although Patent Owner contends the Federal Circuit’s solution in *Arthrex* to the alleged constitutional defect is “insufficient because it does not give a

constitutionally appointed principal officer power to review APJ decisions” (PO Resp. 52), that is not a matter for us to decide.

Patent Owner also argues “[t]he retroactive application of *inter partes* review to patents issued before the enactment of the America Invents Act violates the Due Process clause of the Fifth Amendment. It is also a physical and regulatory taking prohibited by the Takings Clause of the Fifth Amendment.” PO Resp. 52–53. The Federal Circuit has, however, rejected arguments that retroactive application of the AIA is unconstitutional, explaining as follows:

[T]he retroactive application of IPR proceedings to pre-AIA patents is not an unconstitutional taking under the Fifth Amendment. Patent owners have always had the expectation that the validity of patents could be challenged in district court. For forty years, patent owners have also had the expectation that the PTO could reconsider the validity of issued patents on particular grounds, applying a preponderance of the evidence standard. Although differences exist between IPRs and their reexamination predecessors, those differences do not outweigh the similarities of purpose and substance and, at least for that reason, do not effectuate a taking of . . . patents.

*Celgene Corp. v. Peter*, 931 F.3d 1342, 1362–63 (Fed. Cir. 2019). Patent Owner acknowledges the *Celgene* decision, but asserts it was “wrongly decided.” PO Resp. 53. Again, that is not a matter for us to decide.

#### IV. CONCLUSION

For the foregoing reasons, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1–5 of the ’614 patent are unpatentable.

V. ORDER

Accordingly, it is

ORDERED that claims 1–5 of U.S. Patent 6,239,614 B1 are held unpatentable under 35 U.S.C. § 103 as obvious; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of this decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

| Claims                 | 35 U.S.C. § | References                    | Claims Shown Unpatentable | Claims Not Shown Unpatentable |
|------------------------|-------------|-------------------------------|---------------------------|-------------------------------|
| 1–3                    | 103         | Urano, Mutoh021               | 1–3                       |                               |
| 1–3                    | 103         | Mutoh, Mutoh021 <sup>13</sup> |                           |                               |
| 4, 5                   | 103         | Douseki, Ramus                | 4, 5                      |                               |
| <b>Overall Outcome</b> |             |                               | 1–5                       |                               |

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<sup>13</sup> As explained above (Section III.E), we do not reach this ground in light of our determining claims 1–3 are unpatentable on another ground. *See, e.g., Trading Techs.*, 921 F.3d at 1386 (affirming unpatentability on one asserted ground and declining to address unpatentability on an additional ground).

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