

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

AQUILA INNOVATIONS, INC.,
Patent Owner.

Case IPR2019-01526
Patent 6,895,519 B2

Before SALLY C. MEDLEY, DENISE M. POTHIER, and
AMBER L. HAGY, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Denying Patent Owner's Motion to Exclude
37 C.F.R. § 42.64

I. INTRODUCTION

Advanced Micro Devices, Inc. (“Petitioner”)¹ requested an *inter partes* review of all claims (claims 1–11) in U.S. Patent No. 6,895,519 B2 (Ex. 1001, “the ’519 patent”). Paper 2 (“Petition” or “Pet.”), 16. Aquila Innovations Inc. (“Patent Owner”)² filed a Preliminary Response. Paper 10 (“Prelim. Resp.”). With authorization, Petitioner filed a Reply (Paper 11, “Prelim. Reply”), and Patent Owner filed a Sur-reply (Paper 12, “Prelim. Sur-reply”). Pursuant to 35 U.S.C. § 314, we granted the request and instituted *inter partes* review as to all challenged claims on all grounds presented in the Petition. Paper 13 (“Dec. Inst.”). Patent Owner filed a Response (Paper 19, “Resp.”), Petitioner filed a Reply (Paper 24, “Reply”), and Patent Owner filed a Sur-reply (Paper 26, “Sur-reply”).

Patent Owner objected to evidence submitted by Petitioner in its Petition (Paper 16). Patent Owner filed a Motion to Exclude (Paper 31, “Mot. Exclude”), Petitioner filed an Opposition to the Motion to Exclude (Paper 32, “Pet. Opp. Mot. Exclude”), and Patent Owner filed a Reply to support the Motion to Exclude (Paper 33, “PO Reply Mot. Exclude”).

A hearing was held on December 11, 2020, and a transcript of the hearing is included in the record. Paper 36 (“Tr.”).

¹ Petitioner identifies itself and ATI Technologies ULC as the real parties-in-interest. Pet. 4.

² Patent Owner identifies itself, Wi-LAN Technologies Inc., Wi-LAN Inc., and Quarterhill Inc. as the real parties in interest. Paper 6, 2.

We have jurisdiction under 35 U.S.C. § 6(b). For the reasons discussed below, we conclude that Petitioner has shown by a preponderance of the evidence that claims 1–11 of the ’519 patent are unpatentable. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a).

A. Related Proceedings

The parties indicate the ’519 patent is at issue in a pending lawsuit, *Aquila Innovations Inc. v. Advanced Micro Devices*, Case No. 1:18-cv-00554-LY (W.D. Tex. filed July 2, 2018). Pet. 74; Paper 6, 2.

B. The ’519 Patent

The ’519 patent was filed on September 23, 2002, and claims priority to a Japanese application filed on February 25, 2002. Ex. 1001, codes (22), (30). The ’519 patent relates to a system large scale integration (LSI). *Id.* at 1:7–10. The ’519 patent describes an improved system LSI that overcomes various problems in the prior art system LSIs. *Id.* at 3:21–34. The ’519 patent discloses “[a] system LSI dynamically and speedily controls clocks of various frequencies as used in a wide range of operation modes from high-speed to low-speed operation modes, enabling user selection of a system of power consumption type most suitable.” *Id.* at code (57); *see also id.* at 3:23–34.

Figure 2 below shows an LSI:

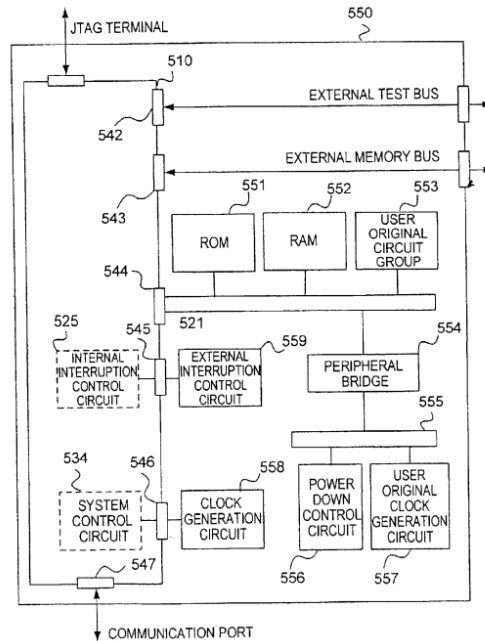


Figure 2, reproduced above, shows a system LSI (e.g., 550) using a CPU. *Id.* at 5:60–61, Fig. 2. LSI 550 includes CPU 510, ROM 551 for storing a clock control library and an application program, system control circuit 534, and clock generation circuit 558. *Id.* at 5:60–61, 6:50–57, 7:9–12, 7:60–67, Figs. 2–4. According to the '519 patent, the LSI's system control circuit 534 and clock generation circuit 558 reduce consumed power without losing the core CPU's versatility. *Id.* at 11:50–54, Figs. 1–5.

The '519 patent's clock control library (e.g., 32 in Figure 6) manages power using an application program (e.g., 31 in Figure 6). *Id.* at 11:61–65, Fig. 6. A main library (e.g., 33 in Figure 6) selects one of the libraries (e.g., 34 in Figure 6) corresponding with the application program's state and permits transitions between clock operating modes. *Id.* at 12:2–5, 12:27–30, Figs. 6, 8(a). Below, Figure 5 illustrates an example of clock operation mode (i.e., eight operation modes STNn (n:integer of 0 through 7)) and the state transitions.

mode (STN3, 31.25 MHz), and (5) a lowest-speed operation mode (STN4, 32.768 MHz). *Id.* at 9:12–17, 9:38–41, 9:49–10:17, Fig. 5.

The '519 patent also describes a prior art microcontroller power management that includes four clock operation modes: high-speed operation mode (operating at 1/2 of the oscillation frequency), low-speed operation mode (operating at 1/4, 1/8, 1/16, and 1/32 of the oscillation frequency respectively), wait mode, and halt mode. *Id.* at 1:63–2:6, 2:61–67, Fig. 10.

C. Illustrative Claim

Petitioner challenges all the claims of the '519 patent. Of the contested claims, claim 1 is the only independent claim, and claims 2 through 11 ultimately depend from claim 1. Below, independent claim 1 illustrates the claimed subject matter:

1. A system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit, comprising:

a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes [“limitation 1.1”];

a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library [“limitation 1.2”];

a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit [“limitation 1.3”]; and

a second memory that stores an application program, wherein calling of said clock control library and changing of said register value are programmably controlled by said

application program to enable user selectable clock frequency transitions [“limitation 1.4”],

wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted [“limitation 1.5”].

Ex. 1001, 14:15–47.

D. Instituted Grounds of Unpatentability

We instituted *inter partes* review of all challenged claims based on all grounds of unpatentability asserted in the Petition, which are as follows:

Claims Challenged	35 U.S.C. §	References
1, 7, 10, 11	103(a) ³	Ober, ⁴ Nakazato ⁵
2–6	103(a)	Ober, Nakazato, Cooper, ⁶ Windows ACPI ⁷
8, 9	103(a)	Ober, Nakazato, Doblar ⁸

Dec. Inst. 2, 69; Pet. 3–4.

³ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. § 103. Changes to § 103 apply to applications filed on or after March 16, 2013. Because the ’519 patent has an effective filing date before March 16, 2013, we refer to the pre-AIA version of § 103.

⁴ US 6,665,802 B1, issued Dec. 16, 2003 and filed Feb. 29, 2000 (Ex. 1004).

⁵ US 6,681,336 B1, issued Jan. 20, 2004 and filed June 16, 2000 (Ex. 1008).

⁶ US 6,823,516 B1, issued Nov. 23, 2004 and filed Aug. 10, 1999 (Ex. 1007).

⁷ Microsoft Corporation (1998), *Microsoft Hardware White Paper, Draft ACPI Driver Interface Design Notes and Reference* (Version 0.91), Redmond, WA (Ex. 1005).

⁸ US 6,516,422 B1, issued Feb. 4, 2003 and filed May 27, 1999 (Ex. 1006).

II. DISCUSSION

A. Principles of Law

To prevail in its challenges to Patent Owner’s claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e) (2012); 37 C.F.R. § 42.1(d) (2018). A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

B. Level of Ordinary Skill in the Art

Petitioner describes the level of ordinary skill as follows:

[a] person of ordinary skill in the art . . . would have a B.S. degree in Electrical Engineering, Computer Engineering, or an equivalent field as well as at least 3 to 5 years of academic or industry experience in computer systems architecture or computer chip design, or comparable industry experience.

Pet. 16. The testimony of David H. Albonesi, Ph.D (Ex. 1003, “Albonesi Declaration”) presents a similar level of ordinary skill. Ex. 1003 ¶ 35.

Patent Owner does not set forth an ordinary artisan’s skill level.

See generally Resp. The testimony of Steven A. Przybylski, Ph.D. (Ex. 2005, “Przybylski Declaration”) states that he “do[es] not necessarily agree with the definition offered” but is “applying the definition of the level of experience of a person of ordinary skill in the art that has been put forward by Dr. Albonesi in his declaration (¶ 35).” Ex. 2005 ¶ 32.

Having reviewed the arguments and evidence in the full record, we adopt Petitioner’s definition above, as we did initially in the Institution Decision, as is consistent with the ’519 patent and the asserted prior art.

C. Claim Construction

In this *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claims in a civil action under 35 U.S.C. § 282(b). *See* 37 C.F.R. § 42.100(b) (2019). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005).

1. The Preamble

Petitioner proposes that we construe the term “system LSI” in the preamble of claim 1 to mean “a ‘single integrated chip, which has a CPU memory, and I/O capability.’” Pet. 14. Petitioner states that the ’519 patent confirms the system LSI includes memory, a CPU, and I/O capabilities. *Id.* (citing Ex. 1001, 5:58–61, 12:34–37, Fig. 2). Relying on Dr. Albonesi’s testimony, Petitioner further states an ordinarily skilled artisan would have had the same understanding. *Id.* (citing Ex. 1003 ¶ 77). Later, Petitioner states “to the extent the preamble is determined as limiting” (Pet. 25), implying that claim 1’s preamble may not be limiting. *See id.*

Patent Owner asserts that the preamble, “[a] system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit” (Ex. 1001, 14:15–19), is limiting because the preamble is “an essential element of the invention.” Resp. 21–22 (citing *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 952 (Fed. Cir. 2006)). Patent Owner additionally states that the preamble provides antecedent bases for the recitations “ordinary operation modes,” “special modes,” and “central processing unit” found in claim 1’s body, and thus the preamble “is a necessary component of the claimed invention.” *Id.* at 22 (citing *Bicon*, 441 F.3d at 952). Patent Owner further contends that “[a] person of ordinary skill in the art would understand ‘a plurality of ordinary operation modes’ to require that the CPU execute instructions at different frequencies.” *Id.* at 24; *see also id.* at 22–25 (citing Ex. 1001, 4:12–18, 8:56–65, 11:34–38, 12:37–45, 13:54–60, Fig. 5; Ex. 2005 ¶ 35), 27.

Petitioner responds that we need not decide whether the preamble is limiting because its recitations are not relevant to the obviousness challenge; rather, Petitioner contends the parties' dispute relates to whether Ober and Nakazato disclose changing a CPU's clock frequency or operating at different frequencies. Reply 2–3. Patent Owner does not further address the construction of claim 1's preamble in the Sur-reply. *See generally* Sur-reply.

Upon considering Petitioner's and Patent Owner's arguments and evidence, we find that the preamble is limiting. Recitations to the "ordinary operation modes" and "central processing unit," as noted by Patent Owner (Resp. 22), are found in both claim 1's preamble (Ex. 1001, 14:15–17) and claim's 1 body (*id.* at 14:21–22, 14:25, 14:28, 14:32–33). Claim 1's "ordinary operation modes" and "central processing unit" recitations in its body thus rely upon and derive antecedent basis from claim 1's preamble, and these recitations in the preamble are essential elements that give meaning to claim 1's invention. *See Bicon*, 441 F.3d at 952.

We further find claim 1's preamble requires "clock frequencies" be "supplied to a central processing unit" because the preamble recites "a plurality of ordinary operation modes . . . in response to clock frequencies supplied to a central processing unit." Ex. 1001, 14:17–18. However, we do not find claim 1's preamble requires the central processing unit (CPU) executes instructions or that the "clock frequencies" differ. Ex. 1001, 14:15–19. No recitation that the CPU *execute instructions* is found in the preamble.

Nor do we agree with Patent Owner that this limitation requires the "clock frequencies" to differ. *See* Resp. 23–25. As support for that

proposition, Patent Owner points to, *inter alia*, the testimony of Petitioner’s declarant, Dr. Albonesi, to the effect that claim 1’s “ordinary operation modes” have two requirements and “the claimed ordinary operation modes operate at different frequencies.” *See, e.g., id.* at 23 (citing Ex. 1003 ¶ 102). We find, however, that Dr. Albonesi’s statement that the “ordinary operation modes” operate at different frequencies refers to the recitation the ““clock frequency transition[s]’ occur between said ordinary operation modes” in the “first memory” limitation of claim 1, not the preamble’s recitation that the “clock frequencies [are] supplied to a central processing unit.” Ex. 1003 ¶ 102. We thus disagree with Patent Owner that Petitioner’s evidence supports construing the “plurality of ordinary operation modes . . . supplied to a central processing unit” in claim 1’s preamble such that the CPU executes instructions at various frequencies as argued. We will address Patent Owner’s assertions related to varying a clock signal’s frequency further below when discussing the “first memory” limitation.

Also, the passages in the ’519 patent cited by Patent Owner do not define or explain the phrase “plurality of ordinary operation modes” as having a customary meaning, such that its construction should be limited to a CPU that executes instructions at different frequencies, as asserted by Patent Owner. *See, e.g.,* Ex. 1001, 4:12–18, 8:56–65, 11:34–38, 12:37–45, 13:54–60, *cited in* Resp. 23–25. Notably, the ’519 patent uses the term “instructions” twice but not when discussing a CPU executing instructions at different frequencies. *See id.* at 6:23–26, 7:38–42. The Specification addresses “control[l]ing a plurality of clocks in the ordinary operation mode” (*id.* at 4:16, 13:59; *see id.* at 8:60–61) and “control[ling] the clock with a lot of frequencies covering the wide range of the operation modes

from the high-speed operation mode to the low-speed operation mode based on the concept of the clock gear” (*id.* at 11:35–39; *see id.* at code (57)). For example, the ’519 patent provides details how this may be achieved, including using “a function (clkgear)” (*id.* at 4:14, 9:4–6) or “Clock Gear” to transition to the clock state and designating values in memory when changing gears (*id.* at 12:37–45). But claim 1, including its preamble, does not recite these details, including a CPU executing instructions at different frequencies.

Dr. Przybylski attempts to distinguish ordinary operation modes from special modes based on disclosure in the Specification, contending “[a] POSITA^[9] reviewing the ’519 patent would understand that central to the distinction between ordinary operation modes and the special modes is the execution of instructions in the former and the absence of execution in the latter.” Ex. 2005 ¶ 35 (citing Ex. 1001, 1:20–26, 1:63–2:9, 4:7–11, 7:28–37, 9:12–17, 9:46–10:17, 10:30–11:5, 13:14–53, 19:7–17, 19:19–26, 19:46–10:17, 10:30–11:5, Figs. 5, 10). We disagree that the ’519 patent makes such a distinction. The ’519 patent describes some examples of “operation modes” where the CPU does not execute instructions, such as the “wait mode” where “the clock of the CPU is halted.” Ex. 1001, 2:3; *see* Ex. 2005 ¶ 35 (citing Ex. 1001, 1:63–2:9). Both Petitioner (Tr. 34:2–6) and Patent Owner (*id.* at 50:9–20) acknowledged during oral hearing that “wait mode,” such as the one addressed in Ober’s column 10, is an ordinary operation mode. *See also* Ex. 1001, 10:10–17 (describing a wait mode as one where “the clock supply to the system is not completely halted”). In contrast, claim

⁹ A person of ordinary skill in the art.

1 of the '519 recites “a first special mode in which a clock supply *to principal constituents* of said central processing unit is halted” (*id.* at 14:41–43; *see also* Ex. 1003 ¶ 84, *cited in* Pet. 14), such that an ordinarily skilled artisan would infer that instructions can still be executed by other constituents of the CPU in special modes. We thus do not give substantial weight to Dr. Przybylski’s testimony in this regard.

Lastly, in the Decision to Institute, we interpreted “system LSI” in the preamble to require “the elements of the claims reside on a chip.” Dec. Inst. 9. Neither party has indicated that our interpretation was improper and we do not find any reason or evidence that now compels any deviation from this interpretation.

Therefore, we determine the preamble is limiting but does not require the CPU to execute instructions at different frequencies. We further determine the recited “system LSI” in the preamble requires the elements of the claims to reside on a chip.

2. “[A] clock frequency transition between said ordinary operation modes”

Petitioner states “ordinary operation modes” as recited in claim 1 has two requirements, including that the “‘clock frequency transition[s]’ occur between said ordinary operation modes.” Pet. 24 (citing Ex. 1001, 14:20–22; Ex. 1003 ¶ 102). Dr. Albonesi similarly testifies “claim 1 requires: (1) that clock frequency transitions occur between ordinary operation modes . . . EX1001, 14:20-22. To state it another way, the claimed ordinary operation modes operate at different frequencies.” Ex. 1003 ¶ 102. Patent Owner states that “claim 1 requires clock frequency transitions between the ordinary operation modes. Petitioner also correctly notes that the ordinary operation modes ‘operate’ at different frequencies.” Resp. 23; *id.* at 22–23.

We agree with both parties that the recitation “clock frequency transition between said plurality of ordinary operation modes” in the “first memory” recitation requires the ordinary operation modes to operate at different frequencies. The “first memory” recitation in claim 1 recites “a clock frequency transition,” which implies the clock frequency undergoes a change (e.g., differs) between ordinary operation modes and thus operates at different frequencies between the ordinary operation modes. *See* Ex. 1003 ¶ 102; *see also* Ex. 2005 ¶ 36. However, we find that the recitation “said ordinary operation modes,” for reasons stated above when addressing the preamble (§ II(C)(1)), does not require the CPU to execute instructions at different frequencies.

3. “[A] clock control library”

Petitioner argues the phrase “a clock control library” should be given “Patent Owner’s construction of this term from the district court proceeding, which is ‘software that controls the change in the frequency of the clock signals in the ordinary operation modes.’” Pet. 15 (citing Ex. 1011, 7). Patent Owner does not, in this proceeding, offer a construction of this phrase. *See generally* Resp. For purposes of this Final Written Decision, we determine that we need not provide an express construction for the phrase “clock control library.” That is, as our reviewing court has held, “only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.” *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Technologies* in the context of an *inter partes* review).

In sum, we agree the recited “clock frequency transition between said plurality of ordinary operation modes” in the “first memory” recitation requires the ordinary operation modes to operate at different frequencies. We need not determine whether the proper construction of the phrase “clock control library” requires software that controls the frequency change of clock signals in ordinary operation modes.

4. Remaining Terms

Petitioner also provides constructions for the phrase “principal constituents of said central processing unit” found in claim 1. Pet. 15. Patent Owner does not construe this phrase. *See generally* Resp. For purposes of this Final Written Decision, we determine that we need not provide an express construction for this or any other claim terms. *See Nidec Motor Corp.*, 868 F.3d at 1017.

D. Obviousness of Claims 1, 7, 10, and 11 Over Ober and Nakazato (Ground 1)

1. Ober (Ex. 1004)

Ober is a United States patent issued on December 16, 2003, and filed on February 29, 2000. Ex. 1004, codes (22), (45). According to Petitioner, Ober is prior art under 35 U.S.C. § 102(e). Pet. 12. Patent Owner does not dispute Ober’s prior-art status. Ober describes a power management system for a microcontroller or System on Chip (SoC) having different subsystems. Ex. 1004, code (57), 3:45–47. Ober’s Figure 1 below shows a power management architecture for a microcontroller or SoC.

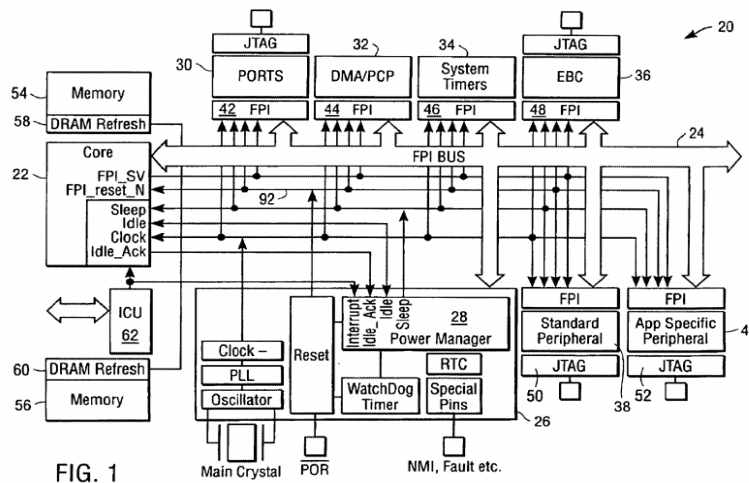


Figure 1 above shows a power management architecture for a SoC. *Id.* at 3:22–26, Fig. 1. Figure 1 shows a microcontroller that includes CPU core 22, flexible peripheral interconnect (FPI) bus 24, power management subsystem 26, major subsystems 30–40, FPI peripheral interface 42–52, and memory banks 54 and 56. *Id.* at 5:28–53, Fig. 1. CPU core 22 is coupled to a system bus (e.g., 24) “to enable the operating system or application program to read and write the SFR^[10] register in the power management state machines as well as the SFRs in each of the FPI peripheral interfaces for each of the subsystems.” *Id.* at 5:31–37, Fig. 1.

Ober’s power management subsystem 26, illustrated in more detail in Figure 2, includes a machine for controlling a central processing unit’s (CPU) power mode. *Id.* at code (57), 3:28–30, 5:38–40, 17:1–5, Figs. 2, 6. Ober states the power management subsystem may provide “four power modes or states: RUN; IDLE; SLEEP; and DEEP SLEEP.” *Id.* at 4:16–19; *id.* at 7:65–67, 15:14–16:67, Fig. 6. Table 8 shows the system’s configuration during RUN, IDLE, and SLEEP modes (*id.* at 12:41–13:42),

¹⁰ Special Function Register.

and Table 9 summarizes the power modes, including RUN, IDLE, SLEEP (distributed clock) and (no distributed clock), and DEEP SLEEP (*id.* at 13:45–15:10).

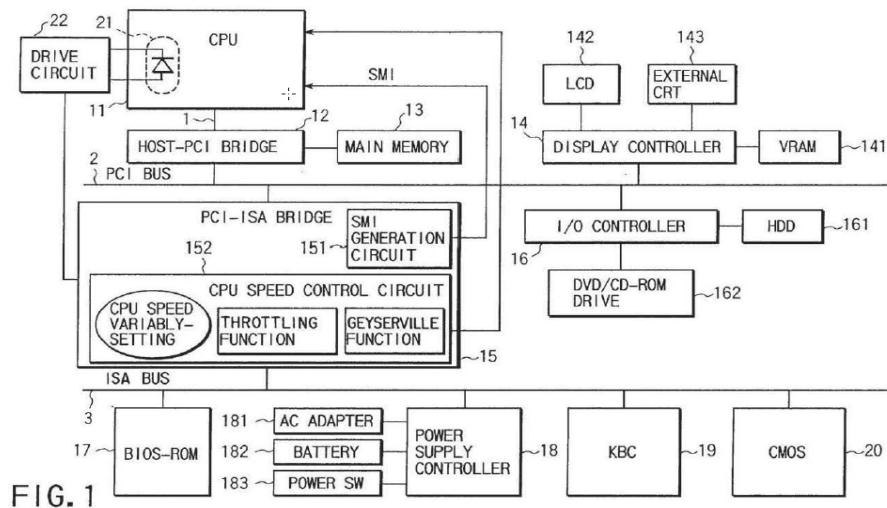
Power management subsystem 26 includes power manager 28 with a power management state machine, programmable SFR register 62, and clock subsystem 64 for generating a system clock signal. *Id.* at 5:58–64, Fig. 2. Ober’s SFR register 62 allows the power management system to be configured for specific applications and is illustrated in Figure 5. *Id.* at 10:10–13, Figs. 2, 5. The bits’ definitions for SFR register 62 are shown in Table 5 and include SlpClk (Sleep clock), which may be divided by 2, 4, or 128 “during Sleep.” *Id.* at 10:13–11:12, Fig. 5. Each subsystem 30–40 also has a separate SFR register (e.g., 116 in Figure 4), which allows the operating system (OS) to control the subsystems during different power modes. *Id.* at 9:20–25, 9:49–51, Fig. 1. The bits’ definition for registers 116 are shown in Table 4. *Id.* at 9:27–47, Fig. 4. “A sleep divide clock (SDCLK) bit and a divided clock (DIVCLK) bit either disables or provides divided clock signal to the subsystem during a SLEEP mode and also may provide a divided clock signal to the subsystem during a normal mode.” *Id.* at 9:65–10:2.

Ober’s clock subsystem 64 may be configured by SFR register 62. *Id.* at 9:4–7. Clock subsystem 64 generates system and management clock signals. *Id.* at 8:52–55, Fig. 3. Main crystal 84 connects to system oscillator 104 to generate an oscillation frequency. *Id.* at 8:58–61, Figs. 2–3. Phase lock loop (PLL) 106 locks in the oscillation frequency, while clock circuit 108 divides the oscillation frequency to provide the system clock frequency. *Id.* at 8:61–64, Fig. 3. The system clock signal may be generated by main

oscillator 84/PLL or shut down. *Id.* at 9:6–8. Management clock 110 can be derived from three sources, including real time clock (RTC) oscillator 114 connected to the 32 kHz crystal 86, system clock oscillator 104, or system clock signal. *Id.* at 8:66–9:3.

2. Nakazato (Ex. 1008)

Nakazato is a United States patent issued on January 20, 2004, and filed on June 16, 2000. Ex. 1004, codes (22), (45). According to Petitioner, Nakazato is prior art under 35 U.S.C. § 102(e). Pet. 12. Patent Owner does not dispute Nakazato’s prior-art status. Nakazato’s Figure 1, reproduced below, discloses a computer system.



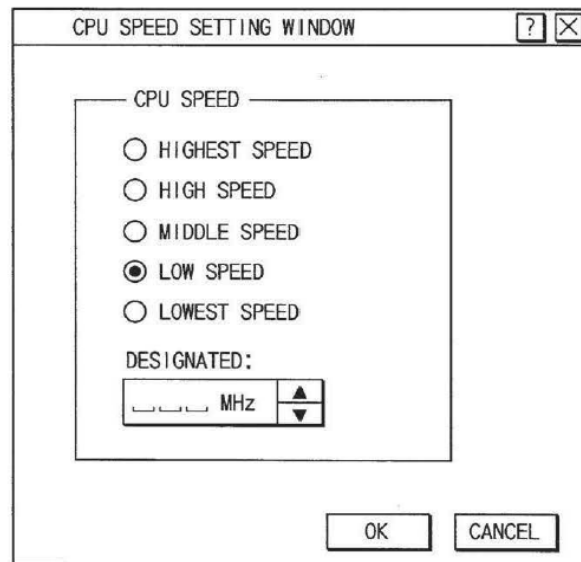
Nakazato’s Figure 1, above, shows a computer system. Ex. 1008, 3:5–7, Fig. 1. The above computer system includes CPU 11, main memory 13, drive circuit 22, and CPU speed control circuit 152. The OS and various programs are loaded in main memory 13. *Id.* at 4:11–20, Fig. 1.

CPU speed control circuit 152 controls the CPU’s processing speed. *Id.* at 5:44–52, Fig. 1. CPU’s processing speed can be controlled at different levels using a CPU throttling function and a GEYSERVILLE function. *Id.*

at 4:20–24. For switching CPU speed, the throttling controller uses the CPU throttling function, and the frequency/voltage controller uses the GEYSERVILLE function. *Id.* at 5:45–6:18. With either function, the CPU speed can be switched by writing necessary data in the internal register of CPU speed control circuit 152. *Id.* at 6:19–21.

A power-saving driver/program, running on the OS, executes CPU speed control circuit 152 and its variable setting of the CPU's processing speed. *Id.* at 7:2–6. The power-saving driver controls CPU speed control circuit 152 through BIOS or directly without BIOS. *Id.* at 7:13–15.

The user designates the CPU speed level using the power-saving driver. *Id.* at 4:25–26, 7:16–19. A dedicated program, such as a program-saving utility, presents the user with a window, such as shown in Figure 2 below.



Nakazato's Figure 2, above, shows a CPU speed-setting window. *Id.* at 3:8–9, 7:19–24, Fig. 2. The selected CPU processing speed is recorded in a predetermined area (e.g., a registry area) of HDD 161, and the power-saving driver can refer to this area. *Id.* at 7:24–27, 9:34–39.

Nakazato describes examples of the CPU processing speed changing. For example, Nakazato states: (1) the CPU processing speed changes from the highest speed to a low speed when the user designates a low speed, (2) the CPU processing speed is maintained as the highest speed when the user designates a highest speed, and (3) the processing speed changes depending on the presence/absence of the AC adapter when the user sets a low speed for battery operation and a high speed for an operation by an external AC power supply. *Id.* at 7:64–8:4.

3. Discussion

In Ground 1, Petitioner contends claims 1, 7, 10, and 11 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ober and Nakazato. Pet. 16–51. We are persuaded Petitioner has established, by a preponderance of the evidence that claims 1, 7, 10, and 11 are unpatentable on this ground.

(a) Claim 1

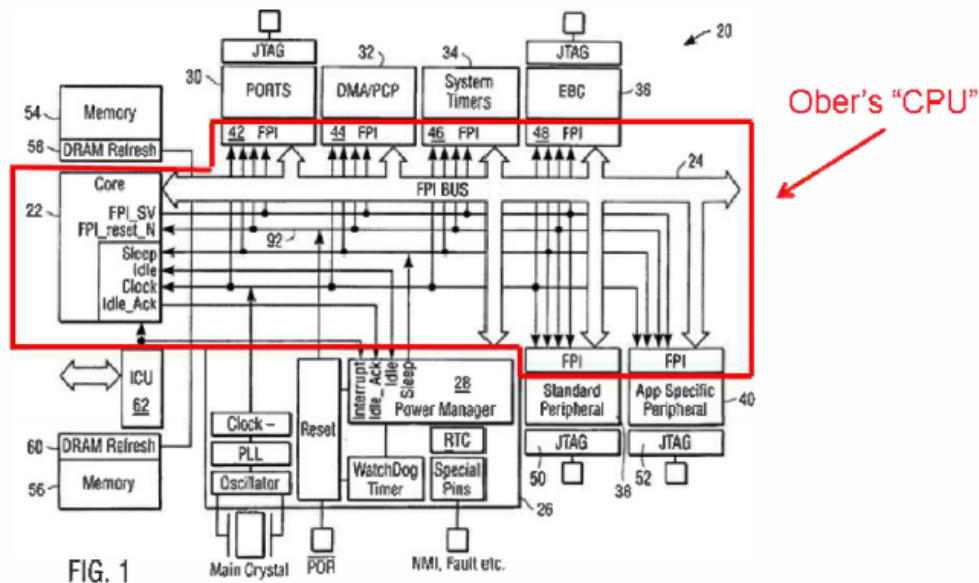
(i) Preamble

Claim 1 recites “[a] system LSI having a plurality of ordinary operation modes and a plurality of special modes in response to clock frequencies supplied to a central processing unit.” Ex. 1001, 14:15–17. As stated in the Claim Construction section, we do not construe this limitation to require the ordinary operation modes to operate at different frequencies or that the CPU executes instructions at different frequencies. Thus, arguments made by Patent Owner in this regard are unavailing. *See* Resp. 13, 27 (stating “nothing in Ober is sufficient to meet that requirement” of “the ordinary operation modes of the ’519 patent operate at different speeds”), 29, 32; *see also* Sur-reply 10–11 (citing Ex. 2005 ¶ 42).

Petitioner contends that Ober teaches or suggests this limitation. Pet. 16–17, 19–25. Petitioner contends that Ober discloses a “system LSI” as a microcontroller or System on Chip (SoC) that can be used with different subsystems, including input/output ports 30 and memory banks 54 and 56. *Id.* at 19–20 (citing Ex. 1003 ¶ 93; Ex. 1004, 3:45–51, 5:41–53) (reproducing Ex. 1004, Fig. 1); *see also* Ex. 2005 ¶ 33 (noting “[t]he ’519 patent is about power management in an integrated circuit, also known as an ‘LSI,’ comprising a variety of different subunits”). Petitioner also contends Ober includes a power management subsystem that can be configured into various power modes that correspond to the recited “plurality of special modes” in the preamble, such as an “IDLE mode” and a “SLEEP MODE (Clock Not Distributed)” where the power optionally can be turned off to most or all subsystems. Pet. 7–8, 16–17 (referring to Section IV.1), 24–25 (citing Ex. 1004, 15:14–16, 16:12–15, 16:19–24). Petitioner also indicates the ’519 patent admits “special operation modes” were known. *Id.* at 4 (citing Ex. 1002, 357–358). Patent Owner does not dispute Petitioner’s showing with respect to the recited “system LSI” and “plurality of special modes.” *See generally* Resp.

We find that Ober teaches the recited “system LSI” and “a plurality of special modes” in the preamble. Specifically, Ober discloses a System on Chip (SoC) or microcontroller that can be used with different subsystems (e.g., 26, 30–40, 52, 54) and core 22. Ex. 1004, 3:45–51, 5:20–53, Fig. 1. Ober further discloses at least two modes (e.g., “IDLE mode” and “SLEEP MODE (Clock Not Distributed)”), which are special modes consistent with the ’519 patent. Ex. 1004, 15:13–36, 16:8–44; *see, e.g.*, Ex. 1001, 10:28–11:5.

Regarding the “central processing unit” in claim 1’s preamble, Petitioner asserts Ober’s SoC includes a “central processing unit” as the term is described in the ’519 patent, which includes a CPU that has a core CPU attached to external devices. Pet. 20–21 (citing Ex. 1001, 6:17–49) (reproducing Ex. 1001, Fig. 1). Petitioner identifies Ober’s CPU below in annotated Figure 1:



Ober’s Figure 1 above, as annotated by Petitioner, identifies Ober’s CPU in red. *Id.* at 22 (reproducing Ex. 1004, Fig.1 (annotated)).

Petitioner contends the ’519 patent describes the CPU (e.g., 510 in Exhibit 1001’s Figure 1) as including a processor (e.g., 511) with a core CPU 512 and caches 511 and 513, various buses (e.g., 521, 531), and other constituents (e.g., elements 520, 522, 523–525, 530, 532–534, 542–546), which include interfaces to other components (e.g., terminals 544–546). *Id.* at 20–22 (citing Ex. 1001, 6:17–49) (reproducing Ex. 1004, Fig. 1). Petitioner argues, “the CPU of the ’519 patent includes a CPU core, caches, and a data bus.” *Id.* at 22. Petitioner further asserts Ober’s CPU “has nearly

identical components as the CPU of the '519 patent” and an ordinarily skilled artisan would have understood that Ober discloses the claimed “central processing unit.” *Id.* at 22; *id.* at 22–23 (citing Ex. 1003 ¶¶ 98–99; Ex. 1004, 5:28–31, 5:38–57).

Patent Owner does not dispute directly Petitioner’s arguments or evidence regarding the recited the “central processing unit.” *See generally* Resp.; *see also* Reply 9 (stating “PO doesn’t challenge AMD’s identification of Ober’s CPU”). Dr. Przybylski, however, testifies:

In the art, the terms “processor”, “central processing unit”, “CPU”, and “core” are used somewhat interchangeabl[y]. In the '519 [patent], the usage though is clear Specifically, the processor 511 is a top-level structure that includes a core CPU 512 for executing instructions and at least the first level caches 513 and 514.

Ex. 2005 ¶ 33 n.1.

Having considered the evidence by both parties, we find Ober’s CPU as identified in the above-annotated Figure 1 (Pet. 22) teaches the “central processing unit” in claim 1. Notably, Dr. Przybylski states the terms “processor,” “central processing unit,” and “core” are *somewhat* interchangeable in the art but provides no further evidence of this assertion. *Id.* Dr. Przybylski further states the processor includes a core and caches, which supports that a core is not the same as a processor. *Id.* Also, the '519 patent’s Specification supports our determination by describing and showing CPU 510 as including processor 511, which further includes core CPU 512, bridges (e.g., 520, 530), buses (e.g., 521, 531), and circuits (e.g., 523, 525). Ex. 1001, 6:17–36, 44–46, Fig. 1.

As for “a plurality of ordinary operation modes . . . in response to clock frequencies supplied to a central processing unit” in the preamble, Petitioner contends Ober teaches or suggests this claimed features. Pet. 16–17, 24–25, 27. Petitioner argues Ober discloses a microcontroller architecture that includes a power management system with a configurable power management state machine to control the CPU’s power modes. Ex. 1004, 3:52–56, *cited in part in* Pet. 19. Petitioner asserts Ober discloses changing CPU clock frequency by dividing the CPU clock and, more specifically, one configurable state in Ober’s power management system “referred to as a ‘Divided clock’ signal.” Pet. 24 (citing Ex. 1004, 9:65–10:2); *id.* at 7–8 (citing Ex. 1004, 9:65–10:2; Ex. 1003 ¶ 65), 16 (referring to Section IV.1¹¹). Petitioner contends this divided clock signal “enables Ober’s ‘clock subsystem’ to provide divided (i.e. lower frequency) clock signals to Ober’s CPU instead of the normal clock signals.” *Id.* at 24 (citing Ex. 1003 ¶ 102; Ex. 1004, 9:65–10:2); *see id.* at 7 (citing Ex. 1004, 9:65–10:2; Ex. 1003 ¶ 65), 26–27. Petitioner further asserts that the “divided clock” concept in Ober causes Ober’s CPU to execute at various frequencies related to the division in the divided clock signal. *Id.* at 24 (citing Ex. 1003 ¶ 103; Ex. 1004, 8:58–64, 15:60–63). Petitioner points to an example in Ober that describes dividing the system clock by 2, 4, or 128, and explains that the system can supply a divided clock signal during “normal operating mode.” *Id.* at 24–25 (citing Ex. 1004, 9:65–10:2, 11:8–13), 27 (citing Ex. 1004, 11:5–13). Petitioner also contends “a POSITA would have found it

¹¹ Section IV.1 is located on pages 6–8 of the Petition and describes Ober.

obvious to use a similar mechanism as is used during SLEEP mode” “during normal operations.” *Id.* at 27 (citing Ex. 1003 ¶ 112).

Petitioner further asserts that Ober recognizes that adjusting the CPU modes during normal operations (e.g., “a plurality of ordinary operation modes”) was “well-known.” *Id.* at 27 (citing Ober 2:17–20). Petitioner indicates the ’519 patent describes a prior-art ST7 clock control circuit when addressing related art in its Background of the Invention section. Pet. 3 (citing Ex. 1001, 1:56–2:2). Petitioner also contends the ’519 patent indicates the ST7 ordinary operation could be controlled by software, suggesting a program “for controlling a clock frequency transition between . . . ordinary operation modes” as recited in limitation 1.1. Pet. 4 (citing Ex. 1001, 3:6–10); *see id.* at 26–27 (discussing SFR 62 to control frequency adjustments).

Patent Owner argues Ober does not disclose “a plurality of ordinary operation modes” as recited in the preamble of claim 1. Resp. 27–36. Many of Patent Owner’s arguments are premised on the contention that Ober does not teach its CPU core executes instructions at different frequencies. *See id.* at 27, 29, 32, 35. However, as we determine above in construing the preamble, executing instructions at different frequencies is not required by claim 1. Similarly, Patent Owner argues that Ober only operates at a single frequency (*see id.* at 27–28, 33–34, 36), which we also determine above is not excluded from the language in claim 1’s preamble. Ex. 1001, 14:15–17. We return to these arguments when addressing the “first memory” limitation below.

Aside from the above arguments, Patent Owner asserts that Petitioner “mischaracteriz[es] Ober’s teachings related to the clock subsystem

supplying the divided clocks to each of the peripherals.” Resp. 28. Patent Owner identifies several of Petitioner’s statements as supposedly contradicting Ober, including: (1) “Ober explains that its system can supply a divided clock signal during ‘normal operating mode’” (*id.* (citing Pet. 24-25); *see id.* at 29 (citing Ex. 1003 ¶ 29)); (2) “Ober’s CPU clock can operate at a variety of frequencies corresponding to the divided clock signal” (*id.* (citing Ex. 1003 ¶ 103); *see id.* at 32–36 (citing Ex. 1004, 2:17–20, 8:53–54, Table 7, 17:15–26; Ex. 2005 ¶¶ 44, 48, 51, 56, 60, 73–74)); and (3) “Ober discloses ‘adjusting the CPU during SLEEP mode’ and changing the speed of the CPU” (*id.* at 29 (citing Ex. 1003 ¶ 111; Pet. 27 (citing Ex. 1004, 11:31-33 and 15:60-63))). *Id.* at 28–29. Patent Owner further argues columns 9 and 10 in Ober, cited by Petitioner, refer to SFR 116 of peripheral interfaces, not the CPU, its core, or SFR 62. *Id.* at 29–31 (reproducing Ex. 1004, Fig. 4) (citing Ex. 1004, 9:22–25, 10:20–30, Figs. 1, 4; Ex. 2005 ¶¶ 69, 70, 76).

Having considered the arguments and evidence by both parties, we find Ober teaches or suggests “a plurality of ordinary operation modes . . . in response to clock frequencies supplied to a central processing unit” as recited in the preamble. Ober states “[i]n general, power management techniques at the microcontroller level are known to utilize centralized control to control the power to the central processing unit (CPU) by reducing the speed or stopping the system clock.” Ex. 1004, 2:17–20 (emphasis added), *cited in* Pet. 27. Dr. Albonesi and Dr. Przybylski also acknowledge that adjusting frequencies of a CPU during the computer’s normal operations were known. Ex. 1028 ¶ 17 (citing Ex. 1004, 2:17–20); *see* Ex. 1029, 54:20–55:2, 62:8–63:5), *cited in* Ex. 1028 ¶ 17. We further find that the

'519 patent also describes a prior-art ST7 core's "conventional clock operation modes," which include changing or adjusting a CPU's clock frequency to achieve the operation modes (e.g., high-speed and low-speed modes), further demonstrating that an "LSI system having a plurality of ordinary operation modes . . . supplied to a" CPU was within the general knowledge of an ordinarily skilled artisan. *See* Ex. 1001, 1:56–2:2, *cited in* Pet. 3; *see also* Ex. 1003 ¶¶ 52–53 (citing Ex. 1001, 1:56–62, 1:65–2:2) (indicating that the '519 patent describes a prior-art ST7 clock circuit with ordinary operation modes resulted from a divided clock).

Additionally, Ober discloses that a clock subsystem (e.g., 64) has the ability to generate different frequencies or speeds during ordinary operation modes. Ex. 1004, 8:58–64, Fig.3 Although discussed in the context of a SLEEP mode, Ober discloses its CPU can configure any reduced speed through SFR 62's register bits (e.g., *id.* at 19:16, 26:24) by using its ClkSrc bits and sleep clock bits, which further discusses a divided system clock. *Id.* at 10:37–53 (Table 5), 11:1–13 (Table 5), 15:60–63. Also, although discussed when addressing SFR 116 and subsystems 30–40, Ober further describes using clock bits to provide a divided clock signal during a normal mode." *Id.* at 9:65–10:2; *see also* Pet. 27 (noting Ober teaches providing a divided clock signal to a subsystem during normal mode and suggests using this technique to supply Ober's CPU during normal operations), *cited in* Reply 8. Dr. Albonesi further testifies, and we credit this testimony, that "a POSITA would have found it obvious to use a similar a mechanism as is used during SLEEP mode based on the teachings of Ober." Ex. 1003 ¶ 112.

As previously discussed above, Ober's CPU or recited "central processing unit" includes the peripheral interfaces or FPIs (e.g., 42–52 in

Ober's Figure 1) of each subsystem (e.g., 30–40 in Ober's Figure 1). Patent Owner has not challenged that Ober's CPU includes the peripheral's FPIs. *See* Reply 9 (stating “[i]mportantly, PO doesn’t challenge AMD’s identification of Ober’s CPU”). Thus, we disagree with Patent Owner’s assertions and evidence (*see, e.g.*, Resp. 29–31, 35) contradict Petitioner’s showing; rather, we agree with Petitioner that Patent Owner’s argument concerning “dividing the clock during ‘normal mode’ is limited to ‘subsystems 30-40[.]’” “acknowledg[es] that at least ‘subsystems 30-40’ can have their clocks adjusted during ‘normal mode[.]’” Reply 9 (reproducing Ex. 1004, Fig. 1 (annotated)); *id.* at 9–10 (citing Ex 1028 ¶ 23). Ober thus teaches its CPU is supplied a divided clock signal in a register (e.g., SFR 116) of peripheral interfaces (e.g., FPIs), which is part of Ober’s “central processing unit,” during an ordinary operation mode (*see* Ex. 1004, 9:65–10:2).

Even further, although we agree that Ober’s RUN mode is an ordinary operation mode, we disagree with Patent Owner that this is the sole ordinary operation mode in Ober. *See* Sur-reply 6 (stating “the RUN mode is the only ordinary operation mode”). Specifically, both parties agree a wait mode is also an ordinary operation or another of the “plurality of ordinary operation modes” as claim 1’s preamble recites. *See* Tr. 34:2–6, 50:9–20. The parties’ respective arguments and evidence are also consistent with the ’519 patent. *See* Ex. 1001, 1:63–64, 2:4–5 (describing a wait mode as a clock operation mode). And Ober’s Table 7, cited by Patent Owner (Resp. 34), along with other portions in Ober teach or at least suggest a different clock in RUN mode (e.g., Divided PLL) than in a WAIT PLL mode. Ex. 1004, 12:13–34 (Table 7), 18:41–58 (indicating Low Speed Clocks=true); *see id.* at 8:2,

Fig. 6. As such, Ober teaches examples of “a plurality of ordinary operation modes” and the modes are “in response to clock frequencies supplied to a central processing unit” as claim 1’s preamble requires.

Collectively, we find these above teachings in Ober, in light of the knowledge that an ordinarily skilled artisan possessed at the time of the invention, teach or suggest an ordinarily skilled artisan would have recognized and known to configure Ober’s CPU to have the ability to generate “a plurality of ordinary operation modes . . . in response to clock frequencies supplied to a central processing unit” within a “system LSI” as claim 1’s preamble recites.

Patent Owner contends that the Decision to Institute relies upon a new theory (i.e., Ober discloses power management techniques to control CPU modes during normal operations was well known) that was not asserted by Petitioner and that this new theory is improper. Resp. 61–62 (citing Dec. Inst. 18). In the Sur-reply, Patent Owner similarly argues that Petitioner cannot raise new theories or combinations in the Reply. Sur-reply 2–3 (citing 35 U.S.C. § 312(a)(3); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018)). Patent Owner contends that Petitioner’s Reply has abandoned its theory in the Petition and now relies on “the combination of Ober and Nakazato” to teach the “‘plurality of ordinary operation modes’ recited in the preamble.” *Id.* at 2 (citing Reply 3–12); *id.* at 2–5 (citing Pet. 16–17, 24–25; Ex. 2012, 23:13–24:10, 25:7–13; Ex. 2023, 91:10–106:8). Patent Owner contends that “Petitioner also argued that a person of ordinary skill in the art would have been motivated to seek out Nakazato for its power-saving driver for the claimed ‘clock control library,’” but “did not argue that Ober

combined with Nakazato would disclose the “plurality of ordinary operation modes.” *Id.* at 4 (citing Pet. 7, 16–18).

We find these arguments unavailing. First, the above discussion relies on Ober’s teachings and what was well-known in the art to disclose the preamble’s limitation, rendering Patent Owner’s arguments regarding Petitioner’s purported reliance on Nakazato moot. Second, Patent Owner takes too limited a view of the ground presented in the Petition and does not account for the Petition as a whole when addressing claim 1’s features. The recited “ordinary operation modes” is in both the preamble and the “first memory” limitation (Ex. 1001, 14:16–18, 21–22), and because the Petition further turns to Nakazato to teach the “clock frequency transition between said ordinary operation modes” in the “first memory” limitation and to teach the ordinary operation modes operating at different frequencies as required for the “first memory” limitation¹² (*see* Pet. 16–19, 25–31), we do not find the Petitioner has raised new theories in the Reply by discussing both Ober’s and Nakazato’s teachings in this regard.

Also, the Decision to Institute did not depart from the Petition by observing that Ober discloses that power management techniques to control CPU power modes during normal operations were known, and in determining that Ober suggests the recited “plurality of ordinary operation modes” in claim 1. Granted, the Decision to Institute, when addressing the preamble, relies on a citation to Ober found in the Petition for the “first memory” limitation. *See* Dec. Inst. 18 (citing Ex. 1004, 2:17–20; Pet. 27). However, consistent with the Petition (*see* Pet. 2–4, 27), the Decision to

¹² As previously discussed, the requirement of different clock frequencies is not found in claim 1’s preamble.

Institute further addresses the '519 patent's description of "conventional clock operation modes" or the recited "ordinary operation modes" language found in the preamble to demonstrate the general knowledge possessed by an ordinarily skilled artisan. Dec. Inst. 19 (citing Pet. 3). Petitioner contends, and we agree, the '519 patent demonstrates that "the ST7 include[s] numerous 'ordinary operation modes' that control the clock frequency of the CPU" (Pet. 3 (citing Ex. 1001, 1:65–2:2)), such as by reducing the system clock speed as discussed in Ober, and that "ordinary operation modes were known" (*id.* at 4). *See also id.* at 2–4 (citing Ex. 1001, 1:20–26, 1:56–2:2). Patent Owner does not dispute that these descriptions in the '519 patent are representative of what a person having ordinary skill in the art knew at the time of the invention. *See generally* Resp.

Based on parties' arguments and evidence, we find Petitioner has demonstrated by a preponderance of the evidence that Ober teaches or suggests claim 1's preamble.

(ii) "a first memory" limitation

Claim 1 recites "a first memory that stores a clock control library for controlling a clock frequency transition between said ordinary operation modes" (limitation 1.1).¹³ Ex. 1001, 14:20–22. Petitioner contends the combination of Ober and Nakazato teaches or suggests this claimed element. Pet. 25–31.

Petitioner asserts an ordinarily skilled artisan would have understood Ober discloses the "first memory" as memory banks 54 and 56 located on

¹³ We use the same numbering as Petitioner for consistency. *See* Pet. 25–44.

Ober's SoC. *Id.* at 25–26 (citing Ex. 1004, 5:50–53; Ex. 1003 ¶ 109) (reproducing Fig. 1 (annotated)). Petitioner further states Ober discusses its SoC runs applications and OSs and that an ordinarily skilled artisan would have understood that the applications and OSs are stored in memory banks 54 and 56 when executing. *Id.* at 26 (citing Ex. 1004, 4:29–32, 5:31–45, 16:12–15; Ex. 1003 ¶ 109). Patent Owner does not address Petitioner's arguments and evidence as to the “first memory.” *See generally* Resp.

Regarding the requirement for a “clock control library,” Petitioner explains that Ober discusses power management subsystem 26 and describes how this system is controlled by a “software configurable register” known as SFR 62. Pet. 26 (citing Ex. 1004, 2:59–62). Petitioner further states “[t]his register includes fields for adjusting the” system clock's frequency using a “sleep divide clock (SDCLK) bit” and “a divide clock (DIVCLK) bit,” which “either disables or provides divided clock signals to the subsystem during a SLEEP mode and also may provide a divided clock signal to the subsystem during a normal mode.” *Id.* at 26–27 (quoting Ex. 1004, 9:65–10:2) (citing Ex. 1003 ¶ 110); *see id.* at 24 (asserting that Ober's “divided clock” concept causes Ober's CPU to execute various frequencies related to the division in the divided clock signal) (citing Ex. 1003 ¶ 103; Ex. 1004, 8:58–64, 15:60–63). Petitioner asserts that Ober's “divided clock” concept causes Ober's CPU to execute various frequencies related to the division in the divided clock signal. *Id.* at 24 (citing Ex. 1003 ¶ 103; Ex. 1004, 8:58–64, 15:60–63).

Petitioner further discusses adjusting the CPU mode during SLEEP mode. *Id.* at 27. Petitioner contends Ober describes that changing bits in register 62 (SLPCLK) will change “the frequency of the system clock during

a sleep mode of operation.” Ex. 1004, 11:31–33, *quoted in* Pet. 27; Pet. 27 (further citing Ex. 1004, 15:60–63). Quoting from Ober, Petitioner states “[t]he CPU core may configure any reduced speed through the power management state machine configuration register bits 19:16 by configuring the clock source CLKSRC bits and the sleep clock bits 26:24.” *Id.* at 27 (quoting Ex. 15:60–63). For example, Petitioner describes Ober’s Table 5 shows the “SlpClk” field is used to reduce CPU clock speed by dividing by 2, 4, or 128. *Id.* (citing Ex. 1004, 11:5–13). Petitioner argues this teaching confirms that the CPU speed changes when the bits are adjusted. *Id.*

Petitioner also notes Ober teaches that “adjusting the CPU mode during normal operation” is known, but “Ober does not explicitly disclose how a divided clock would be configured.” *Id.* at 27 (citing Ex. 1004, 2:17–20), 17, 28 (citing Ex. 1003 ¶ 109). Petitioner argues “a POSITA would have found it obvious to use a similar mechanism as is used during SLEEP mode.” *Id.* at 17 (citing Ex. 1003 ¶ 88), 27 (citing Ex. 1003 ¶ 112). Petitioner further argues that “there are numerous available bits in Register 62 to provide such configuration during operation modes,” and Dr. Albonesi confirms the bit availability. *Id.* at 27–28 (citing Ex. 1004, Table 5; Ex. 1003 ¶ 112). Based on the foregoing, Petitioner contends one skilled in the art would have recognized Ober’s SFR 62 could be used to configure reduced CPU clock speeds during a normal mode by allowing software to write a value representing the clock division amount into register 62, similarly to how this is done during SLEEP mode in Ober. *Id.* at 17 (citing Ex. 1003 ¶ 88), 28 (citing Ex. 1003 ¶ 113¹⁴).

¹⁴ Dr. Albonesi testifies to this finding in paragraph 113, not paragraph 108.

Acknowledging that “Ober does not disclose how and under what conditions its CPU clock frequency would be adjusted” (e.g., operating under differing clock frequencies), the proposed ground contends an ordinarily skilled artisan would “seek out other references that describe how and when to adjust CPU clock frequency, and Nakazato is such a reference.” *Id.* at 28 (citing Ex. 1003 ¶ 114¹⁵); *id.* at 17 (citing Ex. 1003 ¶ 88).

Petitioner argues Nakazato discloses CPU speed control circuit 152 that “controls the processing speed of the CPU 11, and has a throttling controller for switching the CPU speed.” *Id.* at 17, 28 (quoting Ex. 1008, 5:44–48). Petitioner further argues Nakazato’s CPU speed, like Ober’s, can be adjusted by writing data to a register (*id.* at 18, 28 (quoting Ex. 1008, 6:19–21)) and Nakazato’s power saving driver is used to write the data to the register that changes the CPU clock frequency (*id.* at 28–29 (citing Ex. 1008, 7:3–6, Fig. 4A; Ex. 1003 ¶ 116); *id.* at 30 (citing Ex. 1003 ¶ 120)). Petitioner argues that data writing in Nakazato is controlled by a power-saving driver or program running on the OS. *Id.* at 18 (citing Ex. 1008, 7:3–8, 7:19–24), 28–31 (citing Ex. 1008, 7:3–6, 7:13–15, Fig. 4A).

Petitioner maps Nakazato’s power-saving driver to the recited “clock control library for controlling a clock frequency between said ordinary operation modes” in limitation 1.1 because the driver is software that performs the function as claimed, can control the CPU speed control without the use of the system BIOS, and can directly set the circuit’s internal register to change CPU clock frequency. *Id.* at 29 (citing Ex. 1008, 7:13–15, 7:19–27; Ex. 1003 ¶ 116). Petitioner argues that Nakazato’s power-saving driver

¹⁵ Dr. Albonesi testifies to this finding in paragraph 114, not paragraph 109.

changes the CPU clock frequencies using a separate software application referred to as the power-saving utility, which controls the driver by writing information into a predetermined area (e.g., a registry area) and the driver can then refer to this area and cause hardware to change CPU clock frequency once read. *Id.* at 29–30 (citing Ex. 1007, 7:19–27, Fig. 2; Ex. 1003 ¶ 118). Petitioner further states this power-saving utility allows CPU processing speed information to be set by the user. *Id.* at 30 (citing Ex. 1003 ¶ 118; Ex. 1008, 7:19–27). Petitioner also contends both Nakazato’s power-saving utility and its driver are stored in a memory, and thus, Nakazato discloses “a clock control library” stored in “a first memory” as recited. *Id.* at 30–31 (citing Ex. 1008, 5:1–3; Ex.1003 ¶ 119; § Section V.B.).

Petitioner argues that an ordinarily skilled artisan would have found it obvious to use Nakazato’s driver to control Ober’s CPU clock frequency by combining Nakazato’s power-saving driver/utility with Ober’s SoC to achieve a combined system that allows for OS and applications control of CPU clock frequency, and that by combining the teachings, an ordinarily skilled artisan would have recognized Nakazato’s power-saving driver would execute within Ober’s memory banks because Ober’s SoC uses the memory banks for executing its OS and applications. *See id.* at 31 (citing Ex. 1003 ¶ 120–121; “Section.VI.A.1”) (reproducing Ex. 1008, Fig. 2), 18–19. Petitioner further contends the combination would have yielded predictable results because Ober only requires register changes to adjust CPU clock frequency and includes memory for running OS and applications, and Nakazato’s driver is part of OS that adjusts CPU frequency by adjusting a register. *See id.* at 31 (citing Ex. 1003 ¶ 120–121; “Section.VI.A.1”), 18–19.

Patent Owner contends Ober and Nakazato do not disclose limitation 1.1. Resp. 36–43. In particular, Patent Owner contends that the “Petitioner does [not] propose any hardware modifications;” rather, Petitioner proposes that a power saving driver, like Nakazato’s, would write to unused bits in SFR 62 when executed by Ober’s memory banks, causing power manager 28 to supply a low speed clock to the CPU. Resp. 37 (citing Pet. 18); *see* Sur-reply 1–2 (discussing hardware modifications). Patent Owner also argues that Petitioner admits that other modifications to Ober are necessary but that the Petition fails to provide the “modifications a skilled artisan would have been motivated to make” to arrive at claim 1’s invention. Sur-reply 6 (citing *KSR*, 550 U.S. at 418); *see id.* at 6–7 (citing Ex. 1028 ¶¶ 43–46). Patent Owner contends that, in the absence of hardware changes, Petitioner does not explain how an ordinarily skilled artisan “would be able to effect clock frequency transitions simply by writing to blank register fields in the SFR 62.” *Id.* (citing Ex. 1028 ¶ 46). Patent Owner also argues Dr. Albonesi’s testimony (Ex. 1028 ¶¶ 43–46) in this regard is conclusory and not entitled to weight in contrast with Dr. Przybylski’s testimony. *Id.* at 7–8 (citing Ex. 2005 ¶¶ 95–98).

Patent Owner’s arguments are unavailing because claim 1 does not require a hardware modification, but a “a clock control library for controlling a clock frequency transition.” Ex. 1001, 14:20–21. However, in the event that hardware changes are necessary to Ober, we find that, as presented, Nakazato’s driver would involve hardware to change the CPU clock frequency. *See* Pet. 30 (discussing writing to a registry area of “hardware” and the driver causes “hardware” to change CPU clock frequencies) (citing Ex. 1008, 7:19–27; Ex. 1003 ¶ 118); *see* Ex. 1003 ¶ 118

(stating the modification would “cause[] the hardware to change CPU clock frequency”). Also, we find that the combination would involve using Nakazato’s CPU speed control circuit 152 to control CPU processing through power-saving driver/utility’s speed and Ober’s register to control Ober’s CPU clock frequency by writing to SFR 62’s predetermined registry area. *See* Pet. 17–18, 28–31 (citing Ex. 1008, 5:44–48, 6:19–21, 7:13–15, 17:19–27, Fig. 2; Ex. 1003 ¶¶ 116, 118); *see also* Tr. 63:8–15 (discussing modifying SFR 62, which is “hardware”). The presented ground even further proposes to install the driver/utility in Ober’s computer’s OS and applications and to store in memory (e.g., 54, 56 in Ober’s Figure 1) (*see id.* at 28–29 (citing Ex. 1009, 7:3–6, Fig. 4A), 30–31 (citing Ex. 1008, 8:1–3)).

Given the foregoing, and assuming hardware changes were necessary to Ober, we find that an ordinarily skilled artisan would have recognized that the proposed changes to Ober would involve hardware and would include more than writing to blank register fields in SFR 62 to effect clock frequency transitions. *See* Ex. 1003 ¶¶ 114–120. We underscore that an obviousness analysis takes into account “the background knowledge possessed by a person having ordinary skill in the art” (*KSR*, 550 U.S. at 418) and that an ordinarily skilled artisan is “a person of ordinary creativity, not an automaton” (*id.* at 421).

We also disagree with Patent Owner’s contentions that (1) Ober does not suggest SFR 62 may be modified so that more than one frequency is supplied to the CPU in RUN mode, (2) “Ober does not suggest that the unused bits of SFR 62 may be populated,” (3) “writing to the unused bits would cause the clock generator to supply a low speed clock to the CPU core 22.” Resp. 37. These arguments attack Ober alone regarding the

claimed “ordinary operation modes” found in limitation 1.1 (*see* Reply 13–14), whereas the presented ground further turns to Nakazato to provide a teaching to use register bits, such as those in Ober’s SFR 62, to achieve “a clock frequency transition between ordinary operation modes” as claim 1 recites. *See* Pet. 17–19, 25–31.

Patent Owner asserts that Ober’s CPU “operates on a single, fixed frequency that cannot be selected or altered” at RUN mode, which is “the full-speed system clock” and its clock system is not configured to supply a low-speed clock to the CPU that executes instructions. Resp. 33, 13; *see id.* at 27 (citing Ex. 1003 ¶ 102; Ex. 2005 ¶ 51), 34 (citing Ex. 2005 ¶ 51), 35 (citing Ex. 1004, 17:15–26), 39 (citing Ex. 1004, 13:66, 14:48–50; Ex. 2005 ¶ 56), 42 (citing Ex. 2005 ¶ 89); *see also id.* at 32–37 (citing Ex. 1004, 2:17–20, 17:15–26, Table 7; Ex. 2005 ¶¶ 44, 48, 51, 56, 60, 73–74) (reproducing Ex. 1004, Table 7); Sur-reply 6, 10–11 (citing Ex. 2005 ¶ 42). Similarly, Patent Owner contends that Ober’s CPU cannot operate at a variety of frequencies that correspond to the divided clock signal or that Ober’s CPU operating frequency is variable. Resp. 33 (citing Ex. 1003 ¶ 103; Ex. 1004, 8:58–64). Patent Owner further argues the cited passage does not suggest Ober’s CPU’s operating frequency is variable. *Id.* Patent Owner further argues that Ober does not teach or suggest changing a value in SFR 62 that would execute instructions on the low-speed clocks but rather sets the system clock using “ClkSrc” bits of SFR 62. Resp. 33–35, 37.

We disagree. At the outset, we agree with both parties, as previously stated in § II(C)(2), that the recited “a clock frequency transition between said ordinary operation modes” in limitation 1.1 involves the ordinary operation modes operating different frequencies. *See* Ex. 1003 ¶ 102; *see*

also Ex. 2005 ¶ 36. As to Patent Owner’s argument that Ober (or Nakazato for that matter) requires the CPU to *execute instructions* on different clock frequencies or speeds, we found in § II(C)(2) that limitation 1.1 does not require the CPU to execute instructions.

Additionally, the Petition does not discuss Ober’s RUN mode when addressing the “ordinary operation modes” in claim 1 but rather refers to a more general teaching based on additional passages in Ober. Pet. 24–25 (discussing “one configurable state in Ober’s power management system”) (citing Ex. 1004, 8:58–64, 9:65–10:2; Ex. 1003 ¶¶ 102–103), 27 (citing Ex. 1004, 2:17–20), 3 (citing Ex. 1001, 1:56–2:2). That is, Ober’s RUN mode is not the only mode considered an “ordinary operation mode[]” as previously discussed, and the general knowledge possessed by an ordinarily skilled artisan teaches “ordinary operating modes” operating at different frequencies (e.g., high-speed and low-speed) were known. *See* Pet. 2–4 (citing Ex. 1001, 1:56–62, 1:65–2:2); *see id.* at 27 (citing Ex. 1004, 2:17–20). This evidence of record further suggests CPUs operating at different, variable frequencies were known to an ordinarily skilled artisan and thus, the recited “clock frequency transition between said ordinary operation modes” in limitation 1.1 was also known. *See id.* Also, as previously discussed, Ober’s Tables 5 and 7 (Resp. 34, 12–13, 17) and other passages at least suggest a different clock (e.g., System Clock Source) in RUN mode (e.g., Divided PLL) than in other ordinary operation modes, such as a wait PLL mode. Ex. 1004, Tables 5 and 7, 8:2, 18:41–58 (indicating Low Speed Clocks=true), Fig. 6.

Petitioner contends, and we agree, a divided system clock would “divide[] the input clock for all of Ober subsystems” and core 22 because there is only one system clock for every subsystem and peripheral. *See*

Reply 6–7 (citing and reproducing Ex. 1004,¹⁶ Fig. 1 (annotated); *see* Ex. 1029, 90:9–91:4; Ex. 1028 ¶¶ 20–21, 44. Additionally, Dr. Albonesi testifies (Ex. 1028 ¶ 31), and we agree, that Ober’s CPU is not turned off during SLEEP mode, but rather Ober discloses “the PLL and oscillator are not stopped and the clock is distributed to the system.” Ex. 1004, 15:42–43. These assertions notably are unrebutted by Patent Owner. *See generally* Sur-reply.

The presented ground further suggests to an ordinarily skilled artisan that its teaching related to a divided clock can be supplied to Ober’s CPU during ordinary operation modes. *See* Pet. 27–28 (citing Ex. 1004, 2:17–20, 11:31–33, 15:60–63, Table 5; Ex. 1003 ¶ 112), 2–3 (citing Ex. 1001, 1:56–2:2); Ex. 1028 ¶ 22 (citing Ex. 1003 ¶¶ 110–112). Dr. Albonesi testifies, and we agree, that there are at least six available bits in Ober’s register 62, which can provide the clock division configuration during normal operations. Ex. 1003 ¶ 112. Dr. Albonesi refers to an example in Ober’s Table 5, where ReqSlp field in SFR 62 occupies bits 0 and 1 and the RW field begins at bit 4, leaving two empty bits. *Id.* We find that the system clock frequency in Ober can be configured or changed during “ordinary operation modes,” despite Patent Owner’s arguments to the contrary. *See, e.g.*, Resp. 33, 39.

Moreover, Patent Owner’s arguments do not appreciate fully that the presented ground addresses SLEEP mode in Ober to illustrate a suggestion to an ordinarily skilled artisan that a similar technique may be used during ordinary operation modes. *See* Pet. 24–25 (citing Ex. 1004, 8:58–64, 9:65–10:2, 15:60–63; Ex. 1003 ¶¶ 102–103), 27 (stating “a POSITA would have

¹⁶ Petitioner mistakenly refers to Exhibit 1008, which is Nakazato.

found it obvious to use a similar mechanism as is used during SLEEP mode. EX1003, ¶ 112”); *see* Ex. 1028 ¶ 31; Reply 8 (stating “this portion of Ober” cited in Petition’s page 27 “suggests toPOSITAs that such a divided clock can be supplied to Ober’s CPU,” and SFR 62 and Ober’s system clock is “one manner in which such a divided clock can be supplied to Ober’s CPU”) (citing Pet. 27; Ex. 1028 ¶ 22). Also, Dr. Albonesi testifies (Ex. 1028 ¶ 31), and we agree, that Ober’s CPU is not turned off during SLEEP mode, but rather Ober discloses “the PLL and oscillator are not stopped and the clock is distributed to the system.” Ex. 1004, 15:42–43; *see also* Ex. 1028 ¶ 44 (noting “the peripherals merely operate on the clock that is provided to them”). We therefore disagree with Patent Owner’s contention that “Petitioner’s reliance on column 15, lines 60-63 of Ober,” which discusses a SLEEP mode, is “unfounded.” Resp. 33 (citing Ex. 2005 ¶ 74).

Petitioner further relies on Nakazato to teach and suggest the “clock frequency transition between said ordinary operation modes” in limitation 1.1. *See* Pet. 17–19, 27–31. Thus, Patent Owner’s arguments that focus on Ober alone are unavailing. *See* Reply 10 (indicating Patent Owner “improperly focuses on the Ober alone instead of the combination”), 10–11 (addressing the Petition’s discussion of Nakazato teaching the CPU operating at different clock frequencies and noting Patent Owner does not dispute these findings). For example, the Petition contends, and we agree, that Ober does not disclose the conditions where the CPU clock frequency would be adjusted, thus providing a reason one skilled in the art would have looked to other references, such as Nakazato, for its teachings. Pet. 28 (citing Ex. 1003 ¶ 114). Nakazato discloses one known technique for controlling CPU speed using a controller to switch CPU speed and adjusting

the CPU speed through a register, such as Ober's, by writing data in the CPU speed control circuit's internal register. Ex. 1008, 5:44–49, 6:19–21; *see* Pet. 17–18. Additionally, Nakazato teaches a scenario where the processing speed changes “in normal processing” (Ex. 1008, 8:3) when the user sets a low speed for one operation mode (e.g., battery operation) and sets a high speed for another operation mode (e.g., an AC power supply operation) (*id.* at 8:1–4), further suggesting “a plurality of ordinary operation modes.”

Patent Owner does not challenge these findings related to Nakazato's teachings. *See generally* Resp.

Thus, although Ober may disclose a RUN mode embodiment where the low-speed clock is false (Ex. 1004, 17:23) and SLEEP modes where the CPU core clock is stopped but CPU core speed is reduced (*id.* at 15:47, 15:60–62) as argued (*see, e.g.*, Resp. 35, 38), Petitioner shows by a preponderance of the evidence that the combination of Ober and Nakazato teaches “a clock control library for controlling a clock frequency transition between said ordinary operation modes” as recited in limitation 1.1.¹⁷

Patent Owner argues “Petitioner wrongly asserts that the passage in column 9, line 65 through column 10, line 2 of Ober applies to power management subsystem SFR 62.” *Id.* at 39; *see id.* at 39–40 (citing

¹⁷ Notably, limitation 1.1 does not require the “clock frequency transition between said ordinary operation modes” occur at a specific time, such as during the same user operation period. Ex. 1001, 14:21–22. The “clock frequency transition between said ordinary operation modes” can be between operation modes operating at different operable periods, such as between a high speed (e.g., second option in Nakazato's Figure 2) set by a user in one operation period and a low speed (e.g., selected option in Nakazato's Figure 2) at a succeeding operation period. *See* Ex. 1008, 7:31–8:59.

Ex. 1004, 9:49–53, 9:65–10:2; Ex. 2005 ¶ 58), 41 (citing Ex. 1004, 10:1–2; Ex. 2005 ¶¶ 77, 89), 42 (citing Ex. 2005 ¶ 89). Once again, these arguments overlook other passages discussed in the Petition and addressed by Dr. Albonesi as previously discussed in § II(D)(3)(a)(i). *See* Pet. 27–28 (citing Ex. 1004, 11:5–13, 15:60–63; Ex. 1003 ¶ 112).

As discussed, Ober at least suggests to an ordinarily skilled artisan that its CPU is configurable to reduce clock speed through a process of configuring SFR 62’s register bits using its power management state machine. *See* Ex. 1004, 15:60–63; *see* Reply 6 (citing Pet. 27). Ober’s CPU clock can also operate at a variety of frequencies corresponding to a divided clock. Ex. 1004, 11:8–15, 15:60–63; *see also* Ex. 1003 ¶ 103. These passages and testimony refer to the SFR 62, not SFR 116. *See* Ex. 1004, Table 5, 11:8–15, 15:60–63. Also, Petitioner is not proposing to use SFR 116 during ordinary operation modes. *See* Pet. 30–31. Instead, Petitioner proposes to modify SFR 62’s register bits as taught by Nakazato to include the divided clock feature during “ordinary operation modes” based on the general knowledge of an ordinarily skilled artisan, Ober’s teachings in sleep and run modes, and Nakazato’s teachings to disclose or suggest the recited “clock control library for controlling a clock frequency transition between said ordinary operation modes” as claim 1 recites. *See id.* at 17–19, 27–31; *see* Reply 6 (noting “the Petition relies on the combination of Ober and Nakazato to show a CPU that operates at different clock frequencies.”).

Nor does the Petition involve adding a SFR 116 to the Ober’s CPU core or “to join the peripheral power management system in SFR 116 with” SFR 62 (Resp. 40) as Patent Owner argues. *See* Resp. 32 (citing Ex. 2005 ¶¶ 59, 70), 39–40. Although Petitioner appears to state SFR 62 includes

SDCLK bit and DIVCLK bit fields for adjusting the system clock's frequency as Patent Owner asserts (*see* Resp. 39 (quoting Ex. 1004, 9:65–10:2) (citing Ex. 1003 ¶ 110; Pet. 26)), which at least for the SDCLK bit is located in SFR 116 (Ex. 1004, 9:42–48 (Table 4)), the record contains ample other evidence, as discussed above, that Petitioner proposes to adjust the bits within SFR 62 to arrive at the recited “clock frequency transition between ordinary operation modes” in limitation 1.1.

Patent Owner also contends an ordinarily skilled artisan “would have recognized the contrast in teachings between SFR **116** and SFR **62**” and would have “recognized that, consistent with Ober’s stated objective of providing decentralized power management of the peripheral devices, Ober does not suggest that SFR **62** may be used or modified to provide low speed clocks to the CPU during a RUN mode for use during program execution.” *Id.* at 42 (citing Ex. 2005 ¶ 89). We address the decentralized contention below in the Motivation to Combine Arguments section of this decision. Also, as discussed above, Petitioner does not propose to modify SFR 62 to provide different clocks exclusively during *run* mode, but rather during ordinary operation modes, which include more than the run mode. *See, e.g.*, Pet. 24–25, 27–28. Moreover, claim 1 does not require the CPU to perform this function for use during program execution.

Patent Owner also contends that subsystems 30-40 of Ober do not “run on the System Clock” but rather a “local clock.” Resp. 9 (citing Ex. 1004, 9:49–10:6); *see id.* at 12, 43 (discussing “CPU clock supply and low speed clocks are mutually exclusive”); Sur-reply 9. Patent Owner also contends the CPU clock supply and low speed clocks are mutually exclusive in Ober’s power management state machine. Resp. 43 15:46–51. This

argument does not address Petitioner’s discussion to modify Ober’s SFR 62, which generates the system—not a local subsystem’s— clock (*see* Ex. 1004, 8:53–64, Tables 5 and 7, Figs. 1–2), based on Nakazato’s teachings. *See* Pet. 28–31. In any event, claim 1 does not require that a specific clock (e.g., system) supply the clock frequencies to the central processing unit. Ex. 1001, 14:16–18, 21–22.

Having considered each of the parties’ arguments and evidence, we determine Petitioner has proven, by a preponderance of the evidence, that Ober and Nakazato teach or suggest limitation 1.1.

(iii) “a system control circuit” limitation

Claim 1 further recites

a system control circuit which has a register, wherein said system control circuit carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register, and also carries out the clock frequency transition among said ordinary operation modes in response to said clock control library

(limitation 1.2). Ex. 1001, 14:23–29.

Petitioner contends the combination of Ober and Nakazato teaches or suggests this limitation. Pet. 32–34.¹⁸ Petitioner maps Ober’s power management subsystem to the recited “system control circuit.” *Id.* at 32. Petitioner states Ober’s power management subsystem includes a configurable power management state machine for controlling CPU power modes and various subsystems using a register. *Id.* at 32 (citing Ex. 1004, 3:51-56). More specifically, Petitioner contends subsystems 30 through 40

¹⁸ Although stating Ober teaches limitation 1.2, the Petition further discusses “the combination of Ober and Nakazato.” Pet. 34.

have SFR registers configured by an OS to respond to power management commands, and the management system (e.g., 26 in Ober's Figure 2) itself has SFR register 62 configured by way of the OS or a specific application. *Id.* at 32–33 (citing Ex. 1004, 2:59–3:1, 7:36–44, 10:16–28) (reproducing Table 5 in part).

Petitioner contends Ober's Table 5 shows changing a register value to indicate the power mode of Ober's system, including operating in “an ordinary operation mode” if register 62 “is set to ‘No Sleep Request’” and operating in a “special mode” if register 62 “is set to ‘IDLE,’ ‘SLEEP,’ or ‘DEEP SLEEP.’” *Id.* at 33 (citing Ex. 1004, 11:15–21; Ex. 1003 ¶ 124). Based on this discussion, Petitioner asserts Ober's “system control circuit,” which includes a “register,” “carries out the clock frequency transition between said ordinary operation modes and said special modes in response to a change of a value in said register” as limitation 1.2 recites. *Id.*

Petitioner states that Ober suggests register 62 is used to adjust “clock frequency transition among said ordinary operation mode” by discussing programming the system clock frequency in Ober's register 62 with a changed value bit during sleep mode, which leads to a divided system clock. *Id.* at 33 (citing Ex. 1004, 11:6–13, 11:31–33). Petitioner further states Ober discloses dividing a system clock during a normal mode, and an ordinarily skilled artisan would have found it obvious to use a mechanism similar to the SLPCLK register during a normal mode “as described above.” *Id.* at 34 (citing Ex. 1004, 9:65–10:2; Ex. 1003 ¶ 126). “As explained above” (*id.*), Petitioner further contends the combination of Ober and Nakazato teaches or suggests that changes in Ober's CPU clock speed occur in response to a “clock control library” as recited. *Id.* (citing Ex. 1003 ¶ 127). Based on the

foregoing, Petitioner asserts the combination of Ober and Nakazato teaches or suggests “said system control circuit . . . also carries out the clock frequency transition among said ordinary modes in response to said clock control library” in limitation 1.2. *Id.*

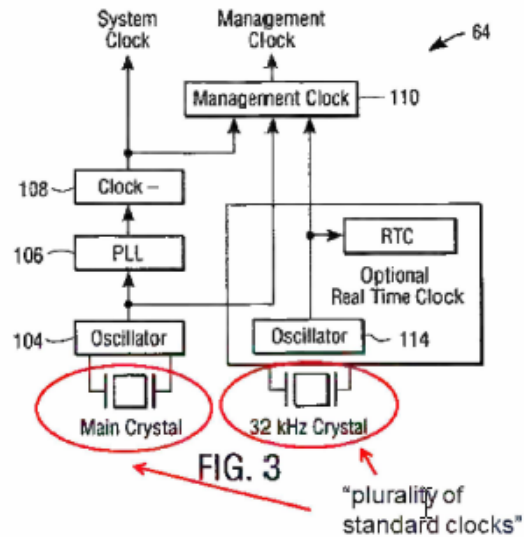
Patent Owner does not contest Petitioner’s arguments and evidence as to limitation 1.2, other than challenging the construction of the “clock frequency transition between ordinary operation modes,” as discussed in § II(C)(2), and disputing that Ober and Nakazato teach the “clock frequency transition between said ordinary operation modes,” as discussed in § II(D)(3)(a)(ii).

Based on Petitioner’s arguments and unrebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Ober and Nakazato teach or suggest limitation 1.2.

(iv) “a clock generation circuit” limitation

Claim 1 further recites “a clock generation circuit that receives a plurality of standard clocks, wherein said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit” (limitation 1.3). Ex. 1001, 14:30–33.

Petitioner contends Ober teaches or suggests limitation 1.3. Pet. 34–36. Petitioner maps Ober’s clock subsystem 64 to the recited “clock generation circuit.” *Id.* at 34 (citing Ex. 1004, 8:53–58). Petitioner states clock subsystem 64 receives “a plurality of standard clocks” as shown in annotated Ober’s Figure 3 shown below.



Ober’s Figure 3 annotated above shows standard clocks, including Main Crystal operating at 15 MHz and a 32 kHz Crystal. Ex. 1004, Fig. 3; *see id.* at 35 (reproducing Ex. 1004,¹⁹ Fig. 3 (annotated)) (citing Ex. 1004, 8:58–64). Petitioner asserts Dr. Albonesi confirms that an ordinarily skilled artisan would have understood that 15 MHz and 32 KHz crystals are standard clocks. *Id.* (citing Ex. 1003 ¶ 131). Based on the above discussion, Petitioner asserts Ober teaches “a clock generation circuit that receives a plurality of standard clocks” as limitation 1.3 recites. *Id.*

Petitioner next contends Ober’s clock subsystem is “control[led] by said system control circuit” as limitation 1.3 recites. *Id.* “As explained above,” Petitioner asserts Ober’s power management subsystem (e.g., 26), which is mapped to the recited “system control circuit,” includes register 62 and describes that clock subsystem 64 may be configured by SFR register 62 within management subsystem 26. *Id.* at 35–36 (citing Ex. 1004, 7:41–44,

¹⁹ The Petition refers to “EX 1008, FIG. 3” (Pet. 35) when discussing Ober’s Figure 3. We presume this is a typographical error.

9:6–8). Petitioner states Ober describes the system clock signal may be generated by the main oscillator/PLL (or shut down) “depending on the configuration of the SFR register 62.” *Id.* at 36 (quoting Ex. 1004, 9:6–8).

Petitioner adds, “[a]s described above,” Ober suggests that register 62 is configured “for how the system clock is divided during normal operations” (*id.* (citing Ex. 1003 ¶ 133)), namely a clock subsystem’s “clock circuit 108 divides the oscillation frequency to provide the system clock frequency” (*id.* (quoting Ex. 1004, 8:59–64)). Petitioner then asserts an ordinarily skilled artisan would have understood that control clock circuit 108 would be configured to divide the system clock according to register 62’s configuration during normal operations. *Id.* (citing Ex. 1003 ¶ 133). Based on the foregoing, Petitioner asserts Ober teaches “said clock generation circuit generates a clock supplied to said central processing unit according to control by said system control circuit” as limitation 1.3 recites.

Patent Owner does not directly challenge Petitioner’s arguments or evidence as to limitation 1.3.

Based on Petitioner’s arguments and unrebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Ober teaches or suggests limitation 1.3.

(v) “a second memory” limitation

Claim 1 further recites “a second memory that stores an application program, wherein calling of said clock control library and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions” (limitation 1.4). Ex. 1001, 14:35–39.

Petitioner asserts the combination of Ober and Nakazato teaches or suggests limitation 1.4. Pet. 37–40. Petitioner contends the recited “second memory” does not have to be separate from the first memory, noting claim 11 of the ’519 patent recites the first and second memory are “the same memory.” Pet. 37; Ex. 1001, 16:12–14 (claiming “said first memory and said second memory are formed to coexist in one memory, sharing memory area of said one memory”). Based on the foregoing, Petitioner maps memory banks 54 and 56 separately or together to the “second memory.” Pet. 37 (citing Ex. 1004, 5:50–53).

Regarding the “second memory storing an application program,” Petitioner contends an ordinarily skilled artisan would have understood memory banks 54 and 56 store applications and software because they are the only memories in Ober’s SoC, suggesting that Ober’s CPU would use these memories to store applications in order to execute any software. *Id.* at 37–38 (citing Ex. 1003 ¶ 136).

Regarding the “calling of said clock control library and changing of said register value are programmably controlled by said application program to enable user selectable clock frequency transitions” recitation, Petitioner contends the combination of Ober and Nakazato teaches or suggests this recited feature. *Id.* at 38–40. Petitioner states “[a]s explained above” (*id.* at 38), Ober has registers that can be programmatically controlled by software, such as an OS or an application, but notes that Ober does not disclose how such software would be implemented. *Id.* at 38 (citing Ex. 1003 ¶ 137); *see id.* at 26–28 (citing Ex. 1004, 2:59–62, Table 5; Ex. 1003 ¶¶ 112–114²⁰).

²⁰ Cited paragraphs 108 and 109 (Pet. 28) do not address Petitioner’s points. We presume Petitioner intended to refer to paragraphs 113 and 114.

Petitioner repeats its discussion related to Nakazato and the “clock control library” recitations, and proposes combining its teachings with Ober’s CPU to execute Nakazato’s utility. *Id.* at 38–39 (citing Ex. 1008, 17:19–27, Fig. 2; Ex. 1003 ¶ 139); *see also id.* at 28–31 (citing Ex. 1008, 6:19–21, 7:3–6, 7:13–15, 7:19–27, Fig. 2; Ex. 1003 ¶¶ 116, 118–120).

More specifically, Petitioner states Nakazato’s setting window (e.g., Figure 2) is a dedicated program (e.g., the power-saving utility), stored in memory, that allows the user to select a clock frequency by writing information into a hard drive’s predetermined registry, and teaches its utility controls a power-saving driver. *Id.* at 38–39 (citing Ex. 1008, 5:1–3, 7:19–27, Fig. 2; Ex. 1003 ¶ 139). Petitioner asserts Nakazato’s above-described utility, when combined with Ober’s system, is stored in “second memory” and teaches or suggests a combined system performing the “calling of said clock control library and changing of said register value” functions in limitation 1.4. *Id.* at 39–40 (citing Ex. 1003 ¶ 140).

Aside from challenging Petitioner’s finding that Ober and Nakazato fail to teach or suggest “the clock control library for controlling a clock frequency transition” (*see* Section III(D)(a)(ii)) and the claim construction of “clock frequency transition” (*see* Section II(C)(2)), Patent Owner does not otherwise challenge Petitioner’s arguments or evidence as to limitation 1.4.

Based on Petitioner’s arguments and unrebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Ober and Nakazato teach or suggest limitation 1.4.

(vi) “*said special modes*” limitation

Lastly, claim 1 recites:

wherein said special modes comprise a first special mode in which clock supply to principal constituents of said central processing unit is halted, a second special mode in which clock supply to an entirety of said central processing unit is halted, and a third special mode in which supply of power to the entirety of said central processing unit is halted

(limitation 1.5). Ex. 1001, 14:40–46.

Petitioner states Ober teaches or suggests limitation 1.5. Pet. 25, 40–44. For “a first special mode in which clock supply to principal constituents of said central processing unit is halted,” Petitioner persuasively maps this recitation to Ober’s IDLE MODE and its related teachings. *Id.* at 40–41 (citing Ex. 1004, 15:14–17; Ex. 1001, 6:23–26, 10:1–34, 10:41–45; Ex. 1003 ¶ 143). For “a third special mode in which supply of power to the entirety of said central processing unit is halted,” Petitioner persuasively maps this recitation to Ober’s DEEP SLEEP MODE or SLEEP MODE (Clock Not Distributed) where “the power from Ober’s central processing unit” is removed, and related teachings. *Id.* at 25, 44 (citing Ex. 1004, 13:1–44, 16:12–15, 16:19–24).

For “a second special mode in which clock supply to an entirety of said central processing unit is halted,” Petitioner maps this recitation to a particular embodiment of Ober’s SLEEP MODE (Clock Not Distributed). Pet. 25, 41–43. More specifically, Petitioner asserts Ober teaches a mode where “the OS or application software also ‘stop[s] the CPU core 22, [and] optionally remove[s] the CPU power and remove[s] power and clocks from most or all of the subsystems.’” *Id.* at 41 (quoting Ex. 1004, 16:12–15) (bolding omitted); *see id.* at 25. Petitioner asserts “not only is the clock

halted, but all of the interfaces and buses connected to the core 22 are also halted” during this mode. *Id.* at 42 (reproducing Ex. 1004, Fig. 1 (annotated)), 43 (reproducing Ex. 1004, 13:1–42 (part of Table 8)) (noting “units powered” by annotation). Petitioner further contends this mapping in Ober is consistent with the ’519 patent. *Id.* at 43 (citing Ex. 1001, 11:13–17; Ex. 1003 ¶ 146).

Patent Owner does not directly challenge Petitioner’s arguments or evidence as to Ober regarding this limitation.

Based on Petitioner’s arguments and unrebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Ober teaches or suggests limitation 1.5.

Petitioner’s Showing of Reasonable Expectation of Success

Petitioner contends that there would have been a reasonable expectation of success in combining Ober and Nakazato because “Nakazato’s software is already described as modifying registers to change a CPU clock frequency and Ober’s system includes registers to change CPU clock frequency.” Pet. 18–19 (citing Ex. 1003 ¶ 91; *KSR*, 550 U.S. at 417).

Patent Owner argues that an ordinarily skilled artisan would not have “enjoyed a reasonable expectation of success reading or writing to the unused bits in the SFR 62 to supply low-speed clocks to the CPU 22” because the references do not demonstrate that the combination results in low speed clocks supplied to the CPU during RUN mode. Resp. 44; *see* Sur-reply 13, 16. Instead, Patent Owner argues “[i]t is more likely that Petitioner’s proposed combination would be ignored or would result in unpredictable behavior that would be undesirable.” Resp. 44; *id.* at 46

(arguing Ober would ignore bits written to SFR 62 or the microcontroller would behave unpredictably if Nakazato's driver wrote to SFR 62); *see* Sur-reply 15 (citing Ex. 2005 ¶¶ 57, 96), 17. Patent Owner provides evidence to support this assertion. Resp. 45 (citing Ex. 1013, pp. 65–66; Ex. 2005 ¶ 57; Ex. 2006, p. 144; Ex. 2008, p. 48; 2009, p. 48). Patent Owner contends an ordinarily skilled artisan would have understood that Ober's state machine runs a finite set of pre-defined states and thus, when entering an undefined state the machine would behave unpredictably. *Id.* at 46–48 (citing Ex. 1004, 17–1–2, 17:13–19:36, Fig. 6; Ex. 2005 ¶¶ 50, 97–98; Ex. 2010, p. 656; Ex. 2011, pp. 296, 304–305); *see* Sur-reply 14–15 (citing Ex. 1004, 17:2–3; Ex. 1013, pp. 65–66; Ex. 2010, p. 262; Ex. 2011, pp. 296, 304, 656). Patent Owner asserts substantial modification of power management block 26 and SFR 26 would be required “to put register bits where none previously existed and to cause those new register bits to produce the effect hypothesized by Petitioner.” *Id.*; *see* Sur-reply 6–7. Patent Owner argues the Petition's theory is conclusory. Sur-reply 12. Patent Owner further contends Ober chose not to operate the free register bits during RUN and IDLE mode and thus, an ordinarily skilled artisan would not have found it obvious to modify Ober as proposed. *Id.* at 61 (citing Ex. 2005 ¶ 93).

Patent Owner further argues Dr. Albonesi admits that writing to unused bits in Ober's SFR 62 may be problem in some implementations. Resp. 46 (citing Ex. 2012, 70:5–18); Sur-reply 13 (citing Ex. 2012, 69:5–71:20). Dr. Przybylski asserts that, without hardware changes to control the system clock divider, writing to SFR 62's unused bits “would have no consequences or some unforeseen and unpredictable consequences.” Ex. 2005 ¶ 98, *quoted in* Resp. 46; Sur-reply 15 (citing Ex. 2005 ¶¶ 57, 96).

In response, Petitioner argues that the Petition “never suggests writing to undefined bits” but rather “*defining* new bits in register 62 for use in dividing the CPU clock.” Reply 15; *id.* at 15–16 (quoting Pet. 27–28). Petitioner further asserts that an ordinarily skilled artisan would have known to make “the appropriate changes to Ober to support these additional bits.” *Id.* at 16. Petitioner further argues that that the Petition did not propose to alter state variables in the system, but further contends that changing a state variable would not cause the system to behave unpredictably because they are meant to change. *Id.* at 17 (citing Ex. 1028 ¶ 51). Petitioner also notes Patent Owner (1) only contends the system “*might* or *may* not work,” (2) does not support these alleged problems with technical explanation, and (3) does not allege these problems are beyond the ordinary skill of an artisan to solve, which does not “rebut a reasonable expectation of success.” *Id.*; *see id.* at 16 (quoting Resp. 47–48).

We disagree with Patent Owner’s arguments and evidence rebut Petitioner’s showing. As explained above, the “ordinary operation modes” encompass more than Ober’s RUN mode. Moreover, we agree with Petitioner that Patent Owner’s assertion that “Ober’s microcontroller *might* behave unpredictably, and *may* even be locked unacceptably” when variables are changed (*see* Resp. 48) does not demonstrate sufficiently that Ober’s microcontroller will behave unpredictably if modified as proposed.

Also, many of Patent Owner’s assertions are premised on the assumption that Ober’s SFR 26 available bits as modified would remain undefined and unused and thus, create an unpredictable and undefined state. *See* Resp. 44 (discussing “writing to unused bits”), 46–47 (discussing “an undefined state”); Ex. 2005 ¶ 57, 97, 98. Alternatively, Patent Owner

contends the presented combination discusses “put[ting] register bits where none previously existed.” Resp. 47. We disagree with these assertions. The presented combination does not propose to add new bits to SFR 62. *See* Pet. 17–19, 27–31; *see also* Ex. 1028 ¶ 48. Rather, the Petition proposes to write the information to “a predetermined area” (e.g., predefined) (Pet. 30), thus the available bits in SFR 62 will not remain undefined or unused. *See id.* at 27 (noting SFR 62 has “available bits . . . to provide such configuration during operation mode”) (citing Ex. 1004, Table 5; Ex. 1003 ¶ 112), 28 (proposing to configure SFR 62 “by allowing software to write a value representing the amount of clock division into a field in register 62”) (citing Ex. 1003 ¶ 108), 30 (stating Nakazato’s “driver would actually cause[] the hardware to change CPU clock frequency once it reads the newly written speed”) (citing Ex. 1003 ¶ 118; Ex. 1008, 7:19–27), 31 (stating “Ober’s CPU clock frequency is controlled via software writing to a register” controlled by Nakazato’s driver) (citing Ex. 1003 ¶ 120); *see also* Ex. 1028 ¶ 49 (stating “I never suggested writing to undefined.”). By defining Ober’s SFR 62 bits as proposed, Ober’s state machine would not enter into an undefined or unpredictable state, such that inputs to other components (e.g., system timers) fail as Patent Owner asserts. *See* Resp. 52; *see also* Sur-reply 13.

Likewise, in contrast to the predetermined and defined register bits in SFR 62 presented by the presented Ober/Nakazato combination (*see* Pet. 17–19, 27–31), Patent Owner cites to various exhibits (*see* Resp. 44–45) addressing reserved bits, undefined bits, and write-only bits. *See* Ex. 1013, pp. 65–66; Ex. 2006, p. 144; Ex. 2008, p. 48; Ex. 2009, p. 48; Ex. 2011, pp. 296, 304–305. Dr. Przybylski’s testimony similarly is premised on the

bits in Ober’s SFR being “undefined” (Ex. 2005 ¶ 57) or “unused” (*see id.* ¶¶ 91, 97, 98).

Also, although Patent Owner (Sur-reply 15) and Dr. Przybylski (Ex. 2005 ¶ 96) contend the frequency provided to the peripherals would be erratic during transitioning from RUN mode to other modes, Ober and Nakazato provide sufficient evidence of how the system can operate at and transition to lower frequencies in a predictable manner in these modes as previously discussed. Dr. Przybylski also confirms that CPU cores operating at multiple frequencies were known at the time of the ’519 patent (Ex. 1029, 54:20–55:2) and “if the CPU or core was designed in order to do that, then it was safe to do” (*id.* at 62:18–63:3) and would not act in an erratic manner.

Motivation to Combine Arguments

Petitioner provides several reasons to combine Ober and Nakazato in Section VI.A.1 of the Petition. Pet. 18–19. Referring back to this section, Petitioner states an artisan would have been motivated to use Nakazato’s power-saving driver to control Ober’s CPU clock frequency. Pet. 31. In the Petition’s Section VI.A.1, Petitioner states Ober and Nakazato relate to (1) managing a computer system’s power (*id.* at 18 (citing Ex. 1003 ¶ 91)), (2) managing power by adjusting the CPU’s frequency (*id.*), and (3) adjusting the CPU frequency by changing a register value (*id.*). Petitioner further states, in another section, Ober and Nakazato relate to “to a system for setting processing speed.” *Id.* at 8. Petitioner also states combining the references would have been nothing more than combining prior art elements according to known methods to yield a predictable result

because Nakazato's driver/utility would merely be executed from Ober's memory banks to adjust Ober's CPU clock control register. *Id.* at 18.

Petitioner additionally reasons that Ober's CPU clock frequency is controlled by software writing to a register and Nakazato's power-saving driver controls CPU clock frequency through a register. *Id.* at 31 (citing Ex. 1003 ¶ 120). Petitioner further argues that an ordinarily skilled artisan: (1) could have combined Nakazato's power-saving driver/utility with Ober's SoC to achieve a combined system that allows for an OS and application to control a CPU clock frequency; and (2) would have recognized, when combining Ober and Nakazato, that Nakazato's power-saving driver would execute within Ober's memory banks because Ober's SoC uses memory banks for executing its OS and applications. *Id.* Finally, Petitioner states the combination would have yielded predictable results because (1) Ober only requires a register change to adjust CPU clock frequencies and includes memory for running OS and application, and (2) Nakazato's driver is part of an OS that adjusts CPU clock frequency by adjusting a register. *Id.* (citing Ex. 1003 ¶ 121).

Patent Owner argues that the Petition does not sufficiently support its motivation to combine Ober and Nakazato, asserting that the Petition and Dr. Albonesi's testimony are conclusory. Resp. 48–61 (citing Ex. 1003 ¶¶ 108–112). Patent Owner asserts the Petition does not assert an ordinarily skilled artisan would have been motivated to modify Ober but rather states an artisan *could* have used the available bits in Ober's SFR register to provide lower speed to the CPU core, which is insufficient to establish a person would have been motivated to modify Ober as proposed. *Id.* at 49 (citing *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019)).

We disagree because, as discussed above, Petitioner and Dr. Albonesi articulate reasoning supported by rational underpinnings explaining why such an artisan *would have* been motivated to make the combination, including defining Ober’s SFR 62 available bits to control CPU clock frequencies. Pet. 17–19, 27–31; *see* Ex. 1003 ¶¶ 114–121.

Patent Owner also argues Ober solves a problem presented by conventional technique to reduce or stop the system clock by providing a decentralized power control of its peripherals and limited power/speed control of the processor and microcontroller. Resp. 49 (citing Ex. 2005 ¶ 45). For this reason, Patent Owner asserts that modifying Ober’s CPU to operate on a low-speed clock would change Ober’s principle of operation and have the opposite effect of setting power for the entire microcontroller rather than addressing the peripherals’ power state in IDLE mode. *See id.* at 49–50 (citing Ex. 2005 ¶ 102; Ex. 1004, 2:43–46). Patent Owner further argues modifying Ober’s RUN mode by using a divided clock would render its microcontroller inoperable for its intended purpose. *Id.* at 51–54. More specifically, Patent Owner contends the modification would modify “Ober to supply low-speed clocks indiscriminately” or globally across the chip, change the input frequency of the peripherals, causing some to fail, and the system timers would not keep time properly. *Id.* at 52 (citing Ex. 2009 ¶ 92; Ex. 1004, 5:41–49, Fig. 1); *see* Sur-reply 13.

Dr. Przybylski contends Ober does not provide any indication that the possible CPU cores come with a specific range of operating frequencies for which they would correctly behave. Ex. 2005 ¶ 99, *quoted in* Resp. 53. Based on the foregoing, Patent Owner argues dividing the clock as proposed in the Petition “might have the unintended side effect of reducing the system

clock below operating range” (Resp. 53) and “might even render it entirely inoperable” (*id.* at 54).

We disagree that the presented ground would change Ober’s principle of operation. As explained above, the Petition addresses the clock frequencies supplied to Ober’s CPU during “ordinary operation modes,” not IDLE or SLEEP mode, which remain as is. *See* Reply 18. Indeed, the ’519 patent (Ex. 1001, 1:54–2:2), Ober (Ex. 1004, 9:65–10:2, 11:1–14, 15:60–63), Nakazato (Ex. 1008, Fig. 2), Dr. Albonesi (Ex. 1028 ¶ 46), and Dr. Przybylski (Ex. 1029, 54:20–55:2, 62:18–63:5) provide ample evidence that a system’s CPU can operate and behave properly at multiple and lower frequencies. Ober also provides some evidence that the system can be programmed so that its clock is not spread indiscriminately, such as in the case of the peripherals or subsystems during an ordinary operation mode (e.g., lower-speed RUN mode), which further suggests that the system would not be rendered inoperable if “a clock frequency transition” occurs “between ordinary operation modes” as claim 1 recites. *See* Reply 18 (citing Ex. 1004, 9:65–10:2); *see also* Ex. 1028 ¶¶ 44 (stating “the peripherals would operate as they are already configured to do so – based on the clock signal they receive”), 46.

Regarding Ober and its decentralizing approach, Patent Owner further contends “Ober distinguishes its inventive microcontroller from the conventional one through the use of decentralized power management control as disclosed in its specification” and teaches away from modifying Ober as proposed. Resp. 36 (citing Ex. 2005 ¶ 44); *see id.* at 13, 42, 54–61; Sur-reply 18–20. More particularly, Patent Owner argues Ober teaches away from combining with Nakazato because Nakazato teaches a centralized

approach to power management that Ober identified as a problem to be solve. *Id.* at 54–55 (quoting *Polaris Indus. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018)), 59, 61.

However, the presented ground for claim 1 does not propose to replace Ober’s decentralized system wholesale with a centralized power management system. Pet. 16–19, 30–31; *see* Reply 19 (stating “nothing in the Petition proposes modifying any core functionality of Ober. Ober is decentralized in the sense that it’s [sic] ‘power management system’ allows for the ‘microcontroller subsystems to be independently controlled,’” “Ober would still maintain its independent control of power settings for subsystems,” and “[t]his functionality would remain in the proposed combination with Ober and Nakazato”) (citing Ex. 1004, 2:45–48; Ex. 1028 ¶¶ 41 45). Rather, the presented ground proposes to apply Nakazato’s technique concerning how to operate a CPU in ordinary operation modes by reducing CPU speeds. *See* Pet. 16–19, 30–31. Moreover, Ober states, even in SLEEP mode, that “the PLL and oscillator are not stopped and the clock is distributed to the system.” Ex. 1004, 15:41–43. Thus, “Ober is not strictly a decentralize power management scheme.” Reply 19 (citing Ex. 1029, 71:22–72:2). Patent Owner furthermore provides unconvincing evidence or support for the statement that “Nakazato teaches [a] centralized power management approach.” Resp. 54.

Patent Owner further argues “Ober’s central purpose is decentralizing the previously centralized power control management schemes that did not optimize power consumption for peripherals.” *Id.* at 55 (citing Ex. 1004, 2:43–46); *see id.* at 55–57 (citing Ex. 1004, 1:17–20, 1:52–54, 2:24–27, 2:43–49; Ex. 2005 ¶ 92). Patent Owner contends that Ober “disparages the

technique of reducing CPU clock frequency to save power at the microcontroller level as unoptimized, complex, and costly.” *Id.* at 55; *see id.* at 55–58 (citing Ex. 1004, 2:17–40, 2:43–44; Ex. 2005 ¶¶ 92, 103). Patent Owner further contends the motivations to combine the references in the Petition “do not account for the statements Ober makes disparaging centralized power control of microcontrollers” (*id.* at 57) and the “combination would result in a system that treated the CPU and all subsystems identically” (*id.* at 58 (citing Ex. 2005 ¶ 92)). Patent Owner contends an ordinarily skilled artisan “would have been led away from implementing an ‘integrated system for adjusting CPU clock speed.’” *Id.* at 59 (citing Ex. 2005 ¶¶ 91–92).

We disagree that Ober teaches away from, discourages an ordinarily skilled artisan from, or would have led an ordinarily skilled artisan away from combining Ober with Nakazato as proposed. As previously stated, the proposed ground does not propose to remove Ober’s decentralized approach. Also, Ober states that “[t]here are several *disadvantages* in utilizing such centralized control at the microcontroller” (Ex. 1004, 2:21–22) (emphasis added), and that “such centralized systems *do not optimize* the power usage of the various subsystems of the microcontroller” (*id.* at 2:21–24) (emphasis added). Although applying a more centralized approach to Ober *may* render its system somewhat inferior, Ober’s discussion would not have led an ordinarily skilled artisan in a direction divergent from using a power management technique that controls power by reducing CPU speed, such as for functions other those related to the peripherals. *See In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012).

Ober further indicates, “*for a given family of microcontroller*” (Ex. 1004, 2:36–37) (emphasis added)—i.e., not all microcontrollers—“multiple power management architectures *may be required*, which increases costs and complexity of the microcontrollers” (*id.* at 2:37–39) (emphasis added). That is, increased costs and complexity discussed in Ober do not apply to all microcontrollers, and merely reflect engineering tradeoffs for consideration. Although Patent Owner contends this statement is “generally” (Resp. 59) or “universally applicable” (*id.* at 60) to all microcontroller, we disagree. *See* Resp. 59–61 (citing Ex. 1004, 2:17–20, 2:24–26, 2:36–39m 2:49–53, 3:13–16). First, Ober discusses power management techniques of a microcontroller (Ex. 1004, 2:17–20) and microcontroller subsystems (*id.* at 2:24–26) *in general*, which does not mean these discussions apply to all microcontrollers. Second, even assuming, without agreeing, the proposed combination results in the noted microcontrollers with multiple power management architectures requiring increased cost and complexity, we repeat that this result would not have led an ordinarily skilled artisan in a direction divergent from the proposed combination, but rather *may* render Ober’s system somewhat inferior.

We have reviewed Patent Owner’s contrary arguments and evidence and given them due consideration, but we do not find that they rebut Petitioner’s persuasive showing and evidence.

(b) Claim 7

Claim 7 depends from claim 1 and further recites:

wherein said system control circuit comprises:

a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit;

a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied; and
a status register that judges a state of said central processing unit immediately after being released from said third special mode.
Ex. 1001, 15:3–13.

Petitioner contends Ober teaches or suggests the additional limitations of this claim. Pet. 45–49. Regarding the recited “a frequency division ratio setting register that sets a frequency division ratio of the clock generated by said clock generation circuit” limitation, Petitioner contends Ober’s power management subsystem 26 includes “a programmable special function register (SFR) 62” and clock subsystem 64 for generating a system clock. *Id.* at 45 (citing Ex. 1004, 5:59–64). Petitioner explains register 62 configures different aspects of system clock generation, including when placing the system in various SLEEP modes by dividing the system clock by 2, 4, or 128. *Id.* (citing Ex. 1004, 11:6–13, 11:31–33).

As to the recited “a clock halting register that receives the clock from said clock generation circuit and individually sets the clock to be halted or supplied” limitation, Petitioner asserts “[a]s explained above,” Ober discloses an IDLE power mode, which “allows the operating [s]ystem or application software to stop the core CPU clocks in order to reduce power consumption.” *Id.* at 46 (quoting Ex. 1004, 15:14–16) (emphasis omitted). Petitioner explains the IDLE mode is activated by a register, such as register 62, which includes a power manager field referred to as “Request Sleep.” *Id.* at 46–47 (citing Ex. 1004, 10:16–28) (reproducing Table 5 in part). Petitioner states Ober explains that the REQSLP (Request Sleep) signal allows the power management state machine “to be configured for different

reduced power modes of operation[:] IDLE, SLEEP, and DEEP SLEEP.” *Id.* at 47 (quoting Ex. 1004, 11:15–21). Based on the foregoing, Petitioner asserts Ober’s register 62 can be set to “Idle Request” where the IDLE mode will be entered into and the clock to the CPU (as well as selected principal CPU constituents optionally) will be halted. *Id.* (citing Ex. 1003 ¶ 154). When a “no sleep request” is made, the clock is supplied to the CPU. *Id.*

Regarding the recited “a status register that judges a state of said central processing unit immediately after being released from said third special mode” limitation, Petitioner contends, “[a]s explained above,” Ober’s DEEP SLEEP MODE maps to the “third special mode.” *Id.* at 48. Petitioner next states Ober describes checking a status register that “judges a state of said central processing unit immediately after being released from said third special mode” as recited. *Id.* (citing Ex. 1011, 11–12). Petitioner asserts Ober discloses a status indicating a CPU state on exit from Deep Sleep Mode,²¹ such as “the CPU must check the status [t]o identify why it came out of a PMSM SFT RW bit.” *Id.* at 48 (quoting Ex. 1004, 16:63–65). Petitioner asserts the “reasons include ‘cold boot, soft boot, watchdog reset or sleep mode wakeup.’” *Id.* (quoting Ex. 1004, 16:65–67). Petitioner notes that Ober does not state where the status is stored, but asserts Ober suggests to an ordinary artisan that it would be stored in Ober’s register, such as register 62 of Ober’s power manager. *Id.* at 48–49 (citing Ex. 1003 ¶ 158). Petitioner also contends register 62 already defines a field referred to as “PMS[T] (Power Management State)” (Ex. 1004, 10:34–36) and the PMST field includes “read only bits” that “enable[] the power management state to

²¹ Petitioner asserts this is “also known as SLEEP MODE (Clock Not Distributed).” Pet. 48.

be read by the system for debug and development.” Pet. 49 (quoting Ex. 1004, 11:24–27). Petitioner asserts an ordinarily skilled artisan “would have found it obvious that PMST could have been used to debug why the CPU ‘came out of’ DEEP SLEEP MODE because it describes the state of the power management state machine.” *Id.* (citing Ex. 1003 ¶ 158²²).

Lastly, Petitioner notes that the ’519 patent uses the term “register” broadly, explaining that a register “may be constituted by separately using a single register or by complexly using two or more registers.” *Id.* at 45 (quoting Ex. 1001, 5:23–27). Thus, even though the ’519 patent describes its registers separately, Petitioner asserts the registers “could still all be implemented as [a] single register under different bit fields.” *Id.* (citing Ex. 1003 ¶ 149). Petitioner next contends register 62 may be both a “frequency division ratio setting register” and claim 1’s “register.” *Id.* at 46. Petitioner makes similar contentions for claim 7’s recited “clock halting register” and “status register.” *See id.* at 47, 49. Petitioner further asserts that an ordinarily skilled artisan “would have found it merely a design choice to use one register with different fields or different registers for storing data” if claim 7 is construed to require physically separate registers from claim 1. *Id.* at 46 (citing Ex. 1003 ¶ 150); *see id.* at 47, 49 (citing Ex. 1003 ¶¶ 155, 159²³ when addressing the “clock halting register” and “status register”).

²² Cited paragraph 153 addresses the “clock halting register” and discusses Ober’s Table 5. We understand Petitioner to be referring to paragraph 158.

²³ Paragraph 154 address the “clock halting register.” Ex. 1003 ¶ 154. We understand Petitioner to be referring to paragraph 159.

Aside from any challenges related to Ober discussed in Section II(D)(3)(a)(i), Patent Owner does not separately challenge Petitioner’s ground for claim 7. *See* Resp. 26–61.

Based on Petitioner’s arguments and un rebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Ober teaches or suggests the limitations as recited in claim 7.

(c) Claims 10 and 11

Claims 10 and 11 depend from claim 1. Claim 10 recites “wherein said first memory and said second memory are two independent memories which are separated from each other.” Ex. 1001, 16:9–11. Claim 11 recites “wherein said first memory and said second memory are formed to coexist in one memory, sharing memory area of said one memory.” *Id.* at 16:12–14.

Petitioner contends the combination of Ober and Nakazato teaches or suggests claims 10 and 11. Pet. 50. Petitioner states Nakazato’s power-saving driver teaches or suggests the recited “clock control library” and Nakazato’s power-saving utility teaches or suggest the recited “application program.” *Id.* (citing Ex. 1003 ¶ 161). Petitioner also states Nakazato describes that its main memory stores both its utility and driver. *Id.* (citing Ex. 1008, 5:1–3). Petitioner also contends Ober discloses that its memory can be two separate memories (i.e., memory banks 54 and 56), which can be dynamic random access memory (DRAM). *Id.* (citing Ex. 1004, 5:50–53). Petitioner contends that an ordinarily skilled artisan would have understood that Ober’s memory banks are effectively main memory because they are DRAM and they are the only memory on Ober’s SoC. *Id.* at 50–51 (citing Ex. 1003 ¶ 161).

Based on the above discussion, Petitioner further contends an ordinarily skilled artisan would have found it obvious to run Nakazato's driver and utility on the same or different memory banks (i.e., memory banks 54 and 56) in Ober's SoC when executing Nakazato's software with Ober's SoC due to the computer memory's nature at any given time. *Id.* at 51 (citing Ex. 1003 ¶ 170²⁴). Petitioner further argues Dr. Albonesi explains that "this would merely depend on how large the OS is, how large Nakazato's driver and utility programs are, how many other applications would be executing on Nakazato's SoC, and how the OS allocates memory to drivers and user applications." *Id.*

Patent Owner does not separately challenge Petitioner's ground for claims 10 and 11. *See* Resp. 26–61.

Dr. Albonesi's Declaration at paragraphs 162, 165, and 170 (Ex. 1003 ¶¶ 162, 165, 170) do not appear to support the Petitioner's discussion of what "Dr. Albonesi explains." Pet. 51 (citing Ex. 1003 ¶ 170). Even so, based on Petitioner's other arguments and evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Ober and Nakazato teach or suggest the limitations as recited in claims 10 and 11.

(d) Conclusion – Claims 1, 7, 10, and 11

For all of the foregoing reasons, and after having analyzed the entirety of the record and assigning appropriate weight to the cited supporting evidence, we determine Petitioner has shown by a preponderance of the

²⁴ Paragraph 170 addresses Ground 2 and ACPI. Ex. 1003 ¶ 170. We understand Petitioner to be referring to paragraphs 162 and 165 to support this assertion.

evidence that claims 1, 7, 10, and 11 are unpatentable over the combination of Ober and Nakazato.

E. Obviousness of Claims 2–6 Over Ober, Nakazato, Cooper, and Windows ACPI (Ground 2)

1. Cooper (Ex. 1007)

Cooper is a United States patent issued on November 23, 2004, and filed on August 10, 1999. Ex. 1007, codes (22), (45). According to Petitioner, it is prior art under 35 U.S.C. § 102(e). Pet. 12. Patent Owner does not dispute Cooper’s prior-art status.

Cooper describes a computer system that can operate at different performance states and can transition dynamically between performance states. Ex. 1007, code (57). To manage performance states, Cooper has a processor that includes configuration control, including adding objects to a configuration specification (e.g., the ACPI (Advanced Configuration and Power Interface) specification) or adding a separate driver to an existing OS to control the processor performance states. *Id.* at 8:30–44, 16:33–34.

Cooper states a Performance Supported States (_PSS) object is “a package of packages describing all of the processor performance states that the given platform can support at any point in time.” *Id.* at 17:8–11. Cooper discloses that each object’s package describes a performance state and contains six parameters: frequency, power, performance control value, voltage control value, and voltage status value. *Id.* at 17:11–14.

Once the OS in Cooper decides to initiate a performance transition, the OS retrieves the object in the _PSS package that describes the state, writes the control value to the PERF_CNT1 register, reads the PERF_CNT2

register to initiate the transition, and determines whether the transition was successful. *Id.* at 18:6–18.

2. *Windows ACPI (Ex. 1005)*

Windows ACPI is a Microsoft white paper, dated November 11, 1998 (Version 0.91), and contains “© 1998 Microsoft Corporation” on each page. Ex. 1005, 1–23. According to Petitioner, this reference is prior art under 35 U.S.C. § 102(b). Pet. 12. As discussed below, Patent Owner disputes Windows ACPI’s prior-art status.

Windows ACPI “documents the Microsoft-provided interface offered by the ACPI Driver to other kernel-mode drivers.” Ex. 1005, 1. Windows ACPI explains “this interface enables drivers to use the ACPI framework (control methods, ACPI Name Space, event handling, and the Global Lock mechanism).” *Id.* at 2. Specifically, “the interface offered by the ACPI Driver enables drivers to: • Run control methods found in the device driver’s device object in the ACPI name space.” *Id.*

Windows ACPI documents (1) the constants and data structures used by the ACPI Driver interface, (2) the ACPI functions that can be called by kernel-mode drivers, and (3) the callback function that can be registered by device drivers. *Id.* at 17–23.

3. *Discussion*

Petitioner contends claims 2–6 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Ober, Nakazato, Cooper, and Windows ACPI (“Ground 2”). Pet. 51–63.

(a) Windows ACPI’s Status as a Printed Publication

Patent Owner argues that Exhibit 1005 (Windows ACPI) is not a printed publication and thus, the combination as presented in Ground 2 must

be rejected. Resp. 64–67 (citing *Hulu, LLC, v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 (PTAB Dec. 20, 2019) (precedential) (hereafter “*Hulu*”). Patent Owner asserts the testimony in “the declaration of Christopher Butler” (Ex. 1021)²⁵ “is unadorned with any of the attachments that are purported subjects of his testimony” and the Petition makes no attempts to connect the ZIP file links in the Butler Declaration with Exhibit 1005. Resp. 65. Patent Owner argues that the testimony (1) shows that the identified ZIP file was on the Microsoft.com website, (2) does not show that the ZIP file was indexed on a directory listing or search engine, linked to a Microsoft.com webpage, or otherwise made accessible such that the public could extract “the purported document from the ZIP file” (Resp. 66) and (3) does not show that the public had an indication that a ZIP file was hosted at

http://www.microsoft.com:80/hwdev/download/acpidri11_98.ZIP. *Id.*

Patent Owner also argues that Petitioner does not provide evidence that the Internet Archive’s Wayback Machine (“the Wayback Machine”) archived any webpage on the Microsoft website that indexed Exhibit 1005, and Exhibit 1005 is “analogous to the FTP document” in *SRI International Inc.*, where the contested document was not indexed or catalogued and could not be found through tools for customary and meaningful research. Resp. 65–66 (citing *SRI Int’l Inc. v. Internet Sec. Sys., Inc.*, 511 F.3d 1186, 1196 (Fed. Cir. 2008)). As for Dr. Albonesi, Patent Owner asserts his testimony is conclusory with no supporting evidence that an ordinarily skilled artisan

²⁵ Exhibit 1021 is entitled “Affidavit of Christopher Butler.” Exhibit 1021 (“the Butler Declaration”).

would have known to look on the hardware development section on “Microsoft.com.” *Id.* at 66–67.

Petitioner disagrees, citing to: (1) the Butler Declaration (Ex. 1021), (2) a Microsoft Windows Driver and Hardware Development webpage (Ex. 1020), (3) Dr. Albonesi’s testimony (Ex. 1003 ¶ 43; Ex. 1028 ¶¶ 57–62), and (4) Dr. Przybylski’s testimony (Ex. 1029, 154:16–155:4, 165:12–21, 167:8–168:7). Reply 23–25. Petitioner argues that Exhibit 1020 demonstrates Exhibit 1005 was indexed on Microsoft’s website. *Id.* at 24 (reproducing Ex. 1020) (highlighting portion titled “ACPI Driver Interface Design Notes and Reference” under “White Papers:”). Petitioner contends that the noted highlighting portion includes a link to the ZIP file that includes Exhibit 1005. *Id.* at 25; *see id.* 25 n.1 (stating that placing a cursor over the highlighted link “is in fact the same zip file as referenced in the Butler declaration”); Ex. 1028 ¶¶ 56–62; Ex. 1029, 154:16–155:4, 165:12–21.

Upon consideration of both parties’ arguments and evidence, we determine that Petitioner has demonstrated by a preponderance of the evidence that Exhibit 1005 was publicly accessible before the critical date of the ’519 patent and qualifies as a printed publication. *Hulu* indicates demonstrating a reference is printed publication is “based on the totality of the evidence.” *Hulu* at 3, 21. The Federal Circuit also indicates determining whether a document is a printed publication “involves a case-by-case inquiry into the facts and circumstances surrounding the reference’s disclosure to members of the public.” *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018) (quoting *In re Klopfenstein*, 380 F.3d 1345, 1350 (Fed. Cir. 2004)).

In our Institution Decision, we noted our understanding that Petitioner had identified February 25, 2002, as the earliest possible priority date of the '519 patent. Dec. Inst. 54. Patent Owner does not challenge the identified priority date. *See* Resp. 64–67.

Petitioner provides several forms of evidence that collectively establish that Exhibit 1005 was publicly accessible as of the critical date. The evidence includes: (1) document indicia, such as a copyright notice (Ex. 1005), (2) other publicly available information related to Exhibit 1005 (Ex. 1020, 1), (3) the Butler Declaration (Ex. 1021), (4) the Albonesi's testimony (Ex. 1003 ¶ 43; Ex. 1028 ¶¶ 56–62), and (5) Dr. Przybylski's deposition testimony (Ex. 1029: 167:8–168:7).

Turning to the evidence, Exhibit 1005 is entitled “Microsoft, Hardware White Paper” and further entitled “Draft ACPI Driver Interface Design Notes and Reference,” and has a version number of “Version 0.91,” a version date of “November 11, 1998” on its cover page, and a 1998 copyright date on all its pages. Ex. 1005, 1–23. Exhibit 1020, a screenshot of Microsoft Windows's Driver and Hardware Development web page as of June 10, 2001 taken from the Wayback Machine (i.e., <https://web.archive.org/web/20010610152934/http://www.microsoft.com/hwdev/OnNow/>), includes a list of various White Papers, including ACPI Design White Papers, such as “ACPI Driver Interface Design Notes and References.” Ex. 1020, 1. This listing describes the white paper as “version 0.91” and having “file date: November 11, 1998” (Ex. 1020, 1), matching Exhibit 1005's cover page (Ex. 1005, 1).

Further, Dr. Przybylski acknowledges Exhibit 1020 was captured on June 10, 2001, and this exhibit is “the Microsoft Windows driver and

hardware development” web page (Ex. 1029, 165:9–10) or “HD Dev site” (*id.* at 165:19). *See id.* at 164:6–165:21. Dr. Przybylski also acknowledged that this web page includes “White Papers” (*id.* at 166:2), “an ACPI Driver Interface Design Notes” (*id.* at 166:4), and “Version 0.91” (*id.* at 166:7), bolstering that Exhibit 1005 was publically accessible on Microsoft’s website as of June 10, 2001.

The Butler Declaration (Ex. 1020) identifies six URLs, including https://web.archive.org/web/19990504172738if_/http://www.microsoft.com:80/hwdev/download/acpidri11_98.ZIP, and explains that such a URL is assigned a format that includes its year, month, and day that it was archived. Ex. 1021, 1. Using the above URL, the link describes a webpage on Microsoft’s web page (i.e., www.microsoft.com) related to hardware development (i.e., “hwdev”) that has a date of November 1998. Thus, the Butler Declaration supports that the URLs of its referred-to zip files, including the above-identified URL, are files on Microsoft’s hardware development webpage, just as Exhibit 1020 illustrates. The Butler Declaration further supports that the above referred-to zip file concerns an ACPI White Paper listed on Exhibit 1020, which is a screenshot of Microsoft’s Driver and Hardware Development webpage, because its date (November 1998) (Ex. 1020, 1) matches with Exhibit 1020’s “ACPI Driver Interface Design Notes and References” zip file link’s date of November 11, 1998 (Ex. 1020, 1).

The Butler Declaration further provides evidence that the identified zip file was archived (e.g., catalogued) on the Wayback Machine as of May 4, 1999 (e.g., “19990504172738if_” portion of the identified URLs) and on other dates (e.g., July and August, 2000 and June, August, and November,

2001), which is prior to the earliest possible priority date of the '519 patent. The Butler Declaration supports this determination even though the referred-to “Exhibit A,” which purportedly includes copies of printouts of the Internet Archives records of the .zip files for the listed URLs, has not been located in the record.²⁶

Patent Owner’s comparison of Exhibit 1005 to the FTP document in *SRI International* does not hold. Resp. 66. An FTP server in *SRI International* was found to be not publically accessible because the server contained no index or catalogue. *SRI Int’l*, 511 F.3d at 1196. Here, Exhibit 1020 provides evidence to the contrary, showing the relevant Microsoft.com website was indexed, catalogued, or organized in some fashion, such that “ACPI Design” information, including the above-identified White Paper matching Exhibit 1005’s description (i.e., ACPI Driver Interface Design Notes and Reference), could be searched and located through a customary search tool (e.g., Microsoft’s hardware development webpages). See Ex. 1020, 1. Notably, Exhibit 1020 includes various hyperlinks, including “ACPI web site” (left column under “See also:”), drop-down menus, such as “White Papers” and “ACPI Design White Papers,” and a “Search” function. See *id.*

²⁶ Petitioner contends that the reference to Exhibit A “is a typographical error” and “a vestige of the Internet Archive’s Wayback Machine’s boilerplate affidavit language.” Pet. Opp. Mot. Exclude 2 n.1. Petitioner also contends “it would be impractical to attach the linked zip files (which are binary files) as a ‘printout.’” *Id.* Patent Owner asserts this argument has been refuted by supplying untimely “‘printouts’ of archived web pages.” PO Reply Mot. Exclude 2. We address the untimeliness issue below.

Exhibit 1020 also indicates the Microsoft.com webpage was obtained using the Wayback Machine because Exhibit 1020 includes the URL <https://web.archive.org/web/20010610152934/http://www.microsoft.com/hwdev/OnNow/>, which according to the Butler Declaration, demonstrates the website was archived or catalogued on June 10, 2001. Ex. 1020, 1 (URL on the page's bottom and June 10, 2001 highlighted on the top right). In any event, the Federal Circuit has stated that “[w]hile cataloging and indexing have played a significant role in our cases involving library references, we have explained that neither cataloging nor indexing is a necessary condition for a reference to be publicly accessible.” *In re Lister*, 583 F.3d 1307, 1312 (Fed. Cir. 2009) (citing *Klopfenstein*, 380 F.3d at 1348).

Dr. Albonesi and Dr. Przybylski only bolster that Exhibit 1005 was made publically available to and could be located by the interested public and ordinary artisans who exercise reasonable diligence. *See SRI Int'l*, 511 F.3d at 1194. Dr. Albonesi testifies that a person having ordinary skill in the art or “the interested public seeking information on how to integrate power management . . . would have known to look at the hardware development section [of] the Microsoft.com website.” Ex. 1003 ¶ 43 (discussing Ex. 1005). In rebutting Patent Owner’s assertions related to Exhibit 1005’s public accessibility, Dr. Albonesi provides even further evidence that Exhibit 1005 could be located and was accessible through the Microsoft website. *See* Ex. 1028 ¶¶ 56–62.²⁷ Also, Dr. Przybylski indicates that moving a mouse over and clicking on the link in Exhibit 1020 labeled “the ACPI Interface Design Notes and Reference” (Ex. 1020, 1), reveals “a

²⁷ Below, we address Patent Owner’s contentions related to the timeliness of this evidence.

captured zip file” (Ex. 1029, 167:21) named “ACPIDRI11_98.zip” (id. at 168:4). *Id.* at 167:8–168:7.

Based on the total evidence in the record, Petitioner has established by a preponderance of the evidence that Exhibit 1005 qualifies as a printed publication.

(b) Claim 2

Claim 2 recites

A system LSI as claimed in claim 1, wherein said clock control library comprises:

a plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit; and

a main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit.

Ex. 1001, 14:48–57.

Petitioner persuasively maps that these limitations are taught or suggested by the combination of Ober, Nakazato, Cooper, and Windows ACPI. Pet. 51–63. When addressing the “plurality of libraries that control said system control circuit and said clock generation circuit to transition the clock frequencies supplied to said central processing unit” limitation in claim 2, Petitioner contends that Ober, Nakazato, and Cooper teach or suggest this element. *Id.* at 57. More specifically and as explained above, Petitioner contends that Cooper states ACPI objects are associated with processor performance control and explains that numerous ACPI objects, known as CPU performance objects, are used with controlling CPU clock frequency in system. *Id.* at 53 (citing Ex. 1007, 16:33–34), 57 (same).

Petitioner states Cooper further explains some ACPI objects include additional ACPI objects, such as “_PSS” object having ACPI sub-objects that describe performance states and contain parameters, including frequency, power, and performance control values. *Id.* at 57 (quoting Ex. 1007, 17:11–14).

Petitioner states all ACPI CPU performance objects in Cooper collectively “constitute the ‘plurality of libraries’” as claim 2 recites, because they are used in the same manner as the libraries described in the ’519 patent (*id.* at 57–58) and perform the same function of “control[ling] said system control circuit and the clock generation circuit as well to transit the clock state supplied to the central processing unit.” *Id.* at 58 (quoting Ex. 1001, 4:31–33; Ex.1003 ¶ 185); *see id.* at 53 (citing Ex. 1001, 4:30–37). Petitioner elaborates, stating Cooper describes “[o]nce the OS has decided to initiate a performance transition,’ the OS through its ACPI interface (i.e. main library), ‘retrieves the[] _PSS package that describes th[e] state,’ ‘writes the control value to the PERF_CNT1 register,’ and performs a ‘read of the PERF_CNT2 register to initiate the transition.’” *Id.* at 58 (citing Ex. 1007, 18:6-13); *id.* at 53–54 (same). Petitioner concludes that the ACPI objects control hardware to initiate a CPU clock frequency like the claimed “plurality of libraries” as recited in claim 2. *Id.* at 58.

Regarding the “main library which is called by said application program and selects any one of said libraries in correspondence with the clock frequency supplied to said central processing unit” element in claim 2, Petitioner contends Ober, Nakazato, Cooper, and Windows ACPI teach or suggest this limitation. *Id.* at 58–61. Petitioner contends Windows ACPI driver (i.e., “a main library” in claim 2) enables other drivers to “[r]un

control methods found in the device driver’s device object in the ACPI name space.” Ex. 1005, 2²⁸, *quoted in* Pet. 58–59. Petitioner further contends the Windows ACPI driver allows another driver to load the same object types as those in Cooper and to execute processes on the object types, such as writing to the “PERF_CNT” registers. Pet. 59 (citing Ex. 1003 ¶ 188). Petitioner provides reasons why the Windows ACPI driver, when combined with Ober, Nakazato, and Cooper, “constitutes a ‘main library,’” including that the driver would be responsible for selecting, loading, and writing the appropriate ACPI objects “in correspondence with the clock frequency supplied to the said central processing unit” as recited in claim 2. *Id.* at 59–60 (citing Ex. 1007, 18:6–13, 19:19–22; Ex. 1003 ¶¶ 189–190); *id.* at 53–54, 58. Petitioner persuasively contends the ACPI driver is also “called by said application program” as claim 2 recites, because it is merely an interface provided by Windows OS to allow other drivers to call ACPI functions. *Id.* at 60 (citing Ex. 1005, 3).

Petitioner persuasively provides reasons to combine Ober, Nakazato, Cooper, and Windows ACPI (*id.* at 51–57, 60–61), including to allow the system to support “a wider variety of OSs and applications” by using the well-known ACPI technology taught by (1) Cooper to control CPU clock frequency and effectuate a clock frequency transition (*id.* at 52–55 (citing Ex. 1003 ¶¶ 169–170, 174, 178; Ex. 1007, 8:32–34, 8:38–40, 16:33–34, 18:6–13, 19:19–22; Ex. 1001, 4:30–37)) and (2) Windows ACPI for the specific implementation of how one would use an OS to control ACPI, including using the Windows ACPI driver to act as a “main driver” that

²⁸ Petitioner indicates support is found on page 3, but we located this discussion on page 2.

selects appropriate ACPI objects as claim 2 recites (*id.* at 54–56 (citing Ex. 1003 ¶¶ 174, 176–177; Ex. 1005, 2)). Petitioner also persuasively asserts that the combination would be nothing more than combining the prior art elements according to known methods to yield predictable results because Cooper and Windows ACPI explain how to modify Nakazato’s driver to control a CPU using ACPI, Ober explains how hardware in such a system would operate, and Nakazato’s utility would then be used to control an ACPI-enabled driver in the same fashion Nakazato describes to cause CPU clock frequency transitions. *Id.* at 56–57 (citing Ex. 1003 ¶¶ 179–180), 60–61 (referring to “Section VI.B.1”) (citing Ex. 1003 ¶¶ 191–192).

Patent Owner argues that Petitioner and Dr. Albonesi do not assert or indicate “that the Ober/Nakazato combination is ACPI-compatible.” Resp. 63. For this reason, Patent Owner argues Petitioner has not provided an adequate reason why an ordinary artisan would have been motivated to install a Windows ACPI driver and objects into the Ober/Nakazato system as proposed. *Id.* at 64. Patent Owner also argues that installing Cooper’s ACPI objects and the Windows ACPI driver within the Ober/Nakazato system would not have yielded predictable results. *Id.* at 63–64 (citing Ex. 1003 ¶ 42; Ex. 1007, 8:57–65). Patent Owner also asserts there is no motivation to install Windows ACPI driver and objects because Nakazato already provides “this power management function.” *Id.* at 64. Patent Owner further argues Petitioner’s explanation is conclusory and based on hindsight. *Id.* (citing *TQ Delta*, 942 F.3d at 1352).

Petitioner contends that Patent Owner’s arguments are “unsupported attorney argument” and “mischaracterize[] the Petition.” Reply 22. Petitioner contends that Ober does not suggest that the reference is ACPI-

incompatible, but in any event, the Petition does not rely on Ober being ACPI-compatible. *Id.* at 22–23 (citing Ex. 1028 ¶¶ 53–55). Rather, Petitioner asserts that the ground proposes to modify the Ober/Nakazato system “to make them ACPI compatible.” *Id.* at 23 (citing Pet. 56; Ex. 1029, 162:20–163:2).

Patent Owner counters that Petitioner now asserts that the ground proposed to make the Ober/Nakazato system “ACPI-compatible,” but this “ignores ACPI’s warning against using unused bits” (Sur-reply 1), which, as argued, would cause unpredictable results in Ober’s SFR 62 (*id.* at 14–15 (citing Ex. 1013, 65–66)).

Petitioner has provided an adequate reason with a rational underpinning why an ordinary artisan would have been motivated to install a Windows ACPI driver and objects into the Ober/Nakazato system. *See* Pet. 52–56; *see* Ex. 1003 ¶¶ 169, 179–80; Ex. 1028 ¶¶ 53–55. Notably, *KSR* overturned the approach previously used by the Federal Circuit requiring that some teaching, suggestion, or motivation must be found in the prior art. *KSR*, 550 U.S. at 415. Thus, Ober need not to state whether it is ACPI-compatible or disclose ACPI features in order to provide a reason with some rational underpinning for installing a Windows ACPI driver and objects into the Ober/Nakazato system. *See id.* at 418. Moreover, to the extent Patent Owner’s argument implies that Ober and Nakazato are not ACPI-compatible (*see* Resp. 63–64), this is counsel’s argument, which cannot take the place of objective evidence. *See Johnston v. IVAC Corp.*, 885 F.2d 1574, 1581 (Fed. Cir. 1989) (noting that attorney argument is “no substitute for evidence”). In any event, Dr. Albonesi testifies that “nothing in Ober suggests that it is

incompatible with ACPI” (Ex. 1028 ¶ 54), and Patent Owner does not contradict this finding. *See generally* Sur-reply.

Turning to Patent Owner’s argument that Petitioner’s reason to combine argument is untimely, the Petition states “Nakazato’s proprietary driver” in the combined Ober/Nakazato system would have limited applicability and would only support a “limited number of OSs and applications that are compatible with such a driver.” Pet. 52 (citing Ex. 1003 ¶ 169). The Petition further states an ordinarily skilled artisan would have thus been motivated to find solutions to support “a wider variety of OSs and applications” and to ensure wider compatibility, such as the teachings related to the ACPI driver and objects, which were well-known and widely-implemented as of the ’519 patent’s priority date. *Id.* at 52–53, 56 (stating “ACPI is a common interface provided by OSs”). Thus, contrary to Patent Owner’s assertion, Petitioner has not presented a “belated attempt” to make Ober/Nakazato system ACPI-compatible. *See* Sur-reply 1.

Dr. Przybylski also recognizes ACPI as a standard to be “leverage[d].” *See* Ex. 162:20–163:4 (responding “Yes” to a question related to “to leverag[ing] the standardized support of ACPI”). This provides one reason an ordinarily skilled artisan would have turned to the teachings in Cooper and Windows ACPI, which both address how to use and implement ACPI-technology. In essence, Petitioner asserts, and we agree, these teachings would have improved the Ober/Nakazato system by ensuring wider compatibility. *See* Pet. 52–55; *see also KSR*, 550 U.S. at 417 (stating “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar

devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.”).

The Petition further addresses how the combination “would be nothing more than combining prior art elements according to known methods to yield predictable results” (Pet. 56 (citing Ex. 1003 ¶ 179)), which is another obviousness rationale supported by *KSR*. See *KSR*, 550 U.S. at 416 (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”); see also Ex. 1028 ¶ 53 (noting Patent Owner’s arguments “fail[] to account for the motivation of a POSITA”).

Also, we disagree with Patent Owner’s assertions that the combination of Ober, Nakazato, Cooper, and Windows ACPI ignores ACPI’s warning against using unused bits and would create unpredictable system. See Sur-reply 1. Rather, as discussed when addressing claim 1 in Section II(D)(3)(a)(ii) and limitation 1.1, the register bits will be defined and used, such that the system will not behave unpredictably.

Having considered the entirety of the trial record, we find (1) the combination of Ober, Nakazato, Cooper, and Windows ACPI discloses the limitations in claim 2 and (2) the Petition provided a reason with a rational underpinning to combine the teachings of Ober, Nakazato, Cooper, and Windows ACPI to provide the limitations recited in claim 2.

(c) Claims 3–6

Claims 3 through 6 ultimately depend from claim 2. Claim 3 recites “said main library is described using a same program language as said application program” (Ex. 1001, 14:58–50); claim 4 recites “said application program and said main library are described using C language” (*id.* at

14:61–63). Petitioner contends the combination of Ober, Nakazato, Cooper, and Windows ACPI teaches these limitations. Pet. 61–62.

Petitioner persuasively maps Windows ACPI and what one skilled in the art would have recognized as a well-known programming language at the time of the invention to the limitations of claims 3 and 4. *Id.* at 61. That is, Petitioner contends (1) selecting a programming language is a mere design choice, the C programming language being well-known at the time of the invention, including for writing OSs and hardware functions; and (2) the Examiner took Official Notice that writing application programs and main libraries in the C programming language was known, which was not challenged during prosecution. *Id.* (citing Ex. 1003 ¶ 195; Ex. 1002, 386–87). Petitioner further contends Windows ACPI describes its driver as being written in C. *Id.* (citing Ex. 1005, 17–23; Ex. 1003 ¶ 196).

Patent Owner does not separately argue claims 3 and 4.

Based on Petitioner’s arguments and unrebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Windows ACPI in combination with Ober, Nakazato, and Cooper disclose claims 3’s and 4’s limitations.

Claim 5 recites “each of said libraries is described using a program language capable of directly controlling said clock generation circuit and said system control circuit” (Ex. 1001, 14:64–67); claim 6 recites “each of said libraries is described using an assembler language” (*id.* at 15:1–2). Petitioner contends the combination of Ober, Nakazato, Cooper, and Windows ACPI teaches these limitations. Pet. 62–63.

Petitioner persuasively maps Cooper's ACPI objects and what one skilled in the art would have recognized related to programming ACPI objects to claim 5's and claim 6's limitations. *Id.* at 62. More specifically, Petitioner contends an ordinarily skilled artisan would have understood ACPI objects and sub-objects were written in a programming language known as ACPI Machine Language (AML), which can issue events to an object and notify the OS, as evidenced by Cooper. *Id.* (citing Ex. 1007, 13:18–21, 14:58–61, 21:28–31). Petitioner contends Cooper also explains that its AML is used to control directly the clock generation circuit and the system control circuit because it writes a control value to one register and reads another register to initiate a transition, both registers being involved with controlling the CPU performance state. *Id.* at 63 (citing Ex. 1007, 18:6–13, 19:4–8; Ex. 1003 ¶ 200). Petitioner further contends an ordinarily skilled artisan would have understood AML itself is an assembler language. *Id.* at 62–63 (citing Ex. 1003 ¶ 199; Ex. 1022, 1; Ex. 1013, ¶ 411).

Patent Owner does not separately argue claims 5 and 6.

Based on Petitioner's arguments and unrebutted evidence, which we find to be persuasive and supported by the cited disclosures, we find Petitioner has proven, by a preponderance of the evidence, that Cooper in combination with Ober, Nakazato, and Windows ACPI disclose claims 5's and 6's limitations.

4. Conclusion

After having analyzed the entirety of the record and assigning appropriate weight to the cited supporting evidence, we determine Petitioner has shown by a preponderance of the evidence that that claims 2–6 are

unpatentable over the combination of Ober, Nakazato, Cooper, and Windows ACPI.

*F. Obviousness of Claims 8 and 9 Over Ober, Nakazato,
and Doblar (Ground 3)*

1. Doblar (Ex. 1006)

Doblar is a United States patent issued on February 4, 2003, and filed on May 27, 1999. Ex. 1006, codes (22), (45). According to Petitioner, Doblar is prior art under 35 U.S.C. § 102(e). Pet. 12. Patent Owner does not dispute Doblar's prior-art status.

Doblar relates to “employing redundant, synchronous clock distribution.” Ex. 1006 1:8–9. Doblar explains that “[a]t the heart of many such synchronization circuits is some form of a phase locked loop (PLL)” (*id.* at 1:22–23) and that a “master clocking signal may be fed into a PLL to produce many identical clock signals (e.g., fanout) that are used to synchronize the components of the computer system” (*id.* at 1:32–34).

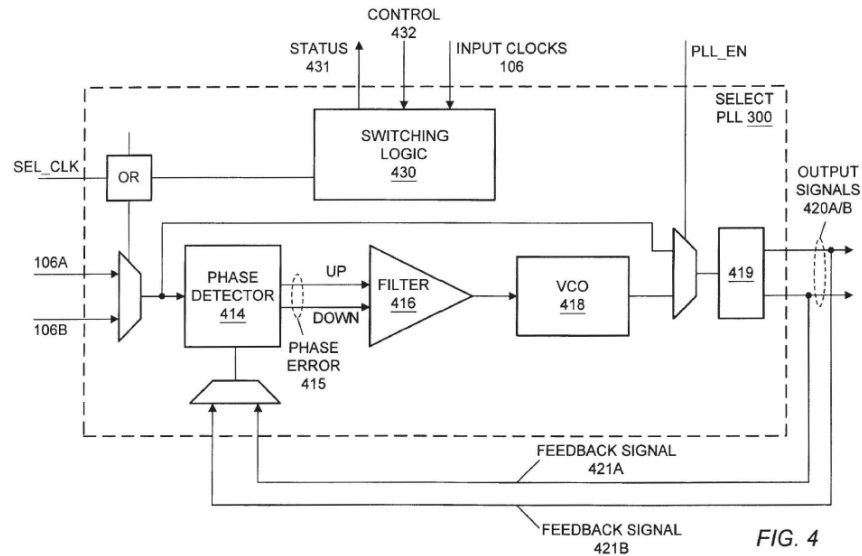
Doblar states

[t]he master clock signal is a critical component of the computer system. The failure of the master clock signal may disable the entire system. Thus, to alleviate this problem, some systems incorporate two master clock signals, one of which is redundant. Upon a failure of the first master clock signal, the system is shut down and may be reinitialized using the second master clock signal.

Id. at 1:35–41. An object of Doblar's system is to “provide a system that can fail-over from one clock source to another clock source without causing a disruption to system operations.” *Id.* at 1:43–45. Doblar describes a system that “causes the second clock source to provide a reference control signal to the second clock source” when the first clock signal fails so as to

provide continuous operation. *Id.* at 2:41–46. Doblar’s preferred embodiments provide a “redundant slave clock” upon “master clock” failure and do not interrupt system operations (e.g., a system halt or restart). *Id.* at 2:47–50.

Below, Doblar shows an embodiment of a select PLL in Figure 4.



Doblar’s Figure 4 shows a select PLL circuit 300. *Id.* at 2:66–67, 6:18–19, Fig. 4. On Figure 4’s left, Doblar’s first clock signal 106A and second clock signal 106B enter the select PLL, and signals 106A and 106B are preferably in phase on a rising edge, but their frequencies may differ by a multiple integer. *Id.* at 3:35–39. Doblar states its PLL receives first and second clock signals 106A and 106B from first and second clock source respectively. *Id.* at 6:20–23. Doblar discusses that an OR block (shown in Figure 4) receives a select clock input SEL_CLK, which “sets the identity of the primary clock input.” *Id.* at 6:26–27. Doblar states the output of the output multiplexer (shown on the right in Figure 4) is multiplied or divided by multiplier/divider 419, such as by 1, 2, or 4, to produce one or more PLL output signals 420 A/B. *Id.* at 6:57–61.

2. Discussion

Petitioner contends claims 8 and 9 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Ober, Nakazato, and Doblar (“Ground 3”). Pet. 63–73.

Claim 8 depends from claim 1 and further recites “wherein said clock generation circuit comprises: a PLL that receives a plurality of standard clocks and generates the clock if needed by multiplying said standard clocks; and a frequency division/selection portion that carries out frequency division or selection of said standard clocks or said multiplied standard clock.” Ex. 1001, 15:14–15, 16:1–6. Claim 9 depends from claim 8 and further recites “wherein one of said standard clocks uses a frequency of 32.768 kHz as a base oscillation.” *Id.* at 16:7–9.

Regarding claim 8, Petitioner persuasively relies on Ober and Doblar to teach or suggest its limitations. Pet. 68–72. For the limitation “a PLL that receives a plurality of standard clocks and generates the clock if needed by multiplying said standard clocks” in claim 8, Petitioner states Doblar suggests this limitation. *Id.* at 68–71. Petitioner initially notes that claim 8 recites “multiplying said standard clocks” “if needed,” and thus should be construed as not requiring multiplication. *Id.* at 68. Petitioner further notes the ’519 patent never receives multiple standard clocks but rather “one clock” which then multiplies the clock frequency itself. *Id.* at 68–69 (citing Ex. 1001, 9:32–33) (reproducing Ex. 1001, Fig. 4 (annotated)).

Petitioner further contends, even if claim 8 requires clock multiplication, Doblar teaches this arrangement. *Id.* at 69. In particular, Petitioner argues Doblar teaches a PLL within a clock generation circuit that receives standard clocks (e.g., clocks signals 106A and 106B), which differ

by an integer multiple. *Id.* at 69–70 (citing Ex. 1006, 3:37–39, 6:19–23) (reproducing Ex. 1004, Fig. 4 (annotated) to show clocks 106 A and 106B). Petitioner further asserts that Doblar suggests the clock sources for the clocks are “standard clocks” because they serve “the master clock signal” for its system. *Id.* at 70 (citing Ex. 1006, 3:39–43; Ex. 1003 ¶ 214). Petitioner contends Doblar’s PLL circuit “is also capable of multiplying the signals via ‘multiplier/divider circuit 419,’ which can multiply or divide ‘the output of the output multiplexer,’ such as ‘by 1, 2, or 4, to produce one or more PLL output signals 420 A/B.” *Id.* at 70 (quoting Ex. 1006, 6:57–61). Petitioner contends, once an input standard clock is selected, the clock is multiplied and outputted, such as the ’519 patent’s²⁹ Figure 4 shows. *Id.* (citing Ex. 1003 ¶ 215).

For the “frequency division/selection portion that carries out frequency division or selection of said standard clocks or said multiplied standard clock” element in claim 8, Petitioner persuasively maps Ober to this limitation. *Id.* at 71–72. Petitioner states Ober discloses clock circuit 108, which is connected to the Ober’s PLL output, and the clock circuit divides the outputted oscillation frequency from Ober’s PLL. *Id.* at 71–72 (citing Ex. 1004, 8:61–64) (reproducing Ex. 1003, Fig. 3 (annotated)).

Petitioner also refers to “section VI.C” for the motivation to modify Ober/Nakazato’s system with Doblar so as to achieve Doblar’s redundant clock scheme. *Id.* at 71 (citing Ex. 1003 ¶ 218). In the Petition’s § IV.C.1

²⁹ Although Petitioner refers to “Figure 4 of the ’519 patent” (Pet. 70), we understand this reference to be a typographical error intended to cite Figure 4 of Doblar similar to Dr. Albonesi’s testimony. *See* Ex. 1003 ¶ 215 (citing Ex. 1006, 6:57–62) (referring to “multiplier/divider circuit 419” in Figure 4).

(*id.* at 64–68), Petitioner discusses Ober’s clock generation circuit receiving clocks, Ober’s clock management system having at least three clocks, Ober’s PLL receiving a clock signal, and Ober’s PLL dividing the oscillation frequency. *Id.* at 64 (citing Ex. 1004, 8:61–9:3, Fig. 3) (reproducing Ex. 1004, Fig. 3 (annotated to show the clocks)), 72 (citing Ex. 1004, 8:61–64). Petitioner asserts Ober discloses PLL 106 receiving a clock but not multiple clocks (*id.* at 64), but contends that a system clock in systems “such as the 32-bit RISC CPU system” in Ober (*id.* at 64–65), “was a critical component in the operation of such system” because if the primary clock fails, the entire system fails. *Id.* at 65 (citing Ex. 1003 ¶ 205; Ex. 1025, 2:40–48; Ex. 1026, 1:15–22)). Petitioner contends an ordinarily skilled artisan would have been motivated to seek out references, like Doblar, “that mitigate against system clock failure.” *Id.*

Petitioner discusses that Doblar explains its master clock is a “critical component of the computer system” and that clock failure may “disable the entire system.” *Id.* (citing Ex. 1006, 1:35–41). Petitioner states Doblar also explains that systems having two master clocks were known but that, in the case of failure, a system reboot was required to engage the second clock. *Id.* (citing Ex. 1006, 2:44–52). Petitioner highlights Doblar’s PLL in a clock generation circuit that receives clocks from sources 106A and 106B and selects one clock as the primary clock input so if one clock fails the other can be used as the primary clock source. *Id.* at 65–66 (citing Ex. 1006, 3:39–43, 6:18–19) (reproducing Ex. 1006, Fig. 4).

Petitioner further contends an ordinarily skilled artisan would have found it obvious to combine Ober, Nakazato, and Doblar. *Id.* at 66. Namely, Petitioner states “[a]s explained above,” system clock failure is

catastrophic to the system’s operation so an ordinary artisan would seek out other approaches to “avoid or mitigate a clock failure, and Doblar is one such system.” *Id.* (citing Ex. 1003 ¶ 209). Because Ober discloses a clock subsystem with similar components to Doblar (*id.* at 66–67 (citing Ex. 1004, 8:53–9:3)), Petitioner asserts modifying Ober’s clock subsystem to include Doblar’s redundant clock architecture “would be nothing more than a simple substitution of one known element for another to obtain predictable results” (*id.* at 67 (citing Ex. 1003 ¶ 210)), including “higher uptime for the system” (*id.* at 68 (citing Ex. 1006, 2:18–21)). Petitioner proposes to replace Ober’s PLL 106 with Doblar’s PLL 300 “to achieve Doblar’s redundant clock scheme.” *Id.* at 67 (reproducing Ex. 1004, Fig. 3 (annotated)), 71–72 (same) (further citing Ex. 1003 ¶ 218). Petitioner asserts the once Ober is modified as proposed, PLL 106 would be fed to Ober’s clock circuit 108, which is “a frequency division/selection portion that carries out frequency division” as claim 8 recites. *Id.* at 72.

Patent Owner contends Petitioner’s ground for claims 8 and 9 “fall[s] with Ground 1’s failure to establish that Petitioner is likely to prevail as to claim 1.” Resp. 67. Petitioner argues that Patent Owner has not overcome the obviousness argument of Ground 1, and thus, Ground 3 should remain. Reply 25–26 (citing Pet. 63–73; Ex. 1028 ¶¶ 63–66). We agree with Petitioner for the reasons stated above related to Ground 1 and claim 1.

Patent Owner additionally asserts claims 8 and 9 are not obvious over Ober, Nakazato, and Doblar “because there is no motivation to combine” (*id.*) and “[a] person of ordinary skill in the art would not be motivated to combine references that independently operate effectively” (*id.* at 68 (citing *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F. 3d 1342, 1370 (Fed.

Cir. 2012)); *see* Sur-reply 20 (same)). Specifically, Patent Owner contends Doblar has a redundant clock system (Resp. 68 (citing Ex. 1006³⁰, 1:47–67), and Ober’s power management state machine has a built-in failsafe (e.g., in DEEP SLEEP and FAULT) to address failure conditions, such as catastrophic failure requiring a complete shutdown or fault condition when exiting a sleep or deep sleep mode. *Id.* (citing Ex. 1004, 16:46–53). Patent Owner argues that each of Ober and Doblar “operate effectively to address failures in the system,” “Dr. Albonesi does not explain why Ober’s existing solution for catastrophic failures is inadequate,” and the proposed combination reflects “impermissible hindsight.” *Id.* at 68–69 (citing *In re Wesslau*, 353 F.2d 238, 241 (C.C.P.A. 1965)); *see* Sur-reply 20. Patent Owner further argues that Petitioner does not identify a circumstance where Ober’s system clock failure does not also result in a system failure that causes the system to shut down completely, and if no circumstance exists, there is no motivation for an ordinarily skilled artisan to look to Doblar for a redundant clock. Sur-reply 20 (citing Ex. 1004, 16:49–50).

Petitioner argues that Patent Owner’s contentions that the motivation to combine Ober with Doblar is redundant over an alleged failsafe already in Ober has no supporting evidence as acknowledged by Dr. Przybylski. Reply 26 (citing Ex. 1029, 40:9–11). Petitioner asserts Patent Owner’s arguments confuse Ober’s system failures during DEEP SLEEP and FAULT states with Doblar’s system clock failures. *Id.* Petitioner argues that Ober confirms that “at least one clock is running during the DEEP SLEEP mode” and a clock signal is required to activate DEEP SLEEP mode. *Id.* (citing Ex. 1004,

³⁰ Patent Owner mistakenly refers to Exhibit 1008 (Nakazato) rather than Exhibit 1006.

15:5–6, 16:55–57; Ex. 1028 ¶ 65). Petitioner further argues that “multiple fault handling can be very beneficial in a computer system to ensure safe operation” (*id.*), and Doblar handles faults differently than Ober (*id.* at 26–27). Petitioner contends an ordinarily skilled artisan may have been motivated to supplement or replace Ober’s fault management with Doblar’s “according to design choice” even if the results may overlap. *Id.* at 27.

Having considered the parties’ arguments and evidence, we find that Petitioner provides a reason with a rational underpinning to combine Doblar with Ober and Nakazato. Petitioner asserts that (1) Ober discloses receiving a clock but not multiple clocks (Pet. 64), (2) Ober’s system clock is a critical component to its system’s operation in case of the clock’s failure (*id.* at 64–65 (citing Ex. 1003 ¶ 205; Ex. 1025, 2:40–48; Ex. 1026, 1:15–22)), and (3) an ordinarily skilled artisan would have been motivated to seek out references, like Doblar, (a) to mitigate against system clock failure (*id.*), (b) to build redundancies (*id.* at 66–67 (citing Ex. 1003 ¶ 209)), and (c) to include “higher uptime for the system” (*id.* at 68 (citing Ex. 1006, 2:18–21)). Notably, the latter rationale has not been challenged by Patent Owner.

Also, Ober discusses state conditions where there is a catastrophic failure or fault condition and does not necessarily relate to clock failures. *See* Ex. 1004, 16:47–57; Ex. 1028 ¶ 65. Thus, although Doblar addresses a master clock failure and providing a redundant clocks upon master clock failure (Ex. 1006, 1:1:47–67), Doblar’s teachings do not necessarily address a system failure as discussed in Ober, as Patent Owner asserts. *See* Resp. 68. On the other hand, Dr. Albonesi testifies that “Ober’s PLL 106 receive a clock,” not “multiple clocks” (Ex. 1003 ¶ 204), and “if the primary clock fails, the entire system will also fail” (*id.* ¶ 205), which implies that when

Ober's clock fails, its entire system will fail or go into a state of catastrophic failure (*id.* ¶ 209). *See* Sur-reply 20 (noting Petitioner does not identify a circumstance where the Ober's system clock failure does not result in a system failure).

In any event, even assuming Ober's approach to clock failure is catastrophic failure resulting in shutdown (*see* Ex. 1004, 16:49–50), this approach differs from Doblar's, which involves redundant clocks that avoid disruption to the system (e.g., shutting down). *See* Pet. 65 (citing Ex. 1006, 1:35–41, 2:44–52). Contrary to Patent Owner's assertions (*see* Sur-reply 20), Ober's approach therefore has inadequacies as noted by the Petition (Pet. 66 (noting system failure due to the clock); *see also* Ex. 1003 ¶ 205), and Doblar's technique improves on Ober by including multiple clocks that introduce include redundancies and mitigate system failure (Pet. 65–68; *see also* Ex. 1003 ¶¶ 205–211).

Having considered the entirety of the trial record, we find (1) the combination of Ober, Nakazato, and Doblar discloses the limitations in claims 8 and 9 and (2) the Petition provided a reason with a rational underpinning to combine the teachings of Ober, Nakazato, and Doblar to provide the limitations recited in claims 8 and 9.

3. Conclusion

After having analyzed the entirety of the record and assigning appropriate weight to the cited supporting evidence, we determine Petitioner has shown by a preponderance of the evidence that that claims 8 and 9 are unpatentable over the combination of Ober, Nakazato, and Doblar.

G. Patent Owner's Constitutional Challenges

Patent Owner contends this proceeding should be terminated because the Board lacks constitutional power to issue a final written decision in this proceeding under the Appointments Clause of the U.S. Constitution. Resp. 69–70. In particular, Patent Owner contends “Administrative Patent Judges (APJs) remain unconstitutionally appointed.” *Id.* at 69. We decline to consider Patent Owner’s constitutional challenge as the issue has been addressed by the Federal Circuit in *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320, 1328 (Fed. Cir. 2019). Although Patent Owner contends the Federal Circuit’s solution in *Arthrex* to the alleged constitutional defect is “insufficient because it does not give a constitutionally appointed principal officer power to review APJ decisions” (Resp. 69), this is not a matter for us to decide.

Patent Owner also argues “[t]he retroactive application of *inter partes* review to patents issued before the enactment of the America Invents Act violates the Due Process clause of the Fifth Amendment. It is also a physical and regulatory taking prohibited by the Takings Clause of the Fifth Amendment.” *Id.* at 70. The Federal Circuit has, however, rejected arguments that retroactive application of the AIA is unconstitutional, explaining as follows:

[T]he retroactive application of IPR proceedings to pre-AIA patents is not an unconstitutional taking under the Fifth Amendment. Patent owners have always had the expectation that the validity of patents could be challenged in district court. For forty years, patent owners have also had the expectation that the PTO could reconsider the validity of issued patents on particular grounds, applying a preponderance of the evidence standard. Although differences exist between IPRs and their reexamination predecessors, those differences do not outweigh

the similarities of purpose and substance and, at least for that reason, do not effectuate a taking of . . . patents.

Celgene Corp. v. Peter, 931 F.3d 1342, 1362–63 (Fed. Cir. 2019). Patent Owner acknowledges the *Celgene* decision, but asserts it was “wrongly decided.” *Id.* at 70. Again, that is not a matter for us to decide.

III. MOTION TO EXCLUDE

Patent Owner moves to exclude Petitioner’s Exhibit 1005 (Windows ACPI) and Exhibit 1028 ¶¶ 56–62. *See generally* Mot. Exclude.

A. Exhibit 1005

Patent Owner argues that Exhibit 1005 should be excluded under Federal Rules of Evidence (FRE) 901(a) because the exhibit has not been authenticated. Mot. Exclude 2. Patent Owner argues “[t]he Petition relies only upon Ex. 1021 . . . to support Exhibit 1005’s admissibility,” and “Petitioner has not presented evidence showing that the document is what Petitioner claims it to be—a document archived by the Wayback machine ‘as of May 4, 1999.’” *Id.* (citing *TRW Automotive U.S. LLC v. Magna Electronics Inc.*, IPR2014-01347, Paper 25 (PTAB January 6, 2016) (Final Written Decision)); *see id.* at 2–3; PO Reply Mot. Exclude 1. Patent Owner further argues that Petitioner attempts to use Dr. Albonesi “to cure the defect.” Mot. Exclude 3 (citing Ex. 1028 ¶¶ 56–62).

Petitioner asserts that this motion should be denied. Pet. Opp. Mot. Exclude 1–5. Petitioner contends the authentication requirement set forth in FRE 901 is “a ‘low bar’” and requires only a rational basis that Exhibit 1005 is what it is asserted to be. *Id.* at 1 (citing *Caterpillar Inc. v. Wirtgen Am.*,

Inc., IPR2018-01091, Paper 49 at 72 (PTAB Nov. 27, 2019) (Final Written Decision) (quoting *United States v. Turner*, 934 F.3d 794, 798 (8th Cir. 2019))). Petitioner also asserts that Exhibit 1005 is authentic because Dr. Albonesi testifies to its authenticity, and Patent Owner never questioned his opinion in this regard during two depositions. *Id.* at 1–2 (citing Ex. 1003 ¶ 43; Ex. 1028 ¶ 61), 3. Petitioner further states Patent Owner has not “suggest[ed] that [Dr. Albonesi’s] opinions are incorrect.” *Id.* at 2. Additionally, Petitioner contends Mr. Butler declares that Exhibit 1005 is a “true and accurate” copy of Windows ACPI. *Id.* Petitioner further argues Exhibit 1005 is authentic under FRE 901(b)(4) based on the totality of the circumstances or FRE 902(7) as self-authenticating. *Id.* at 3–4 (citing *Microsoft Corp. v. FG SRC LLC*, IPR2018-01604, Paper 76 at 12–13 (PTAB Apr. 30, 2020) (Final Written Decision)). Petitioner also argues Patent Owner bears the burden to show Exhibit 1005 is not authentic. *Id.* at 4 (citing 37 CFR § 42.20(c); *Samsung Elecs. Am., Inc. v. Uniloc 2017 LLC*, IPR2017-01798, Paper 32 at 103 (PTAB Jan. 31, 2019) (Final Written Decision)).

In response, Patent Owner argues Petitioner bears the burden to authenticate the evidence it submits. PO Reply Mot. Exclude 1 (citing FRE 901(a)). Patent Owner argues that the Butler Declaration is the only evidence by Petitioner to authenticate Exhibit 1005, it is deficient, and Petitioner admits this deficiency. *Id.* at 1–2 (citing Pet. Opp. Mot. Exclude 2 n.1). Patent Owner further argues that Exhibit 1005 is not self-authenticating because it is not a document archived by the Wayback Machine as of May 4, 1999. *Id.* at 4 (citing *TRW Automotive*, IPR2014-01347, Paper 25).

We agree with Patent Owner that Petitioner bears the burden to authenticate Exhibit 1005. *See* FRE 901 (stating “the proponent must produce evidence sufficient to support a finding that the item is what the proponent claims it is”). But, authentication is a low bar, requiring only a rational basis that Exhibit 1005 is what it is asserted to be. *See Caterpillar*, Paper 49 at 72 (quoting *United States v. Turner*, 934 F.3d 794, 798 (8th Cir. 2019)). Moreover, Patent Owner bears the burden of establishing that Exhibit 1005 is not admissible. *See* 37 C.F.R. § 42.20(c) (indicating the moving party has the burden of proof to establish that it is entitled to the requested relief.).

Upon weighing the parties’ arguments and evidence, Petitioner has provided a rational basis that Exhibit 1005 is what Petitioner purports it to be, a Microsoft Hardware White Paper entitled “Draft APCI Driver Interface Design Notes and Reference.” On the other hand, Patent Owner has not carried its burden of establishing Exhibit 1005 is inadmissible. Notably, Patent Owner never challenged that Exhibit 1005 is what it purports to be or that the exhibit was somehow altered. *See generally* Mot. Exclude. That is, Patent Owner “does not claim that Exhibit 1005 is not a true and correct copy of Windows ACPI.” Pet. Opp. Mot. Exclude 4; *see id.* at 3 (stating “PO never identifies anything to suggest [Exhibit 1005 is not what it purports to be]”). “Nor does PO present any facts that any of the content of Exhibit 1005 suggests that the document is not what [Petitioner] purports it to be, or that it was altered in some way.” *Id.* at 4

Dr. Albonesi, on the other hand, testifies to Exhibit 1005’s authenticity. Dr. Albonesi states “‘Draft ACPI Driver Interface Design Notes and Reference’ (‘Windows ACPI’) is a whitepaper published by

Microsoft.” Ex. 1003 ¶ 43. Dr. Albonesi’s testimony matches Exhibit 1005’s cover page, entitled “Microsoft Hardware White Paper, *Draft* ACPI Driver Interface Design Notes and Reference.” Thus, although not explicitly referring to “Exhibit 1005,” Dr. Albonesi provides a rational basis that Exhibit 1005 is what it purports to be—a white paper published by Microsoft entitled “Draft ACPI Driver Interface Design Notes and Reference.” Patent Owner never challenges Dr. Albonesi’s testimony in this regard. *See* Pet. Opp. Mot. Exclude 2 (“despite having deposed Dr. Albonesi twice, PO never asked him about his opinions on the authenticity of Exhibit 1005, nor does PO even now suggest his opinions are incorrect”).

Additionally, FRE 901(b)(4) indicates that “[t]he appearance, contents, substance, internal patterns, or other distinctive characteristics of the item, taken together with all the circumstances” can authenticate an item, and FRE 902(7) indicates “[a]n inscription, sign, tag, or label purporting to have been affixed in the course of business and indicating origin, ownership, or control” are self-authenticating. Fed. R. Evid. 901(b)(4), 902(7). Exhibit 1005 has multiple references to Microsoft Corporation and a copyright date on its cover page, which are tags or labels affixed in the course of business indicating origin and ownership. Ex. 1005, 1–23. Exhibit 1005 additionally has the appearance and distinctive characteristics of Microsoft’s Hardware White Paper, Draft ACPI Driver Interface Design Notes and Reference, given the title on its cover page. *Id.* at 1. Thus, taking the circumstances together, Exhibit 1005 is also authenticated under FRE 901(b)(4).

As for the holding in *TRW Automotive* cited by Patent Owner, we note that this decision is non-precedential decision, which is not binding on us, and further includes a dissent concerning the majority’s decision to exclude

the document from evidence. *See TRW Automotive*, Paper 25 at 1–11 (dissent).

Accordingly, Patent Owner has not met its burden that Exhibit 1005 is not the document it purports to be and should be excluded.

B. Exhibit 1028, Paragraph 56–62

Patent Owner argues that paragraphs 56 through 62 of Exhibit 1028 are “untimely supplemental evidence.” Mot. Exclude 2; PO Reply Mot. Exclude 3. In particular, Patent Owner argues Petitioner submitted this evidence “months after it let its deadline to submit supplemental evidence lapse without any attempt to cure Patent Owner’s objections.” Mot. Exclude 3 (citing *Dropbox, Inc. v. Synchronoss Technologies, Inc.*, IPR2016-00850, Paper 41 (PTAB October 5, 2016) (Final Written Decision)); *see* PO Reply Mot. Exclude 3 (citing 37 C.F.R. § 42.64(b)(2) (noting that supplemental evidence must be served within ten business days of Patent Owner’s objections)), 4. For this reason, Patent Owner urges us to exclude the noted paragraphs from Exhibit 1028. Mot. Exclude 3. Patent Owner argues “the Board excluded untimely evidence submitted by the petitioner in circumstances akin to those here” in *Toshiba Corp. v. Optical Devices, LLC*, IPR2014-01446, Paper 31 (PTAB Mar. 9, 2016) (Final Written Decision), *aff’d*, 689 F. App’x 976, 976 (Fed. Cir. 2017). PO Reply Mot. Exclude 3–4.

Petitioner counters that Patent Owner has not shown that the noted paragraphs in Exhibit 1028 are inadmissible. Pet. Opp. Mot. Exclude 5. Petitioner contends “Dr. Albonesi’s testimony was proper rebuttal evidence” because the testimony was in response to arguments raised by Patent Owner in its response arguing that Exhibit 1005 was not a qualifying printed publication under 35 U.S.C. § 102. *Id.* at 5–6 (citing *VidStream LLC v.*

Twitter, Inc., 981 F.3d 1060 (Fed. Cir. 2020)). Petitioner also contends “untimely supplemental evidence” is not a proper basis for a motion to exclude. *Id.* at 5. Petitioner argues Patent Owner has not provided a rule of evidence or specifically articulated why these paragraphs should be excluded. *Id.* at 6. Petitioner contends a motion to exclude evidence for the purpose of striking is improper. *Id.* (citing *Palo Alto Networks, Inc. v. Finjan Inc.*, IPR2015-01979, Paper 62 at 66 (PTAB Mar. 15, 2017) (Final Written Decision)). Petitioner further argues Patent Owner has been given notice of the alleged new evidence and arguments raised in Petitioner’s Reply and has had an opportunity to address these issues in its Sur-reply, rendering the motion to exclude unwarranted. *Id.* at 6–7 (citing *VidStream*, 981 F.3d at 1065).

As background, Patent Owner objected to Exhibit 1005 lacking authentication under FRE 901 on March 27, 2020. Paper 16, 3. Petitioner did not respond with supplemental evidence as set forth in 37 C.F.R. § 42.64(b)(2) within ten business days of Patent Owner’s objection. That being said, Patent Owner did not object to Exhibit 1028 within five business days of service of this evidence and prior to filing the motion exclude. *See* 37 C.F.R. § 42.64(b)(1); *see also* Tr. 59:23–25 (stating “JUDGE POTHIER: Counsel, did you actually object to this reply testimony at any point prior to filing your Motion to Exclude? MR. CHERNG: No, we did not.”)

Upon considering the parties’ arguments and evidence, the disputed paragraphs in Exhibit 1028 provide rebuttal evidence relating to issues raised by Patent Owner in its Response (Resp. 64–67) concerning Exhibit 1005’s status as a printed publication, which is permissible. *See* 37 C.F.R. § 42.23(b) (indicating a reply may respond to arguments raised in patent

owner's response); *see also Belden, Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1078 (Fed. Cir. 2015) (holding that the Board did not err in declining to exclude a reply declaration where that declaration fairly responded to issues raised in the response). We, however, do not rely on the disputed testimony for authenticating Exhibit 1005. Moreover, Patent Owner had notice and an opportunity to respond to Exhibit 1028's content in its Sur-Reply, and *VidStream*, in contrast with *Toshiba*, indicates that the Board allowing both sides to provide evidence concerning the challenge to a reference's publication date "in pursuit of the correct answer" is appropriate. *VidStream*, 981 F.3d at 1065.

In addition, Patent Owner reliance's on non-precedential Board opinions, *Dropbox* and *Toshiba*, is not binding on this panel. In *Dropbox*, the Board treated that patent owner's challenge of prior art status as objections to evidence and granted the petitioner the opportunity to file supplemental evidence within 10 days of institution, and the petitioner filed an exhibit (a different copy of the article published in a different source) as supplemental evidence. *See Dropbox*, IPR2016-00850, Paper 41 at 18–19. The patent owner contended that the petitioner did not address whether the article submitted as supplemental evidence was the same as the version submitted with its petition. *See id.* at 19–20. The circumstances in *Dropbox* are not similar to those here.

Lastly, to the extent Patent Owner requests us to strike the disputed paragraphs in Exhibit 1028 because they go beyond what is permitted under 37 C.F.R. § 42.23, an allegation that evidence does not comply with 37 CFR § 42.23 is not a sufficient reason under the Federal Rules of Evidence for

making an objection and requesting exclusion of such evidence. *See Palo Alto Networks*, Paper 62 at 66.

Accordingly, Patent Owner has not successfully carried its burden that paragraphs 56 through 62 of Exhibit 1028 are inadmissible.

Accordingly, we *deny* Patent Owner's Motion to Exclude Exhibit 1005 and Exhibit 1028 ¶¶ 56–62.

C. Summary

As discussed above, we have considered Patent Owner's Motion to Exclude and, for the reasons discussed above, the Motion is denied.

IV. CONCLUSION

For the foregoing reasons, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1–11 of the '519 patent are unpatentable.

V. ORDER

Accordingly, it is

ORDERED that claims 1–11 of U.S. Patent No. 6,895,519 B2 are held unpatentable under 35 U.S.C. § 103 as obvious;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *denied*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of this decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 7, 10, 11	103(a)	Ober, Nakazato	1, 7, 10, 11	
2–6	103(a)	Ober, Nakazato, Cooper, Windows ACPI	2–6	
8, 9	103(a)	Ober, Nakazato, Doblar	8, 9	
Overall Outcome			1–11	

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