

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

IPR2019-01527
Patent 8,117,526 B2

Before JAMESON LEE, BARBARA A. PARVIS,
and NORMAN H. BEAMER, *Administrative Patent Judges*.

BEAMER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

On August 28, 2019, Advanced Micro Devices, Inc. (“Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–3, 5, 9–15, 17, and 21–25 of U.S. Patent No. 8,117,526 B2 (“the ’526 patent”). Paper 2 (“Pet.”). On December 5, 2019, Polaris Innovations Limited (“Patent Owner”) filed a Preliminary Response. (Paper 8, “Prelim. Resp.”).

On March 1, 2020, applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we instituted an *inter partes* review on all challenged claims and all grounds in the Petition. Paper 10, 39.

On May 26, 2020, Patent Owner filed its Response to the Petition. Paper 15 (PO Resp.). On August 18, 2020, Petitioner filed a Reply to Patent Owner’s Response, and on September 29, 2020, Patent Owner filed a Sur-Reply. Paper 18 (Reply); Paper 21 (Sur-Reply).

An oral hearing took place on December 8, 2020. The Hearing Transcript (“Tr.”) is included in the record as Paper 27. After considering the parties’ arguments and supporting evidence, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 9, 12, 24 and 25 of the ’526 patent are unpatentable, but has not demonstrated by a preponderance of the evidence that claims 2, 3, 5, 10, 11, 13–15, 17, and 21–23 of the ’526 patent are unpatentable. 35 U.S.C. § 316(e).

II. BACKGROUND AND SUMMARY

A. The '526 Patent

The '526 patent, titled “Apparatus and Method for Generating a Transmit Signal and Apparatus and Method for Extracting an Original Message from a Received Signal,” was filed on November 29, 2007 and issued on February 14, 2012. It cites, as a related application, provisional US 2009/0110109 A1, filed October 29, 2007. Ex. 1001, codes (54), (22), (45), (60). The patent describes transmitting message data over a memory bus by selectively inverting the data bits of groups of the data, providing indicators indicating whether or not groups of data bits are inverted, and determining check information based on the data and the indicator. *Id.* at Abstr., 6:18–19. The patent also describes recovering the original message data from the received signal by comparing determined check information with received check information and extracting the original message based on the result of the comparison. *Id.*

Groups of data bits of the original message are inverted in accord with an aspect of bus power management known as “data bus inversion,” which is described in the '526 patent as follows:

Data bus inversion can aid bus power management by guarantying [sic] that no more than 50% of data bus lines carrying data bits need to change state, i.e., change state between “0” and “1” or “1” and “0”, at any time. . . . When sending 64 bit message words on the data bus, state changes of certain bus lines will occur between succeeding message words. If it is encountered that more than half of the bus lines would need to have a change state from one message word to the next, the next message word can be inverted. Thus, every logical “1” becomes a logical “0”, and every logical “0” becomes a logical “1.”

Id. at 1:21–34. “Data bus inversion” in this context is also referred to as “low power coding.” *Id.* at Fig. 5. This technique lowers power consumption because it reduces state changes on the bus lines — *i.e.*, it reduces transitions from 0 to 1 or from 1 to 0 — which transitions use up power. Ex. 1016, 2:61–65.

Check information, such as parity bits or error correction codes (ECC), is added to a transmitted message in order to detect or correct errors due to transmission over noisy channels. Ex. 1001, 1:35–37, 2:66–3:1, 6:36–38. Petitioner’s expert, Richard Koralek, Ph.D, explains that check information is redundant information added to a message that allows a receiver to detect and/or correct bit errors that occur during transmission or storage. Ex. 1004 ¶ 28 (hereafter “Koralek Decl.”). For example, a single parity bit can be added to a 7-bit message word, and be assigned a digital “one” if the message has an even number of “ones,” and a “zero” if the message has an odd number of “ones.” Ex. 1008, 4:19–34. When the message is received, the parity bit is recalculated, and if it differs from the transmitted parity bit, an error is indicated. *Id.* at 4:55–5:4. Error correction codes consist of multiple redundant bits that have error correction as well as error detection capabilities. *Id.* at 6:33–38, 7:57–60.

An apparatus for generating a transmit signal as described in the ’526 patent is illustrated in Figure 2 of the patent, reproduced below.

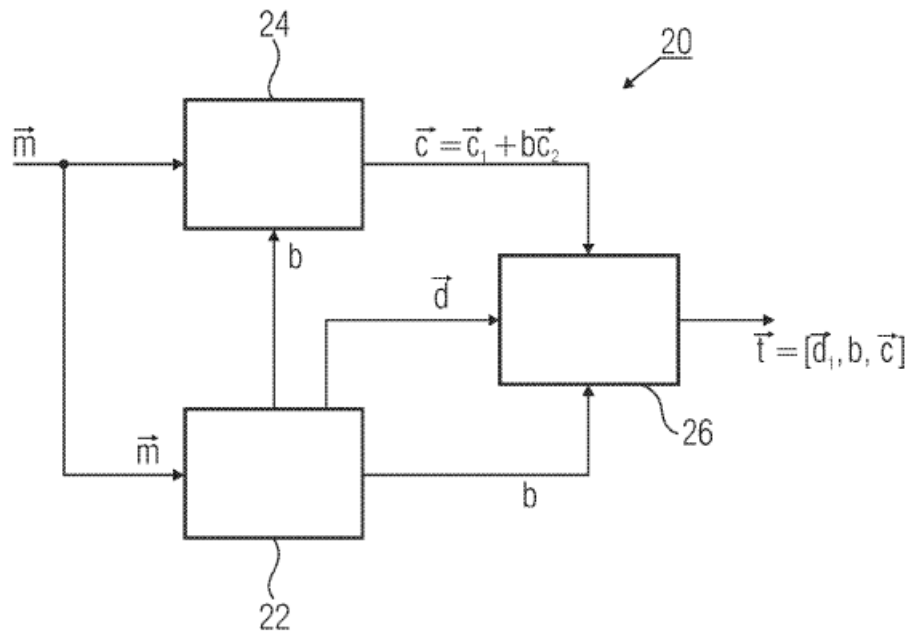


FIG 2

Figure 2 illustrates original message data $\vec{m}$, in the form of a series of multi-bit words, transmitted over a memory bus (for example), and input to processor 24 and circuit 22. Ex. 1001, 3:9–14, 17–18. Circuit 22 determines whether or not to invert each input word based on a bus inversion criteria, and outputs data $\vec{d}$ consisting of words accordingly inverted or unchanged, accompanied by indicators b , which signal whether or not each word is inverted. *Id.* at 10–20. Processor 24 generates check information $\vec{c}$ as a function of the inputs $\vec{m}$ and b . *Id.* at 17–20. Transmitter 26 combines the data $\vec{d}$, indicator b , and check information $\vec{c}$, to form transmitted data $\vec{t}$. *Id.* at 3:23–25.

An apparatus for extracting the original message for the received signal as described in the '526 patent is illustrated in Figure 7 of the patent, reproduced below.

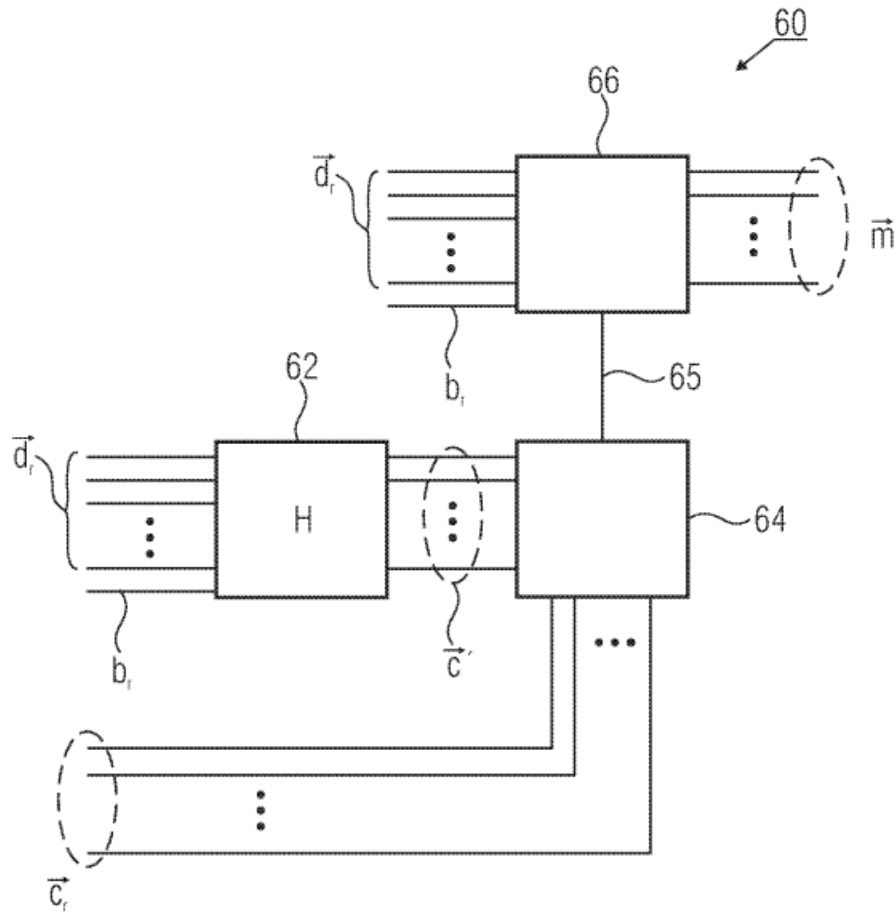


FIG 7

Figure 7 illustrates processor 62 for determining check information $\vec{c}'$ from transmitted data $\vec{d}$ and indicators b , circuit 64 for comparing the determined check information $\vec{c}'$ with received check information $\vec{c}$ to obtain information 65, based on which error detection and/or correction can be performed, and circuit 66, which extracts the original message $\vec{m}$ from transmitted data $\vec{d}$ based on result 65 and indicator b . *Id.* at 6:1–17.

In sum, the '526 patent states that “embodiments described herein relate to a novel combination of encoding for low power and error protection, which makes it possible to use the bus-invert technique in the

presence of errors without any compromise on overall system reliability.”
Id. at 10:17–21.

During prosecution, applicant distinguished cited art, which disclosed both bus inversion and error correction, because the claimed invention determined the error correction bits based on both the original data **and** the inversion indicator. Ex. 1002, 25–27, 31–40; see Koralek Decl. ¶ 65.

B. Illustrative Claim

Challenged claims 1, 12, 14, 24, and 25 are independent. Claims 1 and 12, which exemplify, respectively, the signal transmitting and signal receiving aspects of the claimed invention, are reproduced below.

1. An apparatus for generating a transmit signal comprising data bits, the apparatus comprising:

a circuit for providing an indicator indicating whether the data bits represent an original message or an inverted version thereof;

a processor for determining check information that depends on the data bits and the indicator; and

a circuit for forming the transmit signal including the data bits, the indicator and at least a part of the check information.

12. An apparatus for extracting an original message from a received signal carrying information on data bits representing the original message or an inverted version thereof, an indicator indicating whether the data bits represent the original message or the inverted version thereof, and a check information which depends on the data bits and the indicator, the apparatus being [sic] comprising:

a processor for determining a check information based on the received data bits and a received indicator;

a circuit for comparing the determined check information with received check information; and

a circuit for extracting the original message based on the result of the comparison.

Ex. 1001, 11:15–24, 12:25–37.

C. References

Petitioner relies on the following references (Pet. 3):

- Iglesia et al., US 6,490,703 B1, issued Dec. 3, 2002. Ex. 1007 (“Iglesia”).
- Sridhara et al., *Coding for System-on-Chip Networks: A Unified Framework*, Vol. 13, No. 6 IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 655 (2005). Ex. 1006 (“Sridhara”).
- Uya et al., US 4,417,161, issued Nov. 22, 1983. Ex. 1022 (“Uya”).
- Liu, US 7,102,544 B1, issued Sep. 5, 2006. Ex. 1008 (“Liu”).

D. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1–3, 5, 9–15, 17, and 21–25 of the ’526 patent on the following grounds (Pet. 3)¹:

Claims Challenged	35 U.S.C. §	References
1, 9–13, 24, 25	103(a)	Iglesia, Sridhara
2, 3, 5, 14, 15, 17, 21–23	103(a)	Iglesia, Sridhara, Uya
1, 9, 12, 24, 25	103(a)	Liu, Iglesia
1, 12, 24, 25	102(a)	Liu

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. §§ 102 and 103 that became effective after the filing of the application for the ’526 patent. Therefore, we apply the pre-AIA versions of these sections.

E. Real Parties in Interest

Petitioner identifies itself and ATI Technologies ULC as real parties in interest. Pet. 88. Patent Owner identifies itself, Wi-LAN Inc., and Quarterhill Inc. as real parties in interest. Paper 4, 2.

F. Related Proceedings

The parties identify *Polaris Innovations Ltd. v. Advanced Micro Devices, Inc.*, Case No. 1:18-cv-00555-LY (W.D. Tex.) as a related proceeding (“the Texas litigation”). Pet. 89; Paper 4, 2.

III. ANALYSIS

A. *Legal Standards*

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). “The identical invention must be shown in as complete detail as is contained in the . . . claim.” *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989). “These elements must be arranged as in the claim under review, but this is not an ‘ipsissimis verbis’ test.” *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990) (citations omitted).

A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). The question of obviousness is resolved on the basis of underlying factual determinations, including “the scope and content of the

prior art”; “differences between the prior art and the claims at issue”; and “the level of ordinary skill in the pertinent art.” *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Additionally, secondary considerations, such as “commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy.” *Id.* at 17–18.

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. Rather, an obviousness determination requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); see *KSR*, 550 U.S. at 418 (for an obviousness analysis, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements [in the way the claimed] new invention does”). “Although the *KSR* test is flexible, the Board ‘must still be careful not to allow hindsight reconstruction of references . . . without any explanation as to *how* or *why* the references would be combined to produce the claimed invention.’” *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016) (citation omitted).

Further, an assertion of obviousness “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of

obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); accord *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (stating that “‘conclusory statements’” amount to an “insufficient articulation[] of motivation to combine”; “instead, the finding must be supported by a ‘reasoned explanation’” (citation omitted)); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”).

The motivation to combine must be “accompanied by a reasonable expectation of achieving what is claimed in the patent-at-issue.” *Intelligent Bio-Sys, Inc.*, 821 F.3d at 1367. “The reasonable expectation of success requirement refers to the likelihood of success in combining references to meet the limitations of the claimed invention.” *Id.*

B. Level of Ordinary Skill in the Art

Petitioner relies on its declarant to contend:

A person of ordinary skill in the art [(POSITA)] would have had a Master of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and at least two to three years of academic or industry experience in data-signal transmission, or comparable industry experience. EX1004, ¶20. Alternatively, a POSITA would have a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and at least four to five years of academic or industry experience in data-signal transmission, or comparable industry experience. EX1004, ¶20. A POSITA would have also been familiar with conventional error-correction codes and data-bus inversion. EX1004, ¶20.

Pet. 17 (citing Koralek Decl. ¶ 20). Patent Owner does not advocate for a particular level of skill in the art and also does not dispute Petitioner’s articulation of the level of ordinary skill in the art.

We determine that Petitioner’s description is consistent with the level of skill reflected in the asserted prior art references. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Therefore, for purposes of this Decision, we adopt Petitioner’s unopposed position as to the level of ordinary skill in the art, but without the qualifier “at least” preceding the references to “years of . . . experience” because the qualifier renders the articulated level vague and expands it to include an expert with more than ordinary levels of practical experience.

C. Claim Construction

The Petition was accorded a filing date of August 28, 2019. Paper 3, 1. In an *inter partes* review for a petition filed on or after November 13, 2018, a claim “shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2019); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Under that standard, claim terms generally are given their ordinary and customary meaning, which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Phillips*, 415 F.3d at 1312–13. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.* at 1313. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic

evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). However, in construing the claims, care should be taken to avoid improperly importing a limitation from the specification into the claims. *See Cont’l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797–98 (Fed. Cir. 2019); “use of the phrase ‘present invention’ or ‘this invention’ is not always . . . limiting, such as where the references . . . are not uniform, or where other portions of the intrinsic evidence do not support applying the limitation to the entire patent” (citations omitted)). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Claim terms need only be construed to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011).

1. “checksum”

Petitioner proposes to construe the term “checksum,” recited in challenged dependent claims 5, 9–11, 17, and 21–23, as “a plurality of ECC bits.” Pet. 17–18 (citing Koralek Decl. ¶¶ 69–72). Patent Owner proposes that “[t]he proper construction of ‘checksum’ encompasses a multi-bit error detection or correction data structure whose bits are calculated using non-disjoint sets of inputs, and is not limited to a plurality of ECC bits.” PO Resp. 9 (citing Ex. 2001, ¶¶ 51–63 (the declaration testimony of its expert Dr. Steven A. Przybylski, hereafter “Przybylski Decl.”)).

For its construction, Petitioner relies on the statement in the '526 patent that, “[a]ccording to an embodiment of the present invention the check information may be a parity bit or a checksum comprising a plurality of ECC bits,” and also relies on the reference in the '526 patent to “ECC checksums” in the context of “Hamming codes.” Pet. 18 (citing Ex. 1001, 2:66–3:1, 3:66–4:2, 5:26–27). “ECC” stands for “error correction code” — as stated in the '526 patent, “[a]n error correction code (ECC) can be used in order to recover from single or multiple errors due to transmission over noisy channels.” Ex. 1001, 1:35–37.² “ECC bits” are the bits that make up the ECC code. *Id.* at 5:6–8, 6:35–41. Thus, Petitioner’s proposed construction would implicitly limit “checksum” to multi-bit codes used to correct errors, as opposed to multi-bit codes that only detect errors.

Patent Owner agrees that “checksum” requires a plurality of bits, as opposed to a single parity bit, but argues that the term “checksum” is not limited to a plurality of ECC bits, but rather is used to “describe a variety of different error detection and correction mechanisms.” PO Resp. 9–10 (citing Przybylski Decl. ¶¶ 51, 55). Patent Owner relies on the fact that some claims of the '526 patent require the “checksum” to comprise “error-correcting bits and some do not:

Dependent Claims 9, 10, 11, 21, and 22 require a “checksum,” but do not require the checksum to comprise “a plurality of ECC bits,” or other error-correcting bits. Dependent Claims 5 and 17 require that the checksum comprise “error-correcting bits.” “Checksum,” as the term is used in the '526 patent, is therefore not limited to “a plurality of ECC bits.” If it

² “ECC” sometimes is used to stand for the broader concept of error *control* codes, which encompass both error correction and error detection. Ex. 1006, 655.

were, there would be no reason to specify that the checksum of Claim 5 and 17 comprises “error-correcting bits.”

PO Resp. 13.

We agree with Patent Owner that “checksum” is not limited to a plurality of ECC bits. The above-quoted statement on which Petitioner relies states only that “an embodiment” of the invention may use ECC codes. Claim scope is not limited to a specific embodiment. *Cont’l Circuits*, 915 F.3d at 797–98. Moreover, Petitioner’s reliance on embodiments described in the ’526 patent that use a “Hamming code” undercuts its position, given that Hamming codes are “capable of correcting single errors *and detecting* double errors.” Ex. 1001, 6:36–38 (emphasis added). Also, according to the patent, “additional parity bits . . . are used in order to detect multiple errors.”³ *Id.* at 9:64–65. Finally, as Patent Owner points out, some dependent claims only require a “checksum,” while others require that the checksum comprise “error-correcting bits,” indicating that “checksum” encompasses ECC bits, but is not limited to such embodiments. *Envntl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 699 (Fed. Cir. 1983) (“It is improper . . . to read into an independent claim a limitation explicitly set forth in another claim”).

In addition to arguing against Petitioner’s attempt to limit “checksum” to ECC bits (and we agree that “checksum” is not so limited), Patent Owner would construe that term to “encompass[] a multi-bit error detection or correction data structure whose bits are calculated using non-disjoint sets of inputs. . . .” PO Resp. 9. Patent Owner cites the Hamming code and the

³ The record further demonstrates that another checksum example is a “cyclic redundancy check,” which is an error detection code. Ex. 1007, 4:23–24.

cyclic redundancy check as examples of checksums that are calculated using non-disjoint sets of inputs. *Id.* at 10; Przybylski Decl. ¶ 56.

We agree with Patent Owner that the term “checksum” *encompasses* calculations using non-disjoint sets of inputs, such as for Hamming codes or cyclic redundancy codes. As Petitioner points out, “[b]y using the term ‘encompasses,’ [Patent Owner] leaves the door open for an even broader construction.” Reply 18.

Despite including “encompasses” in its proposed definition of “checksum,” Patent Owner would narrow “checksum” to *exclude* “a set of simple parity bits, calculated from non-overlapping sets of inputs.” PO Resp. 10 (citing Przybylski Decl. ¶ 52). In support, Dr. Przybylski relies on a definition of “checksum” in a 2002 edition of the *Microsoft Computer Dictionary*:

Checksum n. A calculated value that is used to test data for the presence of errors that can occur when data is transmitted or when it is written to disk. The checksum is calculated for a given chunk of data by sequentially combining all bytes of data with a series of arithmetic or logical operations.

Przybylski Decl. ¶ 52 (citing Ex. 1013, 97). However, this definition does not support the proposition that a set of simple parity bits, calculated from non-overlapping sets of inputs, cannot be a checksum, because parity bits are calculated by performing “modulo-2 addition,” *i.e.* “the exclusive-OR or XOR operation,” on data bits. Koralek Decl. ¶¶ 28–29, 32. In other words, parity bits are “calculated for a given chunk of data by sequentially combining all bytes of data with a series of arithmetic or logical operations” — thus satisfying the above definition of checksum, albeit a simple, less robust example of such. *See also* Ex. 1015 (Maxino, *The Effectiveness of Checksums for Embedded Networks*), 6:

The simplest, and least effective, checksums involve a simple “sum” function across all bytes or words in a message. [A] most commonly used simple “sum” function[] [is] XOR

Confirming this is the fact that Patent Owner, in the Texas Litigation, summarized this Microsoft Computer Dictionary definition of “checksum” as simply meaning “a calculated value that is used to test data for the presence of errors.” Ex. 1026, 5.

Moreover, Dr. Przybylski omits the last portion of the above-quoted definition of “checksum,” which states, “[c]hecksums cannot detect all errors, and they *cannot be used to correct erroneous data*.” Ex. 1013, 97 (emphasis added). This squarely contradicts the explicit provision in the ’526 patent that “[a]ccording to an embodiment of the present invention the check information may be . . . a checksum comprising a plurality of ECC bits.” Ex. 1001, 2:66–3:1. Acting as his own lexicographer, Applicant used “checksum” in a broader sense than does this dictionary, because it specifically includes error correction codes (“ECC bits”), whereas the dictionary specifically excludes such codes. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (“An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification”). Thus, the dictionary definition relied on by Dr. Przybylski has little applicability to this proceeding.

Dr. Przybylski also relies on claim 11 of the ’526 patent, which requires the check information to be a “parity bit,” and further requires the parity bit to be determined “using the data bits and a checksum.” Przybylski Decl. ¶ 62 (citing Ex. 1001, claim 11). Based on this, and on equation 14 and the accompanying description in the ’526 patent, which Dr. Przybylski testifies is an embodiment of claim 11, Dr. Przybylski concludes that

“checksum” excludes “parity bits calculated across independent, non-overlapping inputs.” *Id.* (citing Ex. 1001, 7:44-9:47, Equation 14). As explained in the ’526 patent, the embodiment described in connection with equation 14 is an example of a technique by which “extra parity bits are added to the transmit signal in order to detect double errors.” Ex. 1001, 9:10–11. In the context of this particular equation, the calculated parity bit is different from the checksum used to determine that bit. However, neither claim 11 nor any other disclosure in the ’526 patent supports Patent Owner’s argument that checksums in general cannot be made up of parity bits calculated across independent, non-overlapping inputs.

In light of the above, we agree with Patent Owner that, although the term “checksum” encompasses ECC bits in “an embodiment of the present invention,” the term is not limited to ECC (error control code) bits. However, we do not agree that “checksum” excludes “a set of simple parity bits, calculated from non-overlapping sets of inputs.” The term “checksum” encompasses multiple parity bits or other multi-bit error detection as well as error correction codes. It is not necessary for purposes of this Decision to further provide an all-encompassing construction of this term.

2. *“check information that depends on the data bits and the indicator”*

Independent claims 1, 12, 24, and 25 of the ’526 patent require “check information [that or which] depends on the data bits and the indicator,” or “check information based on the received data bits and a received indicator.” Ex. 1001, 11:20–21, 12:32–33, 14:19–20. 14:30–31. Patent Owner submits that the proper construction of these requirements is “check information that protects the data bits and the indicator.” PO Resp. 3. By this, we understand “protects” in this context to mean that the error correction or detection codes

that are embodied in the checksum can correct or detect an error in the transmitted indicator. See Przybylski Decl. ¶ 67. Patent Owner admits that the claims do not explicitly require that the check information protect the indicator, but argues that construing “depends on” in the context of the claim to more broadly mean “be a function of” would render superfluous the requirement that the check information depend upon the indicator, because the check information is already a function of the indicator by virtue of the fact that it is a function of the data bits, which in turn are a function of the original message and the indicator. PO Resp. 4 (citing Przybylski Decl. ¶ 77).

In addition, Patent Owner argues its construction is consistent with numerous disclosures in the ’526 patent directed to protecting the inversion bit (*i.e.*, the indicator) as well as the data by calculating the check information from both the data bits and the indicator. PO Resp. 4–5 (citing Ex. 1001, 2:43–46, 3:17–22, 7:47–55, 10:17–21; Przybylski Decl. ¶¶ 66–68). Patent Owner cites equations in the ’526 patent which show that the check information generated thereby protects the indicator by detecting or correcting errors in the transmitted indicator. *Id.* at 6–7 (citing Przybylski Decl. ¶¶ 68–73). Patent Owner also relies on the prosecution history of the ’526 patent, during which a cited reference was distinguished because “no signal comparable to the indicator” was provide to the error correction circuitry of the reference. *Id.* at 7–8 (citing Ex. 1002, 26; Przybylski Decl. ¶¶ 46–47).

Petitioner challenges Patent Owner’s construction, asserting that the Specification does not define “depends on” to require protection, that the disclosed mathematical functions that Patent Owner relies on in fact show

that the check information is a function of the inversion indicator, and that the reference in the prosecution history was not distinguished based on a distinction between the checksum protecting the indicator versus the checksum being a function of the indicator. Reply 3–5 (citing Ex. 1027 ¶¶ 9–16, 25–28 (hereafter “Koralek Reply Decl.”)).

We are not persuaded that the claims require check information to “protect” the indicator. The claims only literally require that the check information “depend[] on” or be “based on” the indicator. Ex. 1001, 11:20–21, 12:32–33, 14:19–20, 14:30–31. Patent Owner’s construction would improperly import a limitation from the Specification into the claims. *Cont’l Circuits LLC*, 915 F.3d at 797–98. We agree with Petitioner’s arguments that neither the ’526 Specification nor prosecution history requires limiting the claims to check information that “protects” the indicator. Also, Patent Owner’s argument that allowing “depend on” or “based on” to mean “be a function of” would render claim language superfluous is premised on the view that the data bits are a function of the original message and the indicator. PO Resp. 4. But that premise is incorrect, because the data bits are not a function of the indicator — the indicator is merely a bit (zero or one) that the system generates *after* determining whether to invert the original data, to indicate whether or not the original data are inverted. Ex. 1001, 1:43–45, 2:56–59, 3:10–14.

Accordingly, we do not adopt Patent Owner’s proposed construction of “check information that depends on the data bits and the indicator,” and otherwise do not further construe that phrase.

D. Obviousness of Claims 1, 9–13, 24, and 25 Over Iglesia and Sridhara

Petitioner challenges claims 1, 9–13, 24, and 25 as unpatentable under pre-AIA 35 U.S.C. § 103(a) over the combination of Iglesia and Sridhara. Pet. 19–55.

1. Iglesia

Iglesia, titled “Bus Power Savings Using Selective Inversion in an ECC System,” was filed September 30, 1999 and issued December 3, 2002. Ex. 1007, codes (54), (22), (45).

Iglesia discloses an “error correction and selective inversion circuit (ESIC).” *Id.* at Abstr. Figure 5, which includes an ESIC, is reproduced below.

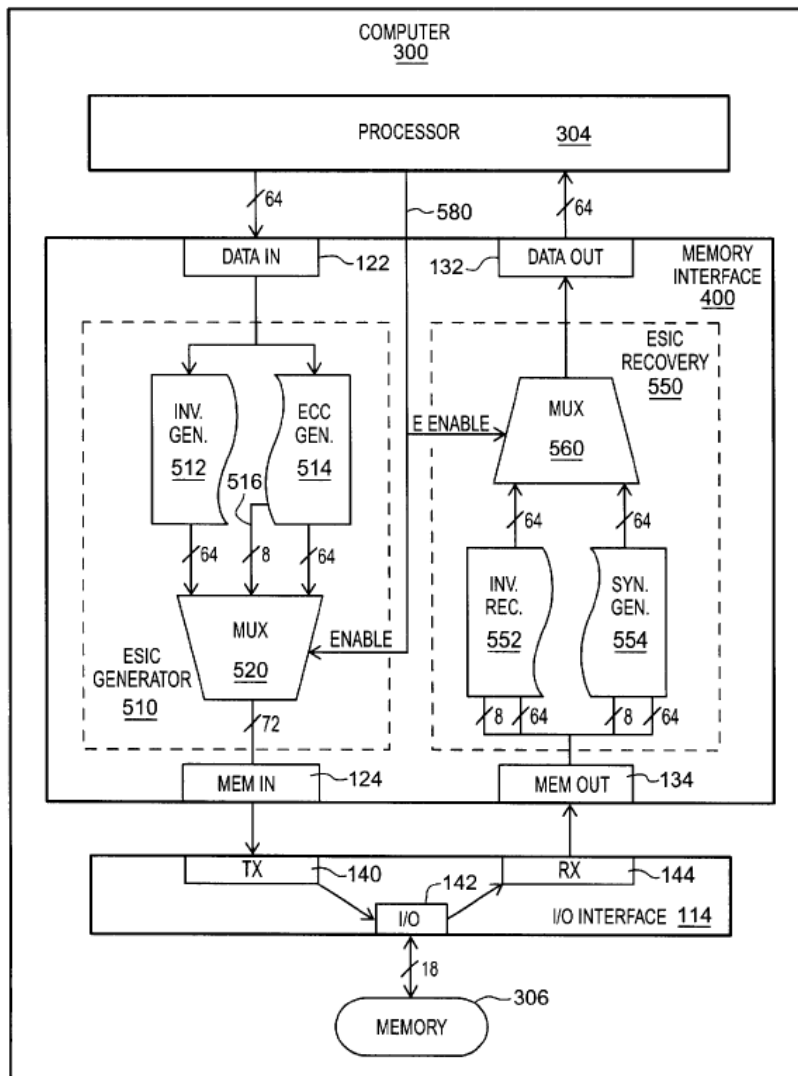


FIG. 5

Figure 5 is a block diagram of memory interface 400, residing between processor 304 and memory 306, through which data is processed while being written from the processor to the memory or retrieved from the memory to the processor. *Id.* at 6:66–7:18. The memory interface includes ESIC generator 510, which in turn includes inversion generator 512 coupled in parallel with ECC generator 514. *Id.* at 7:24–25. Inversion generator 512 determines whether to invert a particular input word depending on the number of “ones” in the word, and sets “flip” bits to indicate whether or not

a word is inverted. *Id.* at Fig. 6, 7:55–8:44. ECC generator 514 operates in parallel with inversion generator 512 and generates, from the input data word, parity bits used for error detection and correction. *Id.* at 3:33–35, 4:31–35, 7:37–41. The outputs of inversion generator 512 and ECC generator 514 are combined by MUX (multiplexer) 520 and output to memory. *Id.* at 7:37–41, 8:42–43.

Memory interface 400 also includes ESIC recovery 550, which in turn includes inversion recovery 552 coupled in parallel to syndrome generator 554. *Id.* at 7:43–45. Inversion recovery 552 uses the “flip” bits to determine whether or not a retrieved data word was inverted when transmitted, and reverses the inversion to restore the original data if so indicated. *Id.*, Fig. 7, 8:45–62. Syndrome generator 554 operates in parallel with inversion recovery 552 and uses the parity bits to perform error detection and correction on the retrieved data. *Id.* at 4:42–59, 7:37–41. The outputs of inversion recovery 552 and syndrome generator 554 are combined by MUX (multiplexer) 560 and output to the processor. *Id.* at 7:49–52.

Iglesia discloses the ability to divide an input word in multiple smaller segments, and perform the inversion generation and recovery steps on each segment separately, with a separate flip bit for each segment. *Id.* at 5:28–33. This is illustrated in Figure 2D, reproduced below.

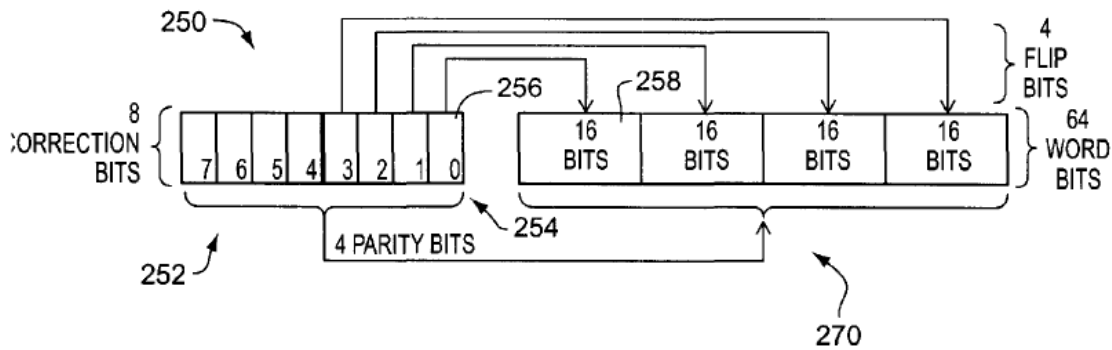


FIG. 2D

Figure 2D illustrates a 64-bit word divided into four 16-bit segments (*e.g.*, segment 258), with a flip bit generated for each segment (*e.g.*, bit 256). *Id.* at 6:53–59. By dividing up the data words in this manner, the inversion process is more effectively performed, resulting in less power consumed. *Id.* at 5:62–63. On the other hand, the additional flip bits reduce the number of available parity bits, and so the syndrome generator can only detect, but not correct, errors. *Id.* at 6:53–54.

Significantly, the flip bits are not input to ECC generator 514 to generate the parity bits, nor are they provided to syndrome generator 554, and so flip bit transmission errors cannot be detected, nor do the parity bits depend on the flip bits. Pet. 28.

2. Sridhara

Sridhara et al., titled “Coding for System-on-Chip Networks: A Unified Framework,” was published in IEEE Transactions on Very Large Scale Integration (VLSI) Systems in 2005. Ex. 1006. Petitioner submits evidence that Sridhara was published before the earliest priority date of the ’526 patent, and therefore argues that this article is prior art to the ’526 patent under pre-AIA 35 U.S.C. § 102(a) or 102(b). Pet. 15–16. Patent Owner does not challenge the prior art status of Sridhara.

Sridhara presents simulation data for 4-bit and 32-bit buses using various coding techniques including low power codes (LPCs) and error correction codes. Ex. 1006, 655. Sridhara describes a “Unified Coding Framework” shown in Figure 4 reproduced below.

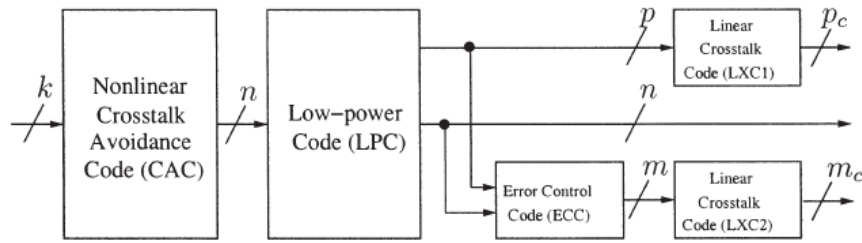


Fig. 4. Unified coding framework.

Figure 4 depicts (i) k -bit data input coded using linear crosstalk avoidance code CAC, which outputs n -bit codeword; (ii) n -bit codeword is further encoded to reduce the average transitions via low power coder LPC, which outputs n -bit codeword and p low-power information bits; (iii) n -bit codeword and p low-power information bits are encoded via error control coder ECC to generate m parity bits for the $n + p$ code bits; and (iv) m parity bits and p low-power information bits are further encoded for crosstalk avoidance via linear crosstalk avoidance coders LXC1 and LXC2 to obtain m_c and p_c bits respectively, that are sent over the bus along with n code bits. *Id.*, at 658.

Sridhara further describes simulations for a “variety of codes based on the proposed unified framework that allow for tradeoff between delay, power, area, and reliability.” Ex. 1006, 658. One simulated technique combines an LPC with a Hamming code, which technique Sridhara calls a “bus-invert Hamming (BIH) code.” *Id.* at 659. The technique is illustrated in Figure 5(b), reproduced below.

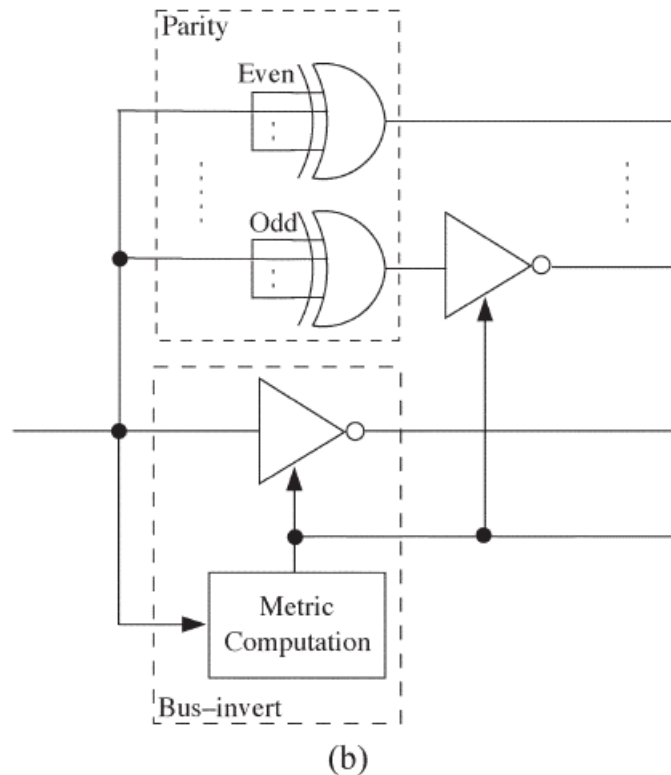


Figure 5(b) depicts a simulated circuit in which bus data enters from the left and is input to XOR gates in a parity portion of the circuit, and also input to an inverter and “Metric Computation” circuit in a “Bus-invert” portion. *Id.* at 659. This technique performs LPC encoding and Hamming encoding operations in parallel, which Sridhara estimates would result in a “21%-33% reduction in encoder delay,” compared to performing the operations serially. *Id.* The Metric computation circuit determines whether a word on the bus is inverted, according to a data bus inversion criteria, and provides an invert bit to enable the inverter accordingly. *Id.* The Parity circuit determines check bits for the data in accord with a Hamming code. *Id.* The circuit makes use of a property of XOR gates: “If an odd (even) number of the inputs of an XOR gate are inverted, then the output is inverted (unchanged).” *Id.* Thus, in order to account for instances where a word is inverted, the parity bits

determined from odd combinations of input bits are inverted by a downstream inverter enabled by the invert bit generated by the Metric computation circuit. *Id.* The circuit outputs (i) the original data, inverted or not inverted according to the metric; (ii) the invert bit; and (iii) the parity bits generated by the Hamming code. *Id.*; *see also* Koralek Decl. ¶ 57.

In summarizing the results of the simulations, Sridhara states that, notwithstanding the above-mentioned estimate regarding reducing encoder delay, the actual simulation of the “BIH” approach “performs worse than Hamming,” and therefore “we exclude BIH . . . from further comparison.” Ex. 1006, 661. On the other hand, Sridhara states that the BIH approach “will become more effective in the future.” *Id.* at 666.

3. *The Combination of Iglesia and Sridhara*

a) *Petitioner’s Arguments*

In relying on the combination of Iglesia and Sridhara, Petitioner argues that Iglesia discloses systems that perform both data bus inversion and error correction on “chunks” of data, rather than an entire data word, to achieve greater power savings, but because it does not disclose protecting the flip bit with error correction, one of ordinary skill would have been led to also use aspects of Sridhara, which it alleges determines parity bits using the flip bit as well as the original data. Pet. 19. Petitioner argues one of ordinary skill would have combined the simulated circuitry disclosed in Sridhara with the physical processor and circuit architecture of Iglesia to arrive at the claimed invention. Pet. 19–20.

Petitioner posits two reasons why one of ordinary skill would have been motivated to combine the teachings of Sridhara and Iglesia. First, Sridhara’s BIH approach would result in a “significant reduction in encoder

delay.” Pet. 20 (citing Koralek Decl. ¶ 75). This statement in Sridhara refers to the fact that, in the above-discussed Figure 5(b), the metric and parity calculations are performed in parallel, rather than the serial approach depicted in Figure 5(a), which Sridhara predicts would achieve a 21%–33% reduction in encoder delay. Ex. 1006, 658–59. Second, Petitioner notes that, in Iglesia, the input data to ECC generator 514 is always uninverted, which, if the data consists of an odd number of bits, would result in parity opposite to that of its inverted counterpart. Pet. 20 (citing Koralek Decl. ¶ 76). Therefore, argues Petitioner, one of ordinary skill would have been motivated to use the flip bits to selectively invert the parity bits in the manner of Sridhara, to ensure that the correct parity bits are transmitted. *Id.*

Petitioner asserts that its proposed combination would have combined widely known low power data bus inversion with Hamming code error correction according to known methods to yield predictable results, and that the combination would have been a simple substitution of “Sridhara’s BIH framework for . . . Iglesia’s ECC and inversion generators on the encoder side and Iglesia’s inversion recovery and syndrome generator on the decoder side.” Pet. 21 (citing Koralek Decl. ¶ 77). Petitioner further argues that the combination would have been predictable because “Sridhara explains how its BIH framework is used with both the encoder and the decoder.” *Id.*

b) Patent Owner’s Response

Patent Owner challenges Petitioner’s reasoning for combining the references, arguing that Petitioner’s assertion that the Sridhara BIH technique reduced encoder delay is belied by the fact that the actual simulation results set forth in Sridhara showed increased delay — in particular, a 4-bit bus simulation of BIH had a 748-picosecond delay,

compared to a 448-picosecond delay for Hamming codes, and a 32-bit bus simulation yielded a 1952-picosecond delay for BIH versus 1005 picoseconds for Hamming. PO Resp. 19–20 (citing Ex. 1006, Tables II, III; Przybylski Decl. ¶ 107). Patent Owner cites the fact that this result caused the authors to “exclude BIH . . . from further comparison.” *Id.* at 20 (citing Ex. 1006, 661; Przybylski Decl. ¶ 108). Patent Owner argues that because Iglesia already performs error encoding and low power encoding in parallel, the increased delay of the Sridhara BIH technique compared to conventional Hamming encoding would have taught away from combining Iglesia and Sridhara and would not have presented a person of ordinary skill with a reasonable expectation of success in making that combination. *Id.* at 23–25 (citing Przybylski Decl. ¶ 110). Patent Owner further argues that because Iglesia already performs error encoding and low power encoding in parallel, there would have been no motivation to modify the Iglesia approach with Sridhara’s BIH technique, even if it did not introduce additional delay. *Id.* at 20–21.

Patent Owner also argues that there would have been no motivation to combine Iglesia and Sridhara by a desire “to correctly encode input data that has an odd number of bits,” and that Petitioner’s declarant’s testimony is conclusory and lacking in any support. PO Resp. 21. Patent Owner points out that both Iglesia and Sridhara describe even-number busses, and neither refers to the need to deal with odd-number busses. *Id.* at 21–22 (citing Ex. 1006, 658 (“In this paper, we assume to [the bus] to be even”); Ex. 1007, 5:14–16 (“Words of data conventionally are processed in sixty four or one hundred twenty eight bits”); Przybylski Decl. ¶¶ 112–113).

In addition, Patent Owner argues Iglesia teaches away from the combination because the approach of Figure 2D of Iglesia, discussed above, and on which Petitioner relies, diverts bits otherwise used for Hamming code parity bits for use as flip bits, thus, limiting the check information to simple error detection parity, whereas the Sridhara BIH technique requires the full error correction capability of Hamming codes. PO Resp. 25–26 (citing Ex. 1007, Figs. 2D, 8, 6:31-35, 6:53-73, 9:18-31; Przybylski Decl. ¶¶ 115–116).

Finally, Patent Owner argues that the combination of Iglesia and Sridhara does not disclose the claimed “check information that depends on the data bits and the indicator.” PO Resp. 26–31. Given Patent Owner’s claim construction arguments discussed in Section III.C.2 above, by this argument Patent Owner is asserting that neither Iglesia nor Sridhara teaches determining check information that *protects* the data bits *and* the indicator. *Id.* at 27. In particular, Patent Owner argues that, in the Sridhara BIH technique, the ECC (check information) is calculated without the invert bit (*i.e.*, the indicator), and therefore does not protect the indicator. *Id.* at 27–29 (citing Przybylski Decl. ¶¶ 84–87, 117). Patent Owner supports the argument by first pointing out that Figure 5(a) of Sridhara shows that the invert bit bypasses the parity generation block, and thus is not protected. *Id.* at 28 (citing Ex. 1006, Fig. 5(a); Przybylski Decl. ¶ 85). Patent Owner next notes the fact that Sridhara Figure 5(b) is a “temporal optimization” of, and “functionally equivalent” to, Figure 5(a). *Id.* at 29 (citing Ex. 1006, Fig. 5(b); Przybylski Decl. ¶¶ 86–87). Thus, argues Patent Owner, “Sridhara leaves unsolved the problem identified by the inventor, protecting the inversion bit from errors.” *Id.* at 29.

c) *Petitioner's Reply*

In reply to these arguments, Petitioner first argues that Sridhara's parallel BIH embodiment does reduce encoder delay compared to performing low power encoding and Hamming encoding serially — calculating that, for a 32-bit bus simulation, the former takes 1,952 picoseconds and the latter 2,238 picoseconds. Reply 12–13 (citing Ex. 1006, Table III; Koralek Reply Decl. ¶ 51). Therefore, Petitioner argues, the timing information set forth in Sridhara does not teach away from combining it with Iglesia, particularly given the statement in Sridhara that the BIH approach “will become more effective in the future.” *Id.* at 14–15 (citing Ex. 1006, 666). To that point, although not mentioned in the Reply, Petitioner's expert Dr. Koralek opines that the BIH approach would improve if embodied in future 45-nanometer processes. Koralek Reply Decl. ¶¶ 52–59. For the same reason, Petitioner argues that one of ordinary skill would have had a reasonable expectation of success in combining Iglesia and Sridhara. *Id.* at 15–16.

In addition, in reply to Patent Owner's argument that neither Iglesia nor Sridhara deal with odd-number busses, Petitioner argues that its argument regarding correctly dealing with odd-number inputs was not directed to data busses, but rather to the or-gate inputs in Hamming encoders, which involve odd-number inputs even when the data bus has an even number of inputs. Reply 13–14 (citing Ex. 1006, 659; Koralek Decl. ¶¶ 39, 76; Koralek Reply Decl. ¶¶ 60–64).

In reply to Patent Owner's argument that Iglesia sacrifices error correction bits for use as flip bits, whereas Sridhara uses Hamming codes for error correction, Petitioner argues that Iglesia discloses the option of

including “anywhere from one to hundreds of correction bits,” thus allowing the use of error correction codes such as Hamming codes. Reply 16–18 (citing Ex. 1007, Figs. 2A, 2B, 6:6–18, 7:28–30; Koralek Decl. ¶¶ 39, 76; Koralek Reply Decl. ¶¶ 65–68).

Finally, Petitioner asserts that the Sridhara BIH technique *does* teach determining check information that protects the data bits *and* the indicator. Reply 5–10. Petitioner bases this on an argument that the Sridhara BIH approach, as illustrated in Figure 5(b), is “functionally identical” to Figure 3 of the ’526 patent. And since it is undisputed that the latter protects the indicator, so does the former. *Id.* at 5. Petitioner supports this assertion by submitting lengthy testimony of its expert Dr. Koralek, supplemented by selected deposition testimony of Patent Owner’s expert, which breaks down the ’526 patent’s Figure 3 and Sridhara Figure 5(b) into three “steps” and compares them, ostensibly with the result that the two approaches are functionally identical insofar as protecting the indicator is concerned. *Id.* at 5–10 (citing Ex. 1001, 3:46–52; Koralek Reply Decl. ¶¶ 16–24, 29–46; Ex. 1028, 71:5–72:1, 77:12–77:16, 80:18–21, 81:7–12, 101:13–18, 112:6–9). In addition, although not mentioned in the Reply, Petitioner’s expert Dr. Koralek cites Figure 4 of Sridhara as showing an error control encoder that protects the indicator. Koralek Reply Decl. ¶ 46 (citing Ex. 1006, 658 (“ECC Generates m parity bits for the $n + p$ code bits”)).

d) Patent Owner’s Sur-Reply

As a threshold matter, Patent Owner objects to Petitioner’s practice of incorporating by reference voluminous portions of its expert Dr. Koralek’s declaration to supplement various arguments that Petitioner made in reply, in violation of 37 C.F.R. § 42.6(a)(3). Sur-Reply 1, 14, 17.

Responding to Petitioner's citation of Sridhara's prediction that its BIH approach "will become more effective in the future," and in particular to Petitioner's expert Dr. Koralek's incorporated-by-reference testimony that the "future" would be embodied in 45-nanometer processes, Patent Owner argues that the testimony is speculative and unsupported by any experimentation or simulation, and that the testimony did not explain why transitioning to a 45-nanometer process would change the relative delay disadvantage of the BIH approach. Sur-Reply 16–21.

Patent Owner also argues that the asserted improvement in delay times attributed to the Sridhara BIH approach of Figure 5(b) is an improvement relative to the approach depicted in Sridhara Figure 5(a), but would not be applicable to the approach of Iglesia Figure 5, which already adopts the parallel implementation of error coding and bit inversion. Sur-Reply 21–22.

Patent Owner also reiterates its challenge to Petitioner's argument that the Sridhara BIH technique teaches determining check information that protects the data bits *and* the indicator. Sur-Reply 13–15. Patent Owner argues that Figure 5(b) of Sridhara is not "topologically equivalent" to Figure 3 of the '526 patent because, unlike Figure 3, Sridhara Figure 5(b) does not extend the code generation matrix *G* to add an additional column to accommodate the indicator bit, without which the generated error code cannot protect the indicator. PO Resp. 31 (citing Przybylski Decl. ¶ 120). In regard to Dr. Koralek's reliance on Sridhara Figure 4, Patent Owner argues that Sridhara Figure 5(b) does not conform to the architecture depicted in Figure 4, and therefore cannot support the argument that Figure

5(b) teaches using error detection or correction codes to protect the indicator. Sur-Reply 14.

e) Analysis

We agree with Patent Owner that Petitioner has not proved by a preponderance of the evidence that a person of ordinary skill in the art would have been motivated to combine the teachings of Iglesia and Sridhara. As Patent Owner points out, the argument that Sridhara's BIH approach reduces encoder delay is undercut by the actual simulation results reported in the article. Pet. 20; PO Resp. 19–20. We are not persuaded by Petitioner's reliance on comparisons of Sridhara Figure 5(b) to Sridhara Figure 5(a) — we agree with Patent Owner that the pertinent comparison is to Iglesia Figure 5. Reply 12–13; Sur-Reply 21. Also, even considering the lengthy incorporation by reference of Dr. Koralek's declaration, we agree with Patent Owner that the testimony of Dr. Koralek regarding the future improved performance of the BIH approach using 45-nanometer technology is speculative and unsupported. Koralek Reply Decl. ¶¶ 52–59; Sur-Reply 16–21. Moreover, the theoretically predicted delay reduction of the BIH approach was due to the fact that the inversion determination and parity calculations would be performed in parallel, rather than serially. Ex. 1006, Fig. 5(b), 658–59. However, the circuit illustrated in Iglesia Figure 5, discussed above, already performs inversion generation and error correction code generation in parallel, thus removing the incentive for one of ordinary skill to look to Sridhara for the same idea. PO Resp. 20–21. To the extent that Sridhara also discloses some version of inversion generation and error correction, the record does not shed light on what a combination would entail or why it would have been made.

Likewise, the asserted need to turn to Sridhara “to correctly encode input data that has an odd number of bits” is not supported in the record. Pet. 20; PO Resp. 20. In particular, the examples in Iglesia each use data words with an even number of bits, and so the depicted circuits do not need to account for circumstances where an odd number of bits are inverted. Ex. 1007, 5:14–16 (“Words of data conventionally are processed in sixty four or one hundred twenty eight bits, depending on the operating system.”). Similarly, Sridhara assumes even-numbered data bus widths. Ex. 1006, 658. We are not persuaded by Petitioner’s clarification, in its Reply, that its argument pertains to a possible odd number of inputs to a Hamming encoder, because (as recognized in the Petition) the embodiment of Iglesia that Petitioner relies on uses simple parity encoding, not Hamming encoding. Pet. 20; Reply 13–14.

To the extent one of ordinary skill would have contemplated extending the circuit of Iglesia to account for odd bus sizes (the motivation for which is only assumed by Petitioner’s expert Dr. Koralek), we are not sufficiently persuaded by Dr. Koralek’s conclusory assertion that “A POSITA would have therefore been motivated to use Sridhara’s BIH framework to ensure that the correct parity bits were transmitted during encoding of an odd number of input bits.” Koralek Decl. ¶ 76. For example, we note that the “odd number of bits problem” could be solved in ESIC recovery 550, by using the received flip bits to cause selective inversion of the received data word before it is input to syndrome generator 554, thus, ensuring that the input tracks (absent transmission error) the original data that was input to ECC generator 514. Ex. 1007, Fig. 5.

We are also not persuaded by Petitioner’s argument, in response to Patent Owner’s assertion that Iglesia teaches away from the combination because it uses simple parity rather than Hamming codes, that Iglesia also teaches using Hamming codes because of the isolated statement in Iglesia that the correction bits “may include anywhere from one to hundreds of correction bits.” PO Resp. 25–26; Reply 16–18. To the contrary, Iglesia specifically states that the preferred approach is to “give[] up this ability” of error correction using Hamming codes in favor of having only error detection capability in order to also use low power coding. Ex. 1007, 6:25–37. The circuit that Petitioner relies on in Iglesia uses simple parity bits, for error detection, whereas that of Sridhara uses Hamming codes for error correction. *Compare* Ex. 1007, Fig. 5, 6:54–57 (“Four of eight correction bits 250 may be integrated into an ESIC system as four flip bits 254, with the remaining four correction bits 252 ***used for error detection without correction***” (emphasis added)), *with* Ex. 1007, Fig. 5, 659 (“The joint code that results from such a combination of bus-invert code BI(1) and ***Hamming code*** is referred to as bus-invert Hamming (BIH) code” (emphasis added)). Petitioner does not sufficiently explain how Sridhara’s BIH framework would combine with Figure 5 of Iglesia if that figure were in turn modified to accommodate the use of Hamming codes. As stated in *Personal Web Technologies, LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017):

[A] clear, evidence-supported account of the *contemplated workings of the combination* is a *prerequisite* to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.

Although Petitioner asserts that the combination of Iglesia and Sridhara would have been a simple substitution of “Sridhara’s BIH framework for . . .

Iglesia's ECC and inversion generators on the encoder side and Iglesia's inversion recovery and syndrome generator on the decoder side" (Pet. 21 (citing Koralek Decl. ¶ 77)), neither Petitioner nor Dr. Koralek explains how this substitution would actually be implemented or how it would work.

In addition, we are not persuaded by Petitioner's assertion that the combination would have been made because "Sridhara explains how its BIH framework is used with both the encoder and the decoder." Pet. 21. Petitioner relies on one simulation example in Sridhara for the encoder disclosure (the BIH circuit of Figure 5(b)), which example uses Hamming codes, and an entirely unrelated example for the decoder (the duplicate-add-parity bus-invert (DAPBI) circuit of Figure 7), which uses parity bits. Koralek Decl. ¶ 77; Ex. 1006, 659–660. Petitioner does not explain how these two different approaches can be combined with Iglesia.

Finally, we agree with Patent Owner that Sridhara does not disclose the claim element that is admittedly missing from Iglesia: "check information that depends on the data bits **and the indicator**." PO Resp. 26–31 (emphasis added); Sur-Reply 13–15. We note that Patent Owner does not present this argument to dispute whether the combination would have been suggested, but rather to dispute the teachings of the references even if the combination were made. *Id.* Nonetheless, Patent Owner's argument undercuts Petitioner's rationale for the combination itself. In particular, Petitioner relies on the fact that the invert bit in Sridhara Figure 5(b) is used to invert check information generated from odd numbers of data bits when the input data is inverted. Pet. 28–29. Although, given our claim construction set forth in Section III.C.2 above, this does in fact literally disclose the requirement of claim 1 that generation of check information

depends on the “indicator” (*i.e.*, the invert bit), Patent Owner credibly notes that the circuit of Figure 5(b) does not **protect** the invert bit from errors — it is used to ensure the Hamming code generated from the data bits has the correct value, but the invert bit itself is not part of the Hamming code calculation. Ex. 1006, Fig. 5(b); PO Resp. 26–31. Logically, if, on the receiver side, the invert bit were erroneously received, the decoder would not detect that. *Id.* We are not persuaded by Petitioner’s expert Dr. Koralek’s testimony,” incorporated by reference, that Sridhara Figure 5(b) protects the invert bit. Reply 6–10 (citing Koralek Reply Decl. ¶¶ 15–24, 29–46). As Patent Owner’s expert Dr. Przybylski testifies, Figure 5(b) does not extend the code generation matrix *G* to add an additional column to accommodate the indicator bit, without which the generated error code cannot protect the indicator. Przybylski Decl. ¶ 120. Thus, even if one of ordinary skill were looking to “improve” the circuit of Iglesia Figure 5 by protecting the flip bits with check information, Sridhara Figure 5(b) and its accompanying description would not supply a means to do so.

Accordingly, based on our review of the record, we determine that that Petitioner has not proved by a preponderance of the evidence that one of ordinary skill in the art would have combined Iglesia and Sridhara in the manner proposed by Petitioner. Therefore, we determine that Petitioner has not proved by a preponderance of the evidence the subject matter of any of claims 1, 9–13, 24, and 25 would have been obvious over that combination.

E. Obviousness of Claims 1, 11–13, 24, and 25 Over Sridhara Alone

For the first time in its Reply, Petitioner argues that “Sridhara teaches or suggests every element of at least claims 1, 11-13, 24, and 25.” Reply 11. No such ground is set forth in the Petition. See Pet. 3. Nonetheless,

Petitioner argues that it set forth this position in its Petition. *Id.* (citing Pet. 21–32, 41–55). However, the portions of the Petition relied on present Petitioner’s obviousness arguments solely based on the *combination* of Sridhara with Iglesia. Sur-Reply 4–5. In particular, Petitioner relies on the system architecture of Iglesia to account for the lack of explicit disclosure in Sridhara of a system with a processor and circuits, and, for each claim element, asserts that “Iglesia in view of Sridhara teaches or suggests” that element. *E.g.*, Pet. 19, 21. Petitioner may not raise an entirely new ground for challenging the claims for the first time in its Reply. *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330 (Fed. Cir. 2019) (citing 37 C.F.R. § 42.23(b), 35 U.S.C. § 312); *Nichia Corp. v. Document Sec. Sys., Inc.*, IPR2018-01165, Paper 28 at 57–59 (PTAB Dec. 10, 2019). Therefore, we do not consider this new ground. Nor would it be necessary to do so for claims 1, 12, 14, and 25, because, as stated in Section III.G below, we have determined that Petitioner has proved by a preponderance of the evidence that claims 1, 12, 24, and 25 are anticipated by Liu.⁴

⁴ Patent Owner, faced for the first time in Petitioner’s Reply with the assertion that Sridhara alone rendered obvious claims 11 and 13, argues that Petitioner has waived the right to make this argument. Sur-Reply 4–9. We agree. *E.g.*, 37 C.F.R. § 42.23(b) (“A reply may only respond to arguments raised in the . . . patent owner response.”). However, even if Sridhara were to be considered alone, we are unable to discern any teaching or suggestion of “determin[ing] the parity bit using the data bits and a checksum,” as required by claim 11. Petitioner merely points to the portion of Sridhara in which the checksum is determined (according to Petitioner) by the data and the indicator. Pet. 42–43. This has nothing to do with a parity bit being determined by a checksum.

Likewise, Petitioner fails to prove that Sridhara would have taught or suggested the “parity-check matrix” required by claim 13. Petitioner relies on Figure 7 of Sridhara, and characterizes it as disclosing the use of

F. Obviousness of Claims 2, 3, 5, 14, 15, 17, and 21–23 Over Iglesia, Sridhara, and Uya

Petitioner challenges independent claim 14 and dependent claims 2, 3, 5, 15, 17, and 21–23 as unpatentable under pre-AIA 35 U.S.C. § 103(a) over the combination of Iglesia, Sridhara, and Uya. Pet. 55–72.

Uya, titled “Complementary Channel Type MOS Transistor Exclusive Or/Nor Logic Gate Circuit,” was filed August 28, 1981 and issued November 22, 1983. Ex. 1022, codes (54), (22), (45). Petitioner relies on Uya for its disclosure of an example of a specific circuit that one of ordinary skill could have used to implement an XOR gate. *Id.* at 56–58.

In support of the combination of Iglesia, Sridhara, and Uya, Petitioner refers to its arguments discussed above for the combination of Iglesia and Sridhara, and supplements them by arguing that a person of ordinary skill in the art would have been further motivated to implement the higher-level description of a conditional inverter in Sridhara with specific circuit details disclosed in Uya. Pet. 55–58. Nothing that Petitioner submits in regard to Uya provides any additional support for combining Iglesia and Sridhara. Because, as discussed above, we determine that Petitioner has not proved by a preponderance of the evidence that one of ordinary skill in the art would have been motivated to combine Iglesia and Sridhara, we likewise determine that Petitioner has not proved by a preponderance of the evidence that claims

Hamming codes. Pet. 52–54. However, Figure 7 does not pertain to the BIH embodiment of Sridhara, which is the basis for all of Petitioner’s other arguments directed to other claims, but rather depicts a completely different embodiment, which Sridhara refers to as “Duplicate-add-parity bus-invert (DAPBI),” and which uses simple parity bits, rather than Hamming codes. Ex. 1006, Table I, 660.

2, 3, 5, 14, 15, 17, and 21–23 are unpatentable over the combination of Iglesia, Sridhara, and Uya.

For completeness of the record, even if the asserted combination were supported, we determine that Petitioner has not proved by a preponderance of the evidence that the asserted combination would have taught or suggested the subject matter of claims 2, 3, 5, 14, 15, 17, or 21–23. Dependent claim 2 requires, for example, “determin[ing] a first check information assuming a first state of the indicator and to modify the first check information using a second check information if an actual state of the indicator is different from the first state.” Ex. 1001, 11:26–29. The second element of independent claim 14 has a commensurate requirement:

[T]he check information is equal to a first check information when the indicator indicates that the data bits represent the original message and the check information is equal to the first check information modified by a second check information when in case [sic] the indicator indicates that the data bits represent the inverted version of the original message.

Id. at 12:48–54. The remaining claims challenged in this asserted ground, i.e., claims 3, 5, 15, 17, and 21–23, depend from claims 2 or 14. *Id.* at 11:30–14:13.

The ’526 patent provides an example of the subject matter to which these limitations of claim 2 and 14 are directed, as shown in Figure 3, reproduced below.

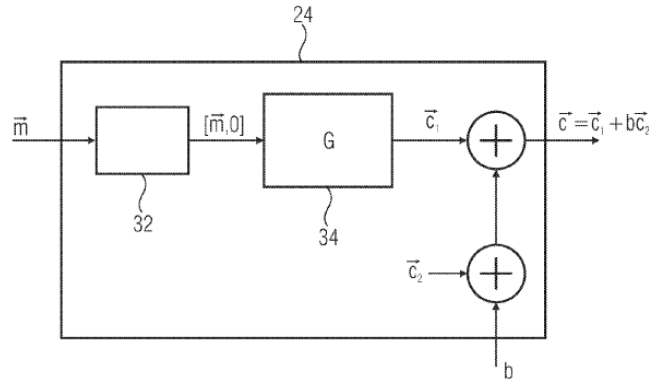


FIG 3

Figure 3 illustrates details of processor 24 (discussed in Section II.A above in connection with Figure 2), which receives original message data $\vec{m}$, in the form of a series of multi-bit words. Circuit 32 appends a zero to the data, in effect provisionally assuming that the indicator b has a value of zero. The modified data is input to code generator matrix G , producing first check information $\vec{c}_1$, which is added to second check information $\vec{c}_2$ if the actual value of b is one. Ex. 1001, Fig. 3, 3:43–61. Thus:

[T]he first check information $\vec{c}_1$ is obtained when assuming that the signaling bit b indicates no inversion, and the second check information $\vec{c}_2$ is only added to the first check information $\vec{c}_1$ in case an inversion of the original message is performed.

Id. at 3:61–66.

For claim 2 and the second element of claim 14, Petitioner relies on Figure 5(b) of Sridhara, which discloses conditionally inverted parity bits generated from an inverter that accepts an initial parity bit from the parity generator and inverts it depending on the state of the invert bit — Petitioner’s expert Dr. Koralek testifies that the inverted parity bit is the claimed “second check information.” Pet. 58–60, 67 (citing Ex. 1006,

Fig. 5(b), 659; Koralek Decl. ¶¶ 143–144). Petitioner further relies on Uya for specific details that it asserts would have been an obvious implementation of the inverter in Sridhara Figure 5(b). *Id.* at 57–58 (citing Ex. 1022, Fig. 4, 3:1–4, 3:41–52; Koralek Decl. ¶¶ 139–140). In particular, Dr. Koralek testifies that the output of transistors Q₅ and Q₆ of the Uya Figure 4 circuit is the claimed “second check information.” *Id.* at 60–63 (citing Ex. 1022, Fig. 4; Koralek Decl. ¶¶ 145–146).

Patent Owner argues that there is no “second check information” that is used to “modif[y]” the “first check information” in Sridhara Figure 5(b), alone or as modified by Figure 4 of Uya. PO Resp. 36–46 (citing Przybylski Decl. ¶¶ 136–150); Sur-Reply 24. In particular, Dr. Przybylski testifies that the asserted second check information is simply an inversion of the asserted first check information, rather than using the second check information to modify the first check information as required by the claims. Przybylski Decl. ¶¶ 147, 150.

In reply, Petitioner points out that, as conceded by Patent Owner, the ’526 patent discloses a “design optimization” that can be performed in which the second check information is simply an “all-ones vector,” which logically inverts the first check information when the inversion bit indicates the original message should be inverted. Reply 26 (citing Ex. 1001, 4:46–63; PO Resp. 37–38; Koralek Reply Decl. ¶¶ 94–95). Accordingly, argues Petitioner, Patent Owner has no basis for arguing that the second check information cannot be an inversion of the first check information. *Id.* at 26–27 (citing Koralek Reply Decl. ¶¶ 96–97).

However, the ’526 patent “design optimization” that Petitioner refers to is only applicable to a specific circumstance: “If the code generator matrix

G is chosen such that $1 \cdot G = 1$, which is true if G is chosen such that the weights of the columns of G are odd . . .” Ex. 1001, 4:47–50. Petitioner fails to show whether this condition is met in its analysis of Sridhara and Uya. The record fails to justify generally attributing the mere inversion of the first check information to be the claimed second check information, absent this specific condition recognized in the ’526 patent.

Therefore, we agree with Patent Owner that Petitioner has not proved by a preponderance of the evidence that the cited references teach or suggest the claim 2 requirement, “wherein the processor is further configured . . . to modify the first check information using a second check information if an actual state of the indicator is different from the first state,” or the commensurate requirement of claim 14. Accordingly, Petitioner has not proved by a preponderance of the evidence that the subject matter of claims 2, 3, 5, 14, 15, 17, and 21–23 would have been obvious over that combination.

G. Anticipation of Claims 1, 12, 24, and 25 By Liu

Petitioner challenges independent claims 1, 12, 24, and 25 as unpatentable under pre-AIA 35 U.S.C. § 102(a) as anticipated by Liu. Pet. 73 n.5, 88 (relying on the discussion of Liu alone at Pet. 73–79, 82–88).

Liu, titled “Method and System for Improving Memory Interface Data Integrity in PLDs,” was filed May 31, 2005 and issued September 5, 2006. Ex. 1008, codes (54), (22), (45). Because Liu issued before the earliest priority date of the ’526 patent, this reference is prior art to the ’526 patent under pre-AIA 35 U.S.C. § 102(a) or 102(b). Pet. 14–15.

Like the ’526 patent, Liu discloses an interface to a memory that stores and retrieves data words via a bus, and which uses both data bus

inversion coding and error detection coding, with both the data bits and the invert bit used to generate the check information. This is illustrated in Figure 3, reproduced below.

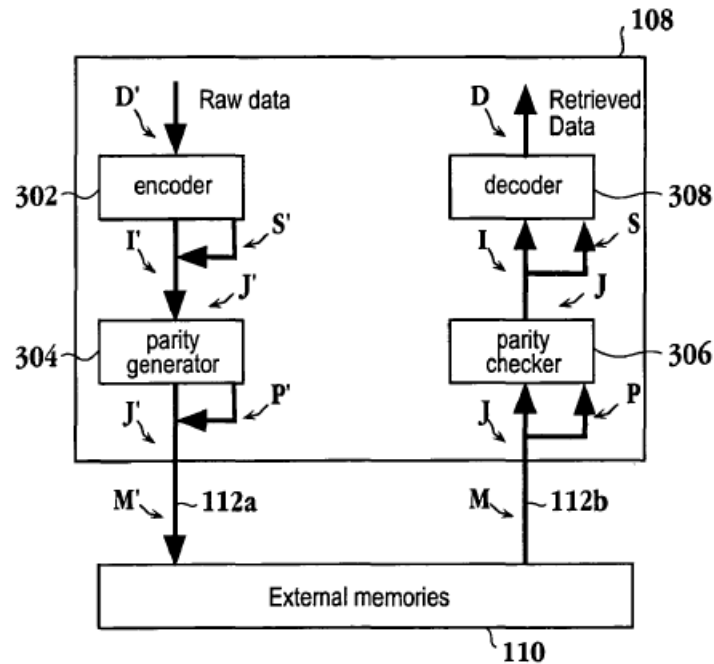


Fig. 3

Figure 3 depicts memory data manager 108 in communication with external memories 110 via buses 112(a) and 112(b). Regarding data being sent to external memories, raw data D' is provided to encoder 302, where it is inverted in accord with the bus inversion coding criteria. Encoder 302 outputs “encoded” data I' (inverted or not inverted in accord with the low power criteria) and status bit S' indicating whether or not a particular word of I' is inverted. I' and S' are combined to form data J', which is input to parity generator 304. Parity generator receives J', generates parity bit P' from that input, and provides the outputs J' and P'. J' and P' are combined to form data M', which is provided to the external memories. Ex. 1008, Figs. 3, 5, Table 1, 3:60–4:49.

As stated in Liu:

One of the drawbacks of [the prior art] arrangement is that the status bit generated by the encoder . . . to indicate encoding of the data, is not included in the raw data . . . sent to the parity generator Thus, any error that may occur with the status bit will go undetected.

....

As can be seen in FIG. 3, encoder 302 and parity bit generator 304 are connected in series. Therefore, the parity bit generator 304 sets the parity bit P' based on the number of logical high values in the data J' inclusive of the status bit S' and data I'. ***Thus, any error that may occur in the status bit S' can be detected.***

Ex. 1008, 3:55–59, 4:35–40 (emphasis added).

With respect to Figure 3, Liu further describes that for data M being retrieved from external memories, the data, including parity bit P, is provided to parity checker 306 to determine if a transmission error occurred, and encoded data I and status bit S are provided to decoder 308 to generate the final data D. Ex. 1008, Fig. 3, 4:50–5:24.

For claim 1, Petitioner asserts that Liu discloses: (i) an “apparatus [data manager 108] for generating a transmit signal comprising data bits”; (ii) with a “circuit [encoder 302] for providing an indicator indicating whether the data bits represent an original message or an inverted version thereof”; (iii) “a processor [parity generator 304] for determining check information that depends on the data bits and the indicator”; and (iv) “a circuit for forming the transmit signal including the data bits, the indicator and at least a part of the check information” [memory data manager 108 outputs M']. Pet. 75–79, 88 (citing, *e.g.*, Ex. 1008, Figs. 3–5, 1:14–16, 6:30–47; Koralek Decl. ¶¶ 171–178).

For claim 12, Petitioner asserts that Liu discloses: (i) “an apparatus [data manager 108] for extracting an original message from a received signal [M], carrying information on data bits representing the original message or an inverted version thereof [I], an indicator indicating whether the data bits represent the original message or the inverted version thereof [S], and a check information which depends on the data bits and the indicator [C]”; (ii) “a processor [parity checker 306] for determining a check information based on the received data bits and a received indicator”; (iii) “a circuit [parity checker 306] for comparing the determined check information with received check information”; and (iv) “a circuit [decoder 308] for extracting the original message based on the result of the comparison.” Pet. 82–87, 88 (citing, *e.g.*, Ex. 1008, Figs. 3, 4, 1:40–43, 2:4, 3:62–66, 6:10–19, 6:24–29;; Koralek Decl. ¶¶ 185–193).

Claims 24 and 25 are the method claim counterparts of claims 1 and 12, and Petitioner argues that the subject matter of these claims is likewise disclosed by Liu. Pet. 88 (citing Koralek Decl. ¶¶ 196–197).

Patent Owner does not address Petitioner’s challenges to claims 1 and 24, and indeed concedes that Liu anticipates those claims. Tr. 58:1–10 (“[W]e agree with the petitioner about what -- their grounds that Liu does anticipate claims 1 and 24. So there is not a dispute there.”). With respect to claims 12 and 25, Patent Owner argues that Liu does not disclose the claim 12 and 25 requirement, “extracting the original message based on the result of the comparison.” PO Resp. 58–61 (citing Przybylski Decl. ¶¶ 174–175, 177). The “comparison” referred to is the comparison between the determined check information with received check information. Ex. 1001, 12:34–37, 14:33–35. Patent Owner argues that “extracting the original

message” requires error correction capability, whereas Liu only performs error detection. PO Resp. 58 (citing Ex. 1008, 4:59–5:4; Ex. 2003: 23:6–14, 23:24–24:18; Przybylski Decl. ¶¶ 174–175); Sur-Reply 25.

Petitioner replies that the claims are not limited to error correction, and that the claim encompasses the operation of Liu, in which the original message is extracted if the parity check indicates no errors, and does not decode the data if the parity checker determines that an error has occurred. Reply 28–29 (citing Ex. 1008, 5:6–19; Koralek Decl. ¶¶ 185–186; Koralek Reply Decl. ¶¶ 102–103).

We agree with Petitioner. In the context of the ’526 patent, there is no basis for limiting “extracting the original message” to require extraction to always occur regardless of the result of the comparison between the determined check information and the received check information, and thus no basis for drawing an artificial boundary between error correction codes and error detection codes, and excluding the latter from the scope of the claims. *See Hewlett-Packard Co. v. Mustek Sys., Inc.*, 340 F.3d 1314, 1326 (Fed. Cir. 2003) (“a prior art product that sometimes, but not always, embodies a claimed method nonetheless teaches that aspect of the invention”). Indeed, for the disclosed embodiments of the ’526 patent, the patent describes a “method for extracting the original message” using a circuit which:

compar[es] the determined check information *c'* with the received check information *C* to obtain information **65** based on which *error detection* and/or correction can be performed. To *extract* the original message *m* the apparatus **60** further comprises the circuit **66**, which *extracts* the original message *m* based on the result **65** of the comparison and the received signal comprising the received data bits and the received indicator *b*.

Ex. 1001, Figs. 6, 7, 5:47–49, 5:66–57, 6:6–17 (emphasis supplied). This error detection/error correction operation is described in Figure 11 set reproduced below.

p_1	p_2	s	
0	0	0	No errors detected
0	0	>0	4 or more errors detected: don't decode
0	1	0	Error hit the parity bit p_2 , ($\bar{m}_1$, $\bar{m}_2$) error free
1	0	0	Error hit the parity bit p_2 , ($\bar{m}_1$, $\bar{m}_2$) error free
0	1	>0	Single correctable error on ($\bar{m}_1$, $\bar{m}_2$)
1	0	>0	Single correctable error on ($\bar{m}_1$, $\bar{m}_2$)
1	1	0	Single error on both $\bar{m}_1$ and $\bar{m}_2$: don't decode
1	1	>0	Double error detected on both $\bar{m}_1$ and $\bar{m}_2$: don't decode

FIG 11

Figure 11 shows a decoding scheme according to an embodiment of the '526 patent. *Id.* at 2:27–28. As can be seen, depending on how many errors occur in the message, and where they occur, sometimes the original message can be obtained and sometimes it can't. *Id.* at 9:64–10:16. No error control or detection scheme can always reproduce the original message regardless on the number of errors. Ex. 1007, 4:19–29.

Accordingly, we determine that Petitioner has proved by a preponderance of the evidence that claims 1, 12, 24, and 25 are anticipated by Liu.

H. Obviousness of Claims 1, 9, 12, 24, and 25 Over Liu and Iglesia

1. Claims 1, 12, 24, and 25

Petitioner challenges independent claims 1, 12, 24, and 25, and dependent claim 9, as unpatentable under pre-AIA 35 U.S.C. § 103(a) over

the combination of Liu and Iglesia. Pet. 73–88. In arguing this ground, Petitioner further asserts that Liu alone “teaches or suggests every element” of these claims. Pet. 73, 75. Because, as discussed above, we have determined that Petitioner has proved by a preponderance of the evidence that claims 1, 12, 24, and 25 are anticipated by Liu, we determine that Petitioner has proved by a preponderance of the evidence that these claims would also have been obvious over Liu and Iglesia, with Liu providing all of the necessary teachings. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (“[I]t is well settled that a disclosure that anticipates under § 102 also renders the claim invalid under § 103, for anticipation is the epitome of obviousness.” (citations and internal quotations omitted)).

Turning to claim 9, that claim depends from claim 1 and additionally requires:

wherein the check information is a checksum, wherein the apparatus is capable of being coupled to a plurality of channels via which the data bits of the transmit signal are to be transmitted simultaneously in parallel, wherein the circuit for providing an indicator is configured to provide a first indicator for a first portion of the data bits and to provide a second indicator for a second portion of the data bits, and wherein the processor is configured to determine the checksum based on the data bits and the first and second indicators.

Ex. 1001, 11:60–12:2.

2. Claim 9

a) Objective Indicia of Nonobviousness

In response to Petitioner’s argument that claim 9 would have been obvious over the combination of Liu and Iglesia, Patent Owner argues that objective indicia of nonobviousness support the patentability of claim 9, citing alleged unsuccessful attempts to combine error correction with low

power encoding as evidence of a long felt but unresolved need for the invention, and the simulations described in Sridhara as evidence of failures of others to arrive at the invention. PO Resp. 54–57. In particular, as evidence of a long felt need, Patent Owner relies on the fact that, as of the 2009 priority date of the '526 patent, error correction codes had been known for decades, and bit inversion had been developed in the 1990s. *Id.* at 56. Also, Patent Owner relies on an article included in the provisional application related to the '526 patent that summarizes the “State Of The Art,” including a bus-invert method assuming an error free environment, and memory systems that used error correction and detection combined with low power encoding. *Id.* (citing Ex. 1003, 14, Fig. 1).

Petitioner argues that Patent Owner has not explained how these prior alleged unsuccessful efforts relate to claim 9, and has not established long term need, citing the fact that Sridhara was only published two years before the filing of the provisional application that relates to the '526 patent. *See* Reply 25. Petitioner also argues that the evidence shows the success of others to come up with the invention of claim 9, citing, *inter alia*, the Sridhara, Liu and Iglesia references. *Id.*

We are not persuaded that the various alleged unsuccessful attempts to combine error correction with low power encoding, or the description of discontinued simulations in Sridhara, are evidence of a long felt but unresolved need for the invention, or of failures of others to arrive at the invention. To establish a long-felt need, the need must have been a persistent one that was recognized by ordinarily skilled artisans. *In re Gershon*, 372 F.2d 535, 538 (CCPA 1967). In addition, the long-felt need must not have been satisfied by another before Patent Owner's invention.

See Newell Cos., Inc. v. Kenney Mfg. Co., 864 F.2d 757, 768 (Fed. Cir. 1988) (“[O]nce another supplied the key element, there was no long-felt need or, indeed, a problem to be solved . . .”).

As to the first element, Patent Owner’s reliance on the discontinued simulations described in Sridhara as evidence of long felt need is insufficient, having taken place in 2005, only two years prior to the priority date of the ’526 patent. This single instance does not demonstrate a need that was “a persistent one that was recognized by those of ordinary skill in the art.” MPEP § 716.04 (2020). As to the second element, the record shows that, prior to the 2007 priority date of the ’526 patent, at least two references—Liu and Sridhara—taught combining data bit inversion with error coding with both the data bits and the status bit protected by the error coding. Ex. 1006, 658 (“ECC Generates m parity bits for the $n + p$ code bits”); Ex. 1008, 4:39–40 (“any error that may occur in the status bit S' can be detected”).

In addition, the only evidence that Patent Owner cites for failures of others, an article included in the provisional application related to the ’526 patent, contains no information establishing the relationship of the alleged unsuccessful attempts to claim 9, and no indication of when those attempts took place. Ex. 1003, 14, Fig. 1. *See Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1313 (Fed. Cir. 2006).

b) Obviousness of Claim 9 Over Liu and Iglesia

As discussed above, Liu discloses a bus inversion encoding approach in which a word of data is inverted, or not inverted, according to the encoding criteria, an invert bit is set accordingly, and both the data and invert bit are used to generate a parity bit. Ex. 1008, Figs. 3, 5, Table 1, 3:60–4:49. However, Liu does not disclose dividing up a data word into

multiple segments, and selectively inverting or not inverting each segment, with a separate flip bit generated for each segment — rather, as also discussed above, Iglesia discloses that concept. Ex. 1007, Fig. 2D, 5:28–33, 6:53–59. As Iglesia taught, by dividing up the data words in this manner, the inversion process is more effectively performed, resulting in less power consumed. *Id.* at 5:29–30, 62–63.

Petitioner notes that the illustrative embodiment of Liu uses a 16-bit data word. Pet. 73; Ex. 1008, Table 1. Petitioner further argues that one of ordinary skill in the art, as of the priority date of the '526 patent, would have known that 64-bit or 128-bit buses were common, and would have been motivated to apply the more efficient bus inversion technique taught by Iglesia to Liu, dividing up the wider bus into segments and generating for each segment its own low power coding, invert bit, and parity bit. Pet. 73–74, 80 (citing Koralek Decl. ¶¶ 168–169, 182). Petitioner's expert Dr. Koralek relies on the statements in Iglesia that "A greater power savings can be obtained by employing two flip bits," and "In general, less power is consumed as the number of flip bits employed increases." Koralek Decl. ¶ 169 (citing Ex. 1007, 5:28–29, 5:62–63). Dr. Koralek testifies that adding a second status bit to Liu would have used a known technique, that both Liu and Iglesia encode and decode data by combining bus inversion codes and parity codes for error detection, and that the combination would have yielded a predictable result. *Id.* ¶ 170. Petitioner therefore argues that, in its proposed combination of teachings, Liu provides the combined error correction and bus inversion coding that includes protection of the indicator, and Iglesia provides explicit motivation to use multiple flip bits to

selectively invert chunks of the input data. Pet. 80 (citing Ex. 1008, Fig. 3, 4:8–15, 6:10–35; Ex. 1007, 5:28–29, 5:62–63; Koralek Decl. ¶ 182).

Turning to the specific requirements of claim 9, Petitioner argues that Liu discloses that Data J' and parity bit P' form data M', which are transmitted together and at the same time on “memory interface bus 112(a),” which is a bus with multiple channels, thus satisfying the requirement “wherein the apparatus is capable of being coupled to a plurality of channels via which the data bits of the transmit signal are to be transmitted simultaneously in parallel.” Pet. 81 (citing Ex. 1008, Figs. 1, 3, 3:25–37, 3:64–66, 4:22, 5:25–35; Koralek Decl. ¶ 183). Petitioner argues that the combination of Liu and Iglesia would have taught or suggested “wherein the circuit for providing an indicator is configured to provide a first indicator for a first portion of the data bits and to provide a second indicator for a second portion of the data bits,” and “wherein the processor is configured to determine the checksum based on the data bits and the first and second indicators,” because when Liu is applied to multiple chunks of input data, the framework would provide an indicator for each chunk of input data, which indicators would be input to the parity generator, generating a checksum made up of multiple parity bits. *Id.* (citing Ex. 1008, Abstr., Figs. 3, 4, 1:40–43, 1:56–59, 2:57–62, 3:62–64, 4:19–22, 4:60–63; Koralek Decl. ¶ 183).

Patent Owner argues that Dr. Koralek’s testimony regarding the motivation to combine Liu and Iglesia is conclusory and unsupported by evidence, and that Petitioner has failed to identify any shortcomings in Liu that would have led to a combination with Iglesia. PO Resp. 47–48. In particular, Patent Owner argues that Liu uses data bus inversion to reduce

switching noise, in contrast to Iglesia's use of data bus inversion to reduce power consumption, and therefore Liu and Iglesia solve different problems in different contexts. *Id.* at 48–51 (citing Ex. 1008, 1:17–22, 1:27–29, 4:8–10, 7:63–65; Przybylski Decl. ¶¶ 157–159). Patent Owner further argues that there would have been no motivation to extend Liu to accommodate larger input data words, because Liu already disclosed that capability, and in any event Iglesia does not teach wide memory bus widths, but rather uses an I/O interface between the memory interface and the memory that reduces 72-bit widths to 18-bit widths on the memory bus. *Id.* at 48–49 (citing Ex. 1007, 3:24–31; Ex. 1008, 3:35–37; 5:29–33; Przybylski Decl. ¶¶ 154–155, 157). Also, Patent Owner argues Liu and Iglesia differ significantly in their technological context, because Iglesia discloses selective inversion in buses internal to a memory controller, whereas Liu applies that technique to a memory bus. *Id.* at 51 (citing Ex. 1007, Fig. 5; Ex. 1008, 1:11–16, 2:10–19, 3:26–35; Przybylski Decl. ¶¶ 158).

In addition, Patent Owner argues that, even if Liu and Iglesia were combined, there would be no teaching of the required “checksum,” because the resulting additional parity bits would simply be a collection of individual parity bits, which, according to Patent Owner, would not be a checksum. PO Resp. 51–54 (citing Przybylski Decl. ¶¶ 165, 168–170).

Patent Owner's arguments do not undermine or diminish the persuasiveness of Petitioner's contentions. Although Liu allows the possibility of using wider buses, the only specific example described uses 16-bit data widths. Ex. 1008, 3:35–37, Table 1. Both Liu and Iglesia teach the advantage of inverting the bits on a bus if a majority of the bits are in a given state. Ex. 1007, 2:65–3:2; Ex. 1008, 2:10–15. Iglesia teaches that, as

the width of a bus increases, it is advantageous to divide the bus into chunks of data, test each chunk to determine whether or not to invert the bits for that chunk, and for each chunk add a bit indicating whether or not inversion was performed. Ex. 1007, Figs. 2A, 2B, 5:14–36. Although Liu is directed to noise suppression and Iglesia is directed to power saving, both deal with data bus inversion combined with error control, and we agree with Petitioner that one of ordinary skill would have considered the teachings of Iglesia reasonably pertinent to implementations of Liu involving bus widths wider than 16-bits, and would therefore have been motivated to make the combination. See *In re Klein*, 647 F.3d 1343, 1348 (Fed. Cir. 2011) (analogous prior art includes references “reasonably pertinent to the particular problem with which the inventor is involved”). In addition, although Liu and Iglesia deal with busses in different relationships to memory with different specific hardware implementations, the test for obviousness is not whether the features of a one reference may be bodily incorporated into the structure of another reference, but rather what the combined teachings of those references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). We thus agree with Petitioner that one of ordinary skill would have been motivated to adapt Liu using the multiple indicator bit approach of Iglesia given the trend towards wider bus widths established in the record. Accordingly, we determine that Petitioner has proved by a preponderance of the evidence that one of ordinary skill in the art would have been motivated to combine Liu and Iglesia.

Given the combination, we agree with Petitioner’s expert that the combination of Liu and Iglesia would have resulted in multiple parity bits

when applied to multiple chunks of input data. Koralek Decl. ¶ 183. We are not persuaded by Patent Owner’s argument that multiple parity bits are not a “checksum”—this argument is based on Patent Owner’s attempt to narrow the construction of “checksum” to exclude a set of simple parity bits, which construction we do not adopt as discussed in Section III.C.1 above. Our review of the record confirms Petitioner’s analysis of the remaining requirements of claim 9, and we note that Patent Owner does not specifically discuss those other requirements.

Having considered both the evidence of obviousness and Patent Owner’s submitted evidence of nonobviousness, and weighed the entirety of the evidence, we determine that Petitioner has proved by a preponderance of the evidence that claim 9 of the ’526 patent would have been obvious over the combination of Liu and Iglesia.

IV. CONSTITUTIONAL CHALLENGE

Patent Owner argues Administrative Patent Judges (APJs) remain unconstitutionally appointed, citing, among other cases, *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320 (Fed. Cir. 2019), *cert. granted sub nom. United States v. Arthrex, Inc.*, 2020 WL 6037206 (Oct. 13, 2020) and *Lucia v. SEC*, 138 S. Ct. 2044, 2049 (2018). PO Resp. 61. Patent Owner argues that although the Federal Circuit attempted to cure this constitutional defect in *Arthrex* by severing Title 5’s removal protections, the solution is insufficient because it did not give a constitutionally appointed principal officer the power to review APJ decisions. *Id.* at 61–62 (citing *Lucia*, 138 S. Ct. at 2049).

Patent Owner also argues that the retroactive application of *inter partes* review to pre-AIA patents violates the Due Process clause of the 5th

Amendment, and is a physical and regulatory taking under the Takings Clause of the 5th Amendment. *Id.* at 62.

We decline to consider Patent Owner’s constitutional challenges. The Federal Circuit has addressed the issue of APJ appointment status in *Arthrex*, 941 F.3d at 1325, 1337– 38 (“This as-applied severance . . . cures the constitutional violation.”); *see also Arthrex, Inc. v. Smith & Nephew, Inc.*, 953 F.3d 760, 764 (Fed. Cir. 2020) (Moore, J., concurring in denial of rehearing) (“Because the APJs were constitutionally appointed as of the implementation of the severance, inter partes review decisions going forward were no longer rendered by unconstitutional panels.”). The Federal Circuit has also addressed the 5th Amendment due process and takings issues in *Celgene Corp. v. Peter*, 931 F.3d 1342, 1362–63 (Fed. Cir. 2019).

V. CONCLUSION⁵

In summary:

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 9–13, 24, 25	103(a)	Iglesia, Sridhara		1, 9–13, 24, 25

⁵ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

2, 3, 5, 14, 15, 17, 21–23	103(a)	Iglesia, Sridhara, Uya		2, 3, 5, 14, 15, 17, 21–23
1, 9, 12, 24, 25	103(a)	Liu, Iglesia	1, 9, 12, 24, 25	
1, 12, 24, 25	102(a)	Liu	1, 12, 24, 25	
Overall Outcome			1, 9, 12, 24, 25	2, 3, 5, 10, 11, 13–15, 17, 21–23

VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 9, 12, 24 and 25 of the '526 patent are unpatentable;

FURTHER ORDERED that Petitioner has not demonstrated by a preponderance of the evidence that claims 2, 3, 5, 10, 11, 13–15, 17, and 21–23 of the '526 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, any party to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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