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SPECIAL ISSUE ON THE 1995 ISSCC: ANALOG, SIGNAL PROCESSING, AND COMMUNICATIONS CIRCUITS

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A Half-pel Precision MPEG2 Motion-Estimation Processor with Concurrent Three-Vector Search

Kazuya Ishihara, Shinichi Masuda, Shinichi Hattori, Hirofumi Nishikawa, Yoshihide Ajioka, Tsuyoshi Yamada, Hiroyuki Amishiro, Shin-ichi Uramoto, Masahiko Yoshimoto, and Tadashi Sumi

Abstract—A half-pel precision MPEG2 motion estimation processor using a 0.5 μm CMOS technology supports all prediction modes in MPEG2 including frame, field and dual-prime prediction, and estimates three vectors concurrently. The multiple processor configuration allows a search range expansion by ± 127.5 , keeping bus traffic constant. It integrates 850 K transistors in a 13.85 mm $\times$ 13.55 mm silicon die. The observed maximum operating frequency is 75 MHz. At 40 MHz for NTSC, the peak computational power is 20 GOPS and the power dissipation is 1.9 W.

I. INTRODUCTION

IMAGE compression is an essential technology in the realization of the digital information highway. The international video compression standard, Moving Picture Experts Group (MPEG2) [1] in particular is an important technology in building digital CATV, digital DBS, digital HDTV and so on. The MPEG2 is based on a motion compensated, inter-frame DCT, and its motion vector estimation has a great impact on video quality.

The motion estimation for MPEG2 requires a huge number of computations to search for the best motion vector. Also a half-pel precision search with various prediction modes such as field based prediction, frame based prediction and dual-prime prediction must be performed to get a better quality image at a lower bit rate. Some VLSI motion estimation engines have been developed and reported, but none of them meets all of the above requirements for MPEG2 motion estimation [2], [3].

This paper describes a half-pel precision MPEG2 motion estimation processor (ME2), which is a key device for the realization of the digital highway. It is capable of processing ITU-R601 (720 pixels $\times$ 480 lines, 30 frames/s) video in real-time in a single chip when the search range is ± 7.5 horizontally by ± 15.5 vertically. It also supports all prediction modes for MPEG2. The ME2 is configured with a 1-D systolic array for integer-pel precision exhaustive block matching and an independent processing unit for half-pel precision search.

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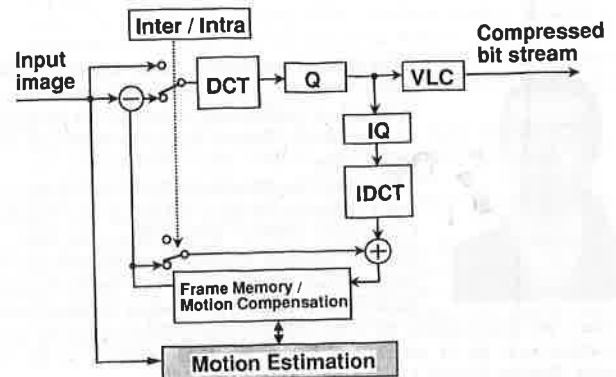


Fig. 1. The MPEG2 algorithm.

It has been fabricated using a 0.5 μm CMOS technology and incorporates 850 K transistors.

In this paper, we will present the architectural features of the ME2. The necessary processing power for the exhaustive block matching is implemented with an 1-D systolic array. The 1-D systolic array structure simplifies the data transfer mechanism. Also, we realized the concurrent three vector search without area penalty by utilizing a novel distortion summation scheme. A half-pel precision processing unit is introduced independently with the integer-pel precision exhaustive block matching unit. It estimates three half-pel precision vectors according to the three integer-pel precision vectors. It also supports dual-prime prediction. The problem with the communication bandwidth to the frame memory, which is a bottleneck for the search range expansion, is solved by introducing the variable pipeline architecture. This architecture requires no additional access to the frame memory in horizontal search range expansion with multiple chip configuration. Also, it requires no external distortion comparison hardware, because one ME2 estimates vectors in wider horizontal search range for one macroblock.

Section II illustrates the MPEG2 algorithm and its motion estimation. Section III addresses the architectural features of the ME2. Then Section IV describes LSI chip implementation and Section V lists the chip characteristics and the system performances. The Conclusion is presented in last section.

II. MOTION ESTIMATION IN THE MPEG2 ALGORITHM

The MPEG2 algorithm is a hybrid coding scheme as shown in Fig. 1. It utilizes the discrete cosine transform, the quan-

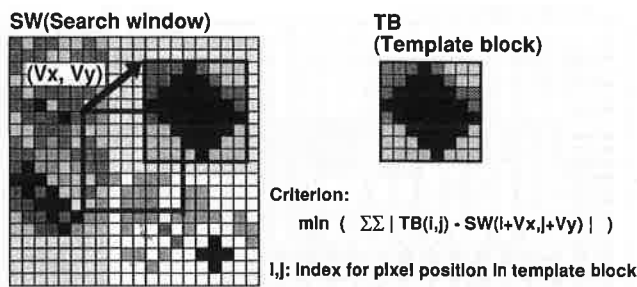


Fig. 2. Block matching technique.

TABLE I
PREDICTION MODES IN THE MPEG2

Picture structure	Prediction mode	Template block size (number of vector)
Field	Field-based prediction	16x16 (one vector)
	16 x 8 MC	16x8 upper, 16x8 lower (two vectors)
	Dual-prime	16x16 (one vector and dmvc)
Frame	Frame-based prediction	16x16 (one vector)
	Field-based prediction	16x8 top, 16x8 bottom (two vectors)
	Dual-prime	16x16 (one vector and dmvc)

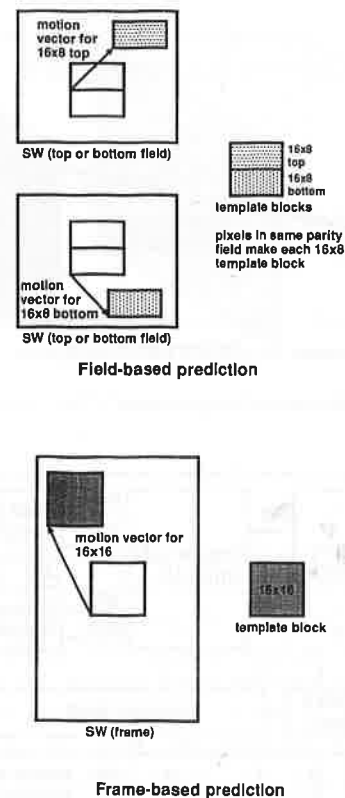


Fig. 3. Three motion vectors for the frame structure picture.

tization and the inter-frame prediction in the source coding part. The motion estimation technique is used to enhance the efficiency of the prediction.

Motion estimation is a procedure to find the best motion vector representing a displacement to the predictor from the position of the template block. Block matching is the most common way of realizing the motion estimation and has often been utilized for the implementation of motion compensated predictive coding. Fig. 2 shows a block matching technique. In block matching, the processor finds the vector whose distortion is a minimum over the search range. The mean absolute difference is one of the criteria of the distortion function, and is suitable for VLSI implementation of block matching based motion estimation because it doesn't require area-consuming multiplication.

Distortion function with mean absolute difference criterion is defined as follows:

$$F_{\text{distortion}} = \sum \sum |TB(i,j) - SW(i + V_{x,j} + V_y)| \quad (1)$$

where $TB(i,j)$ ($i,j = 0,1,2,\dots,N-1$) is the pixel data of the template block and $SW(i,j)$ ($i,j = 0,1,2,\dots,N-1$) is the pixel data of the search window, (V_x, V_y) is the motion vector derived from the minimum $F_{\text{distortion}}$. The provided block size is $N \times N$.

As is seen from the above equations, the block matching with mean absolute difference requires numerous number of subtraction and absolute operations however it needs no

multiplications. For the real-time processing of NTSC resolution video, about 5 giga operations are required when the block size is 16×16 and the search range is ± 7 by ± 15 . Moreover the MPEG2 defines various prediction modes with half-pel precision and bidirectional motion compensation, so the required computational power becomes more serious problem. Table I summarizes the prediction modes in the MPEG2. Fig. 3 shows three motion vectors for the frame structure picture without dual-prime prediction. In the frame based prediction mode, the block size is 16×16 and the one motion vector is detected for a macroblock. In the field based prediction mode, the block size is 16×8 and two motion vectors are detected for a macroblock. For the frame structure pictures, the best prediction mode and motion vectors for a macroblock are selected from three prediction modes, frame-based prediction, field-based prediction, and dual-prime prediction. Fig. 4 illustrates the bidirectional motion compensation. In this case, there are two search windows per macroblock, so the required computational power doubles.

Hence, the requirements for the MPEG2 motion estimation processor are summarized as follows:

- 1) A capability to estimate motion vectors concurrently for various prediction modes,
- 2) a half-pel precision accuracy for motion estimation, and
- 3) an extendible search range according to the system requirements.

In order to meet the above requirements, several architectural enhancements have been made to the ME2.

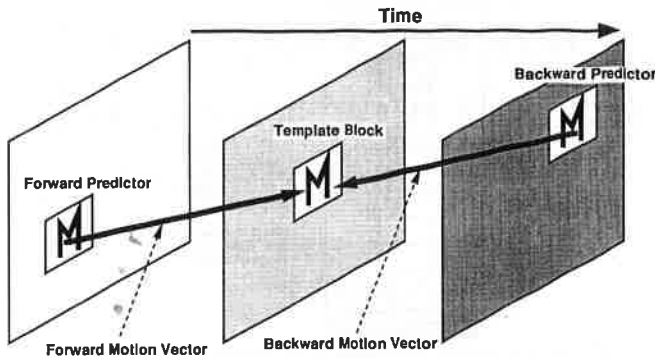


Fig. 4. Bidirectional motion compensation.

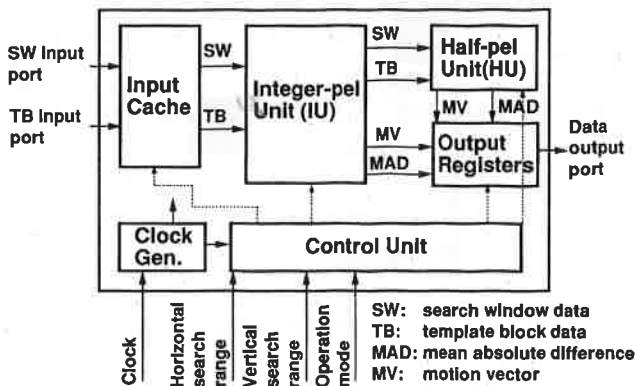


Fig. 5. Block diagram of the ME2.

III. ARCHITECTURE

A. Overall Configuration

The overall block diagram of ME2 is shown in Fig. 5. The matching strategy of ME2 is based on the full search block matching for integer-pels. This operation is performed in an Integer-pel Unit (IU). The full search block matching realizes a better efficiency for finding the optimum vectors than the hierarchical search which has been employed in some other processors [4]. For the half-pel precision search in a Half-pel Unit (HU), only eight candidate vectors surrounding the selected integer-pel vector are evaluated. In both processing units, the matching criterion is the mean absolute difference. The architectural features of the ME2 are as follows:

- 1) 1-D systolic array to achieve highly efficient processing,
- 2) an effective summation scheme to estimate three vectors concurrently,
- 3) a data transfer mechanism from IU to HU to reduce frame memory access,
- 4) on-chip half-pel processors with the dual-prime prediction mode, and
- 5) a variable pipeline stage in a multiple configuration for a wider search range.

B. Integer-pel Unit

The first feature is the 1-D systolic array utilized in the IU. The block diagram of the IU is shown in Fig. 6. The IU

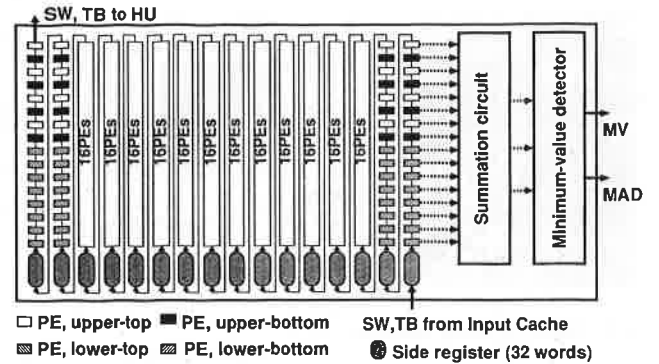


Fig. 6. Block diagram of Integer-pel Unit (IU).

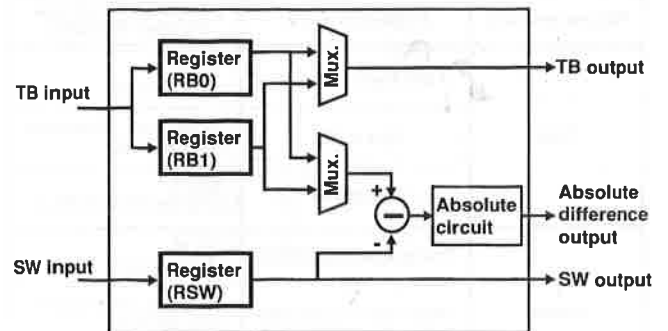


Fig. 7. Schematic diagram of the PE.

consists of 256 processing elements (PE's), summation circuits and a minimum-value detector. The PE's are arranged as the 1-D systolic array [5]. The array has communication paths for pixel data connected between only neighboring processing elements. Therefore the data transfer can be accomplished with only shift registers in the PE and register files in the side registers. Each PE corresponds to a pixel on the template block which is preloaded before processing. With this structure, the processing of block matching and the data transfer are performed simultaneously. During the processing period, the absolute differences over the block for different motion vectors are calculated in the array. Fig. 7 shows a schematic diagram of the PE. The PE consists of two registers (RB0, RB1) for the template block data, one of them is utilized for the calculation and the other is for data input during the calculation. This feature enables highly efficient processing and achieves 10 Giga Operations Per Second (GOPS) peak performance at 40 MHz. This performance is sufficient for real-time processing of NTSC resolution video when the search range is ± 7 by ± 15 .

The second feature is the effective summation scheme. The absolute differences computed in each PE are classified in four groups, upper-top, upper-bottom, lower-top and lower-bottom according to the position of each PE as shown in Fig. 6. Here, upper and lower mean the upper-half and the lower-half of the position. Also, top and bottom mean the parity of the each field. Three different distortions for three vectors are summed up concurrently under a data flow control in the summation circuit. Fig. 8 shows the summation circuits, and Table II summarizes the summation scheme which estimates

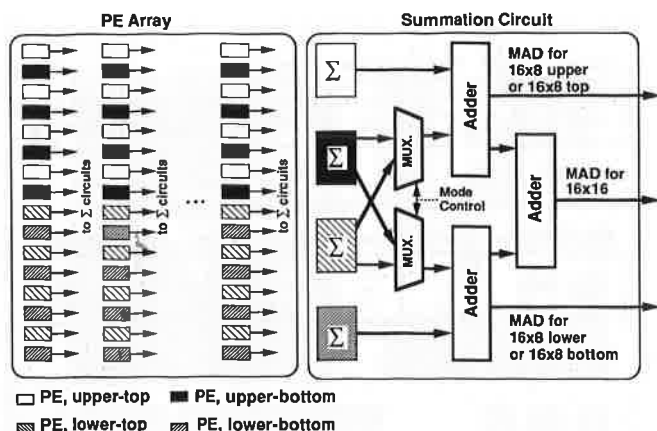


Fig. 8. Block diagram of summation circuit.

TABLE II
DISTORTION SUMMATION SCHEME FOR THREE VECTORS

Picture structure	Template block size (Motion Vector type)	Distortion summation scheme
Field	16 x 8 upper (16 x 8 MC)	$\Sigma_{\text{upper-top}} + \Sigma_{\text{upper-bottom}}$
	16 x 8 lower (16 x 8 MC)	$\Sigma_{\text{lower-top}} + \Sigma_{\text{lower-bottom}}$
	16 x 16 (Field)	$(\Sigma_{\text{upper-top}} + \Sigma_{\text{upper-bottom}}) + (\Sigma_{\text{lower-top}} + \Sigma_{\text{lower-bottom}})$
Frame	16 x 8 top (Field)	$\Sigma_{\text{upper-top}} + \Sigma_{\text{lower-top}}$
	16 x 8 bottom (Field)	$\Sigma_{\text{upper-bottom}} + \Sigma_{\text{lower-bottom}}$
	16 x 16 (Frame)	$(\Sigma_{\text{upper-top}} + \Sigma_{\text{lower-top}}) + (\Sigma_{\text{upper-bottom}} + \Sigma_{\text{lower-bottom}})$

the three vectors concurrently for the field and the frame structure pictures. The summation circuit consists of four Σ circuits, two selectors and three adders. Each Σ circuit has cascaded 4-to-2 compressors in the Wallace's tree and an adder. The cascaded 4-to-2 compressors produce two 13-b accumulated outputs from 64 8-b PE's outputs in the same group, and the adder summed up them to make one 14-b accumulated result. In the frame structure pictures, upper-top and lower-top are summed up to estimate the vector for the top 16×8 template block, upper-bottom and lower-bottom are for the bottom 16×8 template block. Then all groups are summed up for the 16×16 template block. These operations are performed simultaneously for concurrent three vector search. The minimum-value detector finds the minimum distortions and selects the best vectors for each three template block. In the field structure pictures, upper-top and upper-bottom are summed up to estimate the vector for the upper 16×8 template block, lower-top, and lower-bottom are for the lower 16×8 template block. The following operation is the same as for the frame structure pictures. This scheme increases the processing power twice equivalently $((16 \times 16) + 2 \times (16 \times 8))$ absolute differences per cycle, 20 GOPS at 40 MHz, and realizes a concurrent three-vector search with a very small area penalty. Hence, an efficient hardware implementation for the motion estimation with the integer-pel accuracy was achieved.

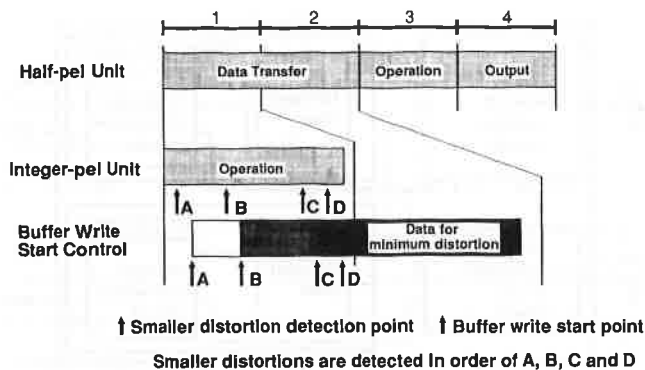


Fig. 9. Data transfer mechanism from the IU to the HU.

C. Half-pel Unit

The third feature is the data transfer mechanism from the IU to the HU. In this architecture, data transfer to the HU is realized by delivering the data from the IU through intermediate buffer memories, instead of the conventional transfer from the off-chip frame memory. The IU's configuration and processing manner allows the candidate search window for the HU to be obtained from the IU. Owing to the 1-D array structure of the IU, HU can get the candidate search window from the IU after the IU detects the motion vector which has minimum distortion. Fig. 9 illustrates the data transfer mechanism. The HU operates with block level pipelining. Stages 1 and 2 are for data transfer from the IU to the HU. Stage 3 is for the actual operation, and stage 4 is for results output. The data transfer can be controlled by the flag indicating the detection of smaller distortion. In this case, smaller distortion was detected in order of A, B, C, and D. The data transfer operations are started whenever the new smaller distortion is detected. Finally, the necessary pixel data for half-pel generation correspond to the minimum distortion D is stored in the buffer memories. This architecture causes no off-chip frame memory access for the HU operation and simplifies the control of the buffer memories. Also, it allows ME2's completely slave mode operation because no evaluated results in the IU are related to the frame memory access.

The fourth feature is the On-chip half-pel processors. Fig. 10 shows the block diagram of the HU. The HU consists of a template data buffer memory (TBM), a search window data buffer memory (SBM) [5] and two half-pel processors. One half-pel processor is for the 16×16 template block and the other for two 16×8 template blocks. These processors calculate the distortions at eight points surrounding the best integer-pel precision vectors and find the optimum half-pel precision vectors for the three template blocks. The processor for the 16×8 template blocks operates twice with a time-multiplexing manner, once for each two 16×8 template blocks to reduce the silicon area. Also, these processors are rearranged to estimate vector for the dual-prime prediction by a mode control. Fig. 11 illustrates the data flow in the dual-prime mode. All data are provided by Input Cache, directly. A Half-pel filter of each processor generates half-pel

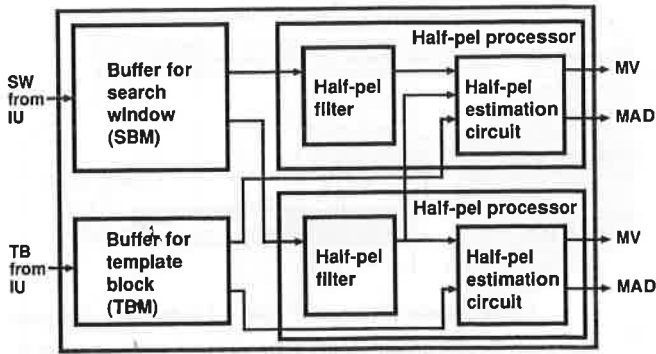


Fig. 10. Block diagram of Half-pel Unit (HU).

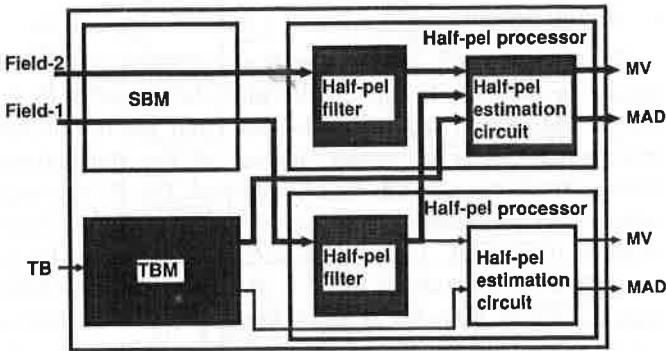


Fig. 11. Dataflow in the dual-prime mode.

precision pixels, indicated by the derived vector, using field-1 and field-2 data. The half-pel estimation circuit generates inter-field interpolated pixels for searching dmv and finds the optimum dmv . With this feature, the half-pel precision motion vectors are estimated in one chip, so the external hardware in a system is reduced.

D. Pipeline Operation and Search Range Expansion

The fifth feature is a newly introduced variable pipeline architecture which allows the expansion of the horizontal search range without external logic. With conventional motion estimation LSI's, search range must be divided and each LSI estimates local optimum vector in divided search range. Therefore, it requires external comparison between distortions for local optimum vectors. Also, it causes a bandwidth increase for the I/O data transfer. Fig. 12 shows ME2's pipelining for various horizontal search ranges. The operations are performed with a block level pipelining, template block data input, IU operation, internal data transfer, HU operation and data output. The IU can evaluate distortions for 16 horizontal by 33 vertical points exhaustively during one pipeline stage, 806 cycles. So, one ME2 searches vectors within the range of ± 7.5 horizontally by ± 15.5 vertically for NTSC or PAL video. Additional pipeline stages should be appended for IU operation to expand the horizontal search range at the expense of through-put. For example, when the horizontal search range is ± 31.5 , three additional pipeline stages are

Horizontal range = ± 7.5 , Vertical range = ± 15.5

Stage1	Stage2	Stage3	Stage4	Stage5	
TB Input	IU op. -8/+7	Data transfer IU→HU	HU op.	Data output	Each pipeline stage needs 806 cycles

Horizontal range = ± 31.5 , Vertical range = ± 15.5

Stage1	Stage2	Stage3	Stage4	Stage5	Stage6	Stage7	Stage8
TB Input	IU op. -32/-17	IU op. -16/-1	IU op. 0/15	IU op. +16/+31	Data transfer IU→HU	HU op.	Data output

Fig. 12. Pipelining of the ME2.

Horizontal range = ± 31.5 , 4-chips configuration

	TBn ME#1	TBn+1 ME#2	TBn+2 ME#3	TBn+3 ME#4	TBn+4 ME#1	TBn+5 ME#2	TBn+6 ME#3
ME#1	TBn -32/-17	TBn -16/-1	TBn 0/15	TBn +16/+31	TBn+4 -32/-17	TBn+4 -16/-1	TBn+4 0/15
ME#2		TBn+1 -32/-17	TBn+1 -16/-1	TBn+1 0/15	TBn+1 +16/+31	TBn+5 -32/-17	TBn+5 -16/-1
ME#3			TBn+2 -32/-17	TBn+2 -16/-1	TBn+2 0/15	TBn+2 +16/+31	TBn+6 -32/-17
ME#4				TBn+3 -32/-17	TBn+3 -16/-1	TBn+3 0/15	TBn+3 +16/+31

Fig. 13. Operation sequence in 4-chips configuration.

appended. With this proposed architecture, one ME2 estimates vectors in a wider search range, so no external comparison is needed.

When expanding the search range, one ME2 can't perform real-time processing for NTSC or PAL video. But a multiple processor configuration with a very simple interleaving scheme improves the through-put and keeps the real-time processing capability for the extended search range. The operation sequence in four-chips configuration is shown in Fig. 13. Each ME2 handles successive template blocks horizontally one after another. In a pipeline stage, every ME2 uses the same search window data. This is because actual searching positions in image of all processing template blocks are identical. So, as a result, this technique eliminates the increase of the I/O data rate in horizontal search range expansion. Because the ME2 with the above architecture requires no external hardware and no extra data transfer for the search range expansion, it has an excellent cascability, allowing a greater system design flexibility.

IV. LSI CHIP IMPLEMENTATION

The critical path of the ME2 is the data path for the mean absolute difference calculation which includes the absolute difference circuit in the processor array and the summation circuit. In the summation circuit, a Wallace's tree structure is adopted. The absolute circuit is configured with simple

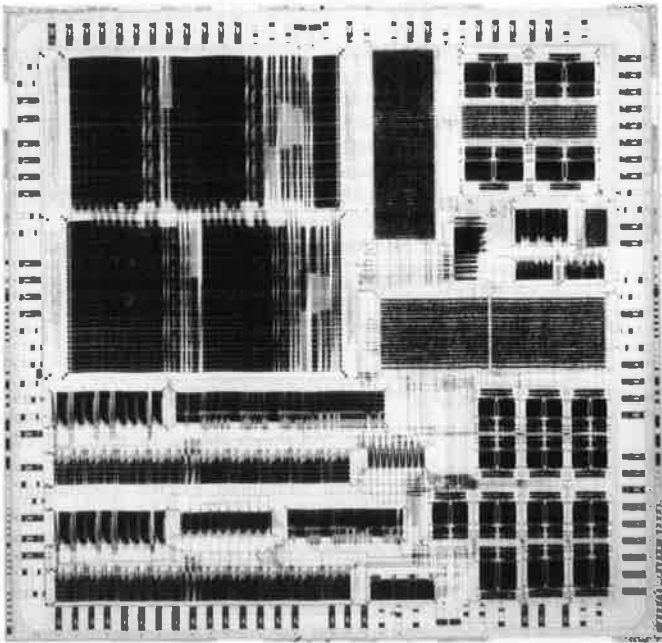


Fig. 14. Photomicrograph of the ME2.

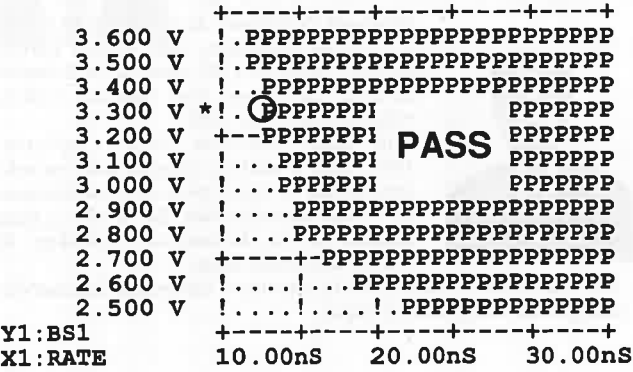


Fig. 15. Shmoo plot of the ME2.

EX-OR gates and the sign bits in the output of subtractors in processor elements are connected to the carry input of 4-to-2 compressors in the Wallace's tree. With this structure, the propagation delay and the hardware amount are reduced compared to a conventional implementation with incrementors for absolute processing. In the critical path, the simulated result of the propagation delay under the worst condition (@ 3.0 V, 125°C) is 18 ns, which is a sufficient value to ensure the 40 MHz operation.

In layout design, a data path compiler [6] was utilized to implement processing units of the IU and the HU. High density physical layout patterns were designed from schematic data in a very short time. Also, all memories were designed with a memory generation system. The ME2 has been fabricated using 0.5 μ m CMOS process technology and incorporates 850 K transistors. A photomicrograph of the ME2 is shown in Fig. 14. The operation with a 75 MHz clock at 3.3 V under room temperature has been confirmed by LSI tester as shown in Fig. 15.

TABLE III
CHARACTERISTICS OF THE ME2

Supply voltage	3.3V
Number of devices	850K
Clock rate	75MHz max. (40MHz for NTSC)
Power consumption	1.9W @3.3V,40MHz (H-range = ± 15.5)
Computational power	20GOPS (equivalently) @40MHz
Horizontal search range	$\pm 7.5, \pm 15.5, \pm 31.5, \pm 63.5, \pm 127.5$
Vertical search range	$\pm 7.5, \pm 15.5$
Operation mode	Field, Frame, Field Dual-Prime, Frame Dual-Prime

TABLE IV
SEARCH RANGE EXTENDIBILITY WITH THE MULTIPLE ME2S

Operation mode	Block size	Vertical range	Horizontal range	Chips needed
Frame	16 x 16 16 x 8 - (top) 16 x 8 - (bottom)	± 15.5 $\pm 7.5(2 \text{ fields})$ $\pm 7.5(2 \text{ fields})$	± 7.5	1
			± 15.5	2
			± 31.5	4
			± 63.5	8
			± 127.5	16
Field	16 x 16 16 x 8 - (upper) 16 x 8 - (lower)	± 15.5	± 7.5	1
			± 15.5	2
			± 31.5	4
			± 63.5	8
			± 127.5	16
Frame Dual-Prime	16 x 8	± 0.5	± 0.5	**
Field Dual-Prime	16 x 16	± 0.5	± 0.5	**

Operating frequency : @40MHz,
Image size : ITU-R601 (720x480pixels), Frame rate : 30
** Number of chips needed depends on the prediction algorithm

V. CHIP CHARACTERISTICS AND SYSTEM PERFORMANCES

Table III summarizes the characteristics of the ME2. The ME2 operates in four modes. The ME2 can provide three half-pel precision vectors concurrently in the field prediction mode or the frame prediction mode. The ME2 can perform real-time processing of NTSC-resolution video at 40 MHz, and its peak computational power is more than 20 GOPS equivalently. The ME2 dissipates 1.9 W at 40 MHz operation, which enables it to be housed in the plastic package. Table IV summarizes the search range extendibility by the multiple ME2's. For example, a ± 31.5 (horizontal) by ± 15.5 (vertical) search range for P-pictures, and two ± 15.5 (horizontal) by ± 15.5 (vertical) search ranges for B-pictures are realized using four ME2's. Also the dual-prime prediction can be implemented with additional ME2's. Hence, flexible motion estimation functions according to the system requirements are realized by using ME2's with various operation modes. Also it reduces the hardware of motion estimation to approximately one-tenth of the conventional hardware.

VI. CONCLUSION

The world's first MPEG2 motion estimation processor with half-pel precision, fully compatible with MPEG2 standard has been described. This chip performs half-pel accuracy exhaustive motion estimation and has real-time processing capability for NTSC or PAL video when the search range is ± 7.5 horizontally by ± 15.5 vertically. In addition, we have introduced several architectural enhancements to the ME2. Highly parallel architecture with 1-D systolic array contributes to the highly efficient processing. For the various prediction modes, the concurrent three vector search according to the effective distortion summation scheme is newly developed. The simplified data transfer mechanism from the IU to the HU eases the frame memory access. For the half-pel precision accuracy, on-chip half-pel processors with dual-prime prediction mode are embedded on the chip. The variable pipeline architecture with multiple processor configuration enables search range expansion. The excellent architecture requires no external distortion comparison and no increase of external data transfer. The ME2 presented above will accelerate the development of low cost and small size MPEG2 video encoder systems which are key components for the realization of the digital highway.

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