

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

TELA INNOVATIONS, INC.,
Patent Owner.

IPR2019-01637
Patent 10,141,335 B2

Before JO-ANNE M. KOKOSKI, KRISTINA M. KALAN, and
WESLEY B. DERRICK, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision

Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–11, 15, 18, 20, and 22–24 of U.S. Patent No. 10,141,335 B2 (Ex. 1001, “the ’335 patent”). Tela Innovations, Inc. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 11. We authorized additional briefing on the issues set forth in the Preliminary Response. Paper 13. Petitioner in turn filed a Reply to Patent Owner’s Preliminary Response (Paper 14) and Patent Owner filed a Sur-Reply to Petitioner’s Preliminary Reply (Paper 15).

We instituted an *inter partes* review of claims 1–11, 15, 18, 20, and 22–24 of the ’335 patent on the ground of unpatentability alleged in the Petition. Paper 16 (“Dec.”). After institution of trial, Patent Owner filed a Patent Owner Response. Paper 28 (“PO Resp.”). Petitioner filed a Reply. Paper 35 (“Reply”). Patent Owner filed a Sur-Reply. Paper 38 (“Sur-Reply”). An oral hearing was held on December 9, 2020, and a transcript of the hearing is included in the record. Paper 45 (“Tr.”).

This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–11, 15, 18, 20, and 22–24 of the ’335 patent are unpatentable.

A. *Related Proceedings*

The parties state that the ’335 patent is at issue in a number of proceedings, including *Intel Corp. v. Tela Innovations, Inc.*, No. 3:18-cv-02848-WHO (N.D. Cal.) (the “NDCA Action”). Pet. 3–5, Paper 5, 2. The parties also state that the ’335 patent was at issue in an International Trade Commission (“ITC”) investigation, Inv. No. 337-TA-1148 (the “ITC

Proceeding”), but was later terminated from the ITC Proceeding. Pet. 3; PO Resp. 3.

B. The '335 Patent

The '335 patent, titled “Semiconductor Cip [sic] Including Region Having Rectangular-Shaped Gate Structures and First-Metal Structures,” is directed to an integrated circuit. Ex. 1001, code (54), 4:37–39. The '335 patent explains that a push for circuit chip area reduction in the semiconductor industry has resulted in improvements in the lithographic process that enable smaller feature sizes to be achieved. *Id.* at 3:60–4:4. In the evolution of lithography, the minimum feature size approached, and subsequently reached a scale less than, the wavelength of the light source used to expose the feature shapes, leading to unintended interactions between neighboring features. *Id.* at 4:5–8. The '335 patent defines the difference between the minimum feature size and the wavelength of light as the lithographic gap. *Id.* at 4:11–13. The '335 patent further describes that an interference pattern occurs as each shape on the mask interacts with the light. *Id.* at 4:16–17. The interference patterns from neighboring shapes can create constructive or destructive interference. *Id.* at 4:17–19. In view of the foregoing, the '335 patent identifies a need for a solution that manages lithographic gap issues as technology continues to progress toward smaller semiconductor device feature sizes. *Id.* at 4:30–33.

The '335 patent describes that a dynamic array architecture is provided to address semiconductor manufacturing process variability associated with a continually increasing lithographic gap. *Id.* at 8:62–65. Figure 2 of the '335 patent, shown below, illustrates a generalized stack of layers used to define a dynamic array architecture.

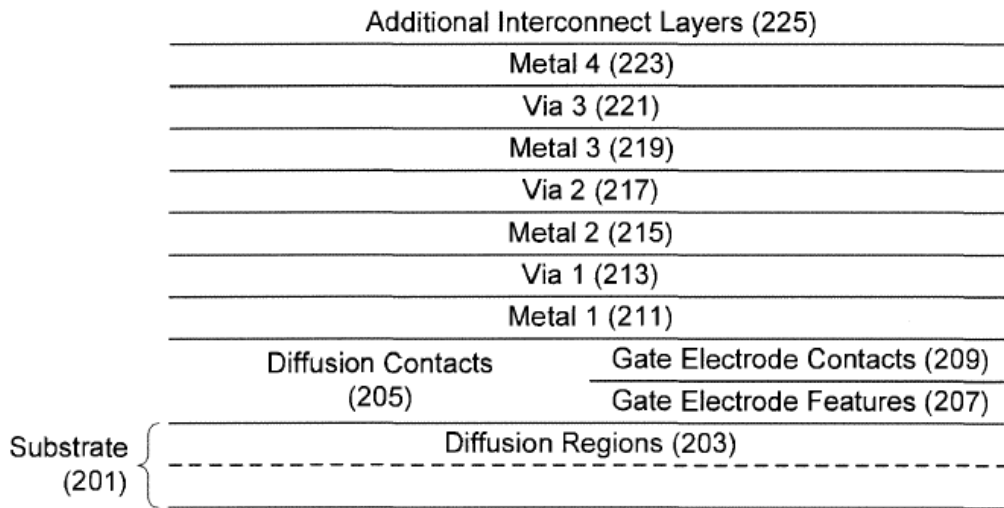


Fig. 2

Figure 2 depicts the generally underlying structure of a dynamic array. *Id.* at 11:4–18. The dynamic array is built up in a layered manner upon base substrate 201 (e.g., a silicon substrate or silicon-on-insulator (SOI) substrate). *Id.* at 11:20–22. Diffusion regions 203 are defined in base substrate 201 and represent selected regions of base substrate 201 within which impurities are introduced for the purpose of modifying the electrical properties of base substrate 201. *Id.* at 11:22–27. Above diffusion regions 203, diffusion contacts 205 are defined to enable connection between diffusion regions 203 and conductor lines. *Id.* at 11:27–29. Gate electrode features 207 are defined above diffusion regions 203 to form transistor gates. *Id.* at 11:32–34. Gate electrode contacts 209 are defined to enable connection between gate electrode features 207 and conductor lines. *Id.* at 11:34–36. Interconnect layers are defined above diffusion contact 205 layer and gate electrode contact layer 209. *Id.* at 11:39–40. The interconnect layers include first metal (metal 1) layer 211, first via (via 1)

layer 213, second metal (metal 2) layer 215, second via (via 2) layer 217, third metal (metal 3) layer 219, third via (via 3) layer 221, and fourth metal (metal 4) layer 223. *Id.* at 11:40–45.

Figure 5 of the '335 patent is shown below:

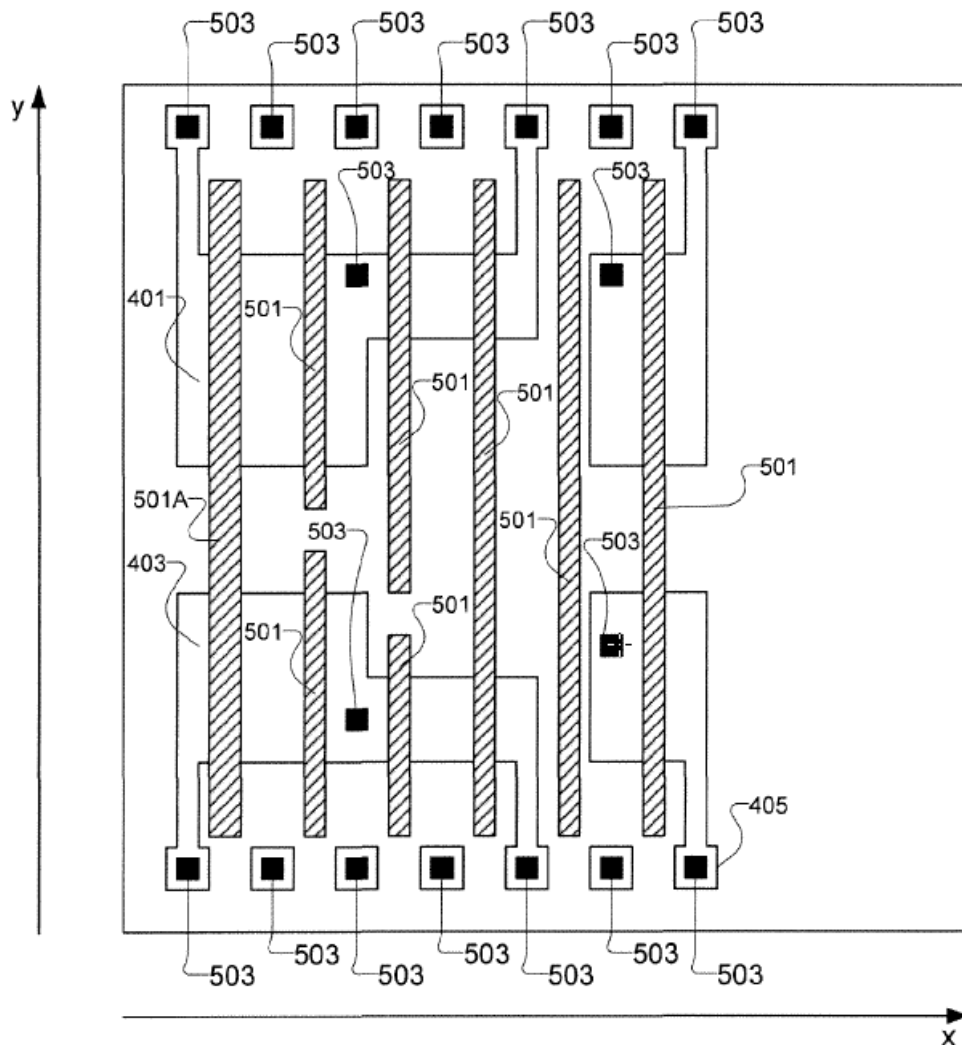


Fig. 5

Figure 5 illustrates an exemplary layout of a dynamic array that includes a gate electrode layer, a diffusion contact layer, and a diffusion layer. *Id.* at 16:10–13. The diffusion layer shows p-diffusion region 401 and n-

diffusion region 403. *Id.* at 15:52–54. The gate electrode layer shows gate electrode features 501 that define the transistor gates. *Id.* at 16:13–15. Gate electrode features 501 are defined as linear shaped features extending in a parallel relationship across the dynamic array in a “y” reference direction. *Id.* at 16:15–18. Gate electrode features 501 form n-channel and p-channel transistors as they cross diffusion regions 403 and 401, respectively. *Id.* at 16:30–32. The ’335 patent describes that each of the gate electrode tracks may be interrupted any number of times in linearly traversing across the dynamic array in order to provide required electrical connectivity for a particular logic function to be implemented. *Id.* at 16:41–44. When a given gate electrode track is required to be interrupted, the separation between ends of the gate electrode track segments at the point of interruption is minimized to the extent possible. *Id.* at 16:45–49. Minimizing the separation between ends of the gate electrode track segments at the points of interruption serves to maximize the lithographic reinforcement, and uniformity therefor, provided from neighboring gate electrode tracks. *Id.* at 16:53–56.

Figure 8B of the ’335 patent is shown below:

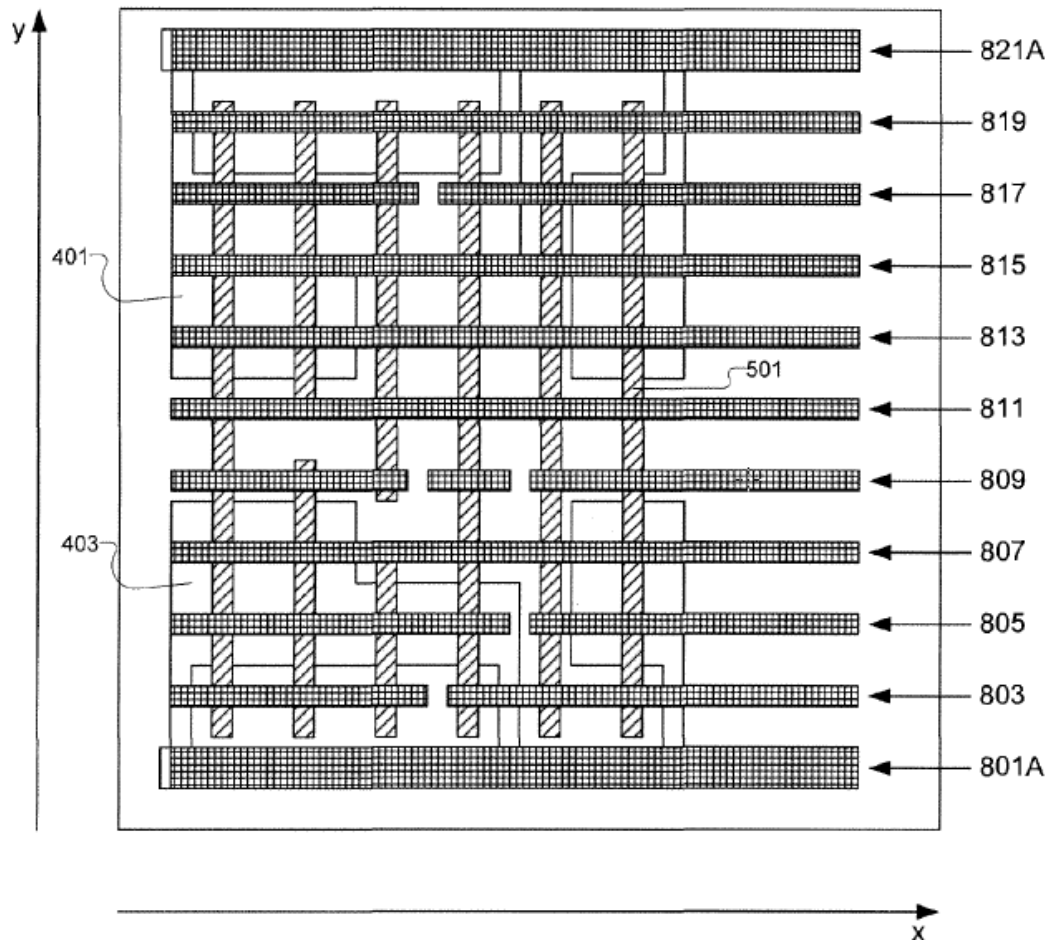


Fig. 8B

Figure 8B depicts metal 1 layer defined above the gate electrode layer of Figure 5, in accordance with one embodiment of the invention. *Id.* at 17:38–41, 21:41–43, 22:21–24. Specifically, metal 1 layer includes a number of metal 1 tracks 801–821 defined to include linear shaped features extending in a parallel relationship across the dynamic array. *Id.* at 21:43–46.

The '335 patent states that a semiconductor chip can include a region having at least ten conductive structures, with some of the conductive structures forming at least one transistor gate electrode. *Id.* at 5:50–57. The conductive structures each have a width in a direction that is perpendicular

to a direction along its lengthwise centerline and that is less than 45 nanometers. *Id.* at 6:16–19, 6:27–30, 6:38–39. The '335 patent further states that the pitch between the lengthwise centerlines of conductive structures is less than or equal to about 193 nanometers. *Id.* at 6:40–46. With regard to the embodiments depicted in Figures 8A and 8B, the '335 patent discloses that the pitch of metal 1 tracks 801–821 and metal 2 tracks 1001 is minimized while ensuring optimization of lithographic reinforcement provided by neighboring tracks. *Id.* at 21:51–55, 22:57–60. In one example, metal 1 tracks 801–821 are centered on a vertical grid of about 0.24 μm for a 90 nm process technology. *Id.* at 21:55–57. In another example, the optimum contacted gate electrode track pitch is 0.36 μm and the optimum metal 2 track pitch is 0.24 μm for a 90 nm process technology. *Id.* at 23:5–8.

C. Illustrative Claim

Petitioner challenges claims 1–11, 15, 18, 20, and 22–24 of the '335 patent. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

1. A semiconductor chip, comprising:
gate structures formed within a region of the semiconductor chip, the gate structures formed in part based on corresponding gate structure layout shapes used as an input to a lithography process, the gate structure layout shapes positioned in accordance with a gate horizontal grid, the gate horizontal grid including at least seven gate gridlines, each gate structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, each gate gridline having at least one gate structure layout shape positioned thereon, wherein adjacently positioned ones of the gate structures are separated from each other by a gate pitch

of less than or equal to about 193 nanometers, each of the gate structures having a width of less than or equal to about 45 nanometers, wherein each pair of the gate structures that are positioned in an end-to-end manner are separated from each other by a line end-to-line end gap of less than or equal to about 193 nanometers;

a first-metal layer formed above top surfaces of the gate structures within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate structures, the first-metal layer separated from the top surfaces of the gate structures by at least one insulator material, adjacent metal layers in the stack of metal layers separated by at least one insulator material, wherein the first-metal layer includes first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, the first-metal structure layout shapes positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, each first-metal structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline, each of the first-metal structures having at least one adjacent first-metal structure positioned next to each of its sides at a y-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of the first-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers;

at least six contact structures formed within the region of the semiconductor chip, the at least six contact structures formed in part utilizing corresponding at least six contact structure layout shapes as an input to a lithography process, the at least six contact structures formed in physical and electrical contact with corresponding ones of at least six of the gate structures, each of the at least six contact structure layout shapes having a substantially rectangular shape and a corresponding length greater than a corresponding width and with the corresponding

length oriented in the x-direction, each of the at least six contact structure layout shapes positioned and sized to form its corresponding contact structure to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact,

wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type, wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region, wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit.

Ex. 1001, 30:2–31:13.

D. Instituted Grounds of Unpatentability

We instituted *inter partes* review of claims 1–11, 15, 18, 20, and 22–24 of the '335 patent on the following ground:

Reference(s)/Basis	Claims Challenged	35 U.S.C. §
Becker, ¹ Greenway ²	1–11, 15, 18, 20, 22–24	§ 103

¹ US 7,446,352 B2, issued Nov. 4, 2008 (Ex. 1006).

² Greenway, Robert, et al., *Interference Assisted Lithography for Patterning of 1D Gridded Design*, vol. 7271, SPIE, p. 72712U-1 (2009) (Ex. 1013).

Petitioner relies on the declaration testimony of Dr. Stanley Shanfield. Ex. 1002; Ex. 1062. Patent Owner relies on the declaration testimony of Dr. Sunil P. Khatri. Ex. 2074.

II. ANALYSIS

A. *Legal Standards*

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) differences between the prior art and the claims at issue; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness, i.e., secondary considerations.³ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). The totality of the evidence submitted may show that the challenged claims would not have been obvious to one of ordinary skill in the art. *In re Piasecki*, 745 F.2d 1468, 1471–72 (Fed. Cir. 1984).

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Petitioner must demonstrate unpatentability by a preponderance of the evidence. 35 U.S.C. § 316(e) (2018); 37 C.F.R. §

³ Patent Owner does not present any objective evidence of nonobviousness in this case and, therefore, we do not address this *Graham* factor.

42.1(d); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (2012) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art “would have been a person having a Bachelor’s degree in Electrical Engineering, Physics or Materials Science with three to five years of industry experience in semiconductor IC design, layout or fabrication,” but that “[a]dditional education might compensate for less experience, and vice-versa.” Pet. 19–20 (citing Ex. 1002 ¶¶ 63–66).

Patent Owner contends that a person of ordinary skill in the art “would have had: (1) a Bachelor’s degree in Electrical Engineering, with five years of experience in semiconductor layout technology and integrated circuit design; (2) a Master’s degree in Electrical Engineering, with three years of experience in the same field; or (3) comparable experience.” PO Resp. 20 (citing Ex. 2074 ¶ 78). Patent Owner also argues that the challenged claims are not obvious under either Petitioner’s or Patent Owner’s definition of the level of ordinary skill in the art. *Id.*

Neither party argues that the outcome of this case would differ based on our adoption of any particular definition of one of ordinary skill in the art. On this record, we find that the differences in the parties’ contentions as to the level of ordinary skill are not consequential, in part because the levels of skill set forth by both Petitioner and Patent Owner are based on a Bachelor’s degree in Electrical Engineering and a length and type of experience that overlap. Accordingly, we adopt Patent Owner’s definition, which overlaps

that set forth by Petitioner, particularly regarding a Bachelor’s degree in Electrical Engineering, with five years of experience in semiconductor layout technology and integrated circuit design, and because it is consistent with the cited prior art. We further note that the prior art itself demonstrates the level of skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that “specific findings on the level of skill in the art . . . [are not required] ‘where the prior art itself reflects an appropriate level and a need for testimony is not shown’” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

C. Claim Construction

We apply the claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. “[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. Only terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner notes that there are disputed claim terms in the NDCA Action—namely, the terms “gate electrode,” “gate structure(s),” and “contact structure(s)” —but asserts that Becker and Greenway render the challenged claims obvious under any of the proposed constructions. Pet. 31–32. In light of this, Petitioner states that the Board does not need to construe any claim term in order to evaluate the asserted prior art. *Id.*

Patent Owner provides the district court’s construction of the claim terms “gate electrode,” “gate structure(s),” and “contact structure(s)” in the NDCA Action, stating that Patent Owner “applies the District Court constructions” of these claim terms. PO Resp. 21–22. Patent Owner, however, does not expressly argue for those constructions, and states that “Petitioner’s obviousness arguments fail regardless of whether any of the above claims constructions are adopted by the Board.” *Id.* at 22.

On the full record now before us, we determine it is not necessary to construe any claim term expressly to resolve the parties’ dispute. *Vivid Techs.*, 200 F.3d at 803; *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in an *inter partes* review).

D. Asserted Prior Art

1. Becker

Becker is a patent titled “Dynamic Array Architecture,” issued on November 4, 2008. Ex. 1006, codes (54), (45). Like the ’335 patent, Becker claims priority to Provisional Application No. 60/781,288, which was filed Mar. 9, 2006. Pet. 33; Ex. 1006, code (60); Ex. 1001, code (60).⁴ Unlike the ’335 patent, Becker does not include what Petitioner characterizes as “new matter” added to the 2015 Application. Pet. 19, 33; Ex. 1008, 21–24, 68–71. Petitioner states that, other “than the claimed dimensions, Becker discloses the very same 1D gridded regular layout and 1D structures found

⁴ Patent Owner does not challenge Becker’s status as prior art, notwithstanding Patent Owner’s arguments about the priority date of the ’335 patent.

in the '335 Patent.” Pet. 33. Becker also has the same inventive entity as the '335 patent. Ex. 1006, code (75); Ex. 1001, code (72).

Becker is directed to “a dynamic array architecture . . . to address semiconductor manufacturing process variability associated with a continually increasing lithographic gap.” Ex. 1006, 4:11–14.

Figure 5 of Becker, shown below, illustrates an exemplary layout of a dynamic array.

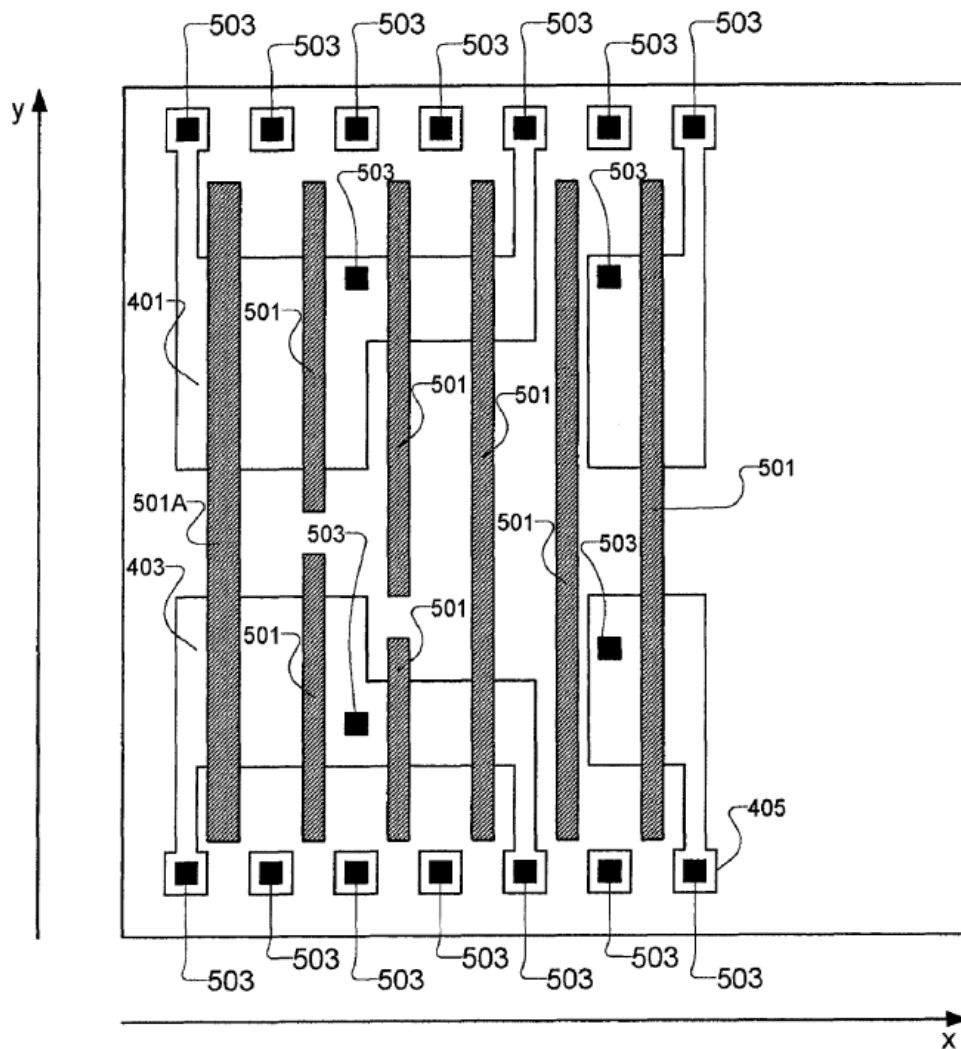


Fig. 5

The dynamic array of Figure 5 includes a gate electrode layer, a diffusion contact layer, and a diffusion layer. *Id.* at 10:55–57, 11:13–16. The diffusion layer shows p-diffusion region 401 and n-diffusion region 403. *Id.* at 10:57–58. The gate electrode layer shows gate electrode features 501 that define the transistor gates. *Id.* at 11:16–18.

Figure 8B of Becker, shown below, illustrates an exemplary layout of a dynamic array.

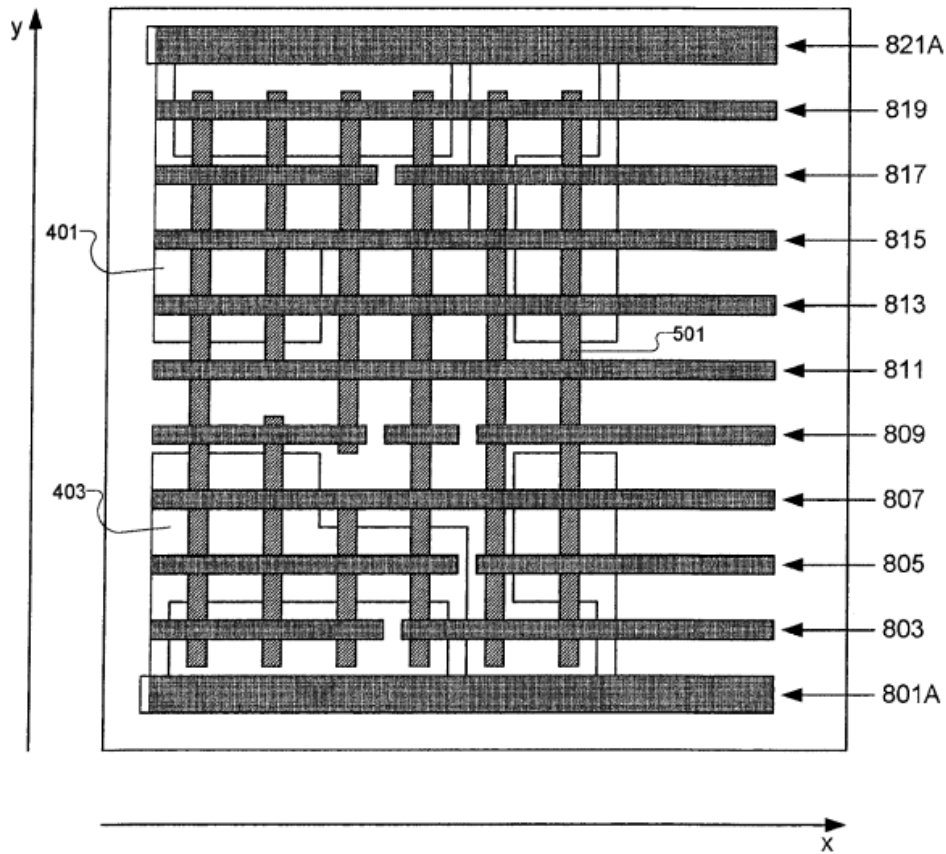


Fig. 8B

Figure 8B depicts a metal 1 layer of Figure 8A (not shown) with larger track widths for the metal 1 ground and power tracks. *Id.* at 3:30–32. Becker states that Figure 8A illustrates a metal 1 layer defined above the gate

electrode contact layer of Figure 6, which in turn depicts a gate electrode contact layer above and adjacent to the gate electrode layer of Figure 5. *Id.* at 12:38–40, 13:29–31. The metal 1 layer of Figure 8B includes a number of metal 1 tracks 801–821 defined to include linear shaped features extending in a parallel relationship across the dynamic array. *Id.* at 13:31–34. Becker discloses that the widths of metal 1 tracks 801 and 821 are the same as the other metal 1 tracks 803–819 in the embodiment of Figure 8A, but in the embodiment of Figure 8B, the widths of metal 1 tracks 801 and 821 are larger than the widths of metal 1 tracks 803–819. *Id.* at 14:1–7.

2. *Greenway*

Greenway is a publication titled “Interference Assisted Lithography for Patterning of 1D Gridded Design.” Ex. 1013, 1. Greenway discloses technical issues with Extreme Ultra Violet Lithography (EUVL), high-index immersion 193nm lithography, double patterning, and nano-imprinting, and that “[n]o satisfactory cost-effective solutions exist for the patterning of 32nm half pitch features and beyond.” *Id.* In view of this, Greenway states that Interference Assisted Lithography (IAL) can be a promising cost-effective lithography solution. *Id.* Greenway further discloses that, because IAL does not need large, expensive lenses, IAL can be adopted for an interference lithography tool and is enabled to extend beyond the pitch limit of current Optical Projection Lithography (OPL). *Id.*

Greenway states that IAL implementation requires converting 2D random layouts to highly regular 1D gridded designs. *Id.* at 2. According to Greenway, 1D “gridded design rules” (GDR) “refer to a layout style in which critical layers are drawn with 1D lines on a coarse grid.” *Id.* Figure 1 of Greenway is shown below:

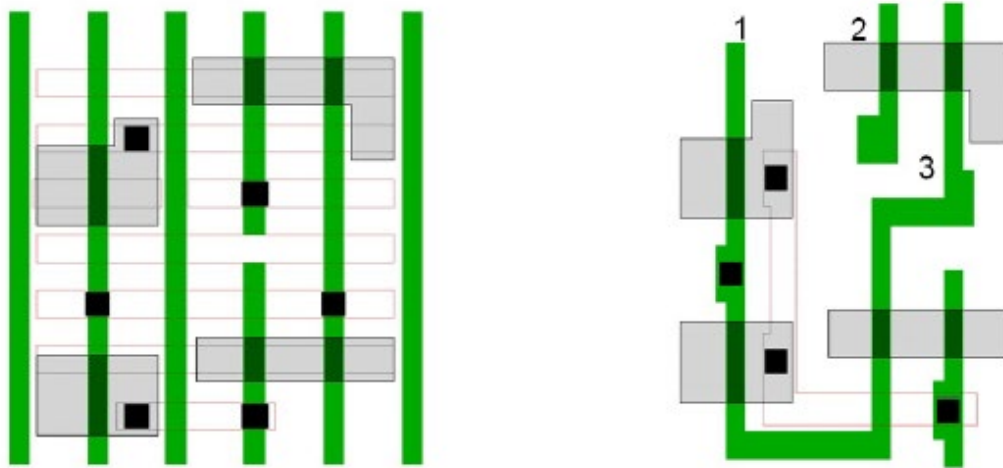


Figure 1. 1D GDR layout (left side) compared to 2D CDR layout (right side).

Figure 1 of Greenway depicts a 1D GDR layout (left side) and a 2D “complex design rules” (CDR) layout (right side). *Id.* at 3. Greenway states that the left side of Figure 1 shows vertical gate lines with a uniform pitch with dummy lines, as needed. *Id.* at 2. Horizontal first metal lines also have a uniform pitch with circuit line segments separated by uniform gaps with diffusion and gate contacts located at intersections of grid lines. *Id.*

Greenway further discloses the design of a 6T SRAM bitcell using 1D regular-pitch gridded design rules. *Id.* at 3. Figure 4 of Greenway is shown below:

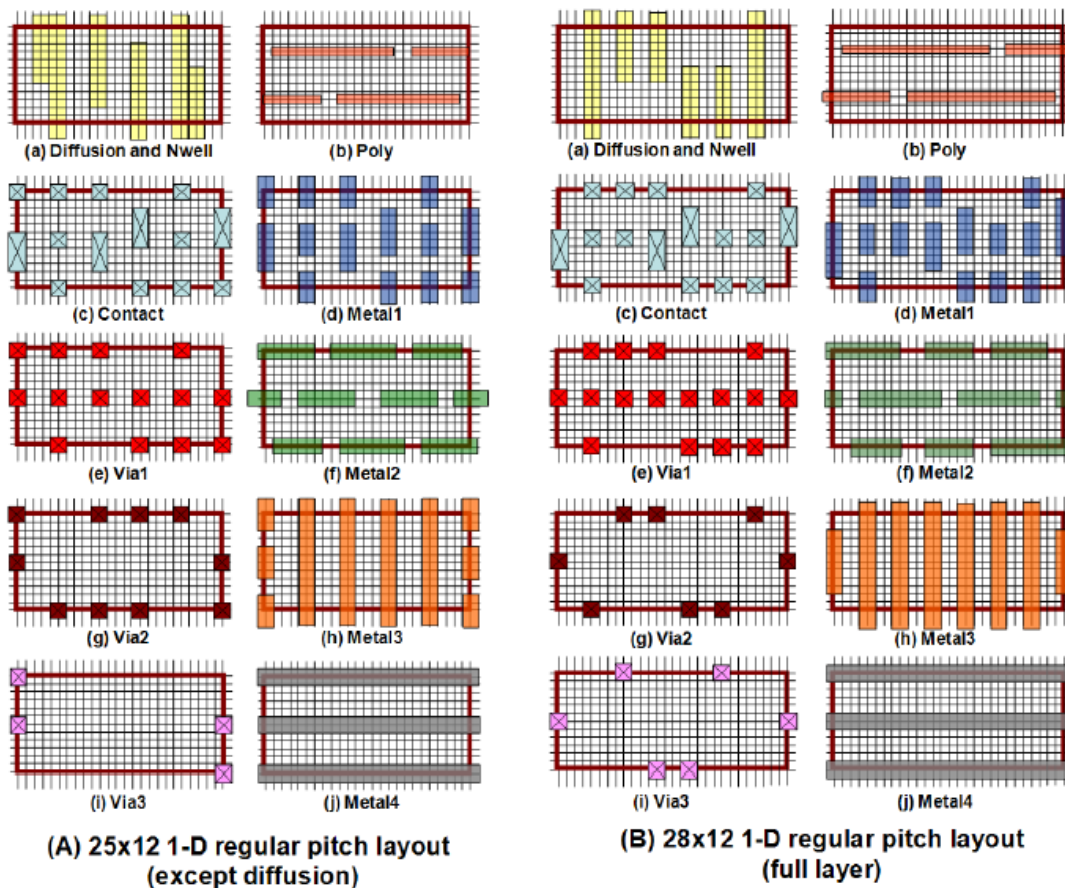


Figure 4. Candidate bitcell layouts.

Figure 4 of Greenway illustrates candidate bitcell layouts. *Id.* at 5. Greenway discloses that Figure 4(A) illustrates one candidate for 1D regular pitch layout in which IAL was not applied to the diffusion layer, but has a smaller size. *Id.* at 4. Figure 4(B) depicts another candidate for a full layer 1-D regular pitch layout in which the diffusion layer is also IAL-compatible. *Id.* Greenway states “[i]n the present study, we consider 6 grids per poly pitch with 22nm per grid.” *Id.*

E. Analysis of Priority Claim

On its face, the ’335 patent claims priority to a number of applications, including U.S. Provisional Patent Application No. 60/781,288,

filed Mar. 9, 2006 (Ex. 1005, “the 2006 Provisional Application”), U.S. Application Ser. No. 11/683,402, filed Mar. 7, 2007 (Ex. 1007, “the 2007 Original Application”), and U.S. Application Ser. No. 14/711,731, filed May 13, 2015 (Ex. 1008, “the 2015 Application”). Ex. 1001, codes (60), (63).

Petitioner challenges the ’335 patent’s claim of priority to the 2006 Provisional Application, arguing that the ’335 patent’s priority date can be no earlier than 2015. Pet. 15–19, 20–31; Reply 4–13. Patent Owner argues that the ’335 patent is entitled to its claimed priority date of March 9, 2006, and, therefore, Becker and Greenway are not prior art. PO Resp. 27–60; Sur-Reply 4–13.

1. Parties’ Arguments Regarding the ’335 Patent Itself and “Scalability”

As Patent Owner notes, 35 U.S.C. § 112 ¶ 1 (pre-AIA) stands for the proposition that a patent specification “shall contain a written description of the invention, and of the manner and process of making and using it” and must “contain a written description of the invention . . . to enable any person skilled in the art . . . to make and use the same.” PO Resp. 27–28. Also, “the written description requirement may be satisfied by any combination of the words, structures, figures, formulas, etc., contained in the patent application.” *Id.* at 28 (citing *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997)).

“It is elementary patent law that a patent application is entitled to the benefit of the filing date of an earlier filed application only if the disclosure of the earlier application provides support for the claims of the later application, as required by 35 U.S.C. § 112.” *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1306 (Fed. Cir. 2008); *see also Research Corp.*

Techs. v. Microsoft Corp., 627 F.3d 859, 871–72 (Fed. Cir. 2010) (holding the later-filed application, with claims that were not limited to a “blue noise mask,” was not entitled to the priority filing date of the parent application, which was “limited to a blue noise mask”); *ICU Med., Inc. v. Alaris Med. Sys.*, 558 F.3d 1368, 1377–78 (Fed. Cir. 2009) (holding that “spikeless” claims “added years later during prosecution” were not supported by the specification which “describes only medical valves with spikes”); *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158–60 (Fed. Cir. 1998) (holding the generic shaped cup claims of the later-filed child application were not entitled to the filing date of the parent application that “disclosed only a trapezoidal cup and nothing more”). “To satisfy the written description requirement the disclosure of the prior application must ‘convey with reasonable clarity to those skilled in the art that, as of the filing date sought, [the inventor] was in possession of the invention.’” *PowerOasis*, 522 F.3d at 1306 (alteration in original). The sufficiency of written description support is based on “an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). It is well settled that the written description requirement of § 112 requires the disclosure to convey that Patent Owner had possession of the entire range of claimed values. *In re Lukach*, 442 F.2d 967, 969 (CCPA 1971).

Petitioner argues that the inventors were not in possession of semiconductor chips with the claimed dimensions at the time of the 2006 Provisional Application and 2007 Original Application, and that those earlier applications did not enable the full claimed range of dimensions. Pet. 20–31. The claim to priority as a continuation is improper, Petitioner

argues, because “the only gate pitch disclosed in the 2006 Provisional Application and the 2007 Original Application is 0.36 μm , or 360nm, well above the 193nm upper bound of the claimed gate pitch range.” *Id.* at 20 (citing Ex. 1005, 8; Ex. 1007, 30–31; Ex. 1002 ¶ 68). Petitioner argues that new matter added to the 2015 Application “described for the first time a semiconductor chip that contains structures spaced apart with a ‘first pitch that is less than or equal to about 193 nanometers’ and having a width that is ‘less than 45 nanometers.’” *Id.* at 20–21 (citing Ex. 1008, 21–23, 68–71; Ex. 1002 ¶ 69). Petitioner also argues that Patent Owner, by accusing Petitioner of infringing the challenged claims with Petitioner’s 10nm processors with a 36nm minimum metal pitch, admits that any lower bound of the “less than or equal to” 193nm range in the claims would be well below 36nm and in the single-digit nanometer range. *Id.* at 24–25 (citing Ex. 1025, 14 (Dr. Khatri testifying that the “expected lower bound is somewhere in the single digit nanometer range.”)). According to Petitioner, the inventors at the time of the 2006 Provisional Application and the 2007 Original Application did not have possession of the claimed subject matter down to the single-digit nanometer range or even as low as 36 nm, nor did those applications teach one of ordinary skill in the art how to achieve those dimensions. *Id.* at 26. In sum, Petitioner argues that the challenged claims are not entitled to the priority date of the 2006 Provisional Application (March 9, 2006) or of the 2007 Original Application (March 7, 2007). Instead, Petitioner argues that the earliest possible priority date for the challenged claims is May 13, 2015, the date the new matter was added to the application that ultimately led to the issuance of the ’335 patent. *Id.* at 30 (citing Ex. 1002 ¶¶ 41–42, 89).

Patent Owner argues that the 2006 Provisional Application provides written description support for the disputed claimed limitations “each of the gate structures having a width of less than or equal to about 45 nanometers” (Ex. 1001, 30:17–18) (“Claim Element A”) and “adjacently positioned ones of the gate structures are separated from each other by a gate pitch of less than or equal to about 193 nanometers” (Ex. 1001, 30:14–17) (“Claim Element B”). PO Resp. 32.

Regarding Claim Element A, Patent Owner argues that the ’335 patent and the 2006 Provisional Application teach a “scalable layout” technique, and, therefore, “the end-product, *i.e.*, the semiconductor chip formed, would be scalable in the same manner.” *Id.* at 33–34. Thus, Claim Element A is supported by the 2006 Provisional Application, argues Patent Owner, because the “predictability of the layout designs claimed in the ’335 Patent” is “sufficient to demonstrate that the inventors possessed minimum feature sizes of less than or equal to about 45nm” that would enable one of ordinary skill in the art “to practice the invention as of the time of filing of the” 2006 Provisional Application. *Id.* at 34. Patent Owner also argues that the 2006 Provisional Application itself “includes a description of 90nm, 65nm, and 45nm process technology.” *Id.* at 36. The feature sizes would be “scaled by a factor of 0.707 in the x-direction and by a factor of 0.707 in the y-direction,” which, after two scalings, Patent Owner argues, would result in the 90nm process technology being scaled down to 45nm process technology. *Id.* at 39–40. Relying on the language of the 2006 Provisional Application that states: “Today minimum feature sizes are approaching 45 nm (nanometers) while the wavelength of the light source used in the photolithography process remains at 193nm,” and “Many believe that

extreme ultra violet (EUV) will not be economically feasible and that the lithographic gap will continue below 45nm,” Patent Owner argues that the specification of the 2006 Provisional Application “expressly discloses features sizes down to 45 nm” and “further scaling of the minimum feature sizes below 45 nm.” *Id.* at 41–42. Patent Owner also points to language in the ’335 patent discussing “dynamic array architecture” generally, which provides: “However, current feature sizes are as small as 65 nm and are expected to soon approach sizes as small as 45 nm.” *Id.* at 42 (citing Ex. 1001, 8:62–9:6).

Regarding Claim Element B, Patent Owner argues that the 2006 Provisional Application provides a written description of an as-fabricated gate pitch of less than or equal to about 193 nm. *Id.* at 43. Patent Owner challenges Petitioner’s position that the only gate pitch disclosed in the 2006 Provisional Application is 360 nm, but does not dispute that a 360 nm gate pitch is expressly disclosed in the 2006 Provisional Application. *Id.* at 44–45. Patent Owner argues that the 2006 Provisional Application expressly discusses scaling down to 45nm technology, relying on the language in the 2006 Provisional Application that provides: “The push for higher performance and smaller die size drives the semiconductor industry to reduce area by approximately 50% every two years. The area reduction provides an economic benefit for migrating to newer technologies. The area reduction is achieved by reducing the feature sizes between 25 and 30 percent.” *Id.* at 46 (citing Ex. 1005, 2; Ex. 2074 ¶¶ 158–159).

Patent Owner also argues that the 2006 Provisional Application expressly provides “support and literal teachings for how to scale down from the 90nm process technology to the 45nm process technology.” PO

Resp. 52–53. Particularly, Patent Owner argues that the Bessel functions detailed and described in the 2006 Provisional Application, particularly in Figures 2 and 3, and in Figure 1 of the '335 patent, demonstrate a lithography process to pattern rectangular gate structures at a gate pitch of 193nm and below. *Id.* at 53–57.

Petitioner replies that Dr. Khatri's scalability argument is "unsupported and discredited." Reply 4. More particularly, Petitioner argues that Patent Owner's argument "hinges on Dr. Khatri's bald assertion that the 2006 Provisional Application 'teaches a [scaling] formula based on simple geometry,' whereby the dimensions of future generation chips are obtained by repeatedly applying a 0.707 shrinking factor." *Id.* at 5. However, Petitioner argues, this application of Moore's Law⁵ is not "infallible" and "has slowed down" in recent times. *Id.* at 5–6 (citing Ex. 1061, 339:21–341:1). Petitioner argues that using Moore's Law to "predict future reductions in chip dimensions is not the same as inventing a chip with reduced chip dimensions, including reduced gate pitches down to unfathomable single-digit nanometer pitches—but that is what the challenged claims of the '335 Patent impermissibly claim." *Id.* at 6. Petitioner argues that the ITC Initial Determination (Ex. 2096, the "ITC Initial Determination") involving related U.S. Patent No. 10,141,334 B2

⁵ Petitioner defines Moore's Law as "the observation that the semiconductor industry has historically strived to reduce chip area by approximately 50% every two years." Pet. 18 n.11 (citing Ex. 1002 ¶ 58 n.6; Ex. 1005, 4 ("The push for higher performance and smaller die size drives the semiconductor industry to reduce area by approximately 50% every two years.")).

(“the ’334 patent”) supports its argument that Patent Owner’s scalability approach is untenable. *Id.* at 7.

Patent Owner responds that the challenged claims “are scalable with the scaling approach and technology that is disclosed in the” 2006 Provisional Application. Sur-Reply 4 (citing Ex. 2074 ¶ 133). Patent Owner again relies on the “predictability of the layout designs claimed in the ’335 Patent” and the asserted understanding of one of ordinary skill in the art that the 2006 Provisional Application “inventors possessed minimum feature sizes of less than or equal to about 45nm.” *Id.* at 5 (citing Ex. 2074 ¶ 135).

2. *Analysis of ’335 Patent Itself and Scalability*

Patent Owner’s argument that the inventors had possession of the claimed 193nm gate pitch ranges and 45nm feature sizes, or anything smaller, at the time of the 2006 Provisional Application or the 2007 Original Application is unavailing.

Looking first at the express disclosures in the 2006 Provisional Application and 2007 Original Application, Patent Owner does not disagree that the smallest gate pitch mentioned therein is 360nm (0.36 μ m). Ex. 1005, 8, 9 11; Ex. 1007, 30–31; Pet. 20; PO Resp. *passim*. Petitioner has reasonably established that the claimed range of less than or equal to about 193nm would extend, at its lower bound, to the single-digit nanometer range. Reply 4–5 (citing Ex. 1061, 329:10–21). The disclosures relied on by Patent Owner in the 2006 Provisional Application and the 2007 Original Application do not support the entire range of gate pitches from 193nm down to the lower bound of the single-digit nanometer range. Pet. 15, 19; *compare* Ex. 1005, 8, 11 (teaching a gate pitch of 360nm), Ex. 1007, 30–31

(teaching a gate pitch of 360nm) *with* Ex. 1008, 21–24 (requiring a gate pitch of less than or equal to about 193nm). This does not show possession of the entire range down to the single-digit nanometer range. *See Lukach*, 442 F.2d at 969. Regarding feature size, the smallest actual feature size mentioned in the 2006 Provisional Application and 2007 Original Application is 65nm. Ex. 1005, 5 (“65nm sized features”); Ex. 1007, 10 (“65 nm sized features”). Figure 1 of the 2006 Provisional Application, titled “Lithography Trends,” emphasizes that Patent Owner did not have possession of smaller gate pitches or feature sizes at the time of that application, but rather, that a 45nm feature size would be expected to be achieved in about 2012. Ex. 1005, Fig. 1; *see Lukach*, 442 F.2d at 969. We find that the disclosures of the 2006 Provisional Application and the 2007 Original Application do not show possession of the 45nm feature size.

Looking next at Patent Owner’s “scalability” theory, we do not agree that the 2006 Provisional Application or 2007 Original Application would inform one of ordinary skill in the art that Patent Owner had possession of the claimed 193nm gate pitch ranges or 45nm feature sizes, or anything smaller, at the time of the 2006 Provisional Application or the 2007 Original Application. In order for Patent Owner to prevail on its argument that the 2006 Provisional Application and the 2007 Original Application support the disclosure of a sub-193nm gate pitch range or 45nm features, the disclosures of those applications must convey with reasonable clarity to one skilled in the art that the inventors possessed the invention claimed in the 2015 Application. *See Ariad Pharms.*, 598 F.3d at 1351. We do not agree that the aspirational language in the 2006 Provisional Application demonstrates that the inventors had possession of the claimed range of gate pitches from

193nm down to the single-digit nanometer range, or possession of 45nm-sized features. Rather, the language of the 2006 Provisional Application describes a layout methodology, but fails to expressly teach scaling down to the gate pitches specified in the 2015 Application or explain to one of ordinary skill in the art how to do so. Even though “scaling” is a mathematical possibility, as argued by Patent Owner, that possibility does not equate to possession of the scaled-down structure itself. At the time of the 2006 Provisional Application and the 2007 Original Application, feature sizes were only “approaching” 45nm (Ex. 1005, 4; Ex. 1007, 3) or “expected to soon approach sizes as small as 45 nm” (Ex. 1007, 10). This language is, in effect, an acknowledgment that 45nm feature sizes were not yet a reality.

Further, nothing in the 2006 Provisional Application shows how to make a 45nm feature, or how one of ordinary skill in the art could have made this happen in the 2006/2007 time frame. Similarly, Dr. Khatri’s scaling formula based on “simple geometry” that Patent Owner proposes to apply to the gate pitches and feature sizes identified in the 2006 Provisional Application is not found in that application. *See generally* Ex. 1005. The application’s use of “Moore’s Law as a crystal ball to predict future reductions in chip dimensions is not the same as inventing a chip with reduced chip dimensions, including reduced gate pitches down to unfathomable single-digit nanometer pitches.” Reply 6. The evidence demonstrates that scaling down feature sizes and gate pitches is not a simple function of time or a mere application of Moore’s Law, but the result of technological innovation that was not in the possession of the inventors at the time of the 2006 Provisional Application or 2007 Original Application. *See* Ex. 1061, 341:2–9; Ex. 1077, 1283:21–1284:3 (ITC hearing transcript).

Thus, we do not agree that, by virtue of Patent Owner's proposed "scalability" theory, the inventors conveyed with reasonable clarity to one skilled in the art that the inventors possessed the invention claimed in the 2015 Application at the time of the 2006 Provisional Application or 2007 Original Application.

3. *Prosecution History*

Petitioner argues that the prosecution history supports its arguments that the '335 patent cannot claim priority to the 2006 Provisional Application. Pet. 15–19. More particularly, Petitioner points to the Examiner's finding that the '335 patent's "allowed claims are not entitled to the claimed March 9, 2006 priority date" of the 2006 Provisional Application. *Id.* at 16 (citing Ex. 1004, 425–429 ("Corrected Notice of Allowability")). The Examiner found that "the claim to priority as a continuation [is] improper" because, for example, claim 1 of the '335 Patent recites a gate pitch "of less than or equal to about 193 nanometers" and a gate width "of less than or equal to about 45 nanometers" that "would have been new matter in application 14/711,731 [the 2015 Application]." *Id.* (quoting Ex. 1004, 427–428). Petitioner takes issue with a declaration submitted to the Office after the issuance of the Corrected Notice of Allowability. *Id.* at 17 (citing Ex. 1004, 434–451 (the "Khatri Declaration")). The Khatri Declaration, according to Petitioner, was "belatedly and improperly submitted" and would not have been reviewed by the Examiner. *Id.* In the Khatri Declaration, Dr. Khatri opined that "the disclosure of a single 360nm gate pitch and recitation of Moore's Law in the 2006 Provisional Application and the 2007 Original Application, without more, provide written description support for a reduced gate pitch of 180nm,

just under the claimed pitch ceiling of 193nm.” *Id.* at 18 (citing Ex. 1004, 450–451, ¶¶ 33.f, 33.i). Petitioner also notes that the Examiner rejected the 2006 priority date claim in other, related applications that also claimed the same “unsupported dimensions,” notwithstanding a similar declaration submitted by Dr. Khatri and considered by the Examiner in support of a similar priority date claim. *Id.* at 21–22 (citing Ex. 1026, the file history for related U.S. Application Ser. No. 15/457,920 (“the ’920 application”)). Thus, Petitioner argues, the 2015 Application “described and claimed for the first time a semiconductor chip with a gate pitch less than or equal to 193nm and a gate width less than 45nm,” thereby adding new matter to the 2015 Application that did not previously appear in the chain of priority applications. *Id.* at 19 (citing Ex. 1008, 21–24 (new paragraph of the 2015 Application); 68–71 (claim 1 of the 2015 Application)).

Patent Owner addresses the Examiner’s “apparent rejection” of the declaration submitted in the ’920 application, in which the Examiner concluded that the claimed “gate pitch of less than or equal to about 193 nanometers” in the ’920 application “does not have sufficient support and would be [] new matter.” PO Resp. 49 (citing Ex. 1026, 529; Ex. 2074 ¶ 164). Patent Owner argues that this position is flawed because it ignores that the gate pitch would likewise be reduced when scaling down the feature size. *Id.*; *see also* Sur-Reply 11–12. Thus, based on the predictable nature of the scaling, Patent Owner argues that the inventors “had possession of a semiconductor chip with a gate pitch of less than 193 nm as recited in the Challenged Claims in March 2006.” PO Resp. 52.

Petitioner replies that the Board should not disturb the Examiner’s finding that the ranges in the ’335 patent claims are not supported by

the 2006 Provisional Application or the 2007 Original Application. Reply 8 (citing Dec. 31–32). Petitioner further points out that in a Request for Continued Examination of the '920 application, the Examiner again found that claims having a gate pitch less than or equal to 193 nm were unsupported by the 2006 Provisional Application, rejecting Dr. Khatri's scalable layout theory. *Id.* at 8–9 (citing Pet. 21–22; Ex. 1076, 3–5, 6–7, 26–27 (asserting the same scalability argument and specifically drawing the Examiner's attention to the similar Khatri declaration)).

For largely the same reasons given above in our analysis of Patent Owner's scalability theory, we are persuaded by Petitioner that the Examiner's finding should stand. The prosecution history of the '335 patent, particularly the statement by the Examiner that the '335 patent is not entitled to the filing dates of the 2006 Provisional Application or the 2007 Original Application, is consistent with our conclusions regarding the scalability theory argued here and presented in the Khatri Declaration. Ex. 1004, 425–429. We do not agree that the Khatri Declaration was not improperly filed “as an ‘Amendment after Notice of Allowance (Rule 312).’” Pet. 17 & n.10 (citing Ex. 1004, 436). We consider it relevant that the Khatri Declaration was submitted following the Examiner's Corrected Notice of Allowability and there is no indication that it was considered by the Examiner. Ex. 1004, 425–429. That the Examiner's did not address the Khatri Declaration arguments in the prosecution of the '335 patent does not change our view of the Examiner's position regarding the priority date. We also note that Patent Owner did not, at that time, appear to have reopened or attempted to reopen prosecution to address the Examiner's earlier assertion. Dr. Khatri's subsequent testimony regarding the opinions in the Khatri Declaration, or his

testimony in related applications, is not, as we discuss above, sufficient to rebut Petitioner's positions, or the Examiner's conclusion. We see no reason, on this complete record, to disturb the Examiner's finding that the ranges in the '335 patent claims are not supported by the 2006 Provisional Application or the 2007 Original Application.

4. *Metal Pitch Range and Gate Width/Gate Pitch*

Petitioner argues that, in its Petition, it asserted that the claimed sub-193nm first-metal spacing also was not supported by the 2006 Provisional Application or the 2007 Original Application (citing Pet. 22–30), and that Patent Owner's failure to address first-metal pitch range, which differs from gate pitch range, is fatal to Patent Owner's case. Reply 10–11. Petitioner also argues that Patent Owner's attempts to conflate gate width with gate pitch are misleading. *Id.* at 11. Even so, Petitioner argues, the gate width described in the research papers Patent Owner relies on do not mention a pitch dimension below a limit of 50nm, and “make clear that the ability to achieve pitches below 64nm was uncertain at best.” *Id.* at 11–12.

Patent Owner responds that Dr. Khatri addressed metal pitch ranges, because the “general scaling approach discussed by Dr. Khatri would necessarily involve the metal pitches.” Sur-Reply 9 (citing Ex. 2074 ¶ 134 (Dr. Khatri testifying that because “the disclosed layout technique is scalable, the end-product, *i.e.* the semiconductor chip formed, would be scalable in the same manner”)). Patent Owner further responds that the “scaling of feature sizes is directly related to the pitches for both the gate and metal layers.” *Id.* at 6.

With little argument in the record before us regarding first-metal pitch range apart from the arguments in the Petition, we discern no persuasive

rebuttal to Petitioner's argument that the 2006 Provisional Application and the 2007 Original Application fail to disclose a first-metal spacing (or second-metal or third-metal spacing) of less than or equal to 193nm as claimed in the '335 patent. *See* Pet. 22–31, 54–55, 63–64, 76–77 (discussing, *inter alia*, metal spacings in claims 1, 2, and 10). We do not credit Patent Owner's argument that its scalability theory would apply generally to both gate pitches and metal layer spacings, because "lithography issues involved in achieving a reduced metal pitch differ significantly from those in play when attempting to reduce a semiconductor chip's gate pitch." Reply 10–11 (citing Ex. 1062 ¶¶ 27–31). Moreover, as discussed above, we do not agree that the scalability theory supports Patent Owner's argument that the inventors possessed the claimed gate pitch and the gate width in 2006/2007; if we were to apply the same reasoning to Patent Owner's arguments about metal spacings, we would agree that the scalability theory is inapplicable to metal spacings as well.

5. *Smayling Papers*

Petitioner relies on two papers authored by a co-inventor of the '335 patent, Dr. Smayling. Pet. 26–30. Petitioner argues that Dr. Smayling opined in 2008 that a 64 nm pitch was well beyond practical limits. *Id.* at 27 (citing Ex. 1015, 2). In 2009, Dr. Smayling opined that no satisfactory cost-effective solutions existed at the time for the patterning of 64 nm pitch features and beyond. *Id.* at 28–29 (citing Ex. 1013, 1).

Patent Owner disagrees that these papers authored by Dr. Smayling "admitted that he did not have possession of a semiconductor chip in accordance with the Challenged Claims in 2006." PO Resp. 57. Rather, Patent Owner argues that one paper "does not implicitly or explicitly support

an assertion that the inventors of the '335 Patent did not possess the invention recited in the Challenged Claims in 2006.” *Id.* at 58 (citing Ex. 1015, 1–2; Ex. 2074 ¶ 182). Patent Owner argues that the other paper relates to mass production and does not provide any admissions that the inventors did not possess the invention of the '335 patent. *Id.* at 59 (citing Ex. 1013; Ex. 2074 ¶ 183).

Petitioner replies that Patent Owner mischaracterizes the Smayling papers. Reply 12. More particularly, Petitioner states that the papers “made clear that those small-pitch dimensions [in the single-digit nanometer range] were well beyond the practical limits of then-available technologies.” *Id.* at 12–13 (citing Ex. 1015, 2). Petitioner asserts that the Rayleigh equation that forms the basis of Dr. Smayling’s papers is not specific to production issues, but applies equally whether the lithography equipment is used for manufacturing, research, or otherwise. *Id.* at 13 (citing Ex. 1062 ¶¶ 42–43).

Although we do not find Dr. Smayling’s papers dispositive on any of the issues, they shed light on the perspective of a co-inventor at the time of the invention. The statement that “‘metal-1 half pitch of approximately 32nm [*i.e.*, 64nm pitch]’ was well-beyond ‘practical limits’ . . . even if ‘1D patterns’ were used” indicates that Dr. Smayling believed a 64nm pitch to be out of reach as of 2008. *Id.* (citing Ex. 1015, 2). The range Patent Owner claims was fully within the possession of the inventors in 2006 was, therefore, well beyond practical limits in 2008, as stated by an inventor himself. We give some weight to Dr. Smayling’s opinions, but rely primarily on Petitioner’s arguments regarding the disclosures in the specification to reach our conclusions.

6. *ITC Initial Determination*

As noted by Petitioner, in the ITC Initial Determination,⁶ the ITC judge also rejected Patent Owner’s scalable layout argument, holding that the ’334 patent at issue in that proceeding is only entitled to a priority date no earlier than May 13, 2015. Reply 2 (citing Ex. 2096, 104–106, 108), 7 (citing Ex. 2096, 108). The ITC Initial Determination found that, although the industry recently (in 2019) produced chips with pitches smaller than 193 nanometers, that “does not mean that the inventors had possession of such small [] pitches in 2006, or believed that those [] pitches were a part of the invention.” *Id.* at 7 (quoting Ex. 2096, 105). In sum, the ITC Initial Determination stated, “the evidence demonstrates clearly and convincingly that the 334 patent’s disclosure does not convey to those skilled in the art, either explicitly or inherently, that the inventors had possession of the entire subject matter of claim 1 as of March 9, 2006” and “the claims at issue [] are only entitled to a priority date of May 13, 2015, the date the new matter was added to the 731 Application.” *Id.* (citing Ex. 2096, 108).

Patent Owner addresses the ITC Initial Determination, but does not focus on the substance of the ITC’s priority date findings, focusing instead on the ITC’s obviousness findings, which we address below. *See* Sur-Reply 13–15.

We find the ITC Initial Determination on the issue of priority date, although not binding, to be consistent with our conclusion, and useful in helping us reach our own determination here.

⁶ The evidence of record does not include any subsequent determinations or papers from the ITC Proceeding.

7. *Conclusion Regarding Priority Date*

On this complete record, we are persuaded that Petitioner has demonstrated that the '335 patent is not entitled to the priority date of the 2006 Provisional Application or the 2007 Original Application, but rather, that the claims at issue are entitled to a priority date of no earlier than the date of the 2015 Application. We now turn to the obviousness arguments based on Becker and Greenway as prior art references.

F. Analysis of Claim-Related Arguments

Petitioner argues that claims 1–11, 15, 18, 20, and 22–24 are unpatentable under 35 U.S.C. § 103(a) over Becker in view of Greenway. Pet. 40–90.

With respect to claim 1, Petitioner argues that Becker and Greenway disclose:

Preamble:⁷ “A semiconductor chip, comprising:” (Pet. 41 (relying on Ex. 1006; Ex. 1013; Ex. 1002 ¶ 108));

Element 1.1a: “gate structures formed within a region of the semiconductor chip, the gate structures formed in part based on corresponding gate structure layout shapes used as an input to a lithography process, the gate structure layout shapes positioned in accordance with a gate horizontal grid, the gate horizontal grid including at least seven gate gridlines,” (Pet. 41–45 (relying on Ex. 1006, Figs. 3C, 3D, 5, 6, 7B, 14, Ex. 1002 ¶¶ 109–112));

⁷ Regardless of whether the preamble is limiting, Petitioner has shown that the recited “semiconductor chip” is disclosed by the prior art.

Element 1.1b: “each gate structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline,” (Pet. 45–46 (relying on Ex. 1006, Fig. 5; Ex. 1013, Fig. 4(A)(b); Ex. 1002 ¶ 113));

Element 1.1c: “each gate gridline having at least one gate structure layout shape positioned thereon,” (Pet. 46 (relying on Ex. 1006; Ex. 1002 ¶ 114));

Element 1.1d: “wherein adjacently positioned ones of the gate structures are separated from each other by a gate pitch of less than or equal to about 193 nanometers,” (Pet. 46–47 (relying on Ex. 1006; Ex. 1013, Fig. 4(A)(b); Ex. 1002 ¶¶ 115–116));

Element 1.1e: “each of the gate structures having a width of less than or equal to about 45 nanometers,” (Pet. 47–48 (relying on Ex. 1006; Ex. 1013, Fig. 4(A)(b); Ex. 1002 ¶¶ 117–118));

Element 1.1f: “wherein each pair of the gate structures that are positioned in and [sic] end-to-end manner are separated from each other by a line end-to-line end gap of less than or equal to about 193 nanometers,” Pet. 48 (relying on Ex. 1006, Fig. 5; Ex. 1013, Fig. 4(A)(b); Ex. 1002 ¶ 119));

Element 1.2a: “a first-metal layer formed above top surfaces of the gate structures within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate structures,” (Pet. 49–50 (relying on Ex. 1006, Figs. 2, 8B; Ex. 1002 ¶¶ 120–121));

Element 1.2b: “the first-metal layer separated from the top surfaces of the gate structures by at least one insulator material, adjacent metal layers in the stack of metal layers separated by at least one insulator material,” (Pet. 50 (relying on what one of ordinary skill in the art would have known, citing prosecution history; Ex. 1002 ¶ 122));

Element 1.2c: “wherein the first-metal layer includes first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, the first-metal structure layout shapes positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines,” (Pet. 50–52 (relying on Ex. 1006, Fig. 8B; Ex. 1002 ¶¶ 123–124));

Element 1.2d: “each first-metal structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline,” (Pet. 52–53 (relying on Ex. 1006, Fig. 8B; Ex. 1002 ¶ 125));

Element 1.2e: “each of the first-metal structures having at least one adjacent first-metal structure positioned next to each of its sides at a y-coordinate spacing of less than or equal to 193 nanometers,” (Pet. 53–54 (relying on Ex. 1006, Fig. 8B; Ex. 1013, Fig. 4(B)(d); Ex. 1002 ¶¶ 126–127));

Element 1.2f: “wherein each pair of the first-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers,” (Pet. 54–55 (relying on Ex. 1006, Fig. 8B; Ex. 1013, Fig. 4(B)(d); Ex. 1002 ¶ 128));

Element 1.3a: “at least six contact structures formed within the region of the semiconductor chip, the at least six contact structures formed in part

utilizing corresponding at least six contact structure layout shapes as an input to a lithography process, the at least six contact structures formed in physical and electrical contact with corresponding ones of at least six of the gate structures,” (Pet. 55–57 (relying on Ex. 1006, Figs. 2, 6; Ex. 1002 ¶¶ 129–131));

Element 1.3b: “each of the at least six contact structure layout shapes having a substantially rectangular shape and a corresponding length greater than a corresponding width and with the corresponding length oriented in the x-direction, each of the at least six contact structure layout shapes positioned and sized to form its corresponding contact structure to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact,” (Pet. 57–58 (relying on Ex. 1006, Figs. 6, 7B; Ex. 1002 ¶ 132));

Element 1.4a: “wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type,” (Pet. 58–60 (relying on Ex. 1006, Fig. 5; Ex. 1002 ¶¶ 133–135));

Element 1.4b: “wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region,” (Pet. 60 (relying on Ex. 1006, Fig. 5; Ex. 1002 ¶ 136));

Element 1.4c: “wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit.” (Pet. 60 (relying on Ex. 1006, Fig. 5; Ex. 1002 ¶ 137)).

On this record, we find that Becker and Greenway disclose all of the limitations of claim 1, as set forth above.

Relying on the Shanfield declaration, Petitioner argues that one of ordinary skill in the art would have been motivated to combine the teachings of Becker and Greenway, and would have had a reasonable expectation of success in doing so. Pet. 40–41 (citing Ex. 1002 ¶¶ 104–107). For example, Petitioner argues that Becker and Greenway are closely related, in that they “apply the *same* 1D gridded layout style to the design of semiconductor chips,” with Greenway going further than Becker and disclosing “fabricating 1D gridded circuits using ‘next generation’ Interference Assisted Lithography (IAL).” *Id.* at 40. Petitioner also argues that one of ordinary skill in the art “would have been motivated to combine Greenway with Becker for the additional reason that Greenway’s Interference Assisted Lithography (IAL) seeks to extend the use of 193nm OPL that underpins Becker, and is touted as being compatible with OPL.” *Id.* at 41. According to Petitioner, there would have been a reasonable expectation of success in combining the teachings of Becker and Greenway “because the authors of Greenway performed ‘circuit and lithography simulations’ to confirm that ‘the proposed bitcell layouts can be successfully printed with IAL.’” *Id.* (citing Ex. 1002 ¶¶ 106–107). We also find that Petitioner’s contended basis for one of ordinary skill in the art combining the teachings in the manner set

forth by Petitioner is supported by the evidence of record. *See* Ex. 1002 ¶¶ 103–106.

Patent Owner states that its “Response does not address Dr. Shanfield’s specific arguments on how the combination of Becker and Greenway purportedly teach the limitations of the Challenged Claims.” PO Resp. 31. In a footnote, Patent Owner argues that, because “Petitioner has failed to assert valid prior art,” Patent Owner “will not address the specific arguments on how the combination of Becker and Greenway purportedly teach the limitations of the Challenged Claims.” *Id.* at 31 n.3. In the same footnote, Patent Owner “maintains that Dr. Shanfield fails to establish obviousness, and that a POSITA would have been motivated to combine Becker and Greenway in the manner proposed by Dr. Shanfield.” *Id.* (citing Ex. 2074 ¶ 128).

Petitioner argues that, because Patent Owner and its expert “provide no analysis to support this conclusory, gratuitous statement,” the “disclosures of Becker and Greenway” are undisputed. Reply 3–4; *see also* Tr. 44:14–17 (Petitioner’s counsel stating “Dr. Khatri admits that he hasn’t considered the prior art . . . Becker and Greenway, that he hasn’t considered the claim mapping at all, that he hasn’t considered motivation to combine.”); 86:12–17 (Patent Owner’s counsel stating that it did not present arguments regarding Petitioner’s obviousness position).

In its Sur-Reply, Patent Owner “contests that the combination of Becker and Greenway render obvious the challenged claims,” but neither provides nor points to specific arguments directed to the combination. Sur-Reply 13–14. Rather, Patent Owner excerpts portions of the ITC Initial Determination and argues that “ITC validity findings can be highly

informative” even in the absence of formal *res judicata* based on ITC determinations of validity. *Id.* at 14–15 (citing Ex. 2096, 126; *Texas Instruments, Inc. v. Cypress Semiconductor Corp.*, 90 F.3d 1558, 1569 (Fed. Cir. 1996)).

In making our decision, we are constrained by the record before us, including what arguments are, or are not, presented to us. Even considering the ITC’s Initial Determination,⁸ we are not persuaded that its reasoning or conclusions are based on the same art and arguments as those before us. The ITC Initial Determination focused on the claim 1 limitation that requires a layer of “at least seven gate gridlines,” apparently relying on Figure 5 of Becker in finding that this element “is not found in either Becker or Greenway.” Ex. 2096, 125–126 (citing “RX-0027 at Fig. 5”). Petitioner, however, relies not only on Figure 5 of Becker, as supplemented by a different declarant’s testimony, but also on Figure 14, to disclose the claim 1 limitation of “gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines.” Pet. 41–45 (relying on Ex. 1006, Figs. 5, 6, 7B, 14; Ex. 1002 ¶¶ 109–112)). Petitioner provides ample and supported reasoning that “Becker Figures 5 and 14 illustrate gate

⁸ As noted by parties, the ’335 patent was at issue in, but was later terminated from, the ITC Proceeding. Pet. 3; PO Resp. 3. Therefore, the ITC Initial Determination does not discuss the ’335 patent. Ex. 2096, 2–3 (“As of the date of this initial determination . . . only the 334 patent and the 523 patent remain asserted.”). Because the ’334 patent at issue in the ITC Proceeding “shares the same specification and has claims that recite the exact same claimed ranges as the ’335 Patent” (Reply 2, 7), and because the parties present arguments based on the ITC Initial Determination, we nevertheless address it.

structures . . . that extend in a common vertical direction and are regularly positioned in accordance with a gate horizontal grid,” and that, more particularly, “Figure 14 illustrates seven gate gridlines regularly spaced apart” and in “Figure 5, a dummy gate would be placed on gridline #7 to improve regularity, similar to the dummy gate on gridline #5.” *Id.* at 43 (citing Ex. 1001, 11:35–38; Ex. 1002 ¶¶ 109–110). As further explained by Petitioner during the hearing, “figure 5 has seven gridlines” and “the ITC does not point to the seven dummy gates that we’re talking about in our brief, in our petitions, and the ITC does not discuss figure 14.” Tr. 44:21–24, 45:2–4; *see also* Pet. 41–45; Reply 3–4. Patent Owner, other than pointing generally to the ITC Initial Determination for the related ’334 patent, does not expressly contest Petitioner’s reasoning regarding this claim element. On this complete record, we are persuaded by Petitioner’s largely un rebutted argument and testimony regarding the obviousness ground based on Becker and Greenway, for the reasons given by Petitioner with respect to claim 1.

We have reviewed Petitioner’s arguments and evidence that Becker and Greenway teach or suggest the limitations of independent claim 1 and dependent claims 2–11, 15, 18, 20, and 22–24. Pet. 40–90. As noted, Patent Owner admits that it does not address the specific arguments on how the combination of Becker and Greenway purportedly teaches the limitations of the challenged claims, because it has focused its arguments on the priority of the ’335 patent. PO Resp. 31. We have found, above, that Petitioner’s arguments and evidence sufficiently establish that Becker and Greenway are prior art. Moreover, we also find that Petitioner’s contentions as to the teachings of Becker and Greenway are well supported, as is Petitioner’s

contended basis for one of ordinary skill in the art combining the teachings in the manner set forth by Petitioner. Thus, after reviewing Petitioner's obviousness arguments and supporting evidence, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence the unpatentability of independent claim 1 and dependent claims 2–11, 15, 18, 20, and 22–24.

III. CONCLUSION⁹

For the reasons discussed above, we determine Petitioner has satisfied its burden of establishing, by a preponderance of the evidence, that the challenged claims are unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–11, 15, 18, 20, 22–24	103(a)	Becker, Greenway	1–11, 15, 18, 20, 22–24	
Overall Outcome			1–11, 15, 18, 20, 22–24	

IV. ORDER

In consideration of the foregoing, it is hereby:

⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

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ORDERED that Petitioner establishes, by a preponderance of the evidence, that claims 1–11, 15, 18, 20, and 22–24 of U.S. Patent No. 10,141,335 B2 are unpatentable; and

FURTHER ORDERED that this is a Final Written Decision; therefore, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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