

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

XMTT, INC.,
Patent Owner.

IPR2020-00145
Patent 7,707,388 B2

Before PHILLIP J. KAUFFMAN, MICHELLE N. WORMMEESTER, and
BRENT M. DOUGAL, *Administrative Patent Judges*.

KAUFFMAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Procedure

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 (2019).

Intel Corporation (“Petitioner”) filed a Petition (Paper 2, “Pet.”) to institute an *inter partes* review of claims 1–39 (the “challenged claims”) of U.S. Patent No. 7,707,388 B2 (Ex. 1001, “the ’388 patent”). *See* 35 U.S.C. § 311. XMTT, Inc. (“Patent Owner”) timely filed a Preliminary Response. Paper 8 (“Prelim. Resp.”). We instituted an *inter partes* review of all of the challenged claims and grounds. Paper 11 (“Dec.”).

During trial, Patent Owner filed a Response (Paper 21, “PO Resp.”), Petitioner filed a Reply (Paper 25, “Pet. Reply”), and Patent Owner filed a Sur-Reply (Paper 27, “PO Sur-Reply”).

We held an oral hearing on March 17, 2021. *See* Paper 34 (“Tr.”); *see also* Paper 32 (Petitioner’s Demonstrative Exhibits); Ex. 2025 (Patent Owner’s Demonstrative Exhibits). Due to discussion regarding claim construction, we ordered supplemental briefing. *See, e.g.*, Tr. 5:20–6–25; *see also* Paper 33 (authorization); Paper 35 (“Pet. Supp. Br.”); Paper 36 (“PO Supp. Br.”).

As explained below, the Petition presents argument and evidence based on an incorrect interpretation of the claims. Consequently, the Petition does not identify how the challenged claims are unpatentable, and Petitioner has not shown by a preponderance of the evidence that any of the challenged claims are unpatentable.

B. Related Matters

The parties identify the co-pending district court litigation of *XMTT, Inc. v. Intel Corporation*, No. 1:18-cv-01810 (D. Del.), as a related proceeding. Pet. 60; Paper 5, 2.

We denied institution on the two Petitions challenging U.S. Patent No. 8,145,879 B2, which claims priority to the application from which the '388 patent issued. *See* Pet. 60; Paper 5, 2; IPR2020-00143, Paper 13; IPR2020-00144, Paper 12.

II. THE CLAIMED SUBJECT MATTER

A. The '388 Patent

The '388 patent, "Computer Memory Architecture for Hybrid Serial and Parallel Computing Systems," relates to a computing system configured to switch between serial and parallel processing to allow efficient computation. Ex. 1001, code (54), 1:25–27.

As background, the '388 patent describes that many software applications require both serial and parallel processing and many parallel systems cannot efficiently process serial code. *Id.* at 1:29–35. To address this problem, the '388 patent describes a computing system having both a serial processor and a plurality of parallel processors. *Id.* at 1:58–67. That system is configured for seamless transitions between serial and parallel processing modes while maintaining memory coherence and providing sufficient performance for streaming applications. *Id.*

The '388 patent describes an embodiment of system 100 that switches from a serial processing mode to a parallel processing mode, and vice versa. *Id.* at 5:46–48. System 100 includes: serial processor 14, serial memory 16,

plurality of parallel processors 12, and plurality of partitioned memory modules 10. *Id.* at 4:30–33, Fig. 2. We reproduce Figures 2 and 4 below.

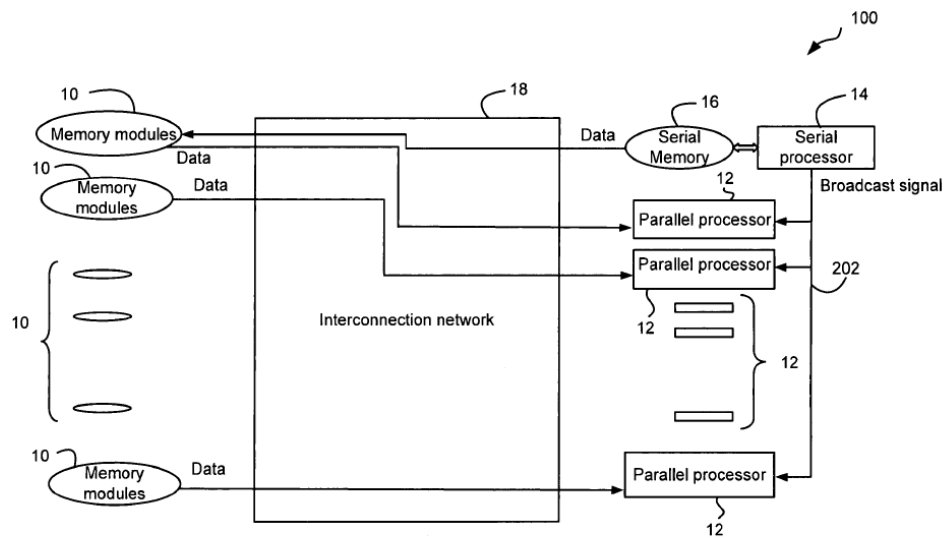


Fig. 2

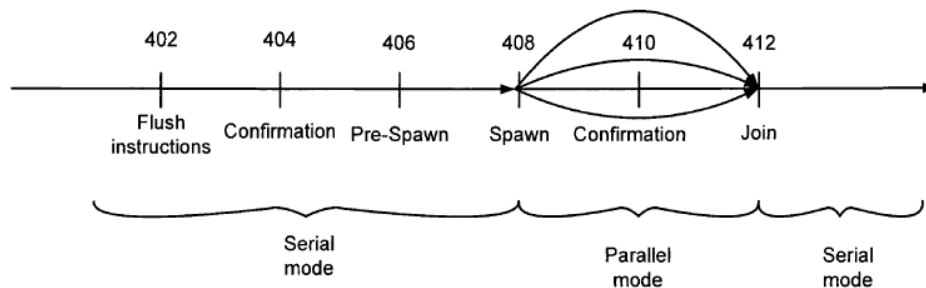


Fig. 4

Figure 2, upper above, is a block diagram that illustrates a computing system embodiment that switches from serial processing mode to parallel processing mode. *Id.* at 3:63–65.

Figure 4, lower above, “is a diagram illustrating an example timeline and transitions between serial and parallel processing modes for a programming model for an example software program.” *Id.* at 4:1–3.

Serial processor 14 of system 100 can process software instructions in serial, and when desired, plurality of parallel processors 12 can process software instructions in parallel. *Id.* at 5:46–52.

In one embodiment, to switch from serial processing mode to parallel processing mode, serial processor 14 commands data flushing (step 402, flush instruction step). *Id.* at 2:12–16; 5:53–56; 9:17–21; Figs. 2, 4. Specifically, serial processor 14 provides for transfer of data from serial memory 16 to at least one of plurality of partitioned parallel memory modules 10 so that parallel processors 12 can access that data. *Id.* at 6:54–58. Next, at least one of plurality of partitioned memory modules 10 acknowledges to serial processor 14 that the data has been queued (step 404). *Id.* at 2:26–33, 9:21–28, Figs. 2, 4. Subsequently, serial processor 14 broadcasts a “prefetching signal” to the parallel processors 12 to start prefetching data from the partitioned memory modules (pre-spawn step 406). *Id.* at 9:29–32; Figs. 2, 4. Serial processor 14 may then broadcast a command to change from serial processing mode to parallel processing mode (spawn step 408). *Id.* at 9:45–49, Fig. 4. After parallel processors 12 each receive acknowledgements confirming their data will be committed to memory modules 10 (step 410), computing system 100 may switch back to serial processing (step 412). *Id.* at 10:19–38, Fig. 4.

The claimed system is capable of a variety of transitions from serial processing mode to parallel processing mode, and vice versa. Specifically, the system can perform a “hard switch” from serial processing mode to parallel processing mode. *Id.* at 11:46–52. Additionally, the system may switch from primarily serial processing to primarily parallel processing, and from only serial or only parallel processing (singular processing) to a hybrid

of serial and parallel processing. *Id.* at 3:34–35, 11:46–52; *see also* 1:45–47 (referring to mixed serial and parallel processing modes as hybrid).

B. Claims 1 and 33

The '388 patent includes 39 claims, all of which are challenged here. Claims 1, 19, 32, and 33 are independent. *See* Ex. 1001, 13:51–18:3. We reproduce claims 1 and 33 below with bracketed notations and some paragraphing added.

1. An apparatus comprising:

[(i)] a serial processor adapted to execute software instructions in a software program primarily in serial;

[(ii)] a serial memory adapted to store data for use by the serial processor in executing the software instructions primarily in serial;

[(iii)] a plurality of parallel processors adapted to execute software instructions in the software program primarily in parallel; and

[(iv)] a plurality of partitioned memory modules adapted to store data for use by the plurality of parallel processors in executing the software instructions primarily in parallel;

[(v)] wherein the serial processor is further adapted, prior to a transition from a serial processing mode to a parallel processing mode, to provide for a transfer of updated data from the serial memory to at least one of the plurality of partitioned memory modules and

[(vi)] to receive a corresponding acknowledgement from the at least one of the plurality of partitioned memory modules that the updated data has been queued or committed prior to any memory requests from the plurality of parallel processors.

Id. at 13:51–14:5.

33. A method of transitioning from a serial processing mode to a parallel processing mode in a computing system, the method comprising:

[(i)] transferring updated data from a serial memory to at least one of a plurality of partitioned memory modules;

[(ii)] receiving a corresponding acknowledgement from the at least one of the plurality of partitioned memory modules that the updated data has been queued or committed to be stored in memory, prior to any memory requests from the plurality of parallel processors;

[(iii)] broadcasting a first signal to the plurality of parallel processors to initiate prefetching of data from at least a portion of the plurality of partitioned memory modules; and

[(iv)] broadcasting a second signal to the plurality of parallel processors for substantially concurrent initiation of a parallel processing mode.

Ex. 1001, 16:36–52.

C. Claim Construction¹

1. *Adapted to execute primarily in serial* *Adapted to execute primarily in parallel*

a) *Introduction*

Independent claims 1, 19, and 32 each recite, “a serial processor *adapted to* execute software instructions in a software program *primarily* in serial.” Ex. 1001, 13:52–53 (emphases added). Those claims similarly

¹ In this *inter partes* review the claim construction standard to be applied is the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). The claim construction standard is that used by Article III federal courts, which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. See 37 C.F.R. § 42.100(b) (2019).

recite that the plurality of parallel processors are “adapted to” execute² “primarily in parallel.” *Id.* at 13:57–59. Dependent claims 2–18 and 20–31 include these limitations by virtue of dependence from independent claims 1 and 19, respectively. Claims 33–39 do not contain these limitations.

In the Preliminary Response, Patent Owner argued that “adapted to” has the narrower meaning of “designed to” rather than the broader meaning of “configured to.” Prelim. Resp. 24–26.

In the Institution Decision, we answered Patent Owner’s argument by preliminarily construing “adapted to” to mean “configured to.” Dec. 6–8. The ’388 patent is clear on that point. *See, e.g.*, Ex. 1001, 2:59–3:6, (describing parallel processors as “*adapted (or, equivalently, configured) to*” execute substantially in parallel), 3:22–23 (describing the serial processor as “configured to” execute in serial), 3:26–28, 3:35–39, 4:39–42. We informed the parties that claim construction was an open issue during trial. Dec. 9.

During trial, the claim interpretation dispute shifted. Rather than focusing on the meaning of “adapted to” with regard to the serial and parallel processors, the focus became the meaning of “primarily” with regard to the serial and parallel processors. Specifically, Patent Owner argues that Nakaya’s processors do not execute “primarily” in serial or “primarily” in parallel, as claimed, because Nakaya’s processors perform serial and parallel processing equally well. *See* PO Resp. 28–32; *see also* PO Resp. 29 (largely agreeing that “adapted to” means “configured to”); Pet. Reply 1–2 (agreeing that “adapted to” means “configured to”).

² We use “execute” as shorthand for executing software instructions in a software program.

To understand the claim construction issue, it is important to distinguish the *individual* serial and parallel processors executing primarily in serial or parallel, from the system³ as a whole executing primarily in serial or parallel. Under the first interpretation, the serial processor must be configured to execute primarily in serial and the parallel processors must be configured to execute primarily in parallel. Under the second interpretation, the processors must be adapted to execute so that the *system* (as contrasted to the individual processors) executes primarily in serial or parallel. In the analysis of the next section, we explain why the second interpretation is the correct one.

At Oral Hearing, we discussed claim construction with the parties. *See, e.g.*, Tr. 5:20–6:25. Because our interpretation differed from that of either party, we invited the parties to submit additional briefing, and they did. *See* Paper 33 (authorization); Pet. Supp. Br.; PO Supp. Br. Our authorization included an abbreviated version of the claim construction that follows. *See* Paper 33.

b) Analysis

We begin with the language of the claims. As stated above, claims 1, 19, and 32 each require a serial processor adapted to execute primarily in serial, and similarly require parallel processors adapted to execute primarily in parallel. We focus primarily on the language of claim 1. Our analysis, however, also applies to claims 19 and 32.

³ Independent claims 1, 19, and 32 are each directed to an “apparatus.” The ’388 patent uses terms “apparatus” and “system” interchangeably. *See, e.g.*, Ex. 1001, 2:59, 4:23–25, 12:5–11.

The Specification describes an embodiment having a serial processor adapted to execute “primarily” in serial, and serial memory adapted to store data for use by the serial processor in executing the software instructions “substantially” in serial. Ex. 1001, 3:1–6. That embodiment also includes a plurality of parallel processors adapted to execute “substantially” in parallel. *Id.* at 2:59–67. Significantly, independent claim 32 refers to the serial processor both as adapted to execute “primarily” in serial, and as adapted to execute “substantially” in serial. Ex. 1001, 16:17–23. In light of these teachings, we find that the Specification uses the terms “primarily” and “substantially” interchangeably.

In a context similar to that of the claims at issue, “substantially” has been interpreted to mean “largely but not wholly that which is specified.” *See, e.g., York Prods. v. Cent. Tractor and Farm & Family Ctr.*, 99 F.3d 1568, 1573 (Fed. Cir. 1996). That interpretation is consistent with the claim language and the Specification.

Returning to the language of claim 1, we determine that “a serial processing mode” refers to the *system* executing primarily in serial on the serial processor. Likewise, “a parallel processing mode” refers to the *system* executing primarily in parallel on the parallel processors. The Specification supports that interpretation. Specifically, the Specification describes that the system may make a hard switch from “serial processing mode” to “parallel processing mode,” or may switch from “primarily serial processing” to “primarily parallel processing.” Ex. 1001, 11:46–52; *see also id.* at 1:58–61, 3:34–35; 5:6–48, 6:54–56; 8:3–5; 10:36–41. Therefore, the Specification explicitly describes primarily serial processing as an example of a serial processing mode, and likewise describes primarily parallel processing as an

example of a parallel processing mode. This suggests that a serial processor as claimed must be adapted to execute in a serial processing mode (a mode of executing so that the system is executing primarily in serial). Likewise, the parallel processor must be adapted to execute in a parallel processing mode (a mode of executing so that the system is executing primarily in serial).

We return to the language of claim 1 having determined that: “adapted to” means “configured to,” “primarily” means “largely but not wholly,” and the serial and parallel processing modes each refer to the execution of the system as a whole. Thus, the claimed serial processor must be configured to have a serial processing mode (a mode where the system executes largely but not wholly in serial on the serial processor). Likewise, the parallel processors must be configured to have a parallel processing mode (a mode where the system executes largely but not wholly in parallel on the parallel processors).

Notably the requirement is to operate “primarily” in serial rather than “only” in serial. Consequently, the system may operate to some lesser degree in other than serial on the serial processor when in the serial processing mode. For example, when in serial processing mode, the system could also operate to some lesser degree in parallel on the parallel processor.

The Specification supports this interpretation. The Specification consistently describes the serial processor as the master processor, commanding both the transition from serial processing mode to parallel processing mode and vice versa. *See, e.g.*, Ex. 1001, 7:47–50, 55–58; *see also id.* at 11:46–52 (contrasting processing “primarily” and “only” in serial or parallel). In order for the serial processor to command a transition from

parallel processing mode to serial processing mode, the serial processor must operate during parallel processing mode. That is, when in parallel processing mode, the system is executing primarily in parallel on the parallel processors, but executes to some lesser amount in other than parallel (i.e., the serial processor commanding the transition to serial processing).

In sum, we determine that independent claims 1, 19, and 32 each require that the serial processor is adapted to execute so that the system executes largely but not wholly in serial on the serial processor. Likewise, the parallel processors are required to be adapted to execute so that the system executes largely but not wholly in parallel on the parallel processor.

Petitioner agrees with our claim interpretation. Specifically, Petitioner contends that the Board's interpretation that the term "primarily" characterizes the capabilities or configuration of the claimed serial and parallel processors with regard to the functioning of the *system* as a whole—not just to the capabilities or configuration of the serial and parallel processors as individual components—is supported by the claims and specification. Paper 35, 1 (referring to our claim construction in Paper 33).

Patent Owner contends that our interpretation "omits the claim's express requirement that the apparatus comprise a distinct serial processor configured for serial execution and parallel processors configured for parallel execution." Paper 36, 3. We disagree with Patent Owner's contention because our interpretation explicitly accounts for a distinct serial

processor and parallel processors.⁴ *See* Paper 33, 5. Patent Owner closes their supplemental briefing by asserting again that “primarily” must be interpreted as a requirement of the individual processors. Paper 36, 5. That interpretation is incorrect for the reasons given in our claim construction above.

2. *Claim 33*

Claim 33 is directed to a method of transitioning from a serial processing mode to a parallel processing mode. Thus, claim 33, like independent claims 1, 19, and 32, calls for a serial processing mode and a parallel processing mode. Unlike the other independent claims, the parallel processing mode of claim 33 is initiated by a second signal (limitation (iv)).

The serial and parallel processing modes of claim 33 are broader than in the other independent claims. Claim 33 does not recite that the system must include a serial processor adapted to execute “primarily” in serial. The method includes a serial processing mode, and for that reason the use of a serial processor is implied; however, that processor is not limited to being adapted to execute so that the system is executing primarily in serial on the serial processor. Claim 33 does not recite that the plurality of parallel processors are adapted to execute “primarily” in parallel. Claim 39 depends from claim 33 and recites that the method further comprises executing primarily in parallel in the parallel processing mode. The presence of this limitation in dependent claim 39 strongly suggests the limitation is not a

⁴ “Claim 1 requires that the system include a serial processor that is adapted to execute software instructions so that the system is executing largely but not wholly in serial. Likewise, claim 1 requires that the system include a parallel processor that is adapted to execute software instructions so that the system is executing largely but not wholly in parallel.” Paper 33, 5.

requirement of in independent claim 33. *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004). Consequently, the parallel processing mode of claim 33 is not limited to executing software instructions primarily in parallel.

In sum, the method of claim 33 includes a serial processing mode and a parallel processing mode initiated by the second signal.

3. *Claim 39*

As mentioned above, claim 39 depends from claim 33 and recites that the method further comprises executing primarily in parallel in the parallel processing mode. The parallel processing mode of claim 39 is similar to the parallel processing mode of independent claims 1, 19, and 32 in that the parallel processing mode is limited to executing primarily in parallel on the plurality of parallel processors.

D. Level of Skill in the Art

In the Institution Decision, we observed that the parties differ somewhat with regard to the education and experience levels of a person of ordinary skill at the time of invention for the '388 patent. Dec. 10–13. We preliminarily accepted Petitioner's view of the level of skill in the art, and considered the prior art of record to be reflective of the level of skill in the art. *Id.* at 10. Since Institution, the parties differ regarding the same two aspects of the level of skill in the art (i.e., education and experience levels).

Regarding education, Petitioner asserts that a person of ordinary skill would have had a Master's or Doctorate degree in electrical engineering, computer engineering, or a related field. Pet. 8; Ex. 1014 ¶¶ 33–36. Patent Owner agrees with the area of study, but not the level of the degree. PO

Resp. 23, Ex. 2009 ¶¶ 50–65. Specifically, Patent Owner asserts a person of ordinary skill would have had a Bachelor’s degree rather than a Master’s or Doctorate degree. PO Resp. 23, Ex. 2009 ¶¶ 50–65.

Regarding experience, the parties agree that a person of ordinary skill would have had about three years of experience. The parties differ in that Petitioner contends that the experience would have been in parallel computing architectures, while Patent Owner more broadly contends the experience would have been in “general computer architecture.” Pet. 8 (citing Ex. 1014 ¶¶ 33–36); PO Resp. 23.

There is very little difference between the skill levels asserted by the parties. As we pointed out in the Institution Decision, the parties only disagree with regard to two of the factors relevant to the level of skill in the art. *See* Dec. 12. There is no dispute with regard to the many other factors that influence the level of skill in the art. Further, also as pointed out in the Institution Decision, Patent Owner’s broader recitation of experience in “general computer architecture” would include experience with both serial and parallel processing. *Id.* In the Response, Patent Owner chose not to dispute other factors of the level of skill inquiry, and chose not to dispute that general experience would include experience with parallel computing architectures.⁵

We determine that a person of ordinary skill in the art at the time of ’388 patent would have had either a Bachelor’s or a Master’s degree in electrical engineering, computer engineering, or a related field, and would have had about three years of experience in computer architecture that

⁵ We informed the parties they could further address the level of skill during the trial. Dec. 13.

included experience with both serial and parallel processing. Our reasoning follows.

Patent Owner contends that the '388 patent identifies the type of problems encountered in the art, namely, computer asset management in contemporary personal computers having a graphics processing unit (GPU) and a central processing unit (CPU). PO Resp. 24; Ex. 1001, 1:28–43. According to Patent Owner, a person having a bachelor's degree would have been aware of the interplay between assets for the CPU and GPU and the basics of parallel computing. PO Resp. 24; Ex. 2009 ¶ 54 (citing Ex. 2011, 28:7–16).

Patent Owner's contention acknowledges that a person of ordinary skill would have had experience in both serial and parallel processing. *See* Pet. 8; Ex. 1014 ¶¶ 33–36. This supports Petitioner's assertion that a person having ordinary skill would include experience with parallel processing. *See* Pet. Reply 5. Regarding Patent Owner's contention of what a person with a Bachelor's degree would have known, Patent Owner cites to the Deposition of Petitioner's expert, Dr. Kaeli. *See* PO Resp. 24 (citing Ex. 2009 ¶ 54, which cites in turn to Ex. 2011, 28:7–16). Contrary to Patent Owner's assertion, Dr. Kaeli does not state certain things are taught in a Bachelor's degree course; rather, Dr. Kaeli states that he taught certain things in a class that was attended by both graduate and undergraduate students. *See* Ex. 2011, 28:7–16. Therefore, the evidence supports our position that such knowledge was obtained either in undergraduate or graduate work.

Patent Owner contends that people without advanced degrees⁶ routinely addressed issues in the field of the invention. PO Resp. 24. As examples, Patent Owner cites to: Vishkin, a background research project cited by Dr. Kaeli, Stanford's Dash team, and the second author of Koufaty (Xiangfeng Chen). *Id.* (citing Ex. 1006, 11; Ex. 1014 ¶¶ 43–45; Exs. 1015, 1022, 1023; Ex. 1005, 15).

Petitioner counters, and we agree, that Patent Owner's contention is factually incorrect in several respects. First, while some authors of the Vishkin paper did not have advanced degrees, an author (Dr. Vishkin himself) had an advanced degree and that person was, by Patent Owner's own acknowledgment, a person of extraordinary skill. PO Resp. 23; Pet Reply 6; Exs. 1007, 1008. Second, several members of the DASH team were Ph.D. students (Lenoski, Laudon, Gharachorloo, Weber), and four members of the team were faculty and presumably had advanced degrees (Gupta, Hennessy, Horowitz, and Lam). Pet. Reply 6–7; Ex. 1015, 2. Third, Xiangfeng Chen had a master's degree in computer science. Pet. Reply 6; Koufaty, 15. Beyond these specific corrections to Patent Owner's assertions, we note that two of Koufaty's authors (Koufaty and Chen) held Master's degrees, and two held doctorates (Poulson and Torrellas). *See* Ex. 1005, 15; Pet. Reply 6–7; PO Resp. 24. The work in the field identified by Patent Owner was done by people with Bachelor's degrees and people having higher degrees. *See* Pet. Reply 6.

⁶ We presume that by "advanced degrees" Patent Owner means degrees beyond a Bachelor's degree.

Patent Owner contends computer engineering was a rapidly evolving field. PO Resp. 25 (citing Ex. 2010, 1; Ex. 2012; Ex. 2009 ¶ 56⁷). Based on this, Patent Owner contends that computer systems relied on abstractions so that engineers with a bachelor's degree could keep pace. *Id.*

While we agree that computer engineering was a rapidly evolving field, Patent Owner presents no supporting evidence for the proposition that computer systems relied on abstractions so that engineers with a Bachelor's degree could keep pace.

Patent Owner contends that persons of ordinary skill focused in one or more specific areas of expertise rather than being fluent in the combination of disparate parallel processing schemes proffered in the Petition. PO Resp. 25 (citing Ex. 2009 ¶ 58). Patent Owner's contention that a person of ordinary skill in the art would have had specialized knowledge is a bit at odds with Patent Owner's overall assertion that experience for a person of ordinary skill in the art would have been in "general computer architecture." *Compare* PO Resp. 23 to 25.

Patent Owner contends that parallel processor and memory arrangements, schedulers, and compilers were part of undergraduate computer science course work. *Id.* (citing Ex. 2009 ¶ 59; Ex. 2014, 7). Patent Owner adds that after two or three years in the industry, a person of ordinary skill would have had basic hands-on familiarity with those topics, as reflected in the average education level in the field of parallel computing. PO Resp. 26 (citing Ex. 2009 ¶ 60; Ex. 2015, 3).

Knowledge of the variety of hardware Patent Owner enumerates suggests that a person of ordinary skill had general computer system

⁷ The relevant testimony is found at paragraph 57 rather than paragraph 56.

knowledge rather than specialized knowledge. Further, as pointed out earlier, Dr. Kaeli stated the courses discussed were taught in a class including both undergraduate and graduate students, following which Patent Owner's attorney continued to refer to the courses as undergraduate courses. *See* Ex. 2011, 28:7–33:19. We accept as true that a person with a Bachelor's degree and three years in the industry would have had familiarity with parallel processor and memory arrangements, schedulers, and compilers.

In the Preliminary Response, Patent Owner argued that the opinion of Petitioner's expert, Dr. Kaeli, is entitled to little or no weight because Dr. Kaeli offered only conclusory assertions regarding the level of ordinary skill. PO Resp. 26 (citing 37 C.F.R. 42.65(a)). In our Institution Decision, with regard to that argument, we observed,

Contrary to Patent Owner's contention, Dr. Kaeli's opinion is not wholly without factual predicates. For example, his opinion is based on his experience (Ex. 1014 ¶¶ 4, 6–14, App'x B), certain enumerated materials (Ex. 1014 ¶ 5), and legal standards (Ex. 1014 ¶¶ 15–16, 20–28, 33–35). Patent Owner does not contest any of these underlying bases.

In the Response, Patent Owner repeats the argument from the Preliminary Response. *See* PO Resp. 26. Repeating that argument, without addressing the underlying bases of Dr. Kaeli's opinion that we identified, does not add support to Patent Owner's position.

Patent Owner argues that Petitioner's reliance on three or four prior art references for the grounds of unpatentability suggests the claims of the '388 patent were not unpatentable. PO Resp. 27. Patent Owner argues that a person of ordinary skill (by either Petitioner's or Patent Owner's definition) would not have been motivated to make the proposed combinations and would not have had a reasonable likelihood of success in

doing so. PO Resp. 27 (citing Ex. 2009 ¶ 62). As a supporting example, Patent Owner contends that a person of ordinary skill in the art would not have had an understanding of how alteration of one aspect of the design may influence the performance or design of other parts. *Id.* at 27–28 (citing Ex. 1014 ¶ 36; Ex. 2009 ¶¶ 63–64).

Although the concepts somewhat interrelate, Patent Owner’s arguments deal more with the expectation of success than the level of skill in the art. As an aside, we note that even combining a large number of references, and we do not consider three or four references a large number of references, without more, does not demonstrate nonobviousness. *See, e.g., In re Gorman*, 933 F.2d 982, 986 (Fed. Cir. 1991); *see also* MPEP § 707.07(f) (9th ed. rev. 11.2013 June 2020).

We agree with Petitioner that Patent Owner acknowledged, “[c]omputer engineering is often an exceedingly complex art in which small changes in even one process step can have extremely significant and unanticipated consequences.” PO Resp. 44; *see* Pet. Reply 6 (identifying this acknowledgment).

As Petitioner observes, Patent Owner’s expert acknowledges that the basic concepts of the ’388 patent were taught to either senior undergraduate students or first year graduate students. Pet. Reply 7; Ex. 1031, 28:15–29:7. Further, other concepts of the ’388 patent were taught in graduate courses. Pet. Reply 7; Ex. 1031, 34:2–14.

Taken as a whole, the arguments and evidence suggest that a person of ordinary skill in the art at the time of ’388 patent would have had either a Bachelor’s or a Master’s degree in electrical engineering, computer engineering, or a related field. Further, that person would have had about

three years of experience in computer architecture that included experience with both serial and parallel processing.

III. PATENTABILITY

A. Asserted Grounds and Evidence

Petitioner asserts that the challenged claims would have been unpatentable on the following grounds:⁸

Claims Challenged	35 U.S.C. §	References
1, 3, 12–14, 17, 18	103(a) ⁹	Nakaya, Nakamura, Koufaty ¹⁰
2, 4–11, 15, 16, 19–39	103(a)	Nakaya, Nakamura, Koufaty, Vishkin ¹¹

B. Obviousness over Nakaya, Nakamura, and Koufaty

Petitioner asserts that claims 1, 3, 12–14, 17, and 18 are unpatentable as obvious over Nakaya, Nakamura, and Koufaty. *See* Pet. 12–33. We

⁸ Petitioner supports its challenge with a Declaration by Dr. David Kaeli (Ex. 1014), and Patent Owner relies on a Declaration by Dr. Murali Annavaram (Ex. 2001).

⁹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the challenged claims of the ’388 patent have an effective filing date before the effective date of the relevant amendment, the pre-AIA version of § 103 applies.

¹⁰ Ex. 1003, U.S. Pat. No. 5,978,830 (Nov. 2, 1999) (“Nakaya”); Ex. 1004, U.S. Pat. App. Pub. No. 2003/0177273 A1 (Sept. 18, 2003) (“Nakamura”); Ex. 1005, “Data Forwarding in Scalable Shared-Memory Multiprocessors,” IEEE Transactions on Parallel and Distributed Systems, Vol. 7, No. 12 (Dec. 1996) (“Koufaty”).

¹¹ Ex. 1006, “Explicit Multi-Threading (XMT) Bridging Models for Instruction Parallelism” (1998) (“Vishkin”).

provide below an overview of only Nakaya because our analysis need not address Nakamura or Koufaty.

1. Overview of Nakaya (Ex. 1003)

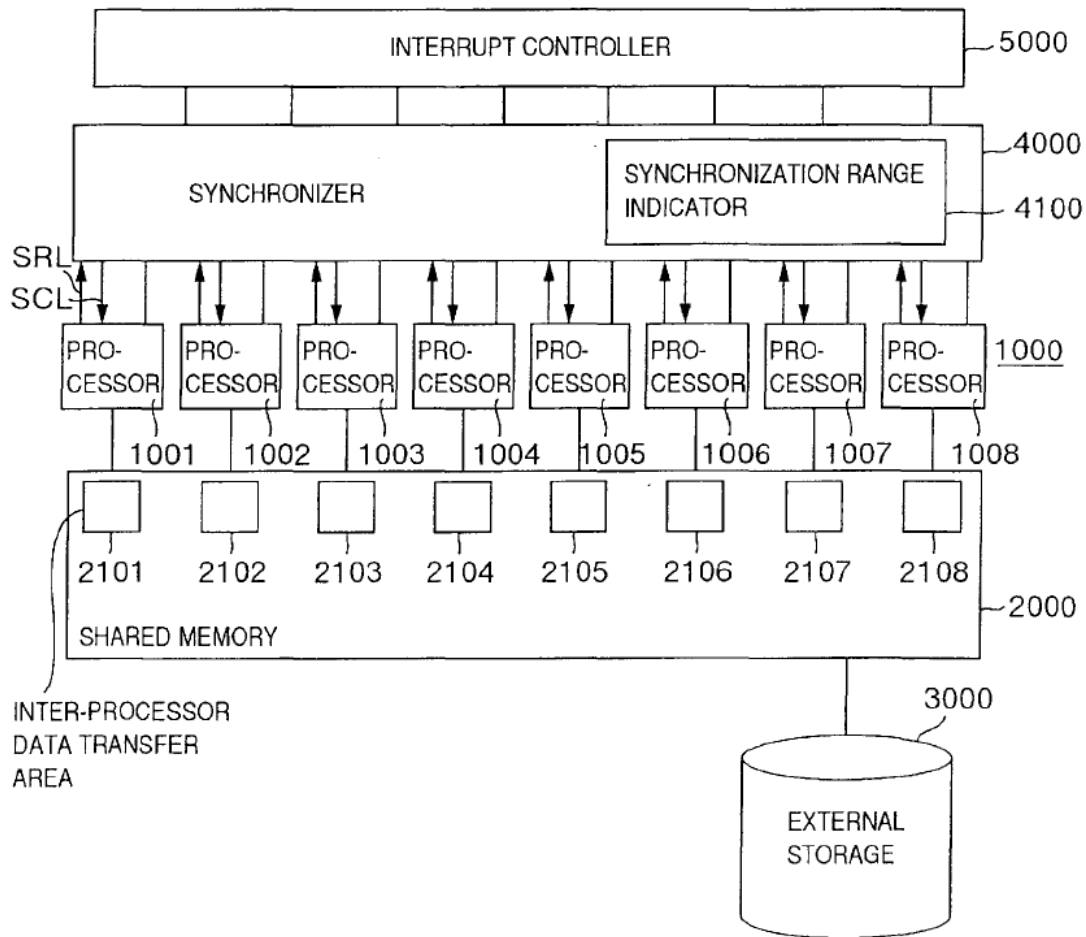
Nakaya, “Multiple Parallel-Job Scheduling Method and Apparatus,” relates to “a multiple parallel-job scheduling method and apparatus suitable for parallel or concurrent execution of a plurality of parallel information processing programs.” Ex. 1003, code (54), 1:5–9.

Nakaya explains that in a conventional computer system used for parallel job execution, the number of serial and parallel processors is fixed. *Id.* at 16:5–7. In contrast, Nakaya’s processors function equally as serial or parallel processors, and Nakaya’s system dynamically changes the ratio of serial to parallel processors to increase utilization of the computer system. *Id.* at 16:24–30; *see also* 1:44–47 (describing that Nakaya’s technique improves utilization of all processors).

When reading Nakaya, it is useful to note that the ’388 patent speaks in terms of “executing software instructions,” while Nakaya refers to processors as executing “jobs.” *See, e.g.*, Ex. 1001, 2:59–63; Ex. 1003, 1:44–47.

Nakaya describes a computer system that includes a group of processors 1000 each connected to shared memory 2000 to read/write data. *Id.* at 7:60–64. For example, group of processors 1000 could include processors 1001–1004 that constitute or behave as serial processors and processors 1005–1008 that constitute or behave as parallel processors. *Id.* at 8:32–37. Synchronizer 4000 is connected to and executes synchronous control of processors 1001–1008. *Id.* at 8:55–58. Nakaya’s Figure 1 follows.

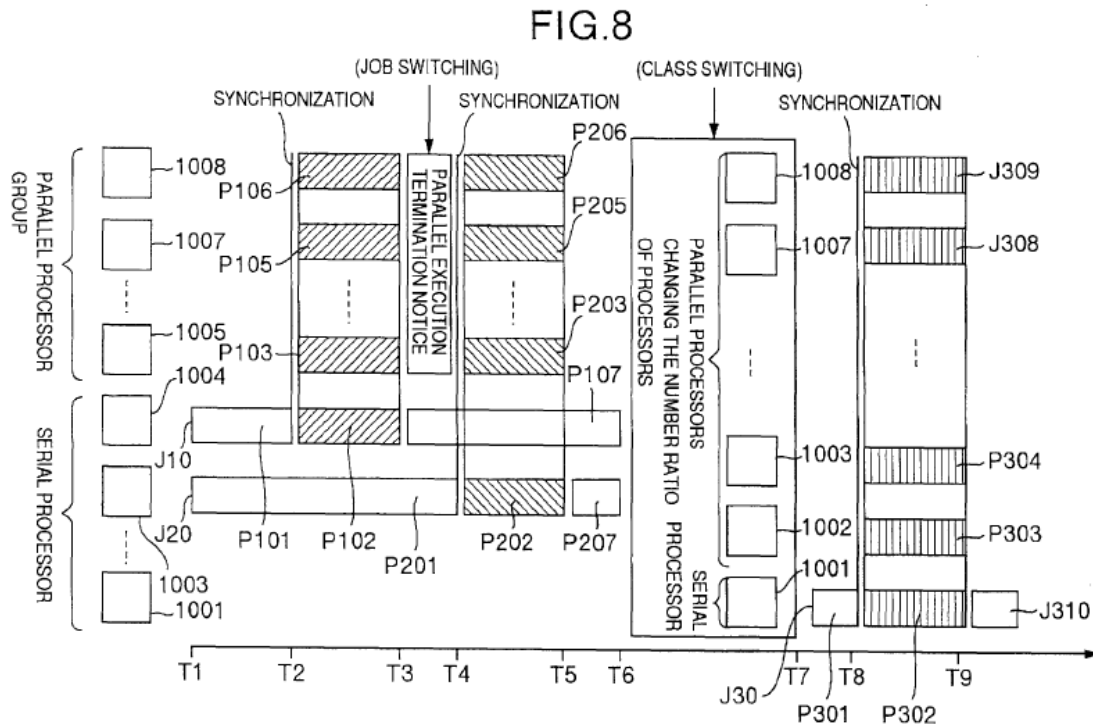
FIG.1



Nakaya's Figure 1, above, "is a diagram showing the overall construction of a computer system." *Id.* at 6:12-13.

Shared memory 2000 includes inter-processor data transfer areas 2101 to 2108 that permit data transfer among processors. *Id.* at 7:64-8:2. For example, processor 1001 may send data to processor 1002 by writing data into data transfer area 2102, and processor 1002 may then reference that data. *Id.* at 8:2-7

Nakaya describes a method of assigning multiple processors to jobs and dynamically changing the number ratio of serial processors to parallel processors. *Id.* at 13:3–6; Fig. 8. Nakaya’s Figure 8 follows.



Nakaya’s Figure 8, above, is a diagram explaining the outline of multiple execution of parallel jobs. *Id.* at 6:32–33, 13:1–2.

For example, in one embodiment, during time interval T1 to T6, processors 1001 to 1004 behave as serial processors and processors 1005 to 1008 behave as parallel processors. *Id.* at 13:9–12. After time T6, only processor 1001 behaves as a serial processor, and processors 1002–1008 behave as parallel processors. *Id.* at 13:12–15.

2. *Independent Claim 1*

a) *Overview of Ground of Unpatentability*

Claim 1 is the sole independent claim subject to the first ground of unpatentability. Ex. 1001, 13:51–15:4. Petitioner argues that the teachings of Nakaya, Nakamura, and Koufaty render claim 1 unpatentable as obvious. *See* Pet. 12–29.

b) *Sufficiency of the Petition*

Patent Owner argues that the Petition is silent regarding the system executing primarily in serial or primarily in parallel. Paper 36, 2. According to Patent Owner, due to that omission, Petitioner has not shown the claims to be unpatentable. *Id.* (citing *Intelligent Bio-Sys. Inc., v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016)).

We agree with Patent Owner that the Petition must identify how the construed claim is unpatentable. *See* 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(4). We analyze the limitation at issue as addressed by the Petition.

Petitioner contends that Nakaya discloses a serial processor (processor 1001) and a plurality of parallel processors (processors 1005–1008). Pet. 19–20, 22–23 (citing Ex. 1003, Abstract, 8:12–25, 8:32–54, 13:7–16, 15:29–61, Figs. 1, 8; Ex. 1014 ¶¶ 102–107, 114–118); *see also* Pet. 12 (asserting that Nakaya’s processors 1001–1008 correspond to serial and parallel processors as claimed). The Petition refers to Nakaya’s synchronization process as corresponding to the transition from serial to parallel processing as claimed. Pet. 26–29 (citing Ex. 1003, 7:63–8:7, 9:13–34, 17:1–10, 18:1–9, Fig. 10; Ex. 1014 ¶¶ 127–136). The Petition asserts that Nakaya’s processor 1001 is a serial processor over the full course of executing the

program, and that processors 1005–1008 are parallel processors over the full course of executing the program. Pet. 20, 22 (citing Ex. 1003, 13:7–16, 15:29–46, Fig. 8; Ex. 1014 ¶¶ 106–107, 117–118).

Throughout the Petition, and the cited portions of Dr. Kaeli’s testimony, Petitioner consistently presents argument and evidence as if executing primarily in serial and executing primarily in parallel are requirements of each processor individually. As detailed in our claim construction above, and as now acknowledged by Petitioner, that is not what claim 1 requires. *See* Paper 35, 1. Claim 1 requires a serial processor adapted to execute so that the *system* is executing primarily in serial on the serial processor, and requires parallel processors adapted to execute so that the *system* executes primarily in parallel on the parallel processor. Neither the Petition, nor Dr. Kaeli’s cited testimony properly addresses how Nakaya’s processors meet this limitation.

Beyond Petitioner’s lack of an explanation, as detailed below, it appears the prior art does not meet the claim limitations at issue.

As summarized above, Petitioner contends that Nakaya’s synchronization corresponds to the claimed transition from serial processing mode to parallel processing mode. Pet. 15–16 (citing Nakaya, 17:39–45; Ex. 1014 ¶ 89).

As detailed above, Nakaya discloses: from T1 to T6 an equal number of processors behave as serial (1001–1004) and parallel processors (1005–1008); from T6 on, only processor 1001 behaves as a serial processor (processors 1002–1008 behave as parallel processors); and at T8, synchronization occurs. Ex. 1003, 13:7–15, 15:29–33 (describing that the ratio between the number of serial and parallel processors changes at T6),

Fig. 8. Therefore, from T6 to T8, Nakaya's system has one processor behaving as a serial processor and seven processors behaving as parallel processors.

Nakaya's system changes the ratio of serial to parallel processors at T6, not at T8 (synchronization). Specifically, prior to T6, the system is processing on four serial and four parallel processors, and after time T6, the system is processing on one serial and seven parallel processors. Nakaya's processor ratio change is akin to the claimed transition from serial processing mode to parallel processing mode. At T8, the ratio of serial to parallel processors being used by the system remains the same (one to seven). That is, at the moment Petitioner contends corresponds to the claimed transition from serial to parallel processing, there is actually no change in the ratio of serial to parallel processors in use by Nakaya's system.

We emphasize that the Petition is deficient because it fails to adequately address how the prior art discloses or suggests a serial processor configured to execute so that the system executes largely but not wholly in serial on the serial processor. Likewise, the Petition does not adequately address how the prior art discloses or suggests a parallel processor adapted to execute so that the system executes largely but not wholly in parallel on the parallel processor.

c) Patentability Arguments in Supplemental Brief

In their Supplemental Brief, Petitioner argues that Nakaya discloses the claimed serial and parallel processors and processing modes under the Board's construction. Paper 35, 2 (referring to our claim construction in Paper 33 and citing *Chamberlain Grp. Inc. v. One World Techs., Inc.*, 944 F.3d 919 (Fed. Cir. 2019); *Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697

(Fed. Cir. 2020); and *Ericsson Inc. v. Intell. Ventures I LLC*, 901 F.3d 1374 (Fed. Cir. 2018)).

We begin with the cases cited by Petitioner. *Chamberlain* is distinguishable in that it addresses whether a patent owner made a new argument at oral hearing. *Chamberlain*, 944 F.3d at 925. Unlike the case at hand, *Chamberlain* does not address the sufficiency of the Petition.

Ericsson and *Apple* address the scope of the reply brief. *Ericsson*, 901 F.3d at 1379; *Apple*, 949 F.3d 697. The legal issue there is similar in that both the reply brief and the supplemental brief come after the petition. *Ericsson* acknowledged that a reply brief is not an opportunity for a petitioner to identify new and different prior art elements that are alleged to satisfy claim requirements. *Ericsson*, 901 F.3d at 1379. Likewise, the Supplemental Brief at issue here is not such an opportunity. In *Apple*, the Federal Circuit determined that the petitioner's reply did not exceed the scope of the petition. *Apple*, 949 F.3d at 706–07. That is not the case here. As detailed above, the Petition did not address how the proposed combination disclosed or suggested a serial processor adapted to execute so that the system executes primarily in serial on the serial processor (serial processing mode) or parallel processors adapted to execute so that the system executes primarily in parallel on the parallel processors (parallel processing mode).

As mentioned above, the Petition must identify how the construed claim is unpatentable. See 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(4). Indeed, the Federal Circuit has stated that it is “of the utmost importance” that petitioners adhere to that requirement. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (cited with

approval in *Apple*, 949 F.3d at 705). Consequently, Petitioner's Supplemental Brief cannot cure the deficiencies of the Petition.

Even if Petitioner could properly rely upon their Supplemental Brief to correct the Petition, it does not do so. Petitioner asserts that from time T7–T8 Nakaya's system operates in serial processing mode, followed by transition at T8, and then operating in parallel processing mode from T8–T9. Paper 35, 3–5. The reference contradicts Petitioner's assertion in at least two respects.

First, as explained above, from time T6–T8, Nakaya's system has one processor behaving as a serial processor and seven processors behaving as parallel processors. That is, from T6–T8, a period Petitioner asserts corresponds to serial processing mode, Nakaya's system is actually in parallel processing mode because it is executing largely but not wholly (seven of eight processors) in parallel on the parallel processors. Second, at T8, a period Petitioner contends corresponds to the claimed transition from serial to parallel processing, Nakaya's system actually does not change the ratio of serial to parallel processors (it remains at one to seven, respectively). Consequently, Nakaya's synchronization cannot correspond to the claimed transition from serial to parallel processing.

d) Conclusion for Claim 1

Petitioner has not shown by a preponderance of the evidence that independent claim 1 is unpatentable.

3. Claims 3, 12–14, 17, and 18

Claims 3, 12–14, 17, and 18 depend from independent claim 1. Therefore, the ground of unpatentability against these claims suffers from the same shortcoming as that of claim 1.

C. Obviousness over Nakaya, Nakamura, Koufaty, and Vishkin

1. *Claims 2, 4–11, 15, 16, and 19–32*

Petitioner asserts that claims 2, 4–11, 15, 16, and 19–32 are unpatentable as obvious over Nakaya, Nakamura, Koufaty, and Vishkin. Pet. 33–59.

Claims 2, 4–11, 15, and 16 depend from independent claim 1. Petitioner does not rely on Vishkin to cure the deficiencies of the ground of unpatentability against independent claim 1. Consequently, Petitioner has failed to show by a preponderance of the evidence that these claims are unpatentable.

Independent claims 19 and 32 are apparatus claims, and like independent claim 1, require that the serial processor is adapted to execute so that the system executes largely but not wholly in serial on the serial processor and require that the parallel processors are adapted to execute so that the system executes largely but not wholly in parallel on the parallel processor. Claims 20–31 depend from independent claim 19. Petitioner does not rely on Vishkin to cure the deficiencies of the ground of unpatentability against independent claim 1. Consequently, Petitioner has failed to show by a preponderance of the evidence that these claims are unpatentable.

2. *Claim 33*

For the ground of unpatentability against claim 33, Petitioner incorporates the analysis of claims 1, 2, and 4 in the first ground of unpatentability. Pet. 56–57. Therefore, the ground of unpatentability against claim 33, like the first ground of unpatentability, presents argument and evidence as if executing primarily in serial and executing primarily in

parallel are requirements of each processor individually. While the scope of claim 33 is somewhat different from the other independent claims, claim 33 still requires a serial processing mode and a parallel processing mode.

Petitioner has not identified how the computer system of the proposed combination performs the method of claim 33 so that it executes in a serial processing mode and in a parallel processing mode. Absent an explanation of the how operation of the proposed combination corresponds to serial and parallel processing modes as claimed, Patent Owner did not have a meaningful opportunity to respond to the ground of unpatentability, and Petitioner has not met its burden to identify how the claim is unpatentable.

Beyond this due process concern, the ground of unpatentability has another shortcoming. The method of claim 33 requires broadcasting a second signal to the plurality of parallel processors for substantially concurrent initiation of a parallel processing mode. In other words, claim 33 requires that the second signal initiate the transition from serial to parallel processing mode.

Petitioner contends that in the proposed combination, the second signal occurs with the timing disclosed by Nakaya's synchronization (i.e., at T8). *See* Pet. 57–58 (incorporating analysis at Pet. 26–27).

We reiterate that the Petition does not explain how the proposed combination corresponds to serial and parallel processing modes as claimed. Rather, the Petition explains how the individual processors of the proposed combination execute in serial or parallel. In other words, Petitioner addresses how the serial and parallel processors are individually adapted to execute, but does not address how the system is adapted to execute (the serial and parallel processing modes).

Even if we consider Petitioner's assertion regarding transition of the individual processors to apply to transition of the system, that assertion still does not meet the requirements of claim 33. Specifically, as explained in our analysis of the first ground of unpatentability above, Nakaya's system changes the ratio of serial to parallel processors (transitions from serial to parallel processing) at time T6. At time T8 (synchronization), the ratio of serial to parallel processors does not change (remaining at one to seven). Therefore, even if we view Petitioner's contention regarding operation of the individual processors as applying to operation of the system as a whole, it still does not meet the requirements of claim 33.

For these reasons, Petitioner has failed to show by a preponderance of the evidence that claim 33 is unpatentable.

3. Claims 34–38

Claims 34–38 depend from independent claim 33. The ground of unpatentability against these claims suffers from the same shortcoming as that of claim 33.

4. Claim 39

As explained in the claim construction above, claim 39, like independent claims 1, 19, and 32, requires that the parallel processing mode execute primarily in parallel. Petitioner relies upon the ground of unpatentability for independent claim 1 for this limitation. Pet. 59. Therefore, the ground of unpatentability for claim 39 also suffers from the same shortcoming as that of claim 1.

IV. CONCLUSION

For the foregoing reasons, we determine that Petitioner has not shown that the challenged claims are unpatentable.

Claim(s)	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 3, 12–14, 17, 18	103(a)	Nakaya, Nakamura, Koufaty		1, 3, 12–14, 17, 18
2, 4–11, 15, 16, 19–39	103(a)	Nakaya, Nakamura, Koufaty, Vishkin		2, 4–11, 15, 16, 19–39
Overall Outcome				1–39

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not shown by a preponderance of the evidence that claims 1–39 of U.S. Patent No. 7,707,388 B2 are unpatentable;
and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2;

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