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Paper 39
Date: October 18, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00518
Patent 9,250,908 B2

Before KEN B. BARRETT, CHARLES J. BOUDREAU, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision on Remand
Determining All Challenged Claims Unpatentable
35 U.S.C. §§ 144, 318(a)

I. INTRODUCTION

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and pursuant to a remand from the United States Court of Appeals for the Federal Circuit in *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373 (Fed. Cir. 2023).[1] For the reasons discussed below, we determine, in view of the Federal Circuit's decision and the record previously developed during trial, that Intel Corporation ("Petitioner")[2] has shown by a preponderance of the evidence that the sole patent claim remaining before us is unpatentable.

A. Procedural History

Petitioner filed a Petition requesting *inter partes* review of U.S. Patent No. 9,250,908 B2 ("the '908 patent," Ex. 1001). Paper 3 ("Pet."). The Petition challenges the patentability of claims 4 and 5 of the '908 patent. Prior to institution, PACT XPP Schweiz AG ("Patent Owner")[3] statutorily disclaimed independent claim 4. Ex. 2002, 9. We instituted an *inter partes* review of the sole remaining claim on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
5	103(a)	Kabemoto,[4] Bauman,[5] Chaney[6]
5	103(a)	Wu,[7] Bauman, Chaney

[1] The Federal Circuit's slip opinion is in the record of this proceeding as Paper 38.
[2] Petitioner identifies Intel Corporation as the real party-in-interest. Pet. 1.
[3] Patent Owner identifies PACT XPP Schweiz AG (formerly known as Scientia Sol Mentis AG) as the real party-in-interest. Paper 5, 2.
[4] U.S. Patent No. 5,890,217, issued Mar. 30, 1999 (Ex. 1005, "Kabemoto").
[5] U.S. Patent No. 5,680,571, issued Oct. 21, 1997 (Ex. 1007, "Bauman").
[6] U.S. Patent No. 5,930,822, issued July 27, 1999 (Ex. 1008, "Chaney").
[7] U.S. Patent No. 6,047,355, issued Apr. 4, 2000 (Ex. 1006, "Wu").

Paper 12, 5, 42. After institution, Patent Owner filed a Response to the Petition. Paper 21 ("PO Resp."). Petitioner filed a Reply (Paper 26, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 28, "PO Sur-reply").

An oral hearing was held on May 20, 2021, and a transcript of the hearing is included in the record. Paper 33 ("Tr.").

On August 9, 2021, we issued a Final Written Decision in this proceeding, determining that Petitioner had not demonstrated by a preponderance of the evidence that dependent claim 5 is unpatentable over Kabemoto, Bauman, and Chaney, based in part on our finding that Petitioner had not persuasively established a motivation to combine the teachings of Kabemoto and Bauman in the manner proposed by Petitioner. Paper 34 ("Final Decision" or "Final Dec."), 8–28, 43–44. Petitioner appealed that determination to the United States Court of Appeals for the Federal Circuit. *See* Paper 35 (Notice of Appeal). We also determined in the Final Decision that Petitioner had not demonstrated by a preponderance of the evidence that dependent claim 5 is unpatentable over Wu, Bauman, and Chaney. Final Dec. 34, 28–44. The parties represent that Petitioner did not appeal that determination regarding the Wu-based ground. Ex. 3001, 1.

As mentioned above, independent claim 4 was disclaimed prior to institution, leaving only its dependent claim 5 remaining in this proceeding. Although the ultimate issue in the case was whether dependent claim 5 would have been obvious over Kabemoto, Bauman, and Chaney, the parties' arguments for the disputed issues and, correspondingly, the Final Decision, focused on whether the underlying independent claim 4 would have been obvious over Kabemoto in view of Bauman. *See, e.g.*, PO Resp. 13–32 (arguing that Kabemoto in view of Bauman does not render claim 4

obvious); Pet. Reply 1–18. Petitioner relied on Chaney for only the limitation added by claim 5 (Pet. 58–63), and Patent Owner only argued that Chaney does not cure the purported defects of the underlying Kabemoto-Bauman ground (PO Resp. 32–33).

On March 13, 2023, the Federal Circuit issued a decision reversing certain of the Board's findings regarding the Kabemoto-Bauman ground and remanded the case to the Board for further proceedings. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th at 1381. Specifically, the court stated that "the Board's determination that the prior art did not teach the segment-to-segment limitation lacks substantial evidence, and we reverse it," and that under *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), a reason to combine may be established by a showing "that there was a known problem of cache coherency in the art, that Bauman's secondary cache helped address that issue, and that combining the teachings of Kabemoto and Bauman wasn't beyond the skill of an ordinary artisan[;] [n]othing more is required [from Petitioner] to show a motivation to combine . . . so we reverse the Board's finding to the contrary." *Id.* at 1379, 1381; *see also id.* at 1379 ("Intel also argues that the Board's rejection of its 'known-technique' rationale for a motivation to combine lacks substantial evidence. . . . We agree and reverse the Board's contrary finding.").

Regarding dependent claim 5, the court stated:

> Although we reverse the two factual findings discussed above, we must remand for the Board to address any remaining dispute about the patentability of claim 5.
>
> Claim 5 recites: "The bus system of claim 4 where the arbiter is operable to allow processor access in chronological sequence." '908 patent claim 5. Intel relied on prior art Chaney to teach this limitation. PACT did not dispute that Chaney taught this added "chronological sequence"

> limitation. But because the Board failed to analyze the invention of claim 5 as a whole, we must remand.

Id. at 1381 (footnote and citations omitted); *see also id.* ("[W]e reverse the Board's findings related to the above-discussed limitations (which appear in claim 5 by virtue of its dependence from claim 4) and remand for further proceedings consistent with this opinion."). The Federal Circuit issued its mandate on April 19, 2023. Paper 37.

The parties state that they "are . . . in agreement that the second ground of the Petition (based on Wu) is not at issue on remand, as that ground was not appealed by Petitioner." Ex. 3001, 1. Accordingly, the ground based on Kabemoto is the only ground remaining before us.

Pursuant to the Board's Standard Operating Procedure 9,[8] the parties met and conferred to discuss a proposed procedure on remand. Ex. 3001. The parties informed us that they "are in agreement that no additional briefing, submission of evidence, or oral argument is necessary to resolve the issues on remand." *Id.* After having considered the specific circumstances of this case and in light of the parties' agreement as to the procedures on remand, we determined that no further briefing on remand is necessary, that there is no need to reopen the evidentiary record, and that no additional oral argument is warranted. Paper 36.

B. Related Proceedings

One or both parties identify the following as matters involving or related to the '908 patent: *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-

[8] Standard Operating Procedure ("SOP") 9 has been replaced by SOP 3, *available at* https://www.uspto.gov/sites/default/files/documents/ptab_sop_3-2023-oct.pdf.

00267 (D. Del. Feb. 7, 2019); *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00273 (W.D. Tex. Apr. 23, 2019); *Intel Corp. v. PACT XPP Schweiz AG*, No. 19-cv-02241 (N.D. Cal. Apr. 25, 2019); and *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-01006 (D. Del. May 30, 2019). Pet. 1; Paper 5, 1–2.

C. The '908 Patent

The '908 patent is titled "Multi-Processor Bus and Cache Interconnection System." Ex. 1001, code (54). According to the Abstract of the '908 patent,

> A multi-processor is provided [with] a segmented cache and an interconnection system for connecting the processors to the cache segments. An interface unit communicates to external devices using module IDs and timestamps.

Id. at code (57).

D. The Challenged Claim

The sole remaining challenged claim of the '908 patent, claim 5, depends from disclaimed independent claim 4. Independent claim 4 and dependent claim 5 are reproduced below.

> 4. A system, the system comprising:
> a processing system comprising
> a plurality of processors; and
> at least one separated cache not part any processor;
> a bus system connecting the processing system to one or more external devices;
> at least one interface transmitting data between the processing system and external devices via the bus system;
> at least some of the plurality of processors, the at least one interface, and the at least one separated cache having a module identification (ID); and wherein
> the at least one interface to transmit data via the bus system using a protocol, comprising:

i. the module ID of an interface, a processor, a separated cache requesting a transmission,
ii. the module ID of an interface, a processor, a separated cache receiving a transmission; and/or
iii. the address of a target within the interface, the processor, the separated cache or the external device unit receiving a train mission; and

wherein the at least one separated cache comprises a separated cache segment for at least some of the plurality of processors; the system further comprising:

an interconnect system interconnecting each of the separated cache segments with each of the processors, each of the processors with neighboring processors, and each of the separated cache segments with neighboring separated cache segments; and

an arbiter, the arbiter controlling access of a processor to the interconnect system.

5. The bus system of claim 4 where the arbiter is operable to allow processor access in chronological sequence.

Ex. 1001, 52:43–53:7.

E. Asserted Ground of Unpatentability

Petitioner asserts that the challenged claim is unpatentable on the following ground, which is the sole ground remaining before us:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
5	103(a)	Kabemoto, Bauman, Chaney

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claim challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish by a

preponderance of the evidence that the challenged claim is unpatentable. 35 U.S.C. § 316(e) (2018); 37 C.F.R. § 42.1(d) (2019).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR*, 550 U.S. at 406. The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness.[9] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. The Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quoting *Custom Accessories, Inc. v. Jeffrey–Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)).

Petitioner's declarant, Dr. Pinaki Mazumder, opines that "[a] person of ordinary skill in the art ('POSITA') at the time of the alleged invention would have had at least a[n] M.S. degree in electrical engineering, and at least three years of experience with processor design and memory

[9] The parties have not directed our attention to any objective evidence of obviousness or non-obviousness.

architecture." Ex. 1003 ¶ 66; *see* Pet. 12. Patent Owner's declarant, Dr. Murali Annavaram, for purposes of his declaration, adopts Dr. Mazumder's definition (with the understanding that the referenced master's degree in electrical engineering includes related fields such as computer engineering). Ex. 2024 ¶ 21.

We determine that the definition offered by Dr. Mazumder comports with the qualifications a person would have needed to understand and implement the teachings of the '908 patent and the prior art of record. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect an appropriate level of skill in the art). For purposes of this decision, we apply Dr. Mazumder's description of the person of ordinary skill in the art.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2019).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner does not propose an explicit claim construction for any term, asserting that every term should be given its ordinary and customary meaning. Pet. 5. Patent Owner similarly does not propose an explicit claim construction for any term. *See* PO Resp. *passim*. In their later respective briefs, the parties each argue that the other has, in the context of the Bauman reference, applied an incorrect construction for "interconnect system"—disputing whether a connection between processors must be direct and have data flowing between the processors in two directions. *See* Pet. Reply 17; PO Sur-reply 12–13.

Claim 4 recites "an interconnect system interconnecting each of the separated cache segments with each of the processors, each of the processors with neighboring processors, and each of the separated cache segments with neighboring separated cache segments." Ex. 1001, 52:66–53:3. The Federal Circuit determined that the three "interconnect system" limitations are not limited to direct connections but also encompass indirect connections. *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th at 1379 n.2 ("Even if the Board is right that Intel's proposed combination relied on Kabemoto's 'snoop bus 22' to teach the segment-to-segment limitation, Kabemoto's snoop bus 22 does so—just with indirect connections.").

We determine that no other claim terms require express construction.

D. The Alleged Obviousness of Claim 5 Over Kabemoto, Bauman, and Chaney

Petitioner alleges that dependent claim 5 of the '908 patent would have been obvious over Kabemoto, Bauman, and Chaney. *See* Pet. 58–63. Claim 5 depends from disclaimed independent claim 4 and, therefore, includes all of the limitations of that underlying independent claim. Petitioner's challenge to dependent claim 5 is premised on the contention

that underlying independent claim 4 would have been obvious over the combination of Kabemoto and Bauman. *See id.* at 19–58 (Petitioner's analysis of the limitations of independent claim 4). Petitioner relies on Kabemoto for much of the claimed subject matter, and contends that Bauman teaches, *inter alia*, a segmented second-level cache that is shared between processors. *See, e.g., id.* at 42. Petitioner relies on Chaney for teachings directed to the recitation of dependent claim 5, namely that regarding accessing in chronological sequence. *See id.* at 58–59.

In the Patent Owner Response and prior to the appeal, Patent Owner's arguments pertained to the limitation reciting "wherein the at least one separated cache comprises a separated cache segment for at least some of the plurality of processors" (identified as "element i" of claim 4) and the "interconnect system" limitation (identified as "element j"). *See* PO Resp. 14. Patent Owner argued that Petitioner had failed to establish that a person of ordinary skill in the art would have had a reason to combine Kabemoto and Bauman for element i or j. *See, e.g., id.* After appeal and on remand, Patent Owner did not make any further arguments. *See* Ex. 3001, 1 (The parties agreeing that "no additional briefing, submission of evidence, or oral argument is necessary to resolve the issues on remand.").

For the reasons discussed below and in light of the Federal Circuit's decision, we determine that Petitioner has shown that claim 5 would have been obvious over Kabemoto, Bauman, and Chaney.

1. Kabemoto (Ex. 1005)

Kabemoto addresses the difficulty, in conventional systems, of achieving high speed processing due to the maintenance of cache coherence. Kabemoto pertains to:

> a cache coherence apparatus for a multiprocessor system in which a plurality of processor modules are connected through a system bus [(external common bus)] and, more particularly, to a coherence apparatus for a cache of a multiprocessor system in which a plurality of processor elements with caches are connected in a processor module through a main storage and an internal common bus [(a snoop bus)].

Ex. 1005, 1:5–11; *id.* at 3:11–14.

Kabemoto's system has the following: several processor modules, each processor module having one or more processors and each processor provided with a cache unit; a main storage shared by the processor group and divided into local storages (each local storage being "distributed main storage"); and a memory control module. *Id.* at 2:66–3:40. "The distributed main storage and the cache unit are connected by a snoop bus (internal common bus) [and t]he processor modules are connected by a system bus (external common bus)." *Id.* at 3:11–14. "The cache unit divides the cache line into a plurality of sublines and manages the same." *Id.* at 3:41–42. Kabemoto's Figure 2 is reproduced below.

FIG. 2

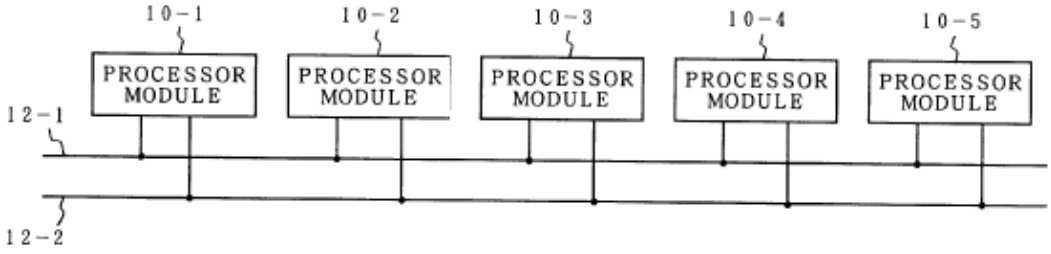


Figure 2 is a block diagram of a multiprocessor module construction of Kabemoto's system. *Id.* at 13:51–52. Figure 2 depicts five processor modules, 10-1 through 10-5, connected via system buses 12-1 and 12-2. *Id.* at 16:8–14. Figure 3 is reproduced below.

FIG. 3

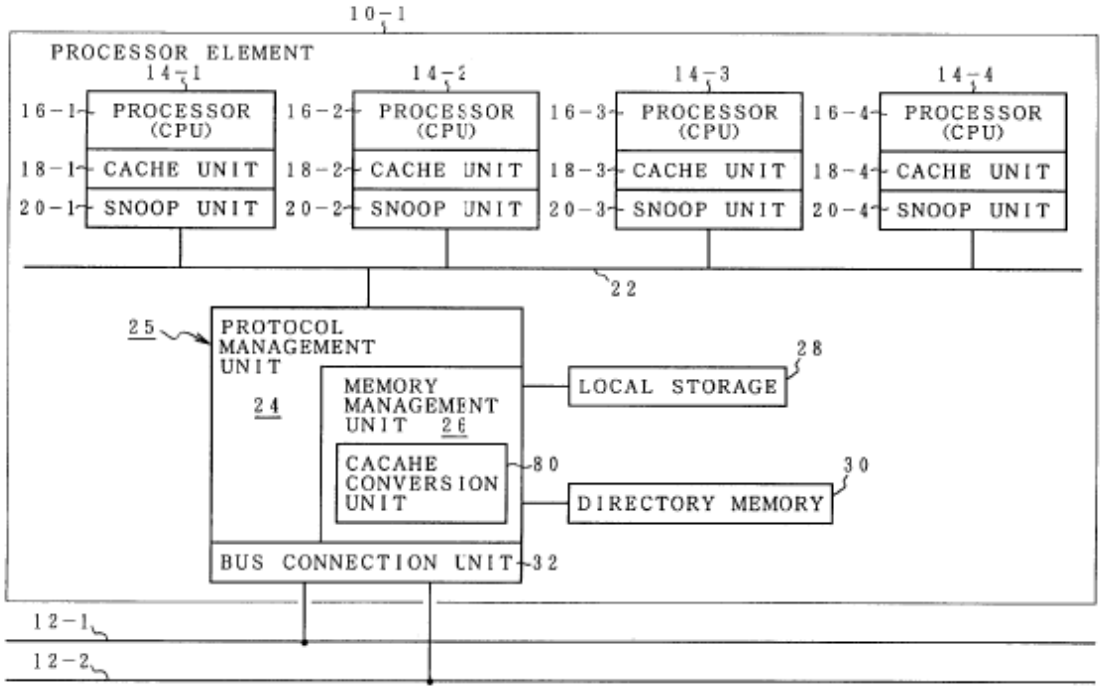
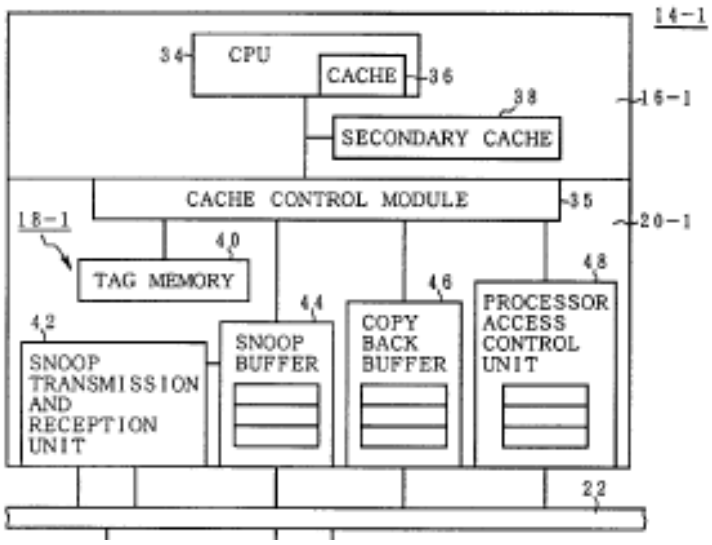


Figure 3 is a block diagram of an internal construction of a processor module of Figure 2. *Id.* at 13:53–54. Figure 3 depicts processor module 10-1 having four processor elements 14-1 to 14-4 connected through snoop bus 22. *Id.* at 16:14–18. Each processor element comprises a processor (central processing unit; "CPU"), a cache unit, and a snoop unit. *Id.* at 16:18–21. "To guarantee a coherence of data among the cache units 18-1 to 18-4 of, for example, the four processor elements 14-1 to 14-4 in FIG. 3 connected by the snoop bus 22, the secondary cache 38 is snooped by the snoop bus 22." *Id.* at 17:27–31.

A cropped version of Figure 4 is reproduced below.

FIG. 4



The figure above is a cropped version of Figure 4, which is a block diagram of an internal construction of the processor module of Figure 3. *Id.* at 13:55–56. Figure 4 depicts secondary cache 38 outside of CPU 34 and primary cache 36 of CPU 34. *Id.* at 17:4–12.

2. Bauman (Ex. 1007)

Bauman pertains to:

> cache architectures for data processing systems and more particularly to a shared memory multi-processor data processing system having a plurality of second-level caches, where each of the second-level is comprised of a separate instruction second-level cache and a separate operand second-level cache.

Ex. 1007, 1:18–23. Bauman discloses a system with eight Instruction Processors (IPs) and two Storage Controllers, with each Storage Controller coupled to four of the Instruction Processors. *Id.* at 4:25–51. Each Storage Controller has a Global SLC (second-level cache), with the two Global SLCs coupled to each other and with each Global SLC directly accessed by

four Instruction Processors and indirectly accessed by the other four Instruction Processors. *Id.* at 4:55–5:4. "[T]he second-level cache [is] divided into a plurality of segments [and e]ach of the segments is dedicated to caching a predetermined portion of addressable memory." *Id.* at 3:35–38.

Figure 1 is reproduced below.

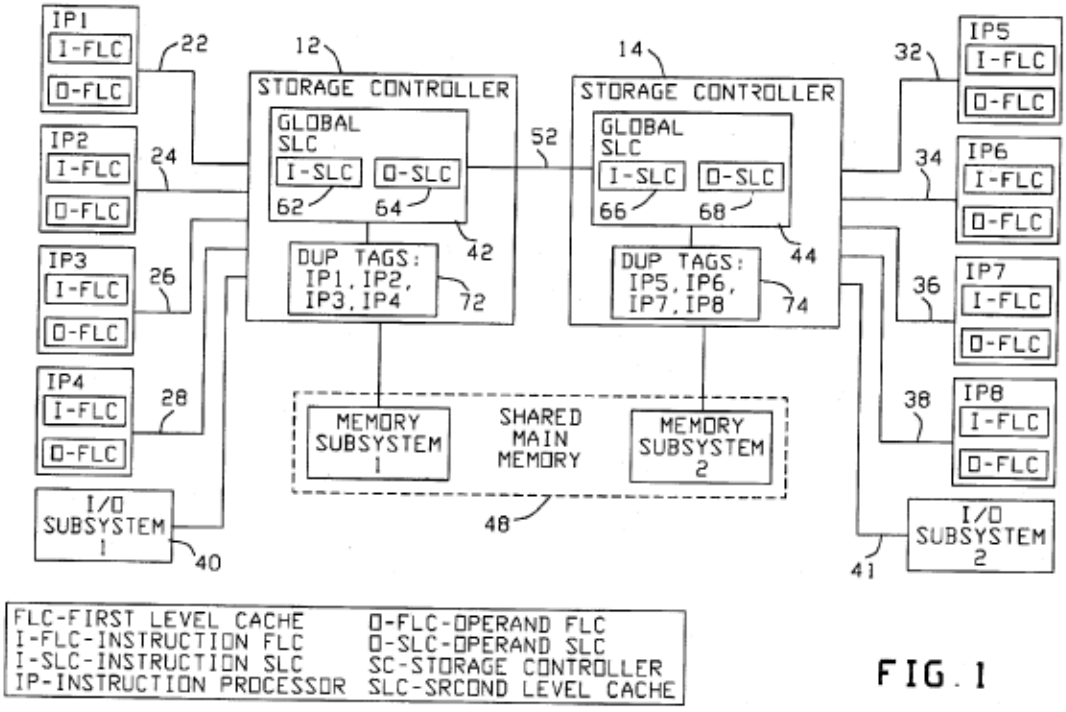


FIG. 1

Figure 1 is a block diagram of a multi-processor data processing system. *Id.* at 3:62–63. The figure shows, *inter alia*, four Instruction Processors, IP1 through IP4, coupled to Storage Controller 12, which has Global SLC 42, which, in turn, has dedicated Instruction Second-Level Cache (I-SLC) 62 and dedicated Operand Second-Level Cache (O-SLC) 64. *Id.* at 4:42–46, 4:56–57, 5:29–32. Bauman explains that "the instruction second-level cache and operand second-level cache tag cycles operate in tandem [and t]his simplifies maintaining cache coherency between the instruction and operand second-level caches." *Id.* at 14:27–31.

3. Chaney (Ex. 1008)

Chaney "pertains in general to multiprocessor computer systems and in particular to a method and system for maintaining cache coherency in such systems." Ex. 1008, 1:19–21. According to Chaney, "[i]n some multiprocessor systems, the caches are 'strongly ordered.'" *Id.* at 1:33–34. "In a strongly ordered system, a processor sees the stores of other processors in the same node in the same order in which the stores are made." *Id.* at 1:34–36; *see also id.* at 4:16–19. Chaney's system of maintaining strong ordering includes "[a]n arbitrator within the processor agent [that] receives the timestamps [for the memory transactions] and the memory transactions." *Id.* at code (57) (Abstract). "Using the timestamps, the arbitrator reorders the memory transactions and sends the transactions to the processors in the order in which the transactions were sent." *Id.*

4. Discussion

Because challenged claim 5 depends directly from independent claim 4 and therefore contains all of the limitations of the underlying independent claim, we first address below the parties' contentions regarding the limitations of independent claim 4 and then address the limitation added by dependent claim 5.

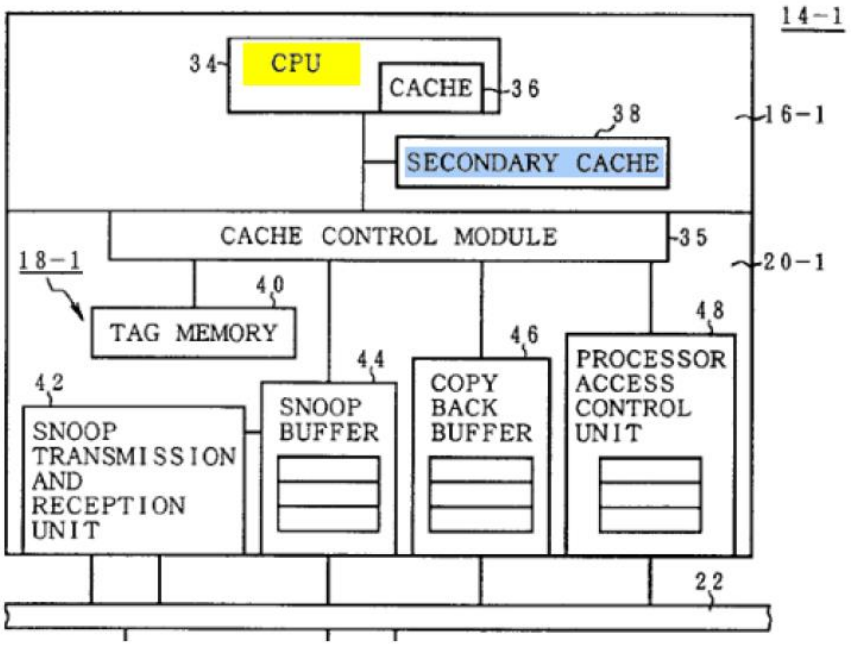
a. [Claim 4] "A system, the system comprising:"

Petitioner contends that Kabemoto discloses a system. Pet. 19 (citing Ex. 1005, 1:6–7, 2:61–65, 9:51–61, 12:63–13:1, 16:8–12, Figs. 2, 3). Kabemoto states that "[t]he invention relates to a cache coherence apparatus for a multiprocessor system." Ex. 1005, 1:6–7. Patent Owner does not raise any arguments regarding the preamble. We find, based on the arguments and evidence presented by Petitioner, that Kabemoto discloses a system.

b. *"a processing system comprising a plurality of processors; and at least one separated cache not part [of] any processor"*

Petitioner contends that Kabemoto discloses a multiprocessor system of a plurality of processor modules, each including a plurality of processors. *Id.* at 19–22 (citing, *inter alia*, Figs. 1–3); *see, e.g.*, *id.* at 20–21 (reproducing Kabemoto's Figure 2, which depicts five processor modules, and Figure 3, which depicts a processor element having four processors (CPUs)). Petitioner also contends that Kabemoto's secondary cache is part of the processing system while being separate from the CPUs. *Id.* at 22–23. Petitioner utilizes an annotated version of Figure 4, reproduced below, to support its position.

FIG. 4



Id. at 23. The figure above is a cropped version of Figure 4, which is a block diagram of an internal construction of a processor module, with Petitioner's annotation of CPU 34 in yellow and secondary cache 38 in blue. *Id.*; Ex. 1005, 13:55–56. Patent Owner does not raise any arguments

regarding these contentions. We find, based on the arguments and evidence presented by Petitioner, that Kabemoto teaches or suggests a processing system of a plurality of processors and a separated cache.

c. "a bus system connecting the processing system to one or more external devices"

Petitioner contends that Kabemoto discloses a bus system in the form of a "system bus (external common bus)." Pet. 23–25 (quoting Ex. 1005, 3:11–14). Petitioner further contends that "Kabemoto's bus system connects each processor module (which includes the claimed 'processing system') to one or more external storage devices via an I/O system." *Id.* at 23–24. According to Petitioner, "Kabemoto's processor modules . . . are connected to heterosystem 505 . . . through system bus 12 . . . , allowing communication with an I/O system," and that I/O system connects processing systems to external devices. *Id.* at 24–25 (citing Ex. 1003 ¶ 86; Ex. 1005, 38:52–54, 38:67–7:4, Fig. 39; Ex. 1009, 644–54). Patent Owner does not raise any arguments regarding these contentions. We find, based on the arguments and evidence presented by Petitioner, that Kabemoto teaches or suggests the "bus system" limitation.

d. "at least one interface transmitting data between the processing system and external devices via the bus system"

Petitioner contends that Kabemoto's bus connection unit 32 is the recited "interface." Pet. 25–28. By the use of an annotated version of Kabemoto's Figure 3, Petitioner contends that "Kabemoto teaches that 'bus connection unit 32 executes a bus access between the memory control module 25 and the system buses 12-1 and 12-2,'" and that, as shown in Figure 3, bus connection unit 32 is the interface for processor module 10-1. Pet. 25–26 (emphasis omitted) (quoting Ex. 1005, 16:52–55; citing *id.* at

10:59–62, 11:66–12:13, 16:48–50, 53:64–65, Fig. 3). Petitioner further contends that Figure 4 shows that bus connection unit 32 is an interface transmitting data between the processing system and external devices via the bus system 12, which is connected to an I/O system. *Id.* at 26–28 (citing Ex. 1005, 38:63–39:10, Figs. 4, 39; Ex. 1003 ¶¶ 92–93). Patent Owner does not raise any arguments regarding these contentions. We find, based on the arguments and evidence presented by Petitioner, that Kabemoto teaches or suggests the "interface" limitation.

e. "at least some of the plurality of processors, the at least one interface, and the at least one separated cache having a module identification (ID)"

Petitioner contends that Kabemoto's "unit ID," or "UID," corresponds to the recited "module identification." Pet. 28–31. Petitioner, referring to an annotated version of Figure 39, further contends that "Kabemoto's UIDs . . . 'are allocated to the modules or units which can be connected to the system bus 12' and 'unit IDs (UIDS) #0 to #4 are allocated to the processor modules 10-1 to 10-5.'" *Id.* at 30–31 (quoting Ex. 1005, 39:16–19; citing *id.* at 10:40–46, 21:17–43, Figs. 8, 39; Ex. 1003 ¶ 96). Petitioner contends that Kabemoto's processor module includes a plurality of CPUs, secondary caches, and a bus connection unit (mapped, respectively, to processors, separated cache, and interface). *Id.* at 28–29 (citing to and annotating Figure 3). Patent Owner does not raise any arguments regarding these contentions. We find, based on the arguments and evidence presented by Petitioner, that Kabemoto teaches or suggests the "module identification" limitation.

f. "wherein the at least one interface to transmit data via the bus system using a protocol, comprising:

i. the module ID of an interface, a processor, a separated cache requesting a transmission,

ii. the module ID of an interface, a processor, a separated cache receiving a transmission; and/or

iii. the address of a target within the interface, the processor, the separated cache or the external device unit receiving a [transmission]"

Petitioner contends that Kabemoto's bus connection unit, mapped to the recited "interface," transmits data by external system bus 12, mapped to the recited bus system, and that Kabemoto discloses examples of data transfer read and write requests, which Petitioner contends are protocols. Pet. 31 (citing Ex. 1005, 2:36–49, 19:52–56, 16:52–55; referring to Section VCI.C of the Petition); *see also id.* at 31–35 (discussing several purported protocols of Kabemoto).

Petitioner further contends that Kabemoto discloses protocols using the recited "module ID of an interface, a processor, a separated cache requesting a transmission." *Id.* at 35–37 (citing Ex. 1005, 9:67–10:15, 19:11–51, 44:36–45:41, Fig. 39; Ex. 1003 ¶¶ 112–113). Petitioner contends that Kabemoto also discloses protocols using the recited "module ID of an interface, a processor, a separated cache receiving a transmission." *Id.* at 38–39 (citing Ex. 1005, 10:3–6, 10:11–15, 19:11–51, 44:36–46:33, Fig. 48; Ex. 1003 ¶¶ 114–115). Petitioner contends that Kabemoto also discloses protocols using the recited "address of a target within the interface, the processor, the separated cache or the external device unit receiving a [transmission]." *Id.* at 39–41 (citing Ex. 1005, 4:29–36, 18:66–19:51, 29:45–55, 44:48–66, 45:42–46:33, Figs. 16, 48; Ex. 1003 ¶¶ 111–118).

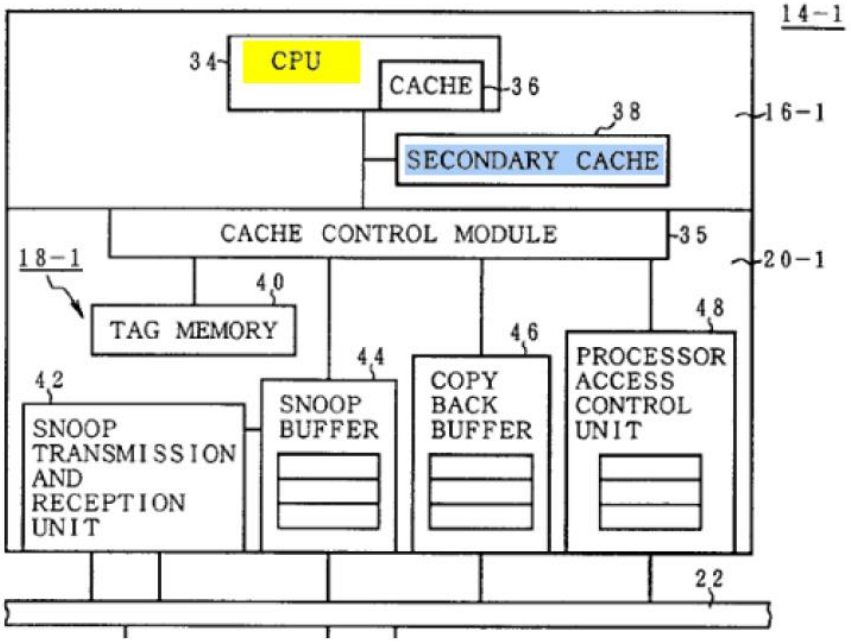
Patent Owner does not raise any arguments regarding these contentions. We determine, based on the arguments and evidence presented by Petitioner, that Kabemoto teaches or suggests the data transmission protocol limitations.

g. "wherein the at least one separated cache comprises a separated cache segment for at least some of the plurality of processors"

Petitioner contends that the combination of Kabemoto and Bauman teaches this limitation, which the parties identify as "element i." Pet. 41–50.

Petitioner contends that Kabemoto discloses a processor (CPU 34) and a separated cache (secondary cache 38), which is connected to the processor. *Id.* at 22–23, 41–42. Petitioner utilizes an annotated and cropped version of Kabemoto's Figure 4, reproduced below, which depicts this relationship for processor element 14-1. *See id.* at 23.

FIG. 4



Pet. 23. Above is Kabemoto's Figure 4, which is a block diagram of an internal construction of the processor module, with CPU 34 in yellow and

secondary cache 38 in blue. *See* Ex. 1005, 17:4–8. According to Petitioner, "Kabemoto discloses segmentation of its cache line to better manage the cache, as "[t]he cache unit divides the cache line into a plurality of sublines and manages the same." Pet. 41 (quoting Ex. 1005, 3:41–42). To address the "plurality of processors" aspect of the claim, Petitioner contends that the CPUs 34 in the four processor elements 14-1 through 14-4 are the recited "processors." *Id.* at 22. Petitioner turns to Bauman for the aspect of the limitation pertaining to a cache segment for some of the plurality of processors. *Id.* at 42.

Petitioner contends that Bauman discloses a separated cache, the global second-level cache (SLC), where there is a segment for a plurality of processors. *Id.* at 42–44. According to Petitioner, "Bauman discloses 'a second-level cache that is shared between the processors where the second-level cache also has a separate instruction cache and operand cache," and that the second-level cache comprises separate cache segments. *Id.* at 42–44 (quoting Ex. 1007, 1:56–63); *see also id.* at 43 (annotated version of Bauman's Figure 1 depicting a blue Global SCL directly provided for four yellow Instruction Processors (IPs)); *id.* at 43–44 (quoting Ex. 1007, 3:35–38 ("A further aspect of the invention has the second-level cache divided into a plurality of segments."). Using annotated figures and relying on the testimony of Dr. Mazumder, Petitioner explains its contentions as to how Bauman discloses cache segments "for at least some of the plurality of processers" as recited in independent claim 4. *Id.* at 44–47.

Petitioner proposes the modification of Kabemoto's system by the substitution of "Bauman's segmented global SLC in place of the secondary cache of Kabemoto's processor module." Pet. 48.

> Within each of Kabemoto's processor modules (which each contain a "processing system"), Bauman's segmented global SLC replaces Kabemoto's secondary caches and is connected to snoop bus 22 on the outside of element 14-1. Rather than four secondary caches housed in four different elements, Kabemoto's processing system would use a single second-level cache divided into four segments. *See id.*, ¶135.

Id. at 54.

Petitioner contends, *inter alia*, that "the combination of Kabemoto and Bauman represents the use of known techniques to improve similar devices in the same way." Pet. 48. Petitioner contends that the two references "address the same problem: maintaining cache coherency even when multiple processors request access to memory." *Id.* (citing Ex. 1003 ¶ 125; Ex. 1005, 2:11–25; Ex. 1007, 5:55–6:14). Petitioner further contends that, "[b]ased on the similar components and structures of the references and the common nature of the problem to be solved, a [person of ordinary skill in the art] would have naturally turned to Bauman's segmented second-level cache to use as the secondary cache in Kabemoto," and that "[f]or similar reasons, this combination would have yielded predictable results." *Id.* at 48–49 (citing Ex. 1003 ¶ 125); *see also* Pet. Reply 3 ("both references use similar techniques to address the same problem: maintaining cache coherency in multiprocessor systems when multiple processors request access to memory." Pet. Reply 3 (citations omitted)). In support, Dr. Mazumder testifies that:

> Based on the similarities between the devices of Kabemoto and Bauman and the problems presented, a [person of ordinary skill in the art] would have naturally been motivated to use Bauman's segmented global SLC in place of Kabemoto's secondary cache. A [person of ordinary skill in the art] would have expected the predictable result that Kabemoto's processing system would comprise one global secondary cache

> with several cache segments rather than several distributed secondary caches.

Ex. 1003 ¶ 125. Petitioner, in the Reply, reiterates its position that, "[g]iven that both references teach the use of known techniques to improve similar devices in the same way—dividing caches into portions and maintaining separate coherence states for each portion that can be updated individually—a POSITA would have been motivated to combine their teachings." Pet. Reply 10 (citations omitted).

During the trial, Patent Owner asserted that Petitioner has failed to satisfy its burden of establishing a reason to combine the references as proposed. *See, e.g.*, PO Resp. 14, 18; PO Sur-reply 4–11. Patent Owner argued, *inter alia*, that "Kabemoto's system already provides a solution to the purported problem, by using its snoop bus to maintain cache coherency," and that "Petitioner does not explain how Kabemoto and Bauman improve similar devices in the same way." PO Resp. 19, 21 (citing Ex. 2024 ¶¶ 43–44; Ex. 1005, 17:27–30)). Patent Owner further argued that "Petitioner does not explain why [a person of ordinary skill in the art] would be motivated to replace Kabemoto's solution to the problem of cache coherency with Bauman's, or even that Bauman's solution is appropriate or beneficial for Kabemoto's particular system." *Id.* at 19; *see id.* at 21–22 ("Petitioner does not explain why [a person of ordinary skill in the art] would be motivated to apply Bauman's improvements . . . to the system of Kabemoto, or reasonably expect the modification to be successful within Kabemoto's system." (citing Ex. 2024 ¶ 44)).

On appeal, the Federal Circuit resolved the foregoing dispute, determining that Petitioner has sufficiently shown a motivation to combine Kabemoto and Bauman. The court's decision states:

> That Kabemoto and Bauman address the same problem and that Bauman's cache was a known way to address that problem is precisely the reason that there's a motivation to combine under *KSR* and our precedent. . . .
>
> [H]ere, there's no dispute that using a global, segmented secondary cache "has been used to improve" cache coherency in multiprocessor systems—as in Bauman—and a person of ordinary skill would "recognize that" such a cache "would improve similar" multiprocessor systems—like the one in Kabemoto—by addressing that same cache coherency problem. . . . There's . . . also no dispute that such a combination would constitute a use of Bauman's secondary cache "according to [its] established function[ ]." . . .
>
> And contrary to the Board's suggestion, Intel never had to show that replacing Kabemoto's secondary cache with Bauman's secondary cache was an "improvement" in a categorical sense. . . . Intel just had to show that Bauman's secondary cache was a "suitable option" to replace Kabemoto's secondary cache. . . .
>
> It's enough for [Petitioner] Intel to show that there was a known problem of cache coherency in the art, that Bauman's secondary cache helped address that issue, and that combining the teachings of Kabemoto and Bauman wasn't beyond the skill of an ordinary artisan. Nothing more is required to show a motivation to combine under *KSR*, so we reverse the Board's finding to the contrary.

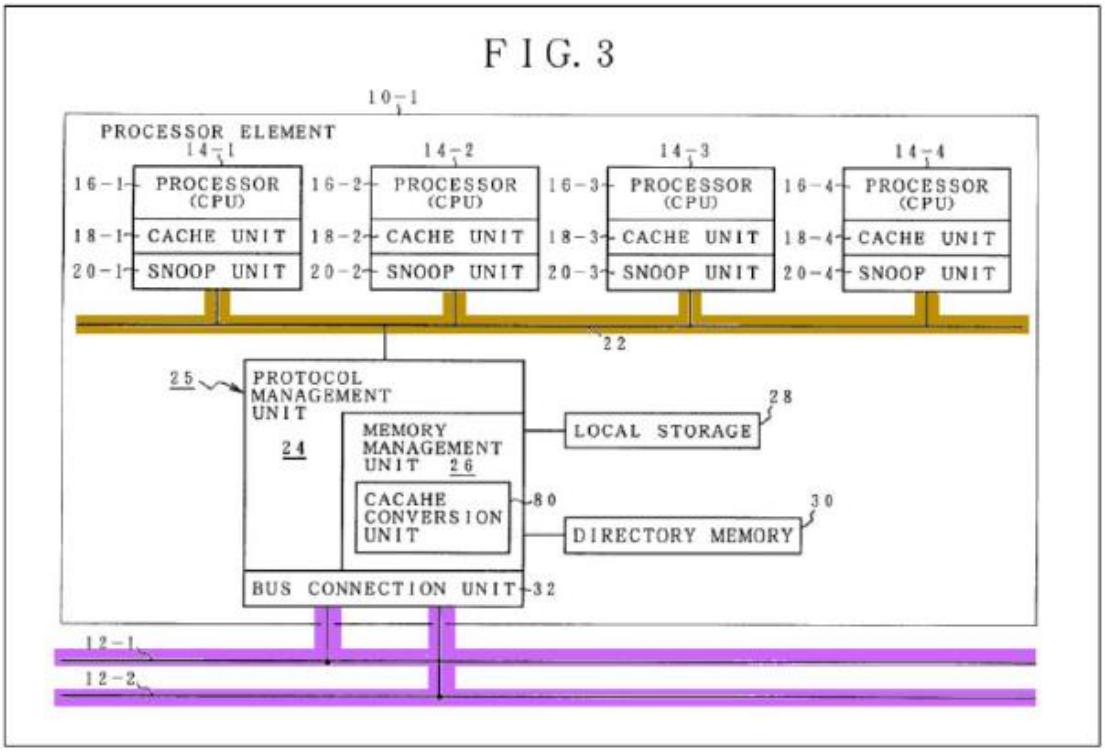
Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th at 1380–1381 (citing *KSR*, 550 U.S. at 417; *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 799–800 (Fed. Cir. 2021)).

We determine, based on the arguments and evidence presented by Petitioner and in light of the Federal Circuit's decision, that the combination of Kabemoto and Bauman teaches or suggests the recited "separated cache segment for at least some of the plurality of processors" and that Petitioner has provided adequate reasoning as to why one of ordinary skill in the art

would have made the proposed combination and has provided adequate evidence to show that a person of ordinary skill in the art would have had a reasonable expectation of success in doing so.

h. "an interconnect system interconnecting each of the separated cache segments with each of the processors, each of the processors with neighboring processors, and each of the separated cache segments with neighboring separated cache segments"

Petitioner contends that the combination of Kabemoto and Bauman teaches this "interconnect system" limitation, which the parties identify as "element j." Pet. 50. Petitioner begins with the contention that "Kabemoto teaches a modular processing system where, within a module, all processors (CPUs) and secondary caches are interconnected by an interconnection system, namely, an internal snoop bus." *Id.* at 50. Petitioner's annotated version of Kabemoto's Figure 3 is reproduced below.

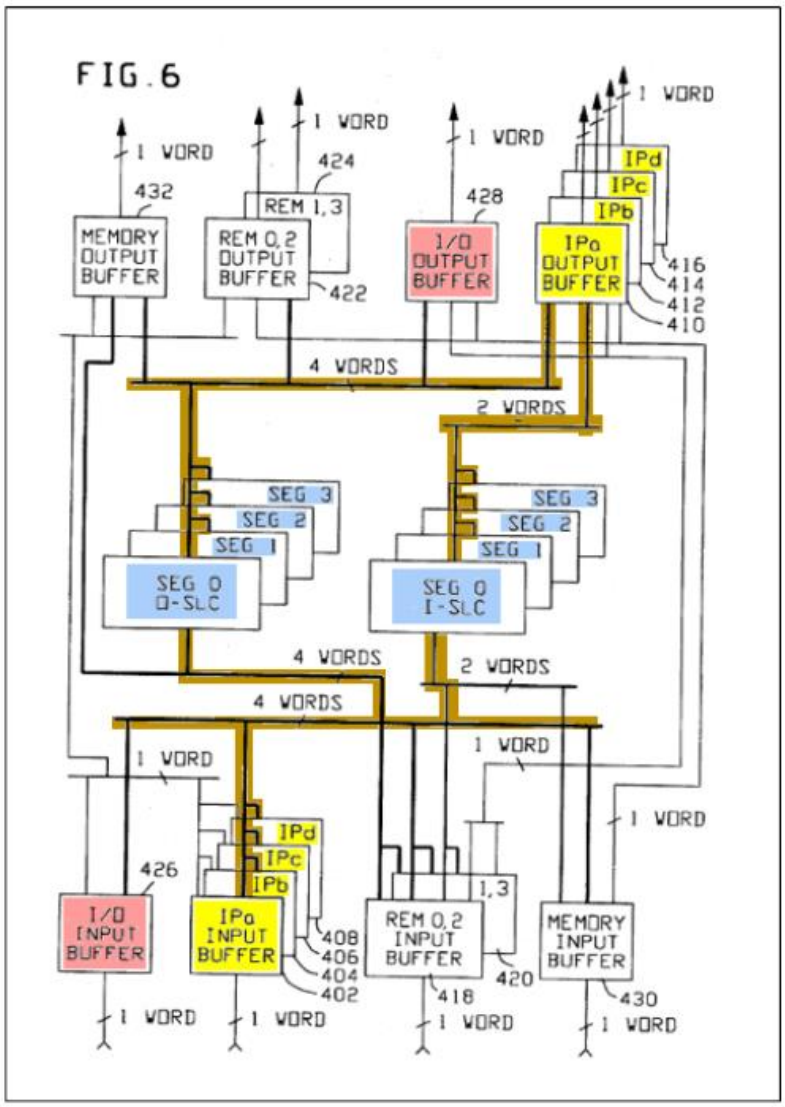


Above is Kabemoto's Figure 3—a block diagram of an internal construction of a processor module—with, *inter alia*, Petitioner's highlighting in gold of snoop bus 22. Pet. 51; Ex. 1005, 13:53–54. Petitioner contends that snoop bus 22 interconnects the four processors located in each of processor elements 14-1 through 14-4. Pet. 51. Petitioner continues:

> Similarly, processor module 10-1 contains four separated caches (secondary cache 38) housed in elements 14-1 through 14-4. *See supra* Section X.A.1.c; *see also* Ex. 1005, FIGS. 3, 4. Because each processor element 14-1 through 14-4 is connected to each neighboring processor element by virtue of snoop bus 22, snoop bus 22 interconnects each separated cache with each neighboring cache. Ex. 1003, ¶130. Likewise, snoop bus 22 interconnects each separated cache with each processor. *Id.*, ¶131.

Id. at 52. Thus, Petitioner contends that the snoop bus is a cache-to-cache interconnection. Because the claim requires a structure that interconnects neighboring cache *segments*, not simply neighboring caches, Petitioner turns to Bauman.

Petitioner's annotated version of Bauman's Figure 6 is reproduced below.



Above is Figure 6 of Bauman, "a block diagram that illustrates the data path between the requesting processors, the second-level cache, and the memory" (Ex. 1007, 11:18–20), with Petitioner's addition of highlighting of certain features. Pet. 53. Petitioner contends that Bauman's Figure 6 discloses processors (yellow), cache segments (blue), and data paths (gold), and that the gold data paths satisfy the three relationships of the "interconnect system" limitation. *Id.* at 53–54. In that regard, Petitioner contends that "Bauman teaches a system in which cache segments are each interconnected to several processors such that data requests from any processor can be made

to any of the cache segments," and that "[t]hese data paths are shown below in gold in Bauman's Figure 6." *Id.* at 52–53 (citing Ex. 1007, 11:18–20, 11:27–40, Fig. 6); *see also id.* at 53 ("[E]ach cache segment (blue) is interconnected to each instruction processor (yellow) via the data paths (gold)."). Petitioner also contends that "each of the cache segments is interconnected to each neighboring cache segment via the data paths." *Id.* at 54 (citing Ex. 1003 ¶¶ 133–134).

Petitioner's proposed combination utilizes Kabemoto's processors and snoop bus (mapped to the recited "interconnection system"), and uses, from Bauman, the segmented global SLC. *See* Pet. 54; *see also, e.g.*, *id.* ("A POSA would have been motivated to use Bauman's segmented global SLC with Kabemoto's internal snoop bus ('interconnect system')."). Petitioner, in articulating the proposed combination, explains that "Bauman's segmented global SLC [(second-level cache)] replaces Kabemoto's secondary caches and is connected to snoop bus 22 on the outside of element 14-1." *Id.* Thus, "[r]ather than four secondary caches housed in four different elements, Kabemoto's processing system [in the proposed combination] would use a single second-level cache divided into four segments." *Id.* (citing Ex. 1003 ¶ 135).

Petitioner contends that a person of ordinary skill in the art would have been motivated to make the proposed combination for the reasons previously given in the context of element i ("a separated cache segment for at least some of the plurality of processors"). Pet. 54 (referencing Section X.A.1.i of the Petition; citing Ex. 1005, 17:26–31; Ex. 1003 ¶ 136). Petitioner further contends that a person of ordinary skill in the art "would have been specifically motivated to make this combination because, as

Bauman teaches, segmenting the global cache 'simplifies maintaining cache coherency between the instruction and operand second-level caches.'" *Id.* (citing Ex. 1007, 14:28–31). According to Petitioner, a person of ordinary skill in the art "would have further understood that Kabemoto's internal snoop bus ('interconnect system') would maintain cache coherence among the various cache segments and the primary caches embedded within each CPU 34 (the claimed 'processor')." *Id.* (citing Ex. 1005, 17:26–31; Ex. 1003 ¶ 136).

During the trial, Patent Owner argued that "Petitioner fails to establish a motivation to combine Kabemoto with Bauman for element j [the "interconnect system" limitation]." PO Resp. 25 (section heading); *see also id.* at 29–32 (Patent Owner arguing, *inter alia*, that "Petitioner points to the reasons to combine offered in connection with element i, but these have been rebutted above."); *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th at 1377 ("[Patent Owner] PACT did not dispute that the combination of Kabemoto and Bauman taught each limitation of claim 4; PACT only argued that Intel failed to demonstrate a motivation to combine Kabemoto and Bauman.").

We agree with Petitioner that Kabemoto's snoop bus interconnects neighboring processors and interconnects the secondary caches with each other and with the processors. *See, e.g.*, Ex. 1005, Figs. 3, 4; Ex. 1003 ¶¶ 129–131. When, as Petitioner proposes, "Bauman's segmented global SLC [(second-level cache)] replaces Kabemoto's secondary caches and is connected to snoop bus 22 on the outside of element 14-1," the snoop bus interconnects cache segments with each other and with the processors as recited in claim 4. *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th at 1379 n.2 ("Even if the Board is right that Intel's proposed combination

relied on Kabemoto's 'snoop bus 22' to teach the segment-to-segment limitation, Kabemoto's snoop bus 22 does so—just with indirect connections. Should there be only one connection from the whole of Bauman's global secondary cache to Kabemoto's snoop bus 22, . . . each of the segments in that secondary cache would still be connected to each other through their shared singular connection to the snoop bus."). And, as discussed above, the Federal Circuit's decision resolved the remaining dispute, determining that Petitioner has demonstrated a motivation to combine Kabemoto and Bauman. *See id.* at 1380–1381.

We determine, based on the arguments and evidence presented by Petitioner and in light of the Federal Circuit's decision, that the combination of Kabemoto and Bauman teaches or suggests the "interconnect system" limitation and that Petitioner has provided adequate reasoning as to why one of ordinary skill in the art would have made the proposed combination and has provided adequate evidence to show that a person of ordinary skill in the art would have had a reasonable expectation of success in doing so.

i. "an arbiter, the arbiter controlling access of a processor to the interconnect system"

Petitioner contends that Kabemoto's processor access unit 48, provided for each processor, is an arbiter, and that a person of ordinary skill in the art "would have understood that processor access unit 48 arbitrates for access to snoop bus 22 on behalf of its associated processor," and, thus, controls access of a processor to the internal snoop bus (mapped to the "interconnect system"). Pet. 55–56 (citing Ex. 1005, 17:27–36, Fig. 4; Ex. 1003 ¶¶ 137–139). Petitioner also contends that Kabemoto discloses an arbiter controlling processors' access to system bus 12 and that an ordinary artisan "would have understood that within Kabemoto's processor module, a

similar arbiter can be used to control access of multiple CPUs (the claimed 'processors') to a shared bus, namely, internal snoop bus 22 ('interconnect system'),'' and that this would yield predictable results. *Id.* at 57–58 (citing Ex. 1003 ¶¶ 140–141).

Patent Owner does not raise any arguments regarding these contentions. We determine, based on the arguments and evidence presented by Petitioner, that Kabemoto teaches or suggests the recited arbiter that is "controlling access of a processor to the interconnect system."

j. [Claim 5] "The bus system of claim 4 where the arbiter is operable to allow processor access in chronological sequence."

Petitioner contends that Chaney, like the system described in the specification of the challenged '908 patent, uses time stamps for chronological sequencing. Pet. 58 (citing Ex. 1001, 39:48–41:29, 46:27–36, 47:5–8, 48:1–8; Ex. 1003 ¶ 143). The Specification of the '908 patent indicates that the use of time stamps for chronological reading is conventional. *See* Ex. 1001, 47:5–8 ("According to a conventional method . . . , the chronologically correct data word is selected when reading on the basis of the associated time stamp stored . . . with it."). Petitioner contends that "Chaney similarly teaches a multiprocessor system that uses time stamps to maintain 'strong order[ing],' meaning that 'a processor sees the stores of other processors . . . in the same order in which the stores are made.'' Pet. 58 (emphasis omitted) (citing Ex. 1008, 1:33–36, 3:7–10, 4:17–20). Petitioner further contends that, "[i]n the case where multiple transactions are requested, Chaney teaches that '[a]rbitrator 400 controls the order in which the transactions . . . are sent to the processors,'" and that is in

the order that the transactions were sent. *Id.* at 59 (quoting Ex. 1008, 5:54–55; citing, *inter alia*, Ex. 1003 ¶ 144).

Petitioner contends that a person of ordinary skill in the art "would have been motivated to use Chaney's arbitrator 400 in place of Kabemoto's arbiter (processor access unit 48)," and that the proposed combination "represents the use of known techniques to improve similar devices in the same way." *Id.* at 59–61 (citing, *inter alia*, Ex. 1003 ¶¶ 145–146). Petitioner also contends that the proposed combination would have yielded predictable results due to the structures and nature of the problems to be solved common to the references. *Id.* at 61 (citing Ex. 1003 ¶ 146).

Petitioner further contends that Chaney provides a reason to combine the references' teachings, asserting that Chaney discloses certain benefits of the use of its arbitrator, and that a person of ordinary skill in the art "would have been motivated to combine the teachings of Kabemoto, Bauman, and Chaney specifically to improve the reliability and speed of Kabemoto's processing system with a reasonable expectation of success." *Id.* at 61–62 (citing Ex. 1003 ¶¶ 147–148). Lastly, Petitioner contends that the proposed combination would have been a simple substitution having predictable results. *Id.* at 62–63 ("[A person of ordinary skill in the art] would have easily substituted Kabemoto's processor access unit with Chaney's strongly ordered arbitrator, with the predictable result that Kabemoto's system would maintain strong ordering.") (citing Ex. 1003 ¶ 149); *see, e.g.*, Ex. 1003 ¶¶ 145–146 (Dr. Mazumder testifying that, "because Kabemoto, Bauman, and Chaney disclose several common structures and architectures, and because they share the same problem to be solved, a [person of ordinary skill in the art] . . . would have expected the predictable result [of using Chaney's

arbitrator in Kabemoto's processor modules (as modified by Bauman)] that Kabemoto's processor module would maintain strong ordering."); *id.* at ¶¶ 147–149.

Patent Owner does not raise any separate arguments regarding these contentions directed to the limitation added by dependent claim 5, instead relying on its arguments, which we have addressed above, concerning the underlying independent claim 4. *See* PO Resp. 32–33 ("[T]he additional disclosure of Chaney does not cure the defects in Petitioner's analysis of claim 4."); *see also Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th at 1381 ("[Patent Owner] PACT did not dispute that Chaney taught this added 'chronological sequence' limitation [of claim 5].").

We determine, based on the arguments and evidence presented by Petitioner and in light of the Federal Circuit's decision, that the combination of Kabemoto, Bauman, and Chaney teaches or suggests that "the arbiter is operable to allow processor access in chronological sequence," as recited in dependent claim 5. For example, we find, based on Petitioner's relied-on teachings of Chaney's arbitrator 400 sending transactions to the processors in the order that the transitions were sent, that Cheney suggests that access is allowed in chronological sequence. We also determine that Petitioner has provided adequate reasoning as to why one of ordinary skill in the art would have made the proposed combination and has provided adequate evidence to show that a person of ordinary skill in the art would have had a reasonable expectation of success in doing so.

5. Conclusion as to Petitioner's Challenge Based on Kabemoto, Bauman, and Chaney

Based on the foregoing, Petitioner has established by a preponderance of the evidence that dependent claim 5 is unpatentable over the combination of Kabemoto, Bauman, and Chaney.

III. CONCLUSION[10]

We determine, in view of the Federal Circuit's decision and the record previously developed during trial, that Petitioner has demonstrated by a preponderance of the evidence that claim 5 of the '908 patent is unpatentable over Kabemoto, Bauman, and Chaney. As mentioned, Petitioner did not appeal our determination in the Final Decision that Petitioner has not demonstrated that claim 5 is unpatentable over Wu, Bauman, and Chaney. Ex. 3001, 1. Thus, that aspect of our prior decision stands and was not addressed in this remand decision.

The table below summarizes our conclusion on remand:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
5	103(a)	Kabemoto, Bauman, Chaney	5	

[10] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), (b)(2).

IV. ORDER

For the foregoing reasons, it is hereby:

ORDERED that claim 5 of the '908 patent has been proven to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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