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Paper 38
Date: August 9, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00525
Patent 8,819,505 B2

Before KEN B. BARRETT, CHARLES J. BOUDREAU, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Challenged Claim Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Intel Corporation ("Petitioner")[1] filed a Petition requesting *inter partes* review of U.S. Patent No. 8,819,505 B2 ("the '505 patent," Ex. 1003). Paper 2 ("Pet."). The Petition challenges the patentability of claim 5[2] of the '505 patent. PACT XPP Schweiz AG ("Patent Owner")[3] filed a Response to the Petition. Paper 20 ("PO Resp."). Petitioner filed a Reply (Paper 23, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 29, "PO Sur-reply"). With our authorization, Patent Owner filed, after its Sur-reply and prior to the final hearing, a copy of *Raytheon Technologies Corp. v. General Electric Co.*, 993 F.3d 1374, 2021 WL 1432964 (Fed. Cir. Apr. 16, 2021). Ex. 2039.

An oral hearing was held on May 20, 2021, and a transcript of the hearing is included in the record. Paper 37 ("Tr.").

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons discussed below, we determine that Petitioner has shown by

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[1] Petitioner identifies Intel Corporation as the real party-in-interest. Pet. 1.
[2] The Petition also has grounds directed to claims 1, 3, 7, 8, 12–18, and 27. However, because those claims have been statutorily disclaimed by Patent Owner, they are treated as if they never were part of the '505 patent. *See* Ex. 2002, 10; *see also* Paper 12, 14–15 (discussion of the status of those disclaimed claims in the Decision Granting Institution). We do *not*, as Petitioner urges, treat the disclaimer of twelve of the challenged claims as Patent Owner "tacitly acknowledging their invalidity." Pet. Reply 1 (Petitioner presenting this argument without citation to supporting authority or to evidence of intent to concede unpatentability).
[3] Patent Owner identifies PACT XPP Schweiz AG (formerly known as Scientia Sol Mentis AG) as the real party-in-interest. Paper 4, 1.

a preponderance of the evidence that claim 5 of the '505 patent is unpatentable.

B. Related Proceedings

One or both parties identify the following as matters involving or related to the '505 patent: *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00267 (D. Del. Feb. 7, 2019); *PACT XPP Schweiz AG v. Intel Corp.*, No. 19-cv-00273 (W.D. Tex. Apr. 23, 2019); *Intel Corp. v. PACT XPP Schweiz AG*, No. 19-cv-02241 (N.D. Cal. Apr. 25, 2019); and *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-01006 (D. Del. May 30, 2019). Pet. 1; Paper 4, 1–2; Paper 9.

C. The '505 Patent

The '505 patent is titled "Data Processor Having Disabled Cores." Ex. 1003, code (54). According to the Abstract, the '505 patent pertains to "[a] data processor having a plurality of data processing cores configured to disable cores found defective by a self-test." *Id.* at code (57). According to the patent,

> [t]he computing power of [certain] processors increases with the number of arithmetic [and] logic units present. Therefore, an attempt is made to integrate as many arithmetic and logic units as possible on one chip, which increases the area required. With an increase in area, there is also a higher probability of a chip having a manufacturing defect making it useless.

Id. at 1:26–32. Testing may be done to detect faults. *Id.* at 2:39–40.

The '505 patent identifies its improvement as making "it . . . possible to replace defective cells by functional cells . . . and thus reduce rejects." *Id.* at 2:14–17. "A cell can be replaced either by the test systems at the time of manufacture of the chips or even by the user in the completely assembled

system." *Id.* at 2:17–19. "All the tests and repair can be performed during operation of the chips." *Id.* at 2:24–25.

"Test vectors can be generated according to the BIST principle within the chip, or outside the unit according to a new method to save on space and costs." *Id.* at 2:19–22. "BIST" is a "[t]raditional known method[]," and refers to "built-in self-test." *Id.* at 1:43, 1:65; *see also id.* at 5:17–19 ("BIST methods according to the related art usually perform the self-test only during the chip RESET phase, i.e., shortly after applying a voltage (when turned on).").

D. The Challenged Claim

The sole remaining challenged claim of the '505 patent, claim 5, depends from disclaimed independent claim 1. Independent claim 1 and dependent claim 5 are reproduced below with emphasis added.

> 1. An Integrated Circuit Data Processor, comprising:
> data processing cores being arranged in an array;
> a plurality of the data processing cores comprising at least one Arithmetic and Logic Unit; and
> wherein the integrated circuit is operative to:
> *perform at least a self-test on the plurality of data processing cores* comprising at least one Arithmetic and Logic Unit; and
> *disable data processing cores found by the self-test to be defective*.
>
> 5. The Integrated Circuit Data Processor [according] to claim 1, *wherein the defective data processing cores are detected in the field*.

Ex. 1003, 13:19–28, 13:39–41 (emphasis added).

E. Evidence

Petitioner relies on the following references:

Reference	Exhibit No.
Peter Ivey, *The ELSA Wafer Scale Integration Project*, IEEE TRANSACTIONS ON COMPONENTS, HYBRIDS, AND MANUFACTURING TECHNOLOGY, Vol. 16, No. 7 (1993) ("Ivey")	1006
Michael Campbell et al., *Hierarchical Fault Tolerance for 3D Microelectronics*, 1990 INTERNATIONAL CONFERENCE ON WAFER SCALE INTEGRATION (Copyright 1990) ("Campbell")	1008

Petitioner also relies on the Declaration of Dr. Paul Franzon (Ex. 1001) and the Second Declaration of Dr. Paul Franzon (Ex. 1050) in support of its arguments, and Patent Owner relies on the Declaration of Dr. Andrew Wolfe (Ex. 2032) in support of its arguments. The parties rely on other exhibits as discussed below.

F. Asserted Ground of Unpatentability

Petitioner asserts that the challenged claim is unpatentable on the following ground:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
5	103(a)	Ivey, Campbell

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claim challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish by a preponderance of the evidence that the challenged claim is unpatentable. 35 U.S.C. § 316(e) (2018); 37 C.F.R. § 42.1(d) (2019).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness.[4] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. The Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (internal quotation marks and citation omitted).

Petitioner, relying on its expert's testimony, asserts: "A person having ordinary skill in the art ('POSA') at the time of the alleged invention would have had at least a[n] M.S. degree in electrical engineering (or equivalent experience) and at least one year of experience with IC [(integrated circuit)] defect tolerance and redundancy techniques." Pet. 14 (citing Ex. 1001 ¶¶ 48–49). Patent Owner does not disagree or propose a different definition of the person of ordinary skill in the art. *Cf.* PO Resp. 22

[4] The parties have not directed our attention to any objective evidence of obviousness or non-obviousness.

(Patent Owner presenting arguments based on Petitioner's definition of a person of ordinary skill in the art). Patent Owner's expert, Dr. Wolfe, applies Petitioner's definition for purposes of his opinion testimony. Ex. 2032 ¶ 24.

We determine that the definition offered by Petitioner comports with the technical level of the '505 patent and the prior art of record. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect an appropriate level of skill in the art). We apply Petitioner's description of the person of ordinary skill in the art.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2019).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

1. The Preamble

Independent claim 1 begins with the recitation "An Integrated Circuit Data Processor, comprising . . . ." Ex. 1003, 13:19. Similarly, dependent

claim 5 recites, "The Integrated Circuit Data Processor [according] to claim 1, wherein . . . ." *Id.* at 13:39–40. The U.S. District Court for the District of Delaware, in parallel litigation, adopted the parties' agreed-upon construction that these preamble phrases are limiting and mean: "All claimed components must exist on a single, integrated circuit." Ex. 2031, 3; *see id.* at 2–3 (the parties' agreement explicitly stating that preambles of other claims are *not* limiting). To the extent necessary for purposes of this decision, we adopt and apply that same understanding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (explaining that only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co*., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

2. In the Field

Dependent claim 5 recites, in its entirety, "The Integrated Circuit Data Processor [according] to claim 1, wherein the defective data processing cores are detected *in the field*." Ex. 1003, 13:39–41 (emphasis added).

Petitioner, in applying Campbell to the challenged claim, contends that "in the field" encompasses detecting defective cores during operation of the computer after assembly (*e.g.*, checking for faults at system start-up). Pet. 34. Petitioner (*id.* at 34–35), in support of its implied construction, directs our attention to the portions of the Specification stating:

> 2.1.7. Checking the Function During Operation
> BIST [(built-in self-test)] methods according to the related art usually perform the self-test only during the chip RESET phase, i.e., shortly after applying a voltage (when turned on). In contrast with that, it is possible or practical to

> perform the methods described here on the chips while the programs are running.

Ex. 1003, 5:16–21.

Patent Owner similarly contends that "in the field" means "under normal operating conditions as opposed to in a laboratory or factory" and "after assembly." PO Resp. 3–4 (citing Exs. 2004, 2005 (dictionaries)); PO Sur-reply 5. Patent Owner confirms that its proposed construction is substantively the same as Petitioner's. PO Resp. 3 ("This understanding of the term 'in the field,' i.e., under the normal operation condition, is also what Petitioner uses in the Petition."); PO Sur-reply 5 ("[I]t is undisputed that 'in the field' in claim 5 means 'after assembly.'"). Patent Owner (PO Sur-reply 6) directs our attention to the Specification's statement: "A cell can be replaced either by the test systems at the time of manufacture of the chips or even by the user in the completely assembled system." Ex. 1003, 2:17–19. Although this provision pertains to replacing a chip—and, thus, is more directly related to the "disable" limitation of independent claim 1 rather than detecting a defective core in dependent claim 5—we find this to be helpful evidence indicating that an activity "in the field" is distinct from an activity in the manufacturing environment, and that "in the field" encompasses testing of an assembled system.

We apply, in this decision, the parties' agreed-upon construction of "in the field" as meaning during operation after assembly.

D. The Alleged Obviousness of Dependent Claim 5 over Ivey and Campbell

Petitioner alleges that dependent claim 5 of the '505 patent would have been obvious over Ivey and Campbell. *See* Pet. 34–35; *see also id.* at 18–23 (Petitioner's analysis of the limitations of underlying independent claim 1). Claim 5 depends from disclaimed independent claim 1 and,

therefore, includes all of the limitations of that underlying independent claim.

Petitioner contends that Ivey teaches or suggests the subject matter of the underlying independent claim 1, and turns to Campbell in addressing the limitation added by dependent claim 5—that pertaining to detecting defective cores in the field.[5] *See* Pet. 18–23, 34–35.

Patent Owner argues that Petitioner has failed to establish a reason why a person of ordinary skill in the art would have combined the references' teachings and has failed to show that there would have been a reasonable expectation of success. PO Resp. 16. Patent Owner further argues that Petitioner has not proven that Campbell is a prior art publication. *Id.* at 52.

1. Overview of Ivey (Ex. 1006)

Ivey discloses a research project called ELSA (European Large SIMD[6] Array), which was part a Wafer Scale Integration ("WSI") project.

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[5] We treat the heading in the Petition for this ground, referencing an alternative where "Claim 5 Is Obvious Over Ivey," as containing an inadvertent error at least because the Petition does not contain an analysis of a single-reference obviousness ground for claim 5. *See* Pet. 34–35; *compare id.* at 34 (Heading C for Ground III), *with id.* at 5 (table of grounds identifying Ground 3 as challenging claim 5 only as "Obvious under §103 over Ivey in combination with Campbell"); *see also* Pet. Reply 3, 6 (reiterating the two-reference ground). Petitioner's new argument, made for the first time in the Reply, that claim 5 is non-limiting is untimely, and, therefore, any implied argument that claim 5 is unpatentable under Ivey alone also is untimely. *See* Pet. Reply 1, 3–6; PO Sur-reply 1–2 (arguing that "[t]his is an attempt to convert an 'inadvertent error' to a new invalidity theory that did not even exist in the first place").

[6] "SIMD" refers to "single-instruction multiple-data." Ex. 1001 ¶ 28; *see also* Ex. 1008, 174 ("single instruction stream—multiple data stream (SIMD)").

Ex. 1006, 626. "ELSA is structured in a three level hierarchy." *Id.* at 627 (endnote omitted; citing *id.* at Fig. 1). Figure 1 of Ivey is reproduced below.

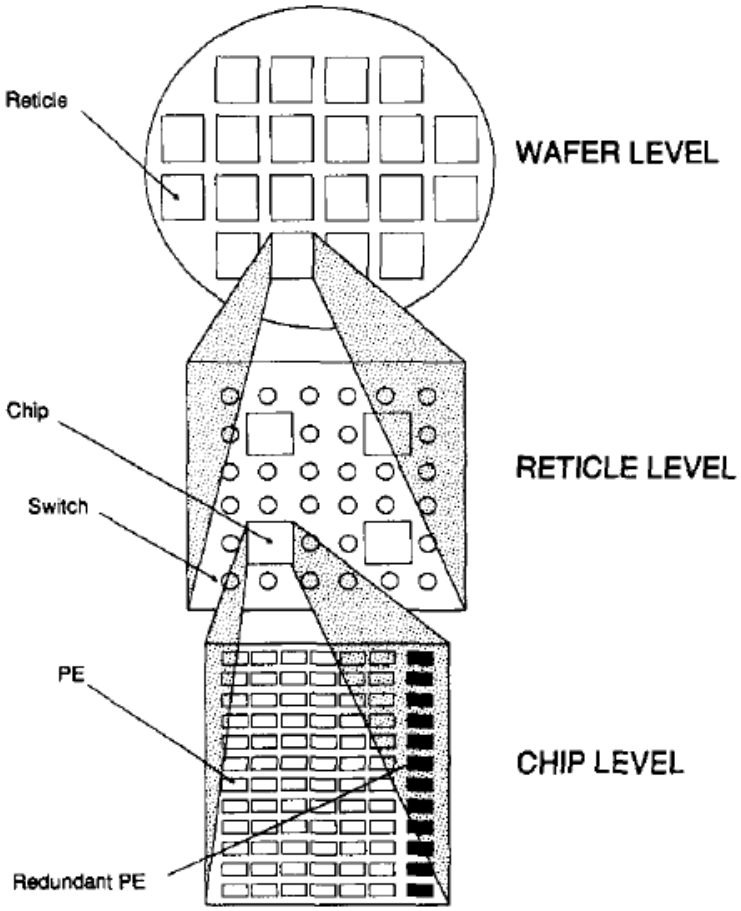


Fig. 1. The ELSA hierarchy.

Figure 1 depicts the ELSA hierarchy, showing the wafer level, the reticle level, and the chip level. *Id.*

"The basic [processing elements (PEs)] are arranged to create a 'chip' level component of 7 × 12 PE's from which, by configuration, a final chip array size of 6 × 12 PE's is constructed . . . [and t]hese chips are then arranged to form a reticle level component which contains 4 chips." *Id.*; *see id.* at 628 ("The basic ELSA chip consists of a 7 by 12 array of PE's, used to produce a final 6 by 12 array."). As shown in Figure 1 above, the seventh column of the chip is filled with redundant (spare) PEs. "The reticle is

stepped and repeated across the wafer, as in the step and repeat process used in conventional IC fabrication, except that connections are made between the edges of adjacent reticles." *Id.* at 627.

"The wafer is built up from 20 placings (Fig. 1) of an identical reticle design, as used for conventional integrated circuit manufacture, except that the reticles abut so that connections can be made between adjacent sites." *Id.* at 630. "At this [reticle] level, reconfiguration switches allow defective chips to be bypassed." *Id.* Ivey, in this regard, further explains as follows:

> Each PE [(processing element)] has a set of switches which are implemented to disconnect a faulty PE and replace it with a redundant one. To simplify testing, each PE contains a test flip-flop which is set or reset by a test program applied to all PE's on the wafer simultaneously.

Id. at 629. Ivey discusses "self-test[s]" using an autonomous test program. *Id.* at 632; *see also id.* at Fig. 5 (captioned as "PE autonomous test circuitry"). "After running a test program . . . [and i]f the result is not as expected, the PE is regarded to be faulty and the comparator output sets a flip-flop." *Id.* at 629 (citing *id.* at Fig. 5).

Figure 6 of Ivey is reproduced below.

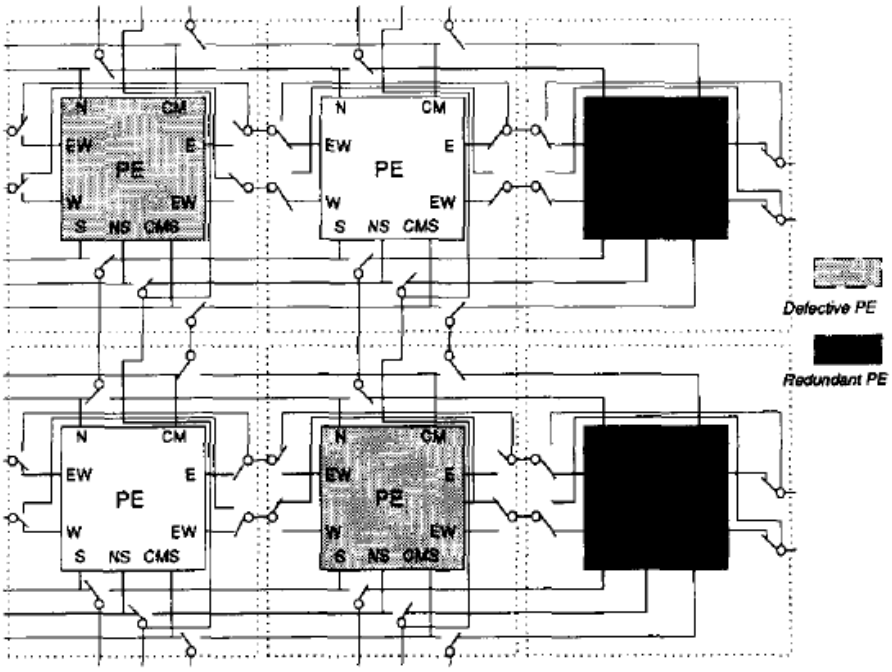


Fig. 6. Reconfiguration at the PE level.

Figure 6 depicts the reconfiguration of the system at the PE level. *Id.* at 629. "The output of this flip-flop is connected to the bypass switching network, so that a PE with a fault disconnects itself from the array." *Id.* Via the switching network and as shown in Figure 6 above, signals are diverted from the bypassed, faulty PE to a redundant (spare) PE. *Id.* "Control of the bypass of a PE can be effected by software as just described, by a laser fuse or floating gate transistor." *Id.*

Ivey also discusses wafer level reconfiguration, stating, "Defects at the wafer level can require reconfiguration of both the global command distribution network and the chip-to-chip interconnection network. The power distribution is also critical." *Id.*

2. Status of Campbell as Prior Art

Patent Owner argues that Petitioner has not shown that Campbell was a printed publication at the time of the claimed invention. PO Resp. 46–52. The parties operate under the assumption that the priority date for the claimed invention is December 22, 1997. *See* Pet. 5; Paper 6 (Preliminary Response), 50 (Patent Owner applying the 1997 date in its analysis); *see also* Ex. 1003, 1:13–15 (the '505 patent claiming priority to a German Patent Application filed on December 22, 1997). Petitioner contends that Campbell was published in 1990, several years before the assumed priority date. *See* Pet. Reply 21; *see also* Pet. 4, 35.

Whether a reference is a printed publication "involves a case-by-case inquiry into the facts and circumstances surrounding the reference's disclosure to members of the public." *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 9 (PTAB Dec. 20, 2019) (precedential) (quoting *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018)). "A given reference is 'publicly accessible' upon a satisfactory showing that such document has been disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it." *Id.* at 10–11 (quoting *SRI Int'l, Inc. v. Internet Sec. Sys., Inc.*, 511 F.3d 1186, 1194 (Fed. Cir. 2008)). The determination as to whether a reference is a printed publication that was publicly accessible is based on the totality of the evidence. *See id.* at 3, 21 (basing the determination at the institution stage on the totality of the evidence). Indicia on the face of the reference, such as a copyright date or ISBN number, "are considered as part of the totality of evidence." *Id.* at 17–18 (citing *Nobel Biocare Servs. AG v. Instradent USA, Inc.*, 903 F.3d 1365, 1377 (Fed. Cir. 2018)).

Campbell (Ex. 1008) is, according to Petitioner, a conference paper published in 1990 by The Institute of Electrical and Electronics Engineers ("IEEE"). *See* Pet. 4–5. Petitioner submitted, with the Petition, a declaration of Gerard P. Grenier, the Senior Director of Content Management of the IEEE, who testifies that "the article and abstract [for Campbell] from IEEE Xplore [digital library] shows the date of publication," and that Campbell was "published in 1991 [sic, 1990] Proceedings, International Conference on Wafer Scale Integration, date of conference January 23–25, 1990." Ex. 1015 ¶¶ 10–11; *see also id.* at Ex. A (Xplore Abstract stating, "Published in: 1990 Proceedings, International Conference on Wafer Scale Integration"). Mr. Grenier further testifies that "[c]opies of the conference proceedings were made available no later than the last day of the conference," which was January 25, 1990. *Id.* ¶ 11. Other evidence includes Campbell's header on some pages reading "1990 International Conference on Wafer Scale Integration" and the line at the bottom of the article reading "CH2814-2/90/0000/0174$01.00 © 1990 IEEE." Ex. 1008, 174,[7] 176.

Patent Owner argues that "neither Petitioner nor its declarant [Mr. Grenier] explains why Campbell was publicly accessible to 'persons interested' and why '[persons] ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.'" PO Resp. 47 (quoting *Hulu*, IPR2018-01039, Paper 29 at 10–11).

In reply to Patent Owner's arguments, Petitioner provides further evidence. *See* Pet. Reply 22–24. For example, Petitioner submits the

[7] We cite herein to the page numbers in the document rather than the exhibit page numbers.

declaration of Dr. Franzon, who testifies that he "attended the 1990 IEEE conference session at which the Campbell paper was presented and received a copy of the article." Ex. 1050 ¶ 12. He attended the conference because he was presenting a paper in the same session as the Campbell paper—the "WSI Fault and Defect Tolerance" session. *Id.* ¶ 13.

Petitioner also notes that Campbell was cited as prior art in a patent having a filing date in 1992, well before the 1997 date of the challenged patent. Pet. Reply 23 (citing Ex. 1052, codes (22), (56)); *see also* Ex. 1052, 7:64–68 ("This [Campbell] paper was presented at the IEEE International Conference on wafer scale integration, held in San Francisco in January 1990, and is herein incorporated by reference."). Petitioner submitted search results of the IEEE Xplore database indicating that Campbell was cited in other IEEE publications prior to the claimed 1997 priority date. Ex. 1053 (result numbers 1 and 3); *see also* Ex. 1054 (Google Scholar search results).

Additionally, Petitioner obtained cross-examination testimony of Patent Owner's expert regarding his familiarity—as a member of IEEE, article publisher, and conference presenter—with IEEE papers being available in libraries and for purchase by the public, and that a conference proceeding is a compilation of articles presented at the conference. *See* Ex. 1049, 61:15–22, 62:10–63:2, 66:7–72:7.

In its Sur-reply, Patent Owner does not challenge substantively and specifically any of Petitioner's evidence. *See* PO Sur-reply 24. Rather, Patent Owner argues that "Petitioner's new evidence is inadmissible," and that "[t]he evidence in the record fails to prove that Campbell was publicly available before the priority date." *Id.* Patent Owner does not elaborate in the Sur-reply on its inadmissibility argument and did not file a motion to

exclude the evidence. *See* 37 C.F.R. § 42.64(c) ("A motion to exclude evidence must be filed to preserve any objection."). Accordingly, Petitioner's exhibits described above are evidence in the record, and we consider that evidence in our analysis.

The person of ordinary skill in the art is an electrical engineer (or similar) having experience with integrated circuit defect tolerance and redundancy techniques. *Supra* Section II.B. IEEE is an organization for electrical engineers, and the Campbell paper was presented in a session titled "WSI Fault and Defect Tolerance" (Ex. 1050 ¶ 13). We find that the totality of Petitioner's evidence, as discussed above and which stands unrebutted, demonstrates that IEEE published Campbell in 1990 as part of a physical volume accessible at least to persons having ordinary skill in the art who would have attended the IEEE conference and was accessible to interested persons in the years between the 1990 conference and the 1997 asserted priority date. In addition to having a copyright notice of 1990, Campbell contains a footer with IEEE indexing and reprint cost information and contains page numbering beginning with page 174, which suggests it is part of a larger document and not merely a draft. Further, Mr. Grenier testifies that the date of publication, as shown on the abstract, was populated from metadata associated with the publication, Ex. 1015 ¶ 10, and that date on the abstract is 1990, *id.* at Ex. A.

Accordingly, for the reasons given above, we determine that Petitioner has shown by a preponderance of the evidence that Campbell was a printed publication before the earliest claimed priority date of the '505 patent, December 22, 1997, and is therefore prior art to the challenged claim.

3. Overview of Campbell (Ex. 1008)

Campbell "describes recent progress in the area of in-use fault tolerance for a massively parallel array processor." Ex. 1008, 174. Campbell discusses the addition of fault tolerance capability to the existing architecture of a three-dimensional (3D) computer. *Id.* "One of the most unique features of the 3D Computer is its physical implementation: a three dimensional stack of silicon wafer scale integrated (WSI) circuits with thousands of interconnects between & through the wafers." *Id.*

Campbell explains that it uses "the term *fault tolerance* for the ability to tolerate failures during the operation of the computer after the 3D stack has been assembled, as opposed to *defect tolerance* to improve circuit yield during initial fabrication of the WSI circuits." *Id.* According to Campbell, "[s]ome form of in-use fault tolerance is essential if highly parallel array processors such as the 3D Computer are to find a home in applications requiring high reliability and self-repairability; however, fault tolerance is not a substitute for defect tolerance in monolithic WSI." *Id.*

According to Campbell, performing a "periodic Built-In Test (BIT) under software control" is a "practical technique[] for fault detection in support of static fault tolerance." *Id.* at 176; *see also id.* at 180 (referring to "the fault map produced during self-testing of the wafers"). In discussing in-use fault tolerance, Campbell explains that "*[s]tatic* fault tolerance refers to the capability to detect failures during operation and briefly stop operation while the hardware and software is reconfigured to avoid the failed hardware," and "*[d]ynamic* fault tolerance refers to the capability to detect and correct failures on the fly with no incorrect output and little or no loss of service." *Id.* at 175. Upon detection of a failure, "[i]f a redundant spare unit is available, it is switched-in to replace the faulty unit." *Id.* at 176.

4. Discussion

a. [Claim 1] An Integrated Circuit Data Processor, comprising:

Petitioner, for the preamble, asserts that

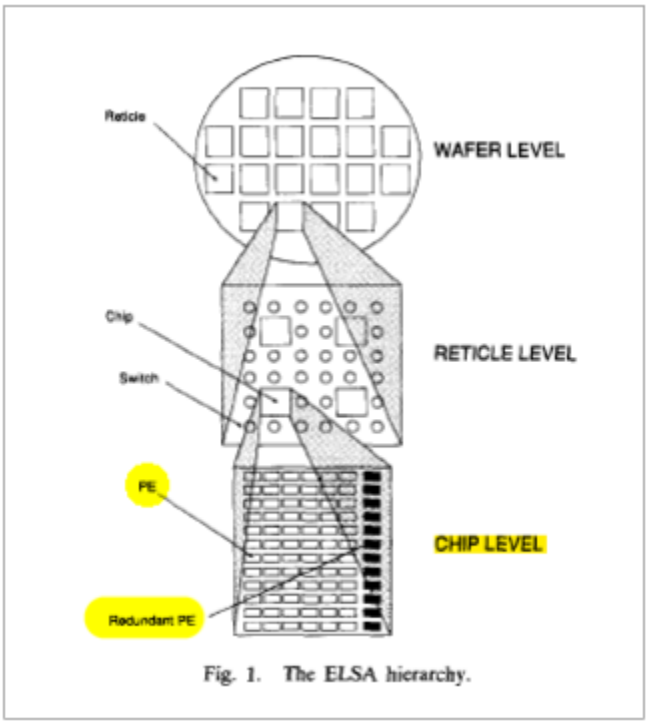
> Ivey discloses a wafer scale integration project to build an "array processor on a 4-in wafer" which is an IC [(integrated circuit)] data processor. Ex. 1006, Abstract. It is an IC because it contains multiple processors integrated in the device and is integrated onto a single wafer. It is a data processor because it is an array processor made up of multiple processing elements that are used to process data. *Id.*; Ex. 1001, ¶¶58-59.

Pet. 18. In other words, Petitioner contends that Ivey discloses an IC data processor in the form of an array processor, and that the array processor is on a wafer. Although Patent Owner, as discussed below, disputes the role of the wafer in Petitioner's proposed combination, Patent Owner does not dispute that Ivey discloses the subject matter of the preamble. *See* PO Resp. 8–9 ("In other words, the entire wafer itself becomes an integrated circuit."). We find that a person of ordinary skill in the art would have recognized that the preamble is taught or suggested by Ivey.

b. data processing cores being arranged in an array

Petitioner asserts that Ivey discloses or renders obvious the limitation "data processing cores being arranged in an array." Pet. 18–20. Petitioner contends that a person of ordinary skill in the art would have understood each of Ivey's processing elements (PEs) to be a separate data processing core "because it is a processor cell in an array and can perform its own processing functions," contends that this is consistent with the description in the challenged patent, and contends that the terms "cells" and "cores" are used interchangeably in the challenged patent. *Id.* at 18 (citing Ex. 1006, 627–628, Fig. 2; Ex. 1003, 2:36–38; Ex. 1004, 4787, 4795; Ex. 1001 ¶ 60).

To explain its position regarding the requirement of the cores being arranged in an array, Petitioner provides an annotated version of Ivey's Figure 1, reproduced below.



Pet. 19. Depicted above is the ELSA hierarchy, showing the wafer level, the reticle level, and the chip level, with Petitioner's highlighting of the labels "CHIP LEVEL," "PE," and "Redundant PE." Ex. 1006, 627. Petitioner asserts that the processing elements of Ivey are arranged in an array. Pet. 19–20 (citing Ex. 1006, 626–627, Fig. 1). Specifically, Petitioner contends that this array is the 7×12 array of PEs "illustrated in Ivey's Figure 1 at the 'chip level' view." *Id.* at 19.

We find that Ivey discloses "data processing cores being arranged in an array," as recited in claim 1, and discloses that array at least at the chip level.

c. a plurality of the data processing cores comprising at least one Arithmetic and Logic Unit

Petitioner asserts that Ivey discloses or renders obvious this limitation. Pet. 20–21. Petitioner asserts that the processing element architecture includes an Arithmetic and Logic Unit (ALU), also referred to as an "adder/subtractor." *Id.* (citing Ex. 1006, 627–628, Fig. 2; Ex. 1001 ¶¶ 64–65; Ex. 1018, 26). Petitioner persuasively shows that Ivey discloses a plurality of data processing cores comprising at least one Arithmetic and Logic Unit.

d. wherein the integrated circuit is operative to:

perform at least a self-test on the plurality of data processing cores comprising at least one Arithmetic and Logic Unit; and

disable data processing cores found by the self-test to be defective.

Petitioner, relying on the testimony of Dr. Franzon, asserts that Ivey discloses or renders obvious these limitations. *Id.* at 21–23 (citing Ex. 1001 ¶¶ 66–68).

These limitations involve the performance of a self-test on "the plurality of data processing cores." Ex. 1003, 13:24–26. Petitioner refers back to its previous discussion of the limitation reciting "data processing cores being arranged in an array" in asserting that the European Large SIMD Array (ELSA) processing elements (PEs) are the plurality of cores of this limitation. Pet. 21 (referencing Section XI.A.1.b of the Petition). Thus, for the self-test limitation, Petitioner is referring to the array of PEs shown in Ivey's "chip level" view. Pet. Reply 9.

Petitioner asserts that the ELSA is operative to perform a self-test on its array of PEs, quoting the following from Ivey: "PE Self-test and

reconfiguration involves the use of the autonomous test program to check each PE within a chip." Pet. 21–22 (emphasis omitted) (quoting Ex. 1006, 632). Petitioner provides an annotated version of Ivey's Figure 5, reproduced below.

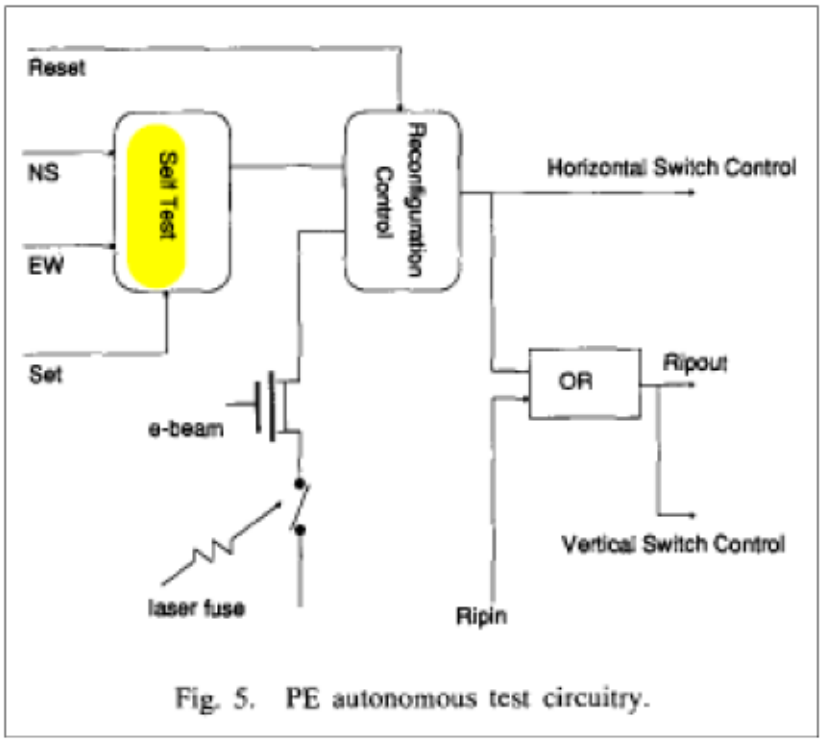


Fig. 5. PE autonomous test circuitry.

Id. at 22. Depicted above is Figure 5 of Ivey, the PE autonomous test circuitry, with Petitioner's highlighting of the self-test component. *Id.*

Petitioner's expert persuasively testifies that "ELSA is operative to perform a self-test on its array of multiple PEs" and that "Ivey explains that ELSA includes a self-test program that tests all of the PEs in the array for defects[.]" Ex. 1001 ¶ 66 (citing Ex. 1006, 629, 632). Patent Owner's expert agrees that Ivey discloses "conceptualizing using a chip self-test that uses an autonomous test program to check each chip on the wafer." Ex. 1049, 41:17–22.

Petitioner further asserts that the self-test circuitry will disable faulty processing elements by disconnecting them from the processor array. Pet. 22–23 (citing Ex. 1006, 629). Ivey explains that "[e]ach PE has a set of switches which are implemented to disconnect a faulty PE and replace it with a redundant one." Ex. 1006, 629. Ivey states, "At the chip level, one redundant column of PE's was employed to replace a faulty PE in each row." *Id.*

We find that Ivey discloses or at least suggests these limitations. A person of ordinary skill in the art would have understood Ivey to teach the performance of a self-test of cores at least at the chip level and disabling defective cores.

> *e. [Claim 5] The Integrated Circuit Data Processor [according] to claim 1, wherein the defective data processing cores are detected in the field.*

Petitioner, relying on the testimony of Dr. Franzon, contends that the combination of Ivey and Campbell teaches this limitation. Pet. 34–35. Petitioner asserts that Campbell teaches detecting failures during the operation of the computer after assembly, as opposed to during initial manufacturing, and contends that this teaching corresponds to the subject limitation's recitation "the defective data processing cores are detected in the field." *Id.* at 34 (citing Ex. 1008, 174–175; Ex. 1001 ¶¶ 90–91).

Campbell discusses both fault tolerance—the ability to tolerate failures during operation—and defect tolerance to improve circuit yield during fabrication. Ex. 1008, 174. Campbell explains that "[s]tatic fault tolerance refers to the capability to detect failures during operation and briefly stop operation while the hardware and software [are] reconfigured to avoid the failed hardware." *Id.* at 175 (italicizing omitted). Campbell

teaches that some form of in-use fault tolerance is essential if certain array processors are to find use in applications requiring high reliability and self-repairability. *Id.* at 174.

Petitioner's proposed combination is the extension, to the field, of Ivey's teachings of a self-test system at the manufacturing stage. Pet. 34; *see also id.* at 35 ("[I]t would have been obvious to a POSA to expand Ivey to field testing as taught by Campbell."); Pet. Reply 2 (confirming our understanding, as stated in the institution decision, that Petitioner's proposed combination is "applying Campbell's general teaching of performing a self-test after assembly (mapped to the detecting of defective cores in the field, as recited in Claim 5) to Ivey's teaching of a self-testing system" (quoting Paper 12, 25)).

In the Reply, Petitioner reiterates its proposed combination:

> Intel's obviousness theory is a straightforward one: a [person of ordinary skill in the art] reading Ivey and Campbell would understand that Ivey's chip-level autonomous self-test could be used in the field just as easily as it could in a fab. Intel is not seeking to combine particular circuitry disclosed in Campbell with Ivey, or vice versa. Rather, as the Board recognized, Intel is combining Campbell's general teaching of field testing with Ivey. Paper 12, 25.

Pet. Reply 8.

We find that Campbell teaches detecting failures during operation, which is "in the field" under the parties' agreed understanding of that phrase. Petitioner has shown persuasively that the combination of Ivey and Campbell teaches or suggests that "defective data processing cores are detected in the field" as recited in claim 5.

f. Reason to Combine and Reasonable Expectation of Success

Petitioner, relying on the testimony of Dr. Franzon, argues that a person of ordinary skill in the art "would have been motivated to combine the teachings of Ivey and Campbell to permit field testing so that processor arrays would not fail during operations." Pet. 34 (citing Ex. 1001 ¶¶ 92–94). According to Petitioner, "[t]his would be an obvious extension of Ivey beyond the manufacturing stage, and would have predictable results." *Id.* Petitioner also argues that the proposed combination would have been obvious as the "combination of prior art elements and techniques according to known methods, and would yield predictable results." *Id.* at 35 (citing Ex. 1001 ¶¶ 92–94).

Patent Owner argues that a person of ordinary skill in the art "would not have been motivated to combine [Ivey's wafers] with Campbell or to modify them in any way, because the Ivey wafers were dysfunctional." PO Resp. 21 (citing Ex. 2032 ¶ 39). Patent Owner further argues that Petitioner has failed to establish a reasonable expectation of success. PO Resp. 41–46; *see also id.* at 16–23. Patent Owner, for the first time at the hearing, argued that a key issue is enablement. Tr. 56:7–57:8 (citing *Raytheon Technologies Corp. v. General Electric Co.*, 993 F.3d 1374, 2021 WL 1432964 (Fed. Cir. Apr. 16, 2021)). Along those lines, Patent Owner further argued that "the wafer, as a whole, wouldn't work in the field" and that "means the wafer is not enabled and there's no reasonable expectation of success." *Id.* at 56:21–57:1.

As the Federal Circuit has explained, "[t]he reasonable expectation of success requirement refers to the likelihood of success in combining references to meet the limitations of the *claimed invention*." *Intelligent*

Bio-Sys., Inc. v. Illumina Cambridge Ltd., 821 F.3d 1359, 1367 (Fed. Cir. 2016) (emphasis added). It is incorrect to view the "reasonable expectation of success" inquiry as an analysis of "whether one would reasonably expect the prior art references to operate as those references intended once combined." *Id.* As to enablement, "[t]o render a claim obvious, the prior art, taken as a whole, must enable a skilled artisan to make and use the claimed invention." *Raytheon Techs.*, 993 F.3d at 1380. "In general, a prior art reference asserted under § 103 does not necessarily have to enable its own disclosure, i.e., be 'self-enabling,' to be relevant to the obviousness inquiry." *Id.* "Even if a reference discloses an inoperative device, it is prior art for all that it teaches." *Beckman Instruments Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989).

Patent Owner asserts that Ivey is a research paper about wafer scale integration, and that the article indicates that the researchers had problems and were not able to accomplish their goals regarding that wafer scale integration. *See* PO Resp. 8–12. Patent Owner argues that Ivey, therefore, discloses a somewhat unsuccessful wafer scale integration. *See id.* at 10 ("It 'outline[s] some of the technology, successful and unsuccessful, of [the ESLA project.]'" (underlining omitted; alterations in original) (quoting Ex. 1006, Abstract)). Patent Owner argues that a person of ordinary skill in the art "would have understood that after assembly [i.e., in the field], the devices described in Ivey would have significant technical issues and a POSITA [person of ordinary skill in the art] would not have been able to complete any test on them due to unsolved and not-yet-understood technical deficiencies." *Id.* at 17 (citing Ex. 2032 ¶¶ 25–26). Specifically, Patent Owner asserts that "in all packaged and assembled wafers discussed in Ivey,

the CLOCK signals malfunctioned," and that "the CLOCK signals are essential in performing the testing." *Id.* at 20 (citing Ex. 2032 ¶ 37). Patent Owner contends that

> a POSITA would have understood that the "in the field" limitation means "after assembly" and includes new packaging structures, such as wires, bonds, and external connections. As shown in Ivey and explained by PO's expert, Dr. Wolfe, these new assembly and packaging structures introduced the fatal CLOCK issues that prevent the Ivey wafer from being used in the field after assembly.

PO Sur-reply 2. Patent Owner argues that, because of the CLOCK signal issues, a person of ordinary skill in the art "would not have had motivation to apply the general teaching of testing after assembly to Ivey's wafer," and "would not have had reasonable expectation of success in doing that either." PO Resp. 20–21 (citing Ex. 2032 ¶¶ 37–38).

Patent Owner's arguments are unavailing because they focus on the shortcomings at the wafer level of Ivey's overall research project and are premised on reducing to practice a successful wafer level device rather than the reference's teachings as understood by the person of ordinary skill in the art. *See, e.g.*, PO Sur-reply 18–19 (indicating that the clock issues were at the wafer level). Ivey also teaches—in the course of attempting to scale up to the wafer level—self-testing and replacing a faulty processing element at the chip level. *See, e.g.*, Ex. 1006, 629 (discussing, in detail, chip level reconfiguration as well as wafer level reconfiguration). Petitioner's articulated case is at the chip level. *See, e.g.*, Pet. 18–20 (identifying Ivey's chip array for the limitation "data processing cores being arranged in an array"); *id.* at 22 (for self-test limitation: "Because Ivey self-tests each PE within a chip and because each PE is a data processing core containing an ALU, Ivey discloses or renders this limitation obvious."); Pet. Reply 9 ("As

explained in Intel's Petition, Ivey teaches performing a self-test and replacing defective PEs at the ***chip-level***." (citing Pet. 15, 18–19, 21–22)).

Patent Owner, in its Sur-reply, points to Petitioner's addressing of the preamble as indicating that Petitioner's case must be constrained to an analysis at the wafer level. *See* PO Sur-reply 3 (referring to Petitioner's assertion (Pet. 18) that "Ivey discloses a wafer scale integration project to build an 'array processor on a 4-in wafer' which is an IC data processor"). Petitioner responded at the hearing, explaining that "Ivey's overall design, . . . that's going to be on a wafer, but the claim elements are practiced at the chip level and that's how we map it out in the Petition." Tr. 60:15–17; *see id.* at 60:4–14 (asserting that Ivey's is a design for a wafer level processor, but the "the data processing array we identify is the array—is the 7 by 12 array of PEs on one of these chips"); Tr. 48:23–49:1 ("So the preamble recites an integrated circuit data processor so the Ivey wafer that's disclosed has a bunch of integrated circuits on it. There's—in one example of 64 by 64 array, so—and those would be the individual chips."). We agree that Petitioner's case is articulated as applying Ivey's teachings at the chip array level. Regardless, we find that a person of ordinary skill in the art, particularly one with knowledge of the known technique of a built-in self-test, would not ignore the chip-level teachings. *See, e.g.*, Ex. 1001 ¶¶ 52, 54, 56, 57 (Dr. Franzon identifying prior art references disclosing self-testing); Ex. 1003, 1:43 (the '505 patent referring to built-in self-test (BIST) as one of the "[t]raditional known methods"); *see also KSR*, 550 U.S. at 421 ("A person of ordinary skill is also a person of ordinary creativity, not an automaton."). We do not agree with Patent Owner's implied argument that the only possible combination that an ordinary artisan would envision is that

of attempting to perform in a field a self-test on a failed wafer scale integration project. *See* PO Sur-reply 3 ("To the extent Petitioner argues that the 'chip' is the chip level hierarchical components integrated on the wafer, the 'chip-level self-test' does not fill the gap because that test still needs to run on the wafer, which cannot function 'in the field.'").

Having fully considered the parties' contentions and evidence, we are persuaded that Petitioner has articulated sufficient reasoning, with rational underpinnings, to persuasively establish that a person of ordinary skill in the art would have been motivated to combine Ivey and Campbell in the manner proposed by Petitioner and would have had a reasonable expectation of success in doing so. As Petitioner asserts, Ivey teaches a chip-level array that is able to perform, using software, a self-test on the cores and disable faulty processing elements. *See* Ex. 1006, 629, Figs. 5, 6. Campbell teaches self-testing after assembly and the value of in-use fault tolerance. Ex. 1006, 174. The level of ordinary skill in the art is relatively high, and a person of such skill would have found it obvious to extend Ivey's self-testing to the field for use after assembly and when the array is in operation, which would have predictably yielded a processor array that would not fail in the field due to faulty cores. *See* Pet. 34–35.

Petitioner's expert, Dr. Franzon, testifies that Ivey's "ELSA is operative to perform a self-test on its array of multiple PEs [(processing elements)]." Ex. 1001 ¶ 66 (citing Ex. 1006, 629, 632). Dr. Franzon notes that Ivey discusses detecting defects in the manufacturing environment but testifies that nothing limits Ivey's autonomous test program to testing in a fabrication environment. Ex. 1050 ¶ 6. Dr. Franzon further testifies that Ivey's self-test program, the autonomous test program, is software and can

be run in the fabrication facility or in the field. *Id.* ¶ 4 (citing Ex. 1006, 629 ("Control of the bypass of a PE can be effected by software as just described[.]")); *cf.* PO Resp. 28 (Patent Owner acknowledging that Ivey suggests bypassing a faulty processing element by the use of software). We find Dr. Franzon's testimony credible and persuasive.

As to Patent Owner's untimely enablement argument made at the hearing, even if Ivey's wafer level device was inoperative, we are not persuaded that a person of ordinary skill in the art would have been unable to make and use, in the field, a chip-level array utilizing the self-testing taught by Ivey. *Cf. Apple Inc. v. Corephotonics, Ltd.*, No. 2020-1438, 2021 WL 2577597, at *4 (Fed. Cir. June 23, 2021) (nonprecedential) (stating, in the context of AIA trial proceedings, "regardless of the forum, prior art patents and publications enjoy a presumption of enablement, and the patentee/applicant has the burden to prove nonenablement for such prior art").

Patent Owner contends that a person of ordinary skill in the art would not have combined Ivey and Campbell because the two references are significantly different. PO Resp. 7. Patent Owner argues that Ivey addresses defect tolerance and a two-dimensional array, while Campbell addresses fault tolerance and a three-dimensional structure. *Id.* at 6–7. Based on these differences, Patent Owner argues that "Petitioner fails to explain why a POSITA would combine the fault tolerance technology in Campbell with the defect tolerance technology in Ivey," and "fails to explain why a POSITA would have transplanted such 3D specific feature in Campbell to the 2D chip in Ivey." *Id.* at 8. Patent Owner's arguments are not persuasive. Petitioner's case does not involve a bodily incorporation of

Campbell's structures onto Ivey's structures. *See MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015) ("[T]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference." (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)); *Lear Siegler, Inc. v. Aeroquip Corp.*, 733 F.2d 881, 889 (Fed. Cir. 1984) (The ordinary artisan is not "compelled to adopt every single aspect of [a reference's] teaching without the exercise of independent judgment."). Petitioner's articulated case is based on the application of Campbell's general teaching of performing a self-test in the field to Ivey's teachings of performing a self-test on cores of a chip. Petitioner's proposed combination retains the self-testing of Ivey. For the same reason, Patent Owner's argument that there would have been no expectation of success in attempting to "increase the complexity of the 2D design of Ivey by incorporating concepts from the 3D design of Campbell" is unavailing. PO Resp. 22–23 (internal quotation marks omitted) (quoting Ex. 2032 ¶ 41).

Patent Owner also argues that Ivey discourages a person of ordinary skill in the art from modifying the design because, *inter alia*, "[t]he reference acknowledges that unsolved problems remain and that most in the field have moved on without solving these problems." PO Resp. 21–22; *but see* Ex. 1006, 634 ("The fact that we have not ultimately achieved a wafer scale device is disappointing, but it does not detract from the overall value of our work on a scientific and, ultimately, a commercial level."). This is unavailing as it is based on the implied premise that, for Ivey to provide a relevant teaching to a person of ordinary skill in the art, it must describe a completely successful wafer scale integration. *See* PO Resp. 22 (referring to

engineers' inability to "achieve required densities"). Even if Ivey discouraged researchers from continuing to attempt wafer-scale integration, that is not a disparagement of the use of self-testing at the chip level, which is what is relevant in this case.

Patent Owner argues that Petitioner's reasoning for combining the references' teachings is conclusory and lacks detailed analysis. PO Resp. 23–26. Patent Owner characterizes Petitioner's reasoning as limited to an assertion that the references are analogous, compatible, and available at the same time. *Id.* We do not agree as this argument fails to acknowledge and address the other reasoning offered by Petitioner. *See* Pet. 34–35.

Relatedly, Patent Owner argues that "the technology in Ivey and the technology in Campbell are not in fact as similar as Petitioner alleges," and "the evidence in the record . . . contradict[s] Petitioner's motivation to combine based on the similarity of the references." PO Resp. 32–33; *see also id.* at 31–33 (section under the heading "Petitioner's motivation to combine based on the similarities fails"). Petitioner's discussion of the references' similarities in subject matter and timing of publication is presented after discussing why a person of ordinary skill in the art would have had reason to combine the references' teachings. *See* Pet. 34–35. Petitioner does not assert those similarities as a standalone or sole motivation as Patent Owner may be implying. *See* PO Resp. 31 (quoting *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017) for the proposition that characterization of references being in the same field "without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion").

Patent Owner takes issue with Petitioner's expert's opinion that the proposed combination could be implemented via the use of Ivey's reset line. PO Resp. 26–30 (citing Ex. 1001 ¶ 94). Petitioner argues that "this modification to Ivey cannot be found anywhere in Campbell," and that Campbell does not disclose how its three-dimensional technology could be combined with Ivey's reset line. *Id.* at 26–27; *see also id.* at 30 ("Petitioner also fails to explain . . . why the fault tolerance mechanism in Campbell would be considered an improvement on the software mechanism that Ivey already provides."). To the extent that the opinion of Petitioner's expert as to how the combination (initiating Ivey's self-test in the field) would be implemented is regarded as a motivation to combine, there is no requirement that the art provide an explicit motivation to combine. *KSR*, 550 U.S. at 418–19. And, Patent Owner's argument incorrectly is premised on bodily incorporating Campbell's structures into Ivey's. Further, we disagree with Patent Owner's argument that Petitioner is improperly attempting to use opinion testimony as a substitute for a disclosure of a claim element in a patent or printed publication. *See* PO Resp. 26–27. Petitioner has addressed all the limitations by citation to the references, and Patent Owner does not identify which claim element purportedly is missing without the expert opinion regarding implementation via the reset line. *See id.*

Patent Owner also argues, without support from its own expert's opinion, that Petitioner's expert incorrectly interpreted Ivey's mention of methods of bypassing a faulty processing element. PO Resp. 28–30 (citing Ex. 1006, 629 ("Control of the bypass of a PE can be effected by software as just described, by a laser fuse or floating gate transistor.")). Patent Owner argues that Ivey identifies three alternative ways, not three required steps,

and using Ivey's software alternative in the field does not amount to an improvement of Ivey by omitting a step. *Id.* at 29–30. The Petition does not discuss this theory that is the subject of Patent Owner's dispute with the opinion of Petitioner's expert. *See* Pet. 34 (citing 1001 ¶ 94, but not proffering reasoning involving improvement by the omission of a step or alternative). We need not discuss the viability of a motivation that is not advocated by Petitioner, and we do not rely on it in reaching a decision on patentability.

Patent Owner argues that Petitioner's motivation to combine is based on unsupported assumptions and that "[a] key assumption here is that the 3D fault detection techniques used in Campbell could somehow be functional and useful in the 2D wafer in Ivey." PO Resp. 33–35. Patent Owner further argues that "Petitioner [does not] attempt to show that one of ordinary skill in the art would have had a reason to use 3D techniques on a 2D wafer, much less have a reasonable expectation of success." *Id.* at 35. Similarly, Patent Owner argues that "[Petitioner's] argument is premised on the assumption that the addition of extra technologies to Ivey would not affect Ivey's existing utilities or operations." *Id.* at 35–36; *see id.* at 36–37 (arguing that there is no reasonable expectation of success in adding the software control of Campbell to Ivey). These arguments by Patent Owner are unavailing because they are premised on Patent Owner's hypothetical combination involving bodily incorporating Campbell's structures, not Petitioner's actual proposed combination. Petitioner proposes utilizing Ivey's self-testing in the field, not adding Campbell's testing circuitry to Ivey's. *See, e.g.*, Pet. 35 ("[I]t would have been obvious to a POSA to expand Ivey to field testing as taught by Campbell."); Pet. Reply 2 ("Intel is

not proposing to combine Campbell's particular self-test circuitry with Ivey.").

Patent Owner next argues that Petitioner's use of a statement of the Examiner is improper. PO Resp. 37–39 (citing Pet. 34–35). Petitioner quotes the Examiner as asserting that "field testing . . . [was] an obvious variation of well-known testing areas." Pet. 35 (quoting Ex. 1004, 4746); *see also id.* at 4. We do not treat the Examiner's statement as established fact and do not rely on it as such. Rather, Petitioner presents other evidence, including Campbell, that teaches self-testing after assembly, i.e. in the field. *See* Ex. 1008, 174.

III. CONCLUSION[8]

Petitioner has shown by a preponderance of the evidence that claim 5 of the '505 patent is unpatentable over Ivey and Campbell.

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
5	103(a)	Ivey, Campbell	5	
Overall Outcome			5	

[8] Should Patent Owner wish to pursue amendment of the challenged claim in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

For the foregoing reasons, it is hereby:

ORDERED that claim 5 of the ’505 patent has been proven to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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