

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00528
Patent 8,686,549 B2

Before KEN B. BARRETT, CHARLES J. BOUDREAU, and
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

OGDEN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Granting Patent Owner's Motion to Exclude
37 C.F.R. § 42.64(c)

I. INTRODUCTION

In response to a Petition (Paper 2, “Pet.”) by Petitioner Intel Corporation (“Intel”), the Board instituted an *inter partes* review of claim 41 of U.S. Patent No. 8,686,549 B2 (Ex. 1003, “the ’549 patent”). Paper 11. Patent Owner PACT XPP Schweiz AG (“PACT”) filed a Patent Owner Response (Paper 20, “PO Resp.”), Intel filed a Reply to the Patent Owner Response (Paper 23, “Pet. Reply”), and PACT filed a Sur-reply (Paper 29, “PO Sur-reply”).

PACT also filed a Motion to Exclude Exhibit 1013 (Paper 33, “Mot. Exclude”), which Intel does not oppose. *See* Paper 34.

We held an oral hearing on May 20, 2021, and the transcript is entered on the record. Paper 38 (“Tr.”).

This is a Final Written Decision under 35 U.S.C. § 318(a) as to whether the claim challenged in the *inter partes* review is patentable. By a preponderance of the evidence on the record before us, Intel has shown that claim 41 of the ’549 patent is unpatentable. We also grant PACT’s Motion to Exclude Exhibit 1013.

II. BACKGROUND

A. RELATED PROCEEDING

As a related matter, the parties identify *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-1006-JDW (D. Del. filed May 30, 2019) (“the related litigation”). Paper 37, 2; Paper 4, 2.

B. THE '549 PATENT (EX. 1001)

The '549 patent describes stacked structures for multicore processors. *See* Ex. 1003, 22:11–23:24, Figs. 7a–h. Figure 7f, reproduced below, illustrates an example of such a structure:

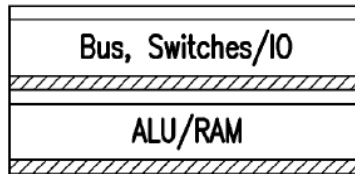


FIG. 7f

Figure 7f is a cross-sectional view of a semiconductor stack, in which there is a “separation of buses with the necessary switching units and the IO^[1] structure from the ALUs^[2] and memories which in this example are situated in the same plane.” Ex. 1003, 23:7–10.

In one embodiment described in the '549 patent, the IO structure is associated with “a dedicated connection (IO channel) to a superregional bus system which may transmit, in particular, data over long distances within the array and/or, in particular, has direct connection to the peripherals.” Ex. 1003, 5:22–26. This dedicated IO connection may “conform to an industrial standard, e.g., PCI,^[3] . . . to thus permit simple and cost-effective connection of the peripheral devices.” *Id.* at 5:29–33; *see also id.* at 19:61–

¹ “IO” refers to input/output, or peripheral access. *See, e.g.,* Ex. 1003, 1:35, 1:58–59, 3:5.

² “ALU” refers to an arithmetic logic unit. Ex. 1003, 46:61.

³ “PCI” refers to the Peripheral Component Interconnect standard. Ex. 1003, 47:6–7.

65 (explaining that the use of industry standards, such as PCI, will “thus permit a simple and uncomplicated connection to the peripheral devices”).

Alternatively, “protocol conversions may also be performed in IOAGs⁴ connected between [a dedicated internal bus system and external devices] so that an internal simplified and optionally proprietary protocol is translated to one or more complex external standard protocols.” Ex. 1003, 19:65–20:2; *see also id.* at 24:11–24. In this embodiment, “[t]he actual management and triggering of the external units may be handled in the IOAGs which may be designed to be much larger and more complex.” *Id.* at 24:22–24.

C. CHALLENGED CLAIM AND ASSERTED GROUNDS OF
UNPATENTABILITY

PACT has disclaimed claims 39 and 40. *See* Ex. 2002. This means that “the patent is treated as though the disclaimed claims never existed.” *Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1383 (Fed. Cir. 1998) (citing *Guinn v. Kopf*, 96 F.3d 1419, 1422 (Fed. Cir. 1996)). However, in addressing the patentability of claim 41, we must also address the limitations of claims 39 and 40 because claim 41 depends from claim 40, which depends from independent claim 39. *See* Ex. 1003, 46:54–47:7.

Independent claim 39 is as follows:

39. A processor integrated device comprising:
- at least two dies that are stacked;
 - an interconnect structure; and
 - an arrangement of programmable data processing units interconnected by the interconnect structure;

⁴ “IOAG” refers to an IO management unit. *See* Ex. 1003, 24:13–14.

wherein:

at least some of the programmable data processing units include Arithmetic Logic Units (ALUs);

the interconnect structure includes switches;

the programmable data processing units are implemented on at least a first one of the at least two dies; and

at least parts of the interconnect structure are implemented on at least a second one of the at least two dies.

Ex. 1003, 46:54–67. Claim 40 depends from claim 39 and recites “further comprising at least one dedicated interface unit that interfaces between the programmable data processing units and an external device.” *Id.* at 47:1–4. Claim 41 depends from claim 40 and recites “further comprising at least one dedicated Peripheral Component Interconnect (PCI) unit.” *Id.* at 47:5–7.

Intel argues two grounds for *inter partes* review that involve claim 41, as summarized in the following table:

Claim Challenged	35 U.S.C. §	References
41	103 ⁵	Yu, ⁶ Akasaka, ⁷ Rathnam ⁸
41	103	Franzon, ⁹ Rathnam

Pet. 5.

D. EXPERT TESTIMONY

For its Petition and Reply, Intel relies on two declarations of Dr. Paul Franzon. Exs. 1001, 1049. For its Patent Owner Response and Sur-reply, PACT relies on a declaration by Dr. William Henry Mangione-Smith. Ex. 2027. We find them both qualified, based on their education and experience, to offer testimony on the subject matter of their respective

⁵ 35 U.S.C. § 103(a) (2006), *amended by* Leahy–Smith America Invents Act, Pub. L. No. 112-29 § 103, sec. (n)(1), 125 Stat. 284, 287, 293 (2011) (effective Mar. 16, 2013). This version of § 103 applies because the effective priority date of claim 41 is before the effective date of the AIA amendments. *See* Pet 98 (Intel not contesting September 3, 2001 as the effective priority date of claim 41); Ex. 1050, 9 (PACT stating that the effective priority date of the '549 patent is September 19, 2002).

⁶ Kee-Ho Yu et al., *Real-Time Microvision System with Three-Dimensional Integration Structure*, Proc. IEEE/SICE/RSJ Int'l Conf. on Multisensor Fusion & Integration for Intelligent Sys. 831 (1996) (Ex. 1006).

⁷ Yoichi Akasaka, *Three-Dimensional IC Trends*, 74 Proc. IEEE 1703 (1986) (Ex. 1008).

⁸ Selliah Rathnam & Gert Slavenburg, *Processing the New World of Interactive Media*, IEEE Signal Processing Mag., Mar. 1998, at 108 (Ex. 1010).

⁹ Paul D. Franzon, *Fault Tolerance in VLSI* (Dec. 1988) (Ph.D. thesis, University of Adelaide) (Ex. 1012).

declarations. *See* Fed. R. Evid. 702(a); *see* Ex. 1001 ¶¶ 5–12; Ex. 1002 (Dr. Franzon’s curriculum vitae); Ex. 2027 ¶¶ 4–9; Ex. 2028 (Dr. Mangione-Smith’s curriculum vitae).

III. GROUNDS OF THE PETITION

For the reasons below, we determine that Intel has shown, by a preponderance of the evidence, that claim 41 is unpatentable under § 103. Before analyzing the Petition’s asserted grounds in detail, we address two matters that will underlie our analysis: the level of ordinary skill in the art, and the claim construction we will apply to the claim terms.

A. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the pertinent art at the time of the invention is one of the factual considerations relevant to obviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). It is also relevant to how we construe the patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). To assess the level of ordinary skill, we construct a hypothetical “person of ordinary skill in the art,” from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct “presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Relying on the testimony of Dr. Franzon, Intel argues that a person of ordinary skill in the art “would have a [Master of Science] degree in Electrical Engineering, and at least one year of industry experience in

computer chip design and semiconductor fabrication or preparation of chip designs for fabrication.” Pet. 10 (citing Ex. 1001 ¶¶ 48–49). PACT does not dispute Intel’s characterization. *See* Ex. 2027 (Dr. Mangione-Smith stating, “I will apply Professor Franzon’s definition for this declaration.”).

Based on Dr. Franzon’s uncontested declaratory testimony, which we find consistent with the technical level of the ’549 patent disclosure and asserted prior art references, we adopt Intel’s formulation of the level of ordinary skill for this decision.

B. CLAIM CONSTRUCTION

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2020). This includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.* The ordinary and customary meaning of a claim term “is its meaning to the ordinary artisan after reading the entire patent,” and “as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1313, 1321. In construing a claim, we consider “[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely made of record” in this proceeding. 37 C.F.R. § 42.100(b).

Neither Intel nor PACT identifies any claim terms as needing an explicit construction or notifies us of any relevant prior claim constructions in another proceeding. *See* Pet. 5 (“Intel believes that no terms need be

construed to resolve the arguments presented herein.”); Ex. 2027 ¶¶ 11–14 (explaining Dr. Mangione-Smith’s understanding of the law of claim construction, but not offering any testimony about specific terms). Because neither party’s arguments hinge on a disputed interpretation of the challenged claim, we do not need to explicitly construe any terms for our decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. GROUND BASED ON YU, AKASAKA, AND RATHNAM

In an *inter partes* review, we may only consider a “ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b).

Intel alleges that claim 41 of the ’549 patent is unpatentable under 35 U.S.C. § 103 as obvious over Yu in view of either Rathnam alone, or in view of Akasaka and Rathnam, all of which Intel alleges are prior art printed publications. Pet. 4–5.

A claim is unpatentable under § 103 for obviousness if the differences between the claimed subject matter and the prior art are “such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). For a combination of references, we consider “whether there was an apparent reason to combine the known elements in the fashion claimed by

the patent at issue.” *Id.* at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). A successful petition must “articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (citing *KSR*, 550 U.S. at 418); *see also* 35 U.S.C. § 322(a)(3); 37 C.F.R. §§ 42.22(a)(2), 42.104(b)(4) (2020).

We base our obviousness inquiry on factual considerations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) any objective indicia of obviousness or non-obviousness that may be in evidence. *See Graham*, 383 U.S. at 17–18.

Based on these factors,¹⁰ Intel has shown by a preponderance of the evidence that claim 41 is unpatentable as obvious over Yu in view of Rathnam, with or without the teachings of Akasaka. Intel has also shown by a preponderance of the evidence that Yu, Rathnam, and Akasaka were printed publications before the effective filing date of the claimed invention. We present our findings and conclusions below.

I. Yu

(a) Overview

Yu describes a multi-layer “real-time microvision system.” Ex. 1006, 831. According to Yu, the system is useful for the design of “intelligent

¹⁰ Neither party has presented evidence of objective indicia of obviousness or non-obviousness, so this does not factor into our decision. *See* Pet. 98 (“reser[ving] the right to respond to any secondary considerations of non-obviousness asserted by [PACT]”); *see generally* PO Resp. (not referring to any objective indicia).

robots which work in dynamic environment[s],” and particularly, “mini or micro-robots because of [the system’s] compactness.” *Id.*; *accord id.* at 835. Yu teaches that such systems need “very fast real-time vision” for the “tracking of ultra-high speed motion or analysis of ultra-high speed reaction.” *Id.*

Figure 1, reproduced below, illustrates the system’s 3D structure:

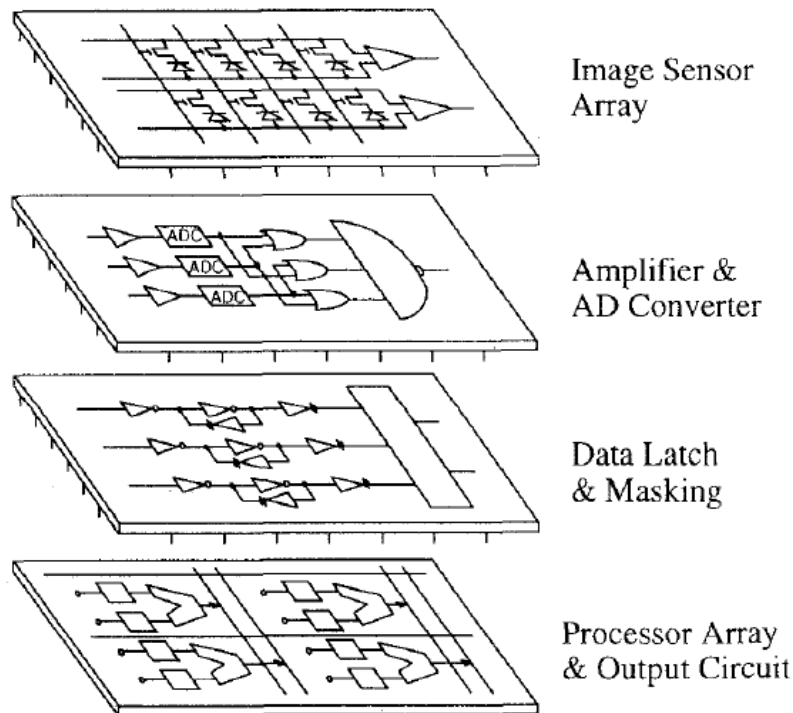


Figure 1: Basic concept of real-time microvision system with 3D integration structure

Figure 1, above, depicts a four-layer device in which each layer has a basic function. Ex. 1006, 832. The four layers include, from top to bottom, (1) an image sensor array, (2) an amplifier and analog–digital (AD) converter, (3) a data latch and masking layer, and (4) a processor array and output circuit. The layers are connected to each other using high-density vertical interconnections; the wafers are bonded together with a technique that uses micro-bumps. *Id.* at 831.

Yu's Figure 2, reproduced below, shows another illustration of the four-layer system:

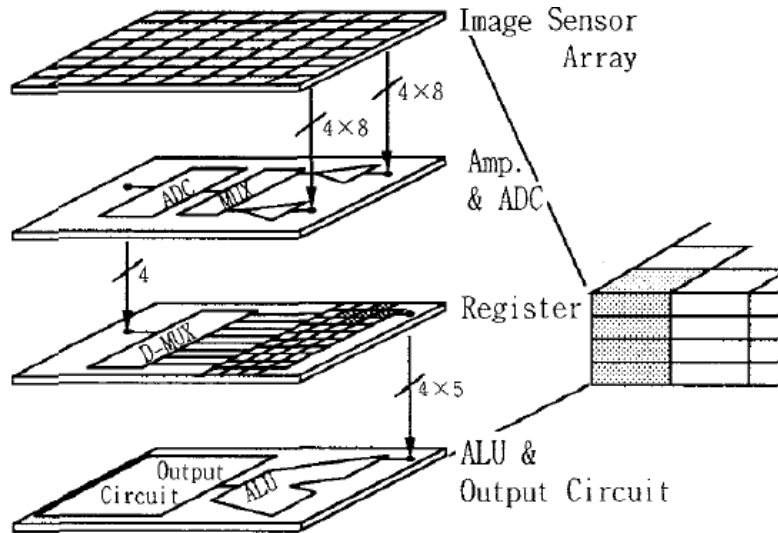


Figure 2: Description of unit system of real-time micro-vision system

Figure 2, above, depicts the same layers as Figure 1. Ex. 1006, 832. The third layer is labeled “Register,” and one of its components is identified as a “D-MUX” (demultiplexer). Within the fourth layer, one of the components is identified as an “ALU” (arithmetic logic unit), and another component is identified as an “Output Circuit.”¹¹

The authors describe an example of using the system to detect edges in video data from the sensor array, using the Laplacian operator. *See id.* at 833–34.

¹¹ According to PACT, a related publication with two overlapping authors describes Yu's chip in more detail, and discloses that the output circuit is formed using “Cu bumps . . . in the back side of the thick Si wafer in order to obtain many output pins.” PO Resp. 21 (emphasis omitted) (quoting H. Kurino et al., *Three-Dimensional Integration Technology for Real Time Micro-Vision System*, 1996 Proc. Innovative Systems in Silicon Conf. 203 (1997) (Ex. 2029)).

(b) Status as a Prior Art Printed Publication

The '549 patent claims priority to an application filed on September 3, 2001. Ex. 1003, 1:10–11. Intel did not contest this date in its Petition. *See* Pet. 9 (“For the purposes of this Petition only, Intel does not contest that the '549 patent is entitled to a September 3, 2001 priority date.”). We do not need to decide the effective priority date of claim 41 for this decision because, for the reasons below, Intel has shown that all asserted references were published before the earliest possible effective filing date of the claimed invention.

In particular, we find that Yu was published in 1996. The heading on Yu’s front page identifies it as a paper for the “1996 IEEE^[12]/SICE/RSJ International Conference on Multisensor Fusion and Integration for Intelligent Systems.” Ex. 1006, 831. Intel argues that Yu “was published by the IEEE in December 1996.” Pet. 4. In support, Intel provides with its Petition a declaration by Gerard P. Grenier, Senior Director of Content Management of the IEEE. Ex. 1007 ¶ 1. Mr. Grenier testifies that “[t]he article and abstract [of Yu] shows the date of publication,” and he states that at the IEEE/SICE/RSJ International Conference on Multisensor Fusion and Integration for Intelligent Systems, copies of the conference proceedings including Yu “were made available no later than the last day of the conference,” which was December 11, 1996. *Id.* ¶¶ 10–11. Finally, he testifies that “[a]s part of its ordinary course of business, IEEE publishes and makes available technical articles . . . for public download through the IEEE

¹² “IEEE” is the Institute of Electrical and Electronics Engineers. Ex. 1007 ¶ 1.

digital library, IEEE Xplore,” and this includes Yu, which “is currently available for public download.” *Id.* ¶¶ 6, 11.

In response, PACT argues that Mr. Grenier’s declaration is insufficient to show that Yu was a printed publication. PO Resp. 56. According to PACT, “There is no explanation as to what happened during the conference, who had access to the conference, and why the International Conference on Multisensor Fusion and Integration for Intelligent Systems related to the relevant art in this case.” *Id.* at 58. PACT also argues that Mr. Grenier came to his position in 1999, and would not likely have personal knowledge about the conference. *Id.* at 60–62 (comparing Mr. Grenier’s testimony in this case with testimony submitted by the petitioner in *Smart Microwave Sensors GmbH v. Wavetronix LLC*, IPR2016-00488, Paper 57 at 27–29 (PTAB July 17, 2017), in which the Board held that the petitioner had failed to show that two references were printed publications).

As to Yu’s public availability on IEEE Xplore, PACT argues that “the paper was added online on August 6, 2002, after the 2001 priority date alleged by [Intel].” PO Resp. 59–60 n.3 (citing Ex. 1007, Ex. A, 1 (“**Date Added to IEEE Xplore:** 06 August 2002”); Pet. 9).

Finally, PACT contends that, other than Mr. Grenier’s declaration, the only evidence that the article was published in 1996 is the line at the bottom of the article reading “0-7803-3700-X/96 \$5.00 ©1996 IEEE,” reflecting an ISBN number and a copyright notice. PO Resp. 58 (citing Ex. 1006, 831).

In response, Intel argues that “PACT chose not to depose Mr. Grenier, and has offered no evidence to challenge Mr. Grenier’s credibility.” Pet. Reply 22. To corroborate Mr. Grenier’s testimony, Intel contends that PACT’s expert, Dr. Mangione-Smith, “admitted that IEEE papers are

routinely presented ‘in front of a crowd,’” “that copies of the papers are distributed at the conference,” and that “members of the public ‘could typically go to IEEE or ACM and pay for a copy of [the paper].” *Id.* at 23 (alteration in original) (quoting Ex. 1048, 70:21, 73:11–12) (citing Ex. 1048, 70:12–72:5, 72:17–73:2, 73:10–20).

Intel also points out that in the related litigation, PACT admitted in response to an interrogatory that the priority date of the ’549 patent “is September 19, 2002, which is after Yu was publicly available online.” *Id.* at 22–23 (citing Ex. 1050, 9 (supplemental response to an interrogatory, identifying September 19, 2002, as the priority date for the ’549 patent)).

Intel also submits what it describes as “a copy of Yu from the physical IEEE publication.” Pet. Reply 23 (citing Ex. 1051 (“Yu physical copy”)). According to Intel, the Yu physical copy was “published in 1996 and bear[s] IEEE, Library of Congress, and ISBN index numbers.” To authenticate this copy, Intel includes a supporting declaration by Rachel J. Watters, a librarian and Head of Research Sharing for the General Library System of Memorial Library in Madison, Wisconsin. Ex. 1054, 1.

In its Sur-reply, PACT argues that Intel’s evidence, including the Yu physical copy and the declaration of Ms. Watters, “is not admissible,” but does not provide any specific argument for why the evidence is not admissible. *See* PO Sur-reply 17. Although PACT objected to the Yu physical copy and the Watters declaration, PACT has not filed any motion to exclude either of these items, so PACT’s objections are not preserved. *See* Paper 24, 2–3, 4 (objecting to Exhibit 1051 on grounds of inadmissibility and to Exhibit 1054 on grounds of untimeliness and inadmissibility); 37 C.F.R. § 42.64(c) (“A motion to exclude evidence must be filed to

preserve any objection. The motion must identify the objections in the record in order and must explain the objections.”).

Having considered the arguments and evidence of both parties, we find that Intel has shown, by a preponderance of the evidence, that Yu was a printed publication before the date of the claimed invention. Our finding is the same regardless of whether the effective priority date of claim 41 is September 3, 2001 (the earliest claimed priority date of the ’549 patent, which Intel accepts for purposes of this proceeding, *see* Pet. 9), or September 19, 2002 (as PACT admits in the related litigation, *see* Ex. 1050, 9), because we find that Yu was a printed publication when it was included in the Yu physical copy published in 1996.

Whether a reference is a printed publication “involves a case-by-case inquiry into the facts and circumstances surrounding the reference’s disclosure to members of the public.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 9 (PTAB Dec. 20, 2019) (precedential) (quoting *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018)). Indicia on the face of the reference, such as a copyright date or ISBN number, “are considered as part of the totality of evidence.” *Id.* at 17–18 (citing *Nobel Biocare Servs. AG v. Intradent USA, Inc.*, 903 F.3d 1365, 1377 (Fed. Cir. 2018)).

The original copy of Yu, submitted with the Petition as Exhibit 1006, provides sufficient indicia on its face to show that the IEEE published Yu in 1996 as part of a physical volume accessible to researchers in the field. In addition to having a copyright notice of 1996, this copy of Yu indicates that it is part of an article in a larger volume (beginning on page 831) identified as “Proceedings,” and it bears the 10-digit ISBN number “0-7803-3700-X”.

We also credit Mr. Grenier’s testimony that the date on the article, 1996, corresponds to the “date of publication.” Ex. 1007 ¶ 10. Despite his lack of personal knowledge as to the preparation and early distribution of the 1996 publication, we find it credible that Mr. Grenier would be familiar with the publication practices of the IEEE in 1996. We also credit the indication in IEEE’s records that Yu was available through IEEE Xplore as early as August 6, 2002, which by PACT’s admission is after the priority date to which the ’549 patent is entitled. Ex. 1007, Ex. A, 1; Ex. 1050, 9.

The other evidence of record further supports this finding, including the admissions of Dr. Mangione-Smith (Ex. 1048, 70:12–72:5, 72:17–73:2, 73:10–20), the Yu physical copy which shows that Yu was found in a physical volume published in 1996 (Ex. 1051), and the accompanying testimony of Ms. Watters, which persuasively authenticates the Yu physical copy (Ex. 1054).

2. *Akasaka*

(a) Overview

Akasaka discloses a 3D integrated circuit used as an image processor. Ex. 1008, 1707. Figure 11, reproduced below, shows an example of this processor:

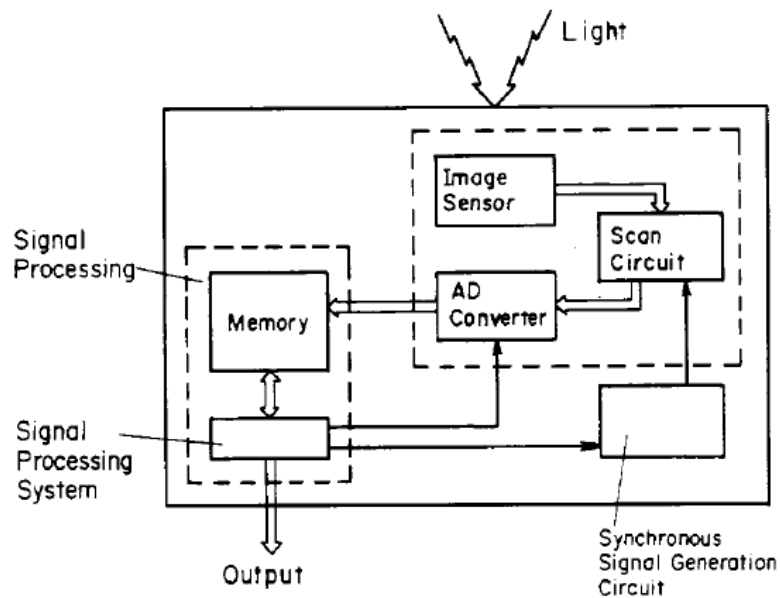


Fig. 11. Schematic block diagram of an image processor system.

Figure 11, above, is a schematic block diagram of an image processor system. Ex. 1008, 1709. As indicated by two dashed-line boxes, the system has two parts: the box on the right includes “a 10-bit linear image sensor, which corresponds to the image sensor in a final 3-D device,” which is associated with a scan circuit and an analog–digital (AD) converter. *Id.* at 1707. The box on the left includes “a 256-bit static RAM” (random access memory), and is part of the signal processing system that includes an “Output” line. *Id.* In the 3D structure, the “video sensor [is] on the top layer, then [the analog–digital] converter, ALU, memory, and CPU [(central processing unit) are] in the lower layers to realize an intelligent image processor in a multilayered 3-D structure.” *Id.* at 1705.

Figure 12, reproduced below, shows the internal structure of the 256-bit static RAM portion of Figure 11:

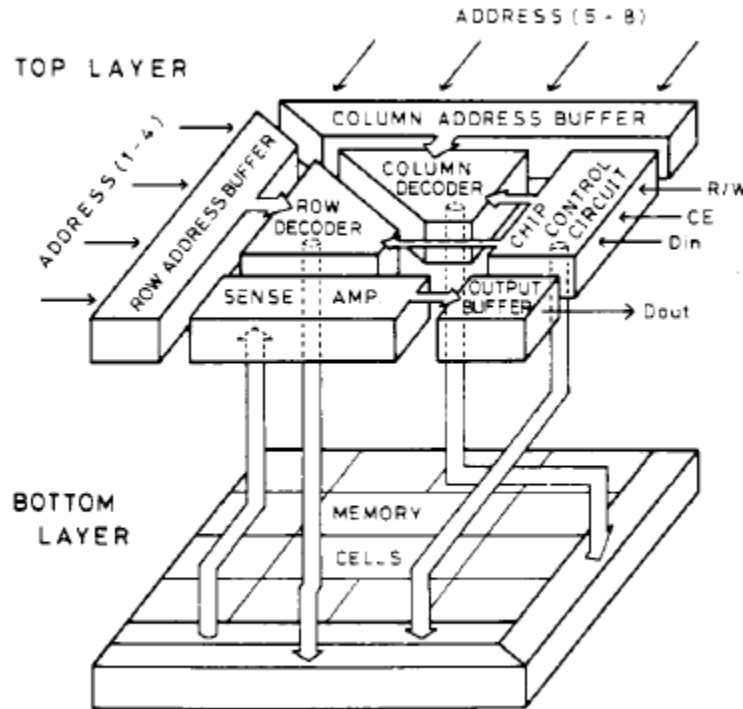


Fig. 12. Block diagram of stacked 256-bit static RAM.

Figure 12, above, is a 3D block diagram in which the blocks represent the components of the static RAM and associated circuitry, and arrows show the flow of information. The image has a top layer and a bottom layer. In the top layer, there is an “output buffer” and an arrow labeled D_{out} , which reflects the output line as shown in Figure 11. *See id.*

(b) Status as a Prior Art Printed Publication

Akasaka is styled as an “Invited Paper” of the “Proceedings of the IEEE,” volume 74, number 12, dated December 1986. Ex. 1008, 1703. To support its contention that Akasaka was a prior art printed publication, Intel submits a declaration by Mr. Grenier, testifying that according to IEEE business records, Akasaka has a publication date of December 1986. Pet. 3

n.2; Ex. 1009 ¶¶ 8–11; *see also* Ex. 1009, Ex. A, 1 (“**Date of Publication:** Dec. 1986”). This evidence is undisputed, and we find, by a preponderance of the evidence, that Akasaka was a printed publication before the date of the claimed invention.

3. *Rathnam*

(a) Overview

Rathnam is a magazine article describing what it calls the “TM-1000,” a “multimedia system on a chip.” Ex. 1010, 108. According to Rathnam, the TM-1000 has “a high-performance [very long instruction word (VLIW)] CPU core,” and is designed to connect to a video input stream via a video decoder chip, and to communicate with a PC. *Id.* Figure 1, reproduced below, depicts the TM-1000 chip:

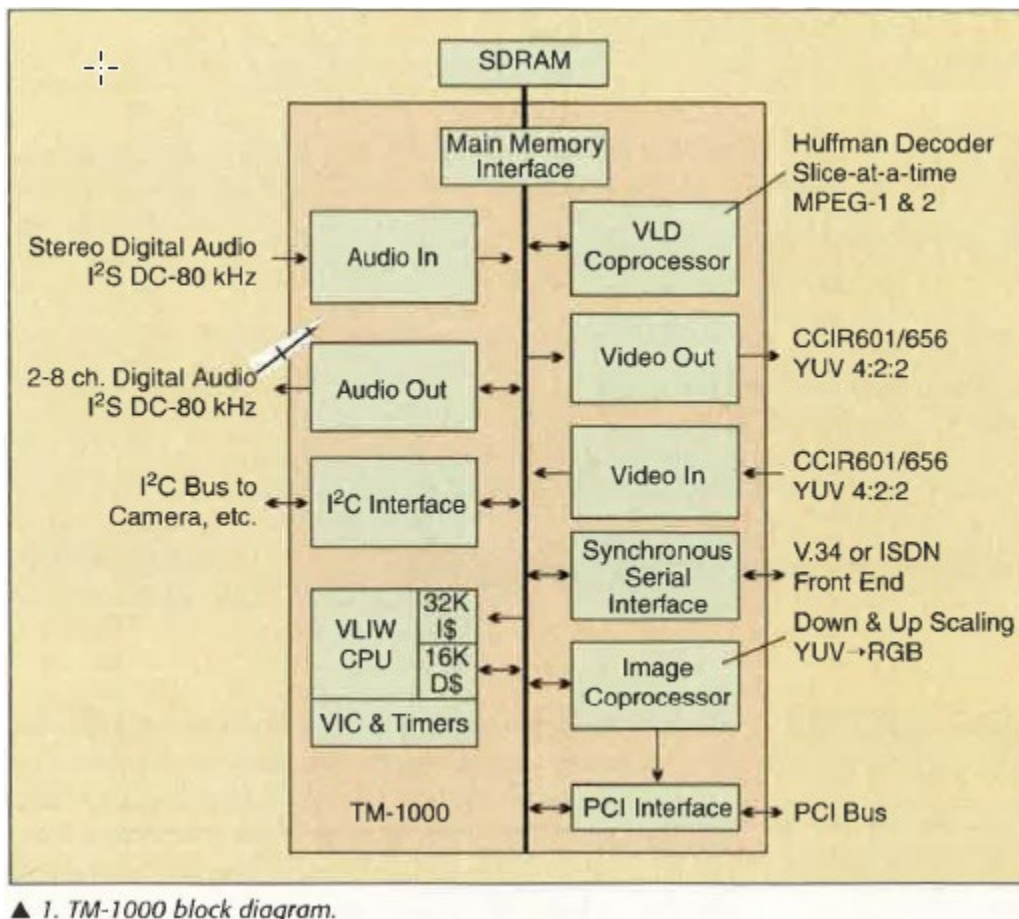


Figure 1 of Rathnam, above, is a block diagram showing parts of the TM-1000 chip, and in the bottom-right corner, there is a “PCI Interface” connected externally to a “PCI Bus.” According to Rathnam, “[t]he glueless PCI interface allows the TM-100 to display video via a host PC’s video card and to play audio via a host PC’s sound hardware.” *Id.* at 109.

(b) Status as a Prior Art Printed Publication

To support its contention that Rathnam was a printed publication, Intel submits a declaration by Mr. Grenier, testifying that according to IEEE business records, Rathnam has a publication date of March 1998. Pet. 3 n.2; Ex. 1011 ¶¶ 8–11; *see also* Ex. 1011 Ex. A, 1 (“**Date of Publication:** Mar. 1998”). This evidence is undisputed, and we find, by a preponderance of the

evidence, that Rathnam was a printed publication before the date of the claimed invention.

4. *Independent Claim 39*

Although PACT has disclaimed independent claim 39 and does not specifically contest Intel’s contentions regarding claim 39, claim 41 inherits its limitations through dependency. Thus, we must consider these limitations in our analysis with respect to claim 41. We find that Intel has shown, by a preponderance of the evidence, that Yu discloses each limitation of claim 39, and also that Yu teaches claim 39 in light of Akasaka.

First, Intel argues that Yu’s device is “[a] processor integrated device,” as recited in the preamble, “because it comprises an array of processors on a die or chip (namely the bottom layer), which is integrated through interconnections to the additional chips stacked on top.” Pet. 29–30 (citing Ex. 1006, 831–33, Figs. 1, 2; Ex. 1001 ¶¶ 85–86).¹³

Next, for the limitation “at least two dies that are stacked,” Intel argues that Yu discloses multiple stacked dies. Pet. 30–32 (citing Ex. 1006, 831–35, Figs. 1, 2, 8; Ex. 1001 ¶ 87).

For the limitation “an interconnect structure,” Intel argues that Yu’s device has an interconnect structure on multiple layers of the device. Pet. 32–34 (citing Ex. 1006, 831–34, Figs. 1–4; Ex. 1001 ¶¶ 88–89).

For the limitation “an arrangement of programmable data processing units interconnected by the interconnect structure,” Intel argues that Yu’s

¹³ Because Intel has shown that Yu discloses the preamble of claim 39, we do not need to resolve, as a matter of claim construction, whether the preamble is limiting.

device has an arrangement of interconnected processors that perform Laplacian operations, which are thus programmable data processing units. Pet. 34–37 (citing Ex. 1006, 831–33, Figs. 1, 2, 4; Ex. 1001 ¶¶ 90–92).

Alternatively, if Yu’s processor is not a “programmable data processing unit,” Intel argues that it would have been obvious to substitute a general purpose processor for Yu’s Laplacian processor, because it is a simple substitution of one known component for another, yielding predictable results and enabling Yu’s system to perform a wider variety of operations. Pet. 36–37 (citing Ex. 1006, 831; Ex. 1001 ¶ 90).

Intel also contends that it would have been obvious to substitute Akasaka’s arrangement of multiple interconnected general purpose processors for Yu’s Laplacian processor because Akasaka teaches that using such processors in parallel would predictably result in faster processing. Pet. 37–39 (citing Ex. 1008, 1703–05, 1712–13, Fig. 25(c); Ex. 1006, 831–32, 834 n.6; Ex. 1001 ¶¶ 93–95).

For the limitation “wherein . . . at least some of the programmable data processing units include Arithmetic Logic Units (ALUs),” Intel contends that at least some of the data processing units in Yu’s fourth layer include ALUs. Pet. 39–41 (citing Ex. 1006, 831–33, Figs. 1–3; Ex. 1017; Ex. 1001 ¶ 96).

Alternatively, Intel argues that Akasaka teaches a plurality of processing elements, including ALUs, and that a person of ordinary skill in the art would have been motivated to substitute these processing elements for those of Yu for the same reasons expressed above for the previous limitation. *See id.* at 40 (citing Ex. 1008, 1705, 1713, Fig. 25(b)–(c); Ex. 1017; Ex. 1001 ¶¶ 97–98).

For the limitation “the interconnect structure includes switches,” Intel argues that Yu’s interconnect structure includes a multiplexer, a demultiplexer, and bus lines that comprise switches. Pet. 41 (citing Ex. 1006, 832; Ex. 1003, 21:50–52 (describing multiplexers as “switching elements”); Ex. 1014, 288, 716 (a dictionary defining a demultiplexer as a switch, and a multiplexer as performing switching operations); Ex. 1001 ¶¶ 99–100).

For the limitation “the programmable data processing units are implemented on at least a first one of the at least two dies,” Intel argues that Yu’s programmable data processing units are implemented on Yu’s lowest die. Pet. 41–43 (citing Ex. 1006, 831–33, Figs. 1, 2; Ex. 1001 ¶ 101).

Finally, for the limitation “at least parts of the interconnect structure are implemented on at least a second one of the at least two dies,” Intel argues that Yu’s interconnect structures, such as the D-MUX and interconnect structures on Yu’s third die, are implemented on a different die than the programmable data processing units on Yu’s lowest die. Pet. 43–45 (citing Ex. 1006, 831–34, Figs. 1–3, 8; Ex. 1001 ¶¶ 102–104).

PACT does not contest the above arguments or evidence. By a preponderance of the evidence, we find that Intel has shown that Yu discloses each limitation of claim 39. We also determine that Yu teaches each limitation of claim 39 in light of the teachings of Akasaka, and that a person of ordinary skill in the art would have been motivated to modify Yu or combine Yu’s teachings with those of Akasaka for the reasons summarized above.

5. *Dependent Claim 40*

Claim 40 depends from claim 39 and further recites “at least one dedicated interface unit that interfaces between the programmable data

processing units and an external device.” Ex. 1003, 1–4. Like claim 39, PACT has disclaimed independent claim 40, but challenged claim 41 inherits the limitation of claim 40 through dependency. Thus, we must consider the limitation of claim 40 in our analysis with respect to claim 41.

Intel argues that the limitation of claim 40 corresponds to Yu’s disclosure of the “Output Circuit” in Figures 1 and 2, reproduced above (*supra* part III.C.1). Pet. 45–47. According to Intel, a person of ordinary skill in the art would have understood this output circuit “to be dedicated to interfacing with an external device like the micro-robot disclosed by Yu.” Pet. 46 (citing Ex. 1001 ¶ 105).

Alternatively, Intel argues that the limitation of claim 40 is “met by the combination of Yu with Akasaka.” Pet. 47. According to Intel, Akasaka’s Figures 11 and 12 (reproduced above in part III.C.2) depict a dedicated output, and a person of ordinary skill in the art “would have looked to Akasaka’s disclosure of how to interface those microprocessors to an external device, thus applying a known technique to improve a known device with a predictable result.” Pet. 47–49 (citing Ex. 1008, 1705, 1707–09, Figs. 11, 12; Ex. 1006, 831–33, 835; Ex. 1001, ¶¶ 106–109).

PACT does not specifically contest Intel’s arguments about the limitation of claim 40. We find that Intel has shown, by a preponderance of the evidence, that Yu discloses the limitation of claim 40. We also determine that a person of ordinary skill in the art would have been motivated to modify Yu’s device to achieve claim 40 based on the teachings of Akasaka, for the reasons summarized above.

6. *Dependent Claim 41*

Claim 41—the claim challenged in this proceeding—depends from claim 40 and further recites “at least one dedicated Peripheral Component Interconnect (PCI) unit.” Ex. 1003, 47:6–7. Intel argues that this limitation is met by Rathnam’s disclosure of “a dedicated PCI interface and a PCI bus, which interfaces between the processor and an external device.” Pet. 57 (citing Ex. 1010, 108–113, 117, Figs. 1, 2; Ex. 1001 ¶ 125).

Citing Dr. Franzon’s testimony, Intel argues that a person of ordinary skill in the art would have understood that “PCI . . . would enhance performance and speed,” Pet. 58 (citing Ex. 1001 ¶ 126), and that using PCI “would yield a predictable and beneficial result, namely compatibility that is driven by application of a technical standard,” Pet. 59 (citing Ex. 1010, 108; Ex. 1001 ¶ 130).

In particular, Intel argues that a person of ordinary skill in the art “would have recognized that Yu’s microvision system was designed to interface with a multitude of external devices, with examples including ‘high level processors,’ ‘some visual devices,’ [and] ‘conventional input devices.’” Pet. 59 (citing Ex. 1001 ¶ 126; Ex. 1006, 831, 835). According to Intel, a skilled artisan “would also have recognized Yu’s stated goal to perform high-speed image processing in real time.” Pet. 60 (citing Ex. 1001 ¶ 128; Ex. 1006, 831). And Intel argues that “Akasaka also discloses a desire to achieve improved performance and speed.” *Id.* (citing Ex. 1008, 1703–05, 1713). Thus, according to Intel, a person of ordinary skill in the art would have “looked to the teachings of Rathnam, which discloses a ‘high-performance’ system ‘designed to concurrently process video, audio,

graphics, and communication data,’ and combined them with Yu and Akasaka.” *Id.*

Intel also argues that, because a person of ordinary skill in the art would have known that both Yu and Akasaka “would predictably benefit from use of a PCI interface,” the ordinarily skilled person “would have been motivated to modify the disclosures of Yu and Akasaka with the more specific disclosure of Rathnam to add a PCI interface, particularly because both are in the same field of image processing and PCI would enhance performance and speed a[s] explained above.” Pet. 60–61. According to Intel, “PCI was one of a finite number of identified, predictable techniques for interfacing hardware devices within a computer with a reasonable expectation of success.” Pet. 62 (citing Ex. 1001 ¶ 129).

In response, PACT makes the following four general arguments, which we address in turn below: (1) that Intel has failed to show that a person of ordinary skill in the art would have had a reason to combine Yu with Rathnam, PO Resp. 13–28, 44–47; (2) that there would have been a reasonable expectation of success in the combination, *id.* at 47–51; (3) that Intel bases its argument to combine the two references on impermissible hindsight, *id.* at 24–25; and (4) that Intel’s combination fails to achieve a PCI “unit,” PO Sur-reply 1–16.

(a) Motivation to Combine

PACT argues that a person of ordinary skill in the art would not have had reason to substitute a PCI interface, as Rathnam teaches, for Yu’s output circuit. *See* PO Resp. 13–28, 44–47.

First, relying on the testimony of Dr. Mangione-Smith, PACT contends that “the PCI Interface . . . is incompatible with the output interface

in Yu” because it lacks card and slot connectors. *Id.* at 19–20 (citing Ex. 2027 ¶¶ 28–49). According to PACT, a PCI interface “uses a ‘slot’ on the bus side and a PCI card on the chip/equipment side.” *Id.* at 13–14 (citing Ex. 2027 ¶ 28). As an example of such a PCI card, PACT provides Figure 1, which we reproduce below with further annotation added by Intel in its Reply:

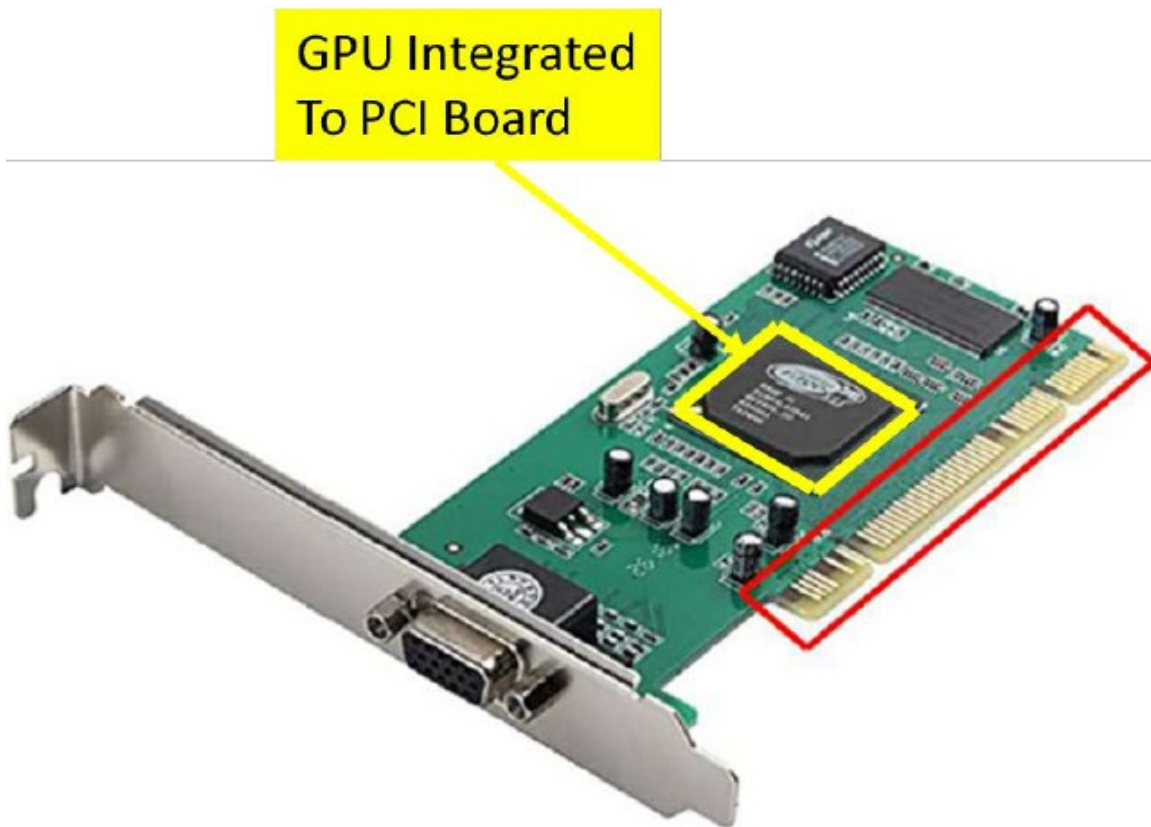
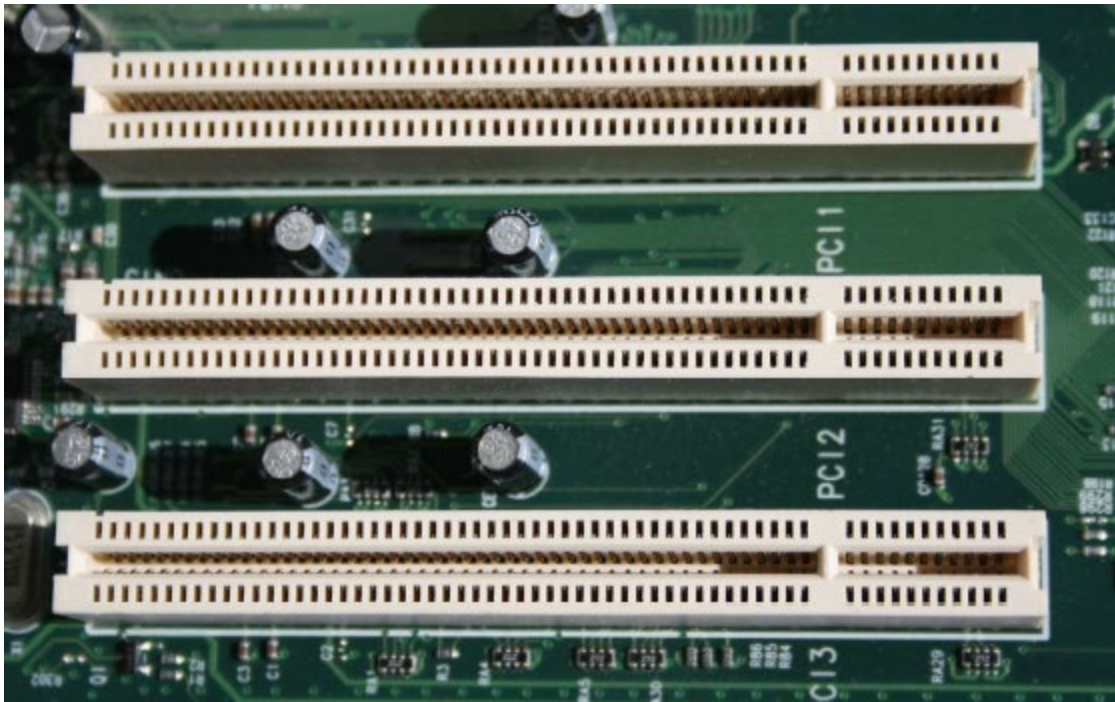


Figure No. 1¹

Pet. Reply 8; *see* PO Resp. 15. PACT’s Figure 1, above, is an annotated version of an ATI Rage XL PCI graphics card taken from the Amazon.com website (Ex. 2031). PO Resp. 14 (citing Ex. 2027 ¶ 28). PACT identifies the PCI interface (a series of parallel conductors protruding from the card) by a

red box. *Id.* In yellow, Intel further identifies a graphics processing unit (GPU) integrated to the PCI-compliant board. *See* Pet. Reply 7–8.¹⁴

As an example of a PCI slot on the bus side, PACT provides Figure 3, which we reproduce below:



PO Resp. 16. According to Dr. Mangione-Smith, Figure 3, above, is taken from the Wikipedia article for “Peripheral Component Interconnect,” and in his view, “accurately depicts the PCI interface around the time of the ’549 invention.” Ex. 2027 ¶ 30 n.3 (citing *Peripheral Component Interconnect*, Wikipedia, https://en.wikipedia.com/wiki/Peripheral_Component_Interconnect (last visited July 29, 2021)). Figure 3 shows three slots, each with parallel conductors inside the slot mirroring the conductors of the card interface in Figure 1.

¹⁴ PACT did not object to Intel’s further annotation in yellow, and reproduced Intel’s annotated version in its Sur-reply. *See* PO Sur-reply 3.

PACT contrasts this physical PCI interface with the physical interface described in Yu, which comprises copper bumps formed on the back side of a thick silicon wafer. PO Resp. 21 (citing Ex. 2029, 205 (a paper relating to the same research project described in Yu)). According to PACT, “because of the special design of the 3D image chip in Yu, it can only use copper bumps to form outlet pins at the bottom of the chip.” *Id.* (citing Ex. 2027 ¶¶ 35–37); *see also id.* at 27 n.2 (arguing that Akasaka discloses a similar bump interface to Yu (citing Ex. 1008, 1704)).

Thus, PACT argues that Intel’s obviousness ground is insufficient because Intel failed to “compare the PCI interface disclosed in Rathnam with the output circuit interface disclosed in Yu,” which “are completely different.” PO Resp. 27. According to PACT, these differences include that “Yu relies upon a two dimensional rectangular array of closely space[d] copper bumps that are used to permanently mate two chips together,” whereas the PCI interface “covers very precise constraints on [the] physical form factor, such as how many pins must be placed on a PCI card, where those pins must be placed relative to each other, [and] how thick the card must be, etc.” *Id.* at 28 (emphasis omitted) (quoting Ex. 2027 ¶¶ 41, 43). PACT alleges that “the standardized PCI interface cannot be adapted to copper bumps, and copper bumps cannot be inserted into PCI slots.” *Id.* at 29 (citing Ex. 2027 ¶ 43). Further, according to PACT, it was “unknown to a [person of ordinary skill in the art] at the time of the invention of the ’549 patent how to implement [a] PCI interface through copper bumps.” *Id.* at 29–30 (citing Ex. 2027 ¶ 44). And PACT cites testimony by Dr. Mangione-Smith that the result of combining Yu with Rathnam “is not predictable and desirable” because an ordinarily skilled artisan lacked the necessary

knowledge and “it would [have taken] a significant amount of time and money to research, and such result is not desirable.” *Id.* at 30–31 (citing Ex. 2027 ¶¶ 44–45).

In response, Intel makes two main arguments. First, Intel argues that, “as PACT’s expert [Dr. Mangione-Smith] concedes, no physical card slot is necessary, as PCI can be implemented ‘in an embedded device,’ e.g., ‘one chip,’” Pet. Reply 2 (citing Ex. 1048, 46:14–47:18), and “in a way that ‘doesn’t use the physical card slots,’” *id.* at 6 (citing Ex. 1048, 13:21–14:4; Ex. 1049 ¶¶ 4–6); *see also id.* at 7 (citing Ex. 1048, 50:15–20 (“[Question by counsel:] . . . [I]n 2001, a person of ordinary skill in the art would know that there’s such a thing as embedded PCI that didn’t use slots; correct? [Answer by Dr. Mangione-Smith:] Yes. I think that’s accurate.”)); Ex. 1010, 108 (“TM-1000 can be placed directly on the PC main-board . . .”).

We find Intel’s first argument and cited supporting evidence persuasive. The evidence shows that a person of ordinary skill in the art at the time of the claimed invention would have been able to implement a PCI unit directly on a chip without the use of a physical card-and-slot configuration.

Intel’s second response to PACT’s argument is that even if a PCI unit required a physical card and slot as PACT contends, connecting a stacked die with a PCI card was well within the ordinary skill in the art at the time of the claimed invention. *See* Pet. Reply 2. Intel disagrees with PACT that there would have been any difficulty in combining prior art stacked dies, like that of Yu, with a PCI interface, because this combination would consist of “chips of varying configurations that are attached to a PCI-compliant card, which is then slotted into a PCI card slot,” like the GPU attached to the PCI-

compliant video card shown above in PACT’s Figure 1 (reproduced above, GPU annotated in yellow). *Id.*; *see also id.* at 7–8 (citing Ex. 1049 ¶ 7). Intel argues that Rathnam, itself, teaches such a configuration in which the video processor chip can “gluelessly interface to the standard PCI bus,” including through a “plug-in card” like that in PACT’s Figure 1. *Id.* at 8 (quoting Ex. 1010, 108).

Intel also argues that in his deposition, Dr. Mangione-Smith made the following two concessions: (1) that “Yu’s chip contains external bumps that can . . . be directly electrically connected to a PCI board”; and (2) “that a 2D output array can be connected to a linear PCI edge connector, and that a chip like Yu’s can be connected to a PCI edge connector even if it is smaller than the edge connector.” Pet. Reply 9 (citing Ex. 1048, 33:13–35:16; Ex. 1049 ¶¶ 7–8).

We find Intel’s second argument and cited supporting evidence persuasive, and agree with Intel that a person of ordinary skill in the art would have been able to incorporate a stacked chip such as that of Yu or Akasaka into a PCI card by mounting the chip to a PCI board analogously to the graphics card shown in PACT’s Figure 1.

Next, PACT contends that Intel’s argument in the Petition is conclusory because it “provides no evidence as to how to adapt this industry standard interface to fit the copper bumps interface in Yu.” PO Resp. 28. Similarly, PACT contends that Intel’s alleged motivation to combine Yu with Rathnam is conclusory because Intel “does not indicate why that combination result is allegedly predictable.” *Id.* at 30. PACT also argues that Dr. Franzon “provides the same conclusory statements, without pointing to

any supporting evidence.” *Id.* at 31 (citing Ex. 1001 ¶ 129; 37 C.F.R. § 42.65(a)).

In response, Intel argues that the ’549 patent “contains no disclosure of how to implement PCI . . . , instead merely assuming that a [person of ordinary skill in the art] would be familiar with such known standards and would know how to implement them.” Pet. Reply 1. Intel identifies only four brief references to PCI in the ’549 patent, none of which provide any specific details about how to incorporate PCI into a stacked chip. *Id.* at 4–5 (citing Ex. 1003, 5:29–33, 19:61–65, 24:6–10, 30:22–27). Intel also contends that “by the time of the ’549 Patent, the PCI standard was well-publicized and in common use across many applications, including the graphics-focused implementations like those described in Yu, Rathnam, and Franzon.” *Id.* at 6–7 (citing Ex. 1010, 1009; Ex. 1049 ¶¶ 4–7).

We disagree with PACT’s argument. The evidence shows that at the time of the claimed invention, PCI was a well-known, conventional technology, and references like Rathnam (like the ’549 patent itself) did not need to provide a person of ordinary skill in the art with any specific details about how to use PCI as the external interface to a video processing chip. This is consistent with the relatively high level of ordinary skill in the art (a Master of Science degree in Electrical Engineering and at least one year of industry experience in computer chip design and semiconductor fabrication or preparation of chip designs for fabrication). *See supra* part III.A (citing Pet. 10). Thus, we find that Intel has met its burden to show a specific motivation to combine Yu with Rathnam, which does not require providing a detailed technical explanation as to how a person of ordinary skill would

have used PCI as the external interface in Yu, as this was well known in the art at the relevant time frame.

Next, PACT argues that “Akasaka expressly admitted that ‘it is not well known what kinds of systems can best be realized in 3-D ICs as opposed to 2-D ICs.’” PO Resp. 31 (quoting Ex. 1008, 1704). PACT then infers that “it is not well known whether a PCI unit can best be realized in 3-D IC.” *Id.*

We disagree with PACT’s inference. Since Akasaka itself discloses a 3D IC, such devices were known in the art as of its publication in 1986. The portion of Akasaka quoted by PACT only suggests that the best applications for (known) 3D stacked chips were not well understood at that time. *See* Ex. 1008, 1704. The evidence shows, however, that a person of ordinary skill in the art would have known, from at least Yu and Akasaka, that it was desirable for 3D stacked chips, used for video processing, to have a dedicated external interface. *See* Ex. 1006, Figs. 1, 2; Ex. 1008, 1709 Figs. 11–12. PACT has not pointed to any evidence that Akasaka teaches away from any particular type of external interface such as PCI.

Next, PACT argues that Intel has failed to show that Yu, Akasaka, and Rathnam are in the same field, such that a person of ordinary skill in the art would have looked to Rathnam’s disclosure of PCI to modify Yu and Akasaka. PO Resp. 31–34 (citing Pet. 60–61). According to PACT, Intel’s analysis “ignores a key difference between Yu and Rathnam,” which is that Yu has an image sensor on its top surface, so it must use a copper bump interface on the bottom substrate of the 3D device, whereas “the image processor[] in Rathnam includes both a VLIW CPU core and an image coprocessor, and it is designed to perform MPEG image decoding and

reconstruction, and does not have a special requirement regarding the interface.” *Id.* at 32 (citing Ex. 2029, 205; Ex. 1010, 113). In its Sur-reply, PACT also points out that in Rathnam’s graphics chip, “the PCI Interface is separate and distinct from the image coprocessor.” PO Sur-reply 10 (citing Ex. 1010, Fig. 1).

PACT further contends that “Rathnam is used for decoding dense video streams,” and “includes a powerful programmable VLIW processor,” whereas “Yu is targeted at analysis of unencoded optical images being sensed in real-time,” and “only requires very simple ALU circuitry.” *Id.* at 33. Thus, PACT contends that Yu and Rathnam are not within the same problem domain.¹⁵ *See* PO Resp. 33–34 (citing *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017)).

In *Securus*, the Federal Circuit held that “a broad characterization of [two prior art references] as both falling within the same alleged field . . . , without more, is not enough for [a petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion.”

¹⁵ PACT does not specifically contend that either Yu or Rathnam is non-analogous to the claimed invention. For clarity, we agree with Intel, and credit Dr. Franzon’s testimony, that both references are analogous art because they are within the field of “image processing.” *See* Pet. 61; Ex. 1001 ¶ 129. In addition, we find that the references are reasonably pertinent to the problem of providing a connection between an image processing chip and an external device. *See In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004); *see also* Ex. 1003, 5:20–38 (the PCI interface may allow connection to peripheral devices such as memories), 19:52–20:5 (same); Ex. 1006, 832 (The output circuit allows processed data to be “transferred to high level processors or some visual devices using 2D or 1D interconnections.”); Ex. 1010, 109 (“The glueless PCI interface allows the TM-1000 to display video via a host PC’s video card . . .”).

Securus, 701 F. App’x at 977 (citing *Microsoft Corp. v. Enfish, LLC*, 662 F. App’x 981, 990 (Fed. Cir. 2016)). But unlike the petitioner in *Securus*, Intel’s argument does not rely solely on a broad characterization of Yu, Akasaka, and Rathnam as being in the same field. As we discuss above, Intel has identified specific reasons why it contends a person of ordinary skill in the art would have selected PCI as the output interface in Yu or Akasaka (for example, because PCI is an industry standard interface known to be suitable for transferring data from an image processing chip to a PC), and supports that rationale with testimonial evidence. *See* Pet. 57–63; Ex. 1001 ¶¶ 126–129.

As to PACT’s focus on particular details of Yu (e.g., the image sensor on the top surface and copper bumps on the bottom surface) or Rathnam (e.g., the VLIW CPU core and image coprocessor) that PACT contends are incompatible with each other, Intel argues that it “does not seek to bodily incorporate Yu and/or Akasaka with Rathnam, but rather to combine the chips of Yu and/or Akasaka with the teaching of Rathnam that such chips could easily be combined with the known, standardized, and popular PCI interface.” Pet. Reply 13. Also, according to Intel, “[t]hat Yu and Rathnam perform different functions with different types of processors . . . is also irrelevant, as the claims include no limitations regarding the types of processors or functions performed.” *Id.* at 15.

Intel also argues that in combining Yu with Rathnam, “the issue is not whether Yu’s microbumps can be interfaced to a PCI card slot . . . —but whether a [person of ordinary skill in the art] would have found it obvious to substitute a PCI interface, as known in the art, for Yu’s output circuit.” Pet. Reply 14. Intel contends that “Yu does not limit its output interface to any

specific implementation or external connectivity, but rather gives the flexibility of choosing a desired output interface for implementing its stacked-die chip (disclosing a generic ‘output circuit’).” *Id.* (citing Ex. 1006, Figs. 1–2).

We find Intel’s arguments persuasive. To establish a persuasive reason to combine in support of an obviousness showing, Intel need not show that Yu and Rathnam are physically combinable or compatible, or are otherwise physically similar; rather, Intel need only show that Rathnam motivates a person of ordinary skill in the art to select PCI for Yu’s external interface. *See In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) (“[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review.”); *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973) (“Combining the teachings of references does not involve an ability to combine their specific structures.”).

Next, PACT argues that Intel has failed to show that the alleged advantages of Rathnam are due to PCI, rather than Rathnam’s other features. PO Resp. 34–35. According to PACT, these other features include “a full-blown VLIW CPU that runs ‘high-quality video and audio applications . . . using high-level languages such as “C” and “C++.””” *Id.* at 34 (alteration in original) (quoting Ex. 1010, 108). PACT contends that it is this VLIW core that is responsible for Rathman’s “high performance,” and Rathnam does not discuss the performance of the PCI interface. *Id.* at 35 (citing Ex. 1010, 108).

We find this argument unavailing. Although we agree that Rathnam does not explicitly attribute its high performance and speed to the use of PCI, Intel also relies, independently, on Dr. Franzon’s unrebutted testimony

that PCI was known at the time of the claimed invention to “enhance performance and speed.” Ex. 1001 ¶ 129. Dr. Franzon also testifies that a person of ordinary skill in the art would have known that PCI “is beneficial because it increases the number and type of third party products that can be interfaced with the system, particularly storage systems,” which “would increase the marketability of the resulting vision system.” *Id.* (citing Ex. 1010, 108); *see also* Pet. 59 (arguing that an ordinarily skilled artisan would have recognized “a predictable and beneficial result, namely compatibility that is driven by application of a technical standard”). PACT does not present evidence to rebut this testimony, and we find it persuasive.

Next, PACT argues that Intel “provides no explanation at all as to why a [person of ordinary skill in the art] would select the PCI protocol among other bus protocols.” PO Resp. 36. PACT cites a textbook stating that there were so many bus standards available in 1999 that “[t]he world would probably be a better place if all but one would suddenly vanish.” *Id.* (quoting Ex. 2003, 158). PACT also argues that “Rathnam itself discloses other interface options for image signals.” *Id.* (citing Ex. 1010, Fig. 1). According to PACT, neither Intel nor Dr. Franzon presents evidence comparing PCI to other bus techniques. *Id.* (citing Pet. 60; Ex. 1001 ¶¶ 128–129).

We disagree with this argument. Intel does not need to establish that PCI was the best possible output interface for the devices in Yu or Akasaka; rather, Intel need only show that a skilled artisan would have had reason to use PCI in Yu or Akasaka for its established function. *See KSR*, 550 U.S. at 417 (“[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.”). In addition, the mere existence of many suitable bus interfaces

does not make the selection of any one of them less obvious. *See Merck & Co. v. Biocraft Labs., Inc.*, 874 F.2d 804, 807 (Fed. Cir. 1989).

Next, PACT argues that Intel has made an insufficient obvious-to-try argument, by omitting evidence that there was “(1) a design or market need to solve a particular problem, and (2) that ‘there are a finite number of identified, predictable solutions’ that would lead to an expectation of success.” PO Resp. 37 (quoting *Grunenthal GMBH v. Alkem Labs. Ltd.*, 919 F.3d 1333, 1345 (Fed. Cir. 2019)). PACT also contends that Intel “does not identify any ‘particular problem’ in Yu or Akasaka that relates to their output circuits,” and “[i]n fact, the output circuits in Yu and Akasaka seem to work just fine for their purposes.” *Id.* (citing Ex. 1006, 832; Ex. 1008, 1710).

In response, Intel argues that “there need not be any particular problem with Yu or Akasaka for a [person of ordinary skill in the art] to migrate to an industry standard; such standards provide compatibility, creating a ‘market need’ for their implementation.” Pet. Reply 16 (citing Ex. 2003, 157–58 (expressing the view that “[t]he world would probably be a better place” if the computer market coalesced around a single bus standard among a list that includes PCI)).

We find Intel’s argument and cited supporting evidence persuasive that at the time of the claimed invention, there was a market need for using a standardized bus interface to solve the problem of numerous incompatible systems, that PCI was one of a finite number of such standards that were available in the industry at the time, and that PCI was a predictable solution to that standardization problem, which could be implemented by a person of ordinary skill in the art. Thus, Intel’s argument on this basis weighs in favor of obviousness. *See KSR*, 550 U.S. at 421 (“When there is a design need or

market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.”).

Next, PACT argues that Intel failed to cite paragraphs 133–138 of Dr. Franzon’s declaration relating to the motivation to combine, so we should disregard that testimony. PO Resp. 44–47 (citing *Fidelity Nat’l Info. Serv., Inc. v. Datatransury Corp.*, IPR2014-00491, Paper 9 at 8 (Aug. 13, 2014)).

We do not find this argument persuasive because although paragraphs 133–138 of Dr. Franzon’s declaration are not cited in the Petition, they essentially correspond to arguments made in the Petition, as PACT acknowledges. *See* PO Resp. 46 (“The uncited testimony repeats the same conclusory arguments in the Petition without adding any underlying evidence or data.”). Also, the thrust of Dr. Franzon testimony in these paragraphs, as it relates to claim 41, is essentially the same as testimony found in other parts of his declaration that Intel cites in its Petition. *Compare* Ex. 1001 ¶¶ 135–136, *with* ¶¶ 126–129, *and* Pet. 58–62 (citing Ex. 1001 ¶¶ 126–129). Thus, even without the testimony that appears in paragraphs 133–138, Intel has cited portions of Dr. Franzon’s declaration sufficient to show that a person of ordinary skill in the art would have had reason to combine Yu with Rantham’s teachings.

Next, PACT takes issue with Dr. Franzon’s reference to the “PCI Local Bus Specification,” which Intel did not file as an exhibit in this proceeding. *Id.* at 46 (citing Ex. 1001 ¶ 135).

We do not find this argument persuasive. Dr. Franzon cites the PCI Local Bus Specification in an attempt to show that it “refers to the PCI as a

‘standard’ multiple times.” Ex. 1001 ¶ 135.¹⁶ This is a minor point, and not critical to Intel’s presentation, because PACT does not dispute that PCI is an industry standard. *See* PO Resp. 46 (arguing that the text that Dr. Franzon quotes in the PCI Local Bus Specification “ignores that there are many competing standards [than PCI]”); *id.* at 28 (agreeing with Intel that “PCI is an ‘industry standard’” (quoting Pet. 58)). Thus, we do not find PACT’s argument to be a persuasive rebuttal to Dr. Franzon’s overall testimony as to the motivation to combine Yu with Rathnam.

Finally, in its Sur-reply, PACT argues that Intel “bases its conclusions on what ‘could’ be done, not what ‘would’ be done, which is insufficient.” PO Sur-reply 11 (citing PO Reply 17; Ex. 1049 ¶ 5; *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1360–61 (Fed. Cir. 2019)).

We disagree with this argument because although Intel and Dr. Franzon do argue that Yu “can” be modified by using a PCI interface, Intel also clearly and persuasively argues that a person of ordinary skill in the art *would have been motivated* to make the proposed changes to Yu, based on the teachings of Rathnam. *See, e.g.*, Pet. 58–62; Pet. Reply 16 (“[T]he Petition asserts that Rathnam’s specific disclosure of PCI could be combined with Yu and/or Yu and Akasaka, and a [person of ordinary skill in the art] would be motivated to do so.”). Thus, we find that Intel has shown that there would have been a motivation to combine Yu with the teachings of Rathnam, with or without Akasaka.

¹⁶ Intel responds to PACT’s argument by pointing out that this PCI specification “is cited as known prior art on the face of the ’549 patent, and is dated 1995.” Pet. Reply 17 (citing Ex. 1003, 13). But this citation’s appearance in the ’549 patent does not help substantiate the point that Dr. Franzon was trying to make in his declaration.

(b) Reasonable Expectation of Success

PACT argues that Intel has failed to establish a reasonable expectation of success in combining Yu or Akasaka with Rathnam. PO Resp. 47–51. According to PACT, Intel’s argument as to the reasonable expectation of success consists of only a single conclusory sentence in conjunction with its obvious-to-try argument, which is insufficient. *Id.* at 49–50 (citing Pet. 62; *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1383 (Fed. Cir. 2019)). PACT also argues that a person of ordinary skill in the art “would not have known how to implement [a] PCI interface through either copper bumps or flip chips.” *Id.* at 50 (citing Ex. 2027 ¶¶ 41–51).

In response, Intel cites a passage in the Petition arguing that “using PCI (a known technique) to interface Yu’s known microvision system with external devices would yield a predictable and beneficial result, namely compatibility that is driven by application of a technical standard.” Pet. Reply 20 (citing Pet. 58–59). Intel also contends that its argument that there was a reasonable expectation of success, as part of its obvious-to-try argument, is also applicable to its general argument that a person of ordinary skill in the art would have combined Yu with Rathnam. *Id.* at 20–21 (citing Pet. 62).

We disagree that Intel failed to show a reasonable expectation of success in combining Rathnam’s teachings with Yu or Akasaka to achieve the device of claim 41. Intel submits testimonial evidence that PCI was a well-known industry standard at the time of the claimed invention. *See* Ex. 1001 ¶¶ 40, 126, 129. Especially given the relatively high level of ordinary skill in the art, we find by a preponderance of the evidence that a

person of ordinary skill would reasonably expect to succeed in adapting Yu's device to use a PCI interface according to claim 41.

(c) Alleged Impermissible Hindsight

Citing the '549 patent, Intel argues in its Petition that a person of ordinary skill in the art "would have understood implementing PCI to be beneficial because conforming to an industry standard would 'permit simple and cost-effective connection of the peripheral devices.'" Pet. 58 (quoting Ex. 1003, 5:29–33).

PACT argues that it is improper for Intel to rely on the '549 patent itself as part of the alleged motivation to modify Yu with a PCI interface. PO Resp. 24–25 (citing *Millennium Pharm., Inc. v. Sandoz Inc.*, 862 F.3d 1356, 1367 (Fed. Cir. 2017)). PACT also contends that Intel mischaracterizes that quote from the '549 patent.

We need not determine whether Intel's citation to this passage in the '549 patent is impermissible hindsight because we do not rely on this passage for teaching a motivation to combine Yu with Rathnam. Rather, as discussed above in part III.C.6(a), we find that Intel has shown a motivation to combine based on the teachings of Yu in light of Rathnam or in light of Rathnam and Akasaka.

Nor does Intel rely solely on this passage to show that PCI was a predictable industry standard with enhanced performance and speed. *See In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971) (A reconstruction based on hindsight reasoning is proper "so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made and does not include knowledge gleaned *only* from applicant's disclosure" (emphasis added)). Instead, Intel relies

primarily on Rathnam and the testimony of Dr. Franzon. *See* Pet. Reply 10 (“Intel’s Petition relies on both Rathnam’s express teaching of PCI . . . , and the general undisputed knowledge of a [person of ordinary skill in the art]” (citing Pet. 57–63)); *see also* Ex. 1001 ¶ 129 (“PCI would enhance performance and speed” in Yu’s device, and “[t]his would have yielded a predictable and desirable result of efficiently connecting Yu’s microvision system with an external device.”); *id.* (An ordinarily skilled artisan would have known that “using a standard-based interface is beneficial because it increases the number and type of third[-]party products that can be interfaced with the system, particularly storage systems,” thus “increas[ing] the marketability of the resulting vision system.” (citing Ex. 1010, 108 (Rathnam teaching that PCI allows an image processor to interface “directly on the PC main-board or on a plug-in card”))).

Thus, we do not agree that Intel’s arguments and evidence are insufficient to show obviousness because of impermissible hindsight.

(d) PCI “Unit”

In its Sur-reply, PACT argues that Intel’s Petition fails to identify a PCI “unit” as recited in claim 41, and “attempts to bypass the structural limitations of the PCI ‘unit’ by conflating PCI ‘unit’ with PCI ‘interface.’” PO Sur-reply 1–16.¹⁷

First, PACT presents cross-examination testimony from its expert, Dr. Mangione-Smith, that in devices such as the PCI graphics card in PACT’s

¹⁷ PACT made this argument for the first time in its Sur-reply, and could have made the argument in its Patent Owner Response. However, Intel did not file a motion to strike, and addressed this argument—at least to some extent—in the oral hearing. *See, e.g.*, Tr. 74:7–75:25, 80:6–21.

Figure 1, “what typically is going to happen is that there will be something called the *bus interface unit that changes . . . the electrical signals from one side, such as a graphics chip, to the other side, such as the PCI,*” and “that bus interface unit, in many cases, *will be off of that graphics chip.*” PO Sur-reply 3–4 (quoting Ex. 2027, 25:12–22).

In contrast to this configuration that uses a separate chip for PCI processing, PACT argues that the ’549 patent discloses an embodiment of an interface unit (e.g., a PCI unit), called an “IO management unit” or “IOAG,” which “can be on a different stacking layer than the ALUs in a 3D stacked processor.” PO Sur-reply 4 (citing Ex. 1003, 24:13–14, 21:45–50).

According to PACT, an array of processing elements (PAEs) can be more efficient if each PAE only has a small IO interface with a simple internal bus protocol, which is connected to external units through IOAGs that can be “much larger and more complex.” *Id.* at 5 (emphasis omitted) (quoting Ex. 1003, 24:11–24). Each IOAG can have its own sequencer, microcontroller, memory, address translation units, and interrupt controllers. *Id.* at 5–6 (citing Ex. 1003, 24:25–32). PACT contends that this disclosure about IOAGs “rebut[s] [Intel’s] statement that ‘the ’549 Patent does not identify or solve any problems in implementing a PCI interface, nor provide any PCI implementation details.’” *Id.* at 6 (quoting Pet. Reply 4).

We disagree that the ’549 patent’s disclosure of IOAGs provides any implementation details specific to the PCI standard. Although the ’549 patent states that an IOAG can optionally be used to implement PCI or other protocols, such as RapidIO, Firewire, USB, Ethernet, RAMBUS, or DDR-RAM, *see* Ex. 1003, 5:29–37, 19:61–20:2, PACT does not point to any

disclosure in the '549 patent describing any particular structure or logic that would be necessary to implement PCI in particular.

Next, PACT argues that Intel and its expert, Dr. Franzon, have admitted that to implement a PCI interface, one could simply attach Yu's chip to a PCI card without including a PCI unit in Yu's chip itself. *See* Sur-reply 6–8 (citing Pet. Reply 7; Ex. 1048, 57:6–10; Ex. 1049 ¶ 7–8). This, according to PACT, “negates [Intel]’s obviousness theory of *substituting* a PCI interface in place of Yu’s . . . output circuits.” *Id.* at 8 (citing Pet. Reply 14, 17–18). PACT contends that “simply electrically connecting the Yu . . . chip[] on a PCI board” does not achieve a “processor integrated device” comprising a PCI “unit,” as recited in claim 41. *See id.* at 8–9.

PACT’s argument in the Sur-reply assumes that we must construe the term “processor integrated device” in claim 41 to be a single-chip structure, an issue the parties have not addressed in the briefing and was not suggested until PACT’s Sur-reply.¹⁸ But we do not need to decide this claim construction issue. In addition to alternatively proposing to modify Yu by attaching it to a PCI card, Intel primarily argues that a person of ordinary skill in the art would have modified Yu by selecting PCI as the protocol for the “output circuit” on the bottom layer of Yu’s stacked chip, as shown in Yu’s Figure 2. *See* Pet. 61–63; Pet. Reply 6–7; Ex. 1049 ¶ 5. In the oral hearing, Intel reiterated that this as its main rationale for combining Yu with

¹⁸ In the oral hearing, counsel for Intel questioned whether claim 41 requires the PCI unit to be on either of the two stacked dies, but argued that the issue did not matter, since Intel is proposing to modify Yu by placing the PCI unit on its bottom layer. *See* Tr. 75:8–25.

Rathnam. Tr. 74:7–75:25, 80:6–21. As we discuss above, we find this rationale persuasive. *See supra* part III.C.6(a).

Next, PACT argues that Intel has failed to specifically identify a PCI “unit,” and that its arguments regarding a PCI “interface” fail to identify a specific motivation to combine Yu with specific hardware (a “unit”) that will implement the PCI interface as recited in claim 41. *See* PO Sur-reply 11–13 (citing Pet. 29, 57–62; Pet. Reply 12–17, 20–21). By contrast, PACT argues that the ’549 patent discloses that there is a specific advantage to using an IOAG and its physical hardware on one of the layers of the 3D stacked device, so that the array of PAEs can be more efficient, since each PAE need only have a small IO interface with a simple internal bus protocol, whereas the IOAG can be “much larger and more complex.” *Id.* at 14–15 (quoting Ex. 1003, 24:11–24).

We find this argument unavailing because claim 41 does not require the use of an IOAG as the dedicated interface unit, nor does the ’549 patent specification. *See* Ex. 1003, 47:5–7 (requiring only a “dedicated Peripheral Component Interconnect (PCI) unit”); *see also id.* at 5:20–37 (stating that a PAE may have a dedicated external interface that may correspond to an industry standard such as PCI, and that “[p]rotocol conversions *may also* be performed in IOAGs” (emphasis added)); 19:52–20:2 (describing a dedicated external interface corresponding to an industry standard such as PCI and stating that, “[i]f necessary, protocol conversions *may also* be performed in IOAGs” (emphasis added)). Moreover, the motivation expressed in the ’549 patent for adding PCI-related hardware need not be the same motivation that Intel relies on in its Petition. *See KSR*, 550 U.S. at 419 (“In determining whether the subject matter of a patent claim is obvious,

neither the particular motivation nor the avowed purpose of the patentee controls.”).

Next, PACT argues that by focusing on a “PCI interface,” which need not have particular hardware, Intel has failed to show “that the hardware of the ‘PCI unit’ can be successfully implemented on the ‘processor integrated device’ identified by [Intel],” with a reasonable expectation of success. PO Sur-reply 15 (citing Ex. 1049 ¶ 6 (Dr. Franzon stating that implementing PCI “requires both hardware and logic as explained in the PCI standard”)).

According to PACT, “[s]imply implementing a PCI standard or a PCI interface would not lead to Petitioner’s proposed combination,” which is to substitute a PCI interface for Yu’s output circuits. *Id.* at 16 (citing PO Reply 14). PACT contends that “[t]hroughout the IPR proceeding, Petitioner and its expert have not identified the claimed ‘PCI unit’ in the context of claim 41,” and has thus failed to establish a motivation to combine or a reasonable expectation of success. *Id.*

We disagree with this argument. Although Intel refers to a “PCI interface” in its briefs, Intel has made clear that it considers this interface to include hardware on Yu’s lower die. *See* Pet. 45–47, 59 (pointing to Yu’s “Output Circuit” on the lower die); Pet. Reply 14 (“[T]he issue is not whether Yu’s microbumps can be interfaced to a PCI card slot . . . —but whether a [person of ordinary skill in the art] would have found it obvious to substitute a PCI interface, as known in the art, for Yu’s output circuit.”); Tr. 75:4–7 (“[A] person of ordinary skill in the art . . . would understand that what you could do simply is put the PCI unit on the layer as Yu is designed to do.”); *id.* at 75:19–21 (“[W]hat we’re proposing . . . [is] exactly the design that Yu puts forth—it’s putting its interface on the bottom stack”); *id.* at

80:11–14 (“Yu is telling us you have a 3D stack, you’re going to have your bottom stack and your output interface, and that’s where you’re going to put your output interface.”).

For the reasons given above, we find that Intel has persuasively shown that Rathnam discloses a PCU “unit” as recited in claim 41, and that a person of ordinary skill in the art would have had motivation to modify Yu’s “output circuit” on Yu’s lower die by implementing a PCI “unit” (including hardware) according to Rathnam’s teachings, with a reasonable expectation of success. *See supra* parts III.C.6(a)–(c).

7. Conclusion

Having considered the arguments and evidence presented in this *inter partes* review, we find Intel’s arguments persuasive, including its arguments (1) that Yu discloses (or Yu in light of Akasaka teaches) all the limitations of claim 41 except for the selection of PCI as the interface unit; (2) that Rathnam teaches the use of a PCI unit in a video processing device like that of Yu or Akasaka; and (3) that a person of ordinary skill in the art would have been motivated to combine Rathnam’s teachings with Yu or the combination of Yu and Akasaka, with a reasonable expectation of success. For the reasons given above, PACT’s responsive arguments do not overcome Petitioner’s persuasive showing. Thus, we determine that Intel has shown, by a preponderance of the evidence, that claim 41 of the ’549 patent would have been obvious over Yu and Rathnam, with or without Akasaka, and is thus unpatentable.

D. GROUND BASED ON FRANZON AND RATHNAM

For the final ground, Intel alleges that claim 41 of the '549 patent is unpatentable under 35 U.S.C. § 103 as obvious over Franzon in view of Rathnam. Pet. 5.

Above, we determine that the sole challenged claim is unpatentable on the other ground based on Yu, Akasaka, and Rathnam, and this is dispositive to the case. Thus, we do not need to decide whether the claim is also unpatentable on the ground based on Franzon and Rathnam. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).

E. PACT'S MOTION TO EXCLUDE EXHIBIT 1013

PACT has filed a Motion to Exclude Exhibit 1013. Paper 33. Exhibit 1013 is a statement by Teresa Chitty, the University Librarian at the University of Adelaide, that Exhibit 1012 (the asserted Franzon reference) is a Ph.D. thesis that “has been catalogued [at the library] following normal practice, which prevailed at the time it was submitted,” and “placed into the University of Adelaide’s Library collection” and then was “publicly available for use in the Library.” Ex. 1013.

In its Motion, PACT argues that while Exhibit 1013 was in the form of a declaration, it did not contain the required acknowledgement under 37 U.S.C. § 1.68. Paper 33, 1–3; *see also* PO Resp. 51–54. As PACT notes, we agreed with PACT on this point in our Institution Decision. Paper 33, 1 (citing Paper 11, 41).

In response to the Motion to Exclude, Intel filed a notice stating that it “will not be advancing Exhibit 1013 at oral argument in this matter” and

“does not oppose [PACT]’s Motion to Exclude Evidence (Exhibit 1013).”
Paper 34, 2.

Because Exhibit 1013 lacks an acknowledgement under 37 U.S.C. § 1.68 and is therefore not proper testimony in this proceeding, we find that all assertions made in the exhibit are inadmissible hearsay. Fed. R. Evid. 801(c), 802. Therefore, PACT’s unopposed Motion to Exclude is *granted*.

IV. CONCLUSION¹⁹

For the reasons above, Intel has shown by a preponderance of the evidence that the challenged claim of the ’549 patent is unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
41	103(a)	Yu, Akasaka, Rathnam	41	
41	103(a)	Franzon, Rathnam ²⁰		
Overall Outcome			41	

¹⁹ Should PACT wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw PACT’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If PACT chooses to file a reissue application or a request for reexamination of the challenged patent, we remind PACT of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2) (2020).

²⁰ As we explain above, we do not reach the ground based on Franzon and Rathnam.

V. ORDER

In consideration of the foregoing, it is
ORDERED that claim 41 of the '549 patent is unpatentable;
FURTHER ORDERED that PACT's Motion to Exclude Exhibit 1013
(Paper 33) is *granted*; and
FURTHER ORDERED that parties to this proceeding seeking judicial
review of our decision must comply with the notice and service requirements
of 37 C.F.R. § 90.2.

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