

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00531
Patent 9,436,631 B2

Before KEN B. BARRETT, CHARLES J. BOUDREAU, and
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

OGDEN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In response to a Petition (Paper 2, “Pet.”) by Petitioner Intel Corporation (“Intel”), the Board instituted an *inter partes* review of claim 4 of U.S. Patent No. 9,436,631 B2 (Ex. 1003, “the ’631 patent”). Paper 13. Patent Owner PACT XPP Schweiz AG (“PACT”) filed a Patent Owner Response (Paper 22, “PO Resp.”), Intel filed a Reply to the Patent Owner Response (Paper 28, “Pet. Reply”), and PACT filed a Sur-reply (Paper 31, “PO Sur-reply”).

We held an oral hearing on May 21, 2021, and the transcript is entered on the record. Paper 36 (“Tr.”).

This is a Final Written Decision under 35 U.S.C. § 318(a) as to whether the claim challenged in the *inter partes* review is patentable. We determine that Intel has not shown, by a preponderance of the evidence on the record before us, that claim 4 of the ’631 patent is unpatentable on the grounds asserted.

II. BACKGROUND

A. RELATED PROCEEDINGS

As related matters, the parties identify *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-00267-RGA (D. Del. terminated Apr. 24, 2019); *PACT XPP Schweiz AG v. Intel Corp.*, No. 6:19-cv-00273-ADA (W.D. Tex. terminated May 30, 2019); *Intel Corp. v. PACT XPP Schweiz AG*, No. 3:19-cv-02241 (N.D. Cal. terminated May 30, 2019); and *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-1006-JDW (D. Del. filed May 30, 2019) (“the co-pending litigation”). Paper 24, 2; Paper 26, 1.

B. THE '631 PATENT (EX. 1001)

The '631 patent claims a priority date of March 5, 2001, which Intel does not contest in the Petition. Pet. 9; Ex. 1003, 1:19–22.

The patent describes “[a] bus system for transferring data between parts of a multiprocessor system,” in which the bus system “is divided into a plurality of segments.” Ex. 1003, code (57). The system includes processing units which form a processing array (PA), composed of processing array elements (PAEs). *Id.* at 2:3–8. Each PAE can include a processor, memory, networking cells, I/O, or other components. *See id.*

In describing how the PAEs are connected to each other, the '631 patent incorporates by reference and builds on a German application by a common inventor that discloses a flexible bus system. Exs. 1010, 1011 (English translation).¹ This German application eventually issued as Vorbach et al., US 6,405,299 on September 6, 2016 (Ex. 1012, “Vorbach”). Ex. 1003, 1:19–21, 14:63–15:40. According to the '631 patent, Vorbach “describes a method of constructing flexible data channels within a PAE matrix according to the algorithms to be executed,” and “[d]ata to be transmitted may be precisely assigned to one source and/or one destination.” Ex. 1003, 14:63–15:2. Vorbach itself states that it is directed to the problem that, “[e]specially when the [processing] units are used for computation of algorithms, it is necessary for a plurality of data (packets) to be transmitted simultaneously between the individual configured function areas of a unit.” Ex. 1012, 1:38–

¹ The German application, DE 197 04 742 A1, was published in 1998. Ex. 1010, code (43); Ex. 1012, code (30). Intel contends that it qualifies as prior art under 35 U.S.C. § 102(b), and PACT does not challenge this assertion. Pet. 10 n.3.

41; *accord* Ex. 1011 § 1.2. So Vorbach intended to “create a bus system that can transmit data between a plurality of function blocks, where multiple data packets can be on the bus at the same time.” Ex. 1012, 1:58–61, *accord* Ex. 1011 § 1.3.

Figure 2 of Vorbach is reproduced below:

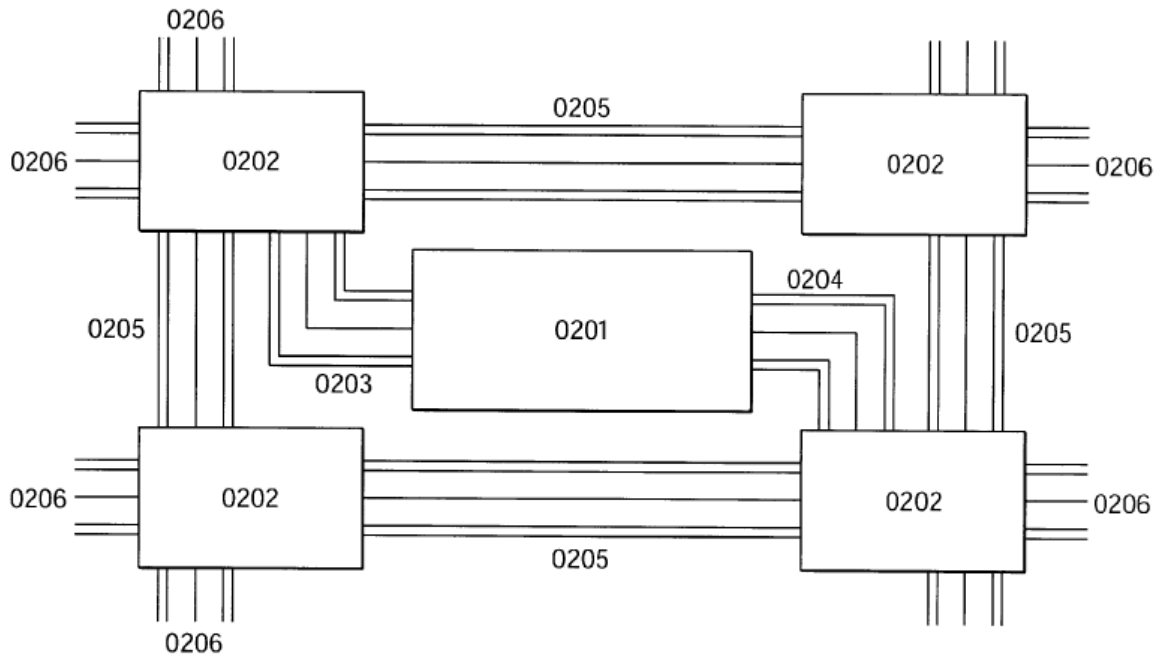


Fig. 2

Figure 2, above, illustrates one recurring part of a two-dimensional array of configurable processing cells (PAEs) 0201 and bus control circuits 0202. *See* Ex. 1012, 3:5–7, 10:22–33; *accord* Ex. 1011 §§ 2.1, 5. Each PAE 0201 connect to bus control circuits 0202 through one of two bundles of data lines 0203 or 0204. Ex. 1012, 10:36–38, 10:41–44; *accord* Ex. 1011 § 5. Bus control circuits 0202 connect to each other through bus segments 0205, and connect externally to other bus control units in the PA through bus segments 0206. Ex. 1012, 10:38–41; *accord* Ex. 1011 § 5. “Each bus segment can be used and connected independently of the others, with the interconnection

being the responsibility of the nodes.” Ex. 1012, 3:26–28; *accord* Ex. 1011 § 3.1.

According to the ’631 patent, Vorbach discloses how PAEs can be connected to each other with “flexible data channels . . . according to the algorithms to be executed.” Ex. 1003, 14:63–66. The ’631 patent adds to this disclosure “additional possibilities . . . (hereinafter referred to jointly as GlobalTrack) that permit flexible allocation and interconnection during run time.” *Id.* at 15:3–9. In particular, the ’631 patent states that by properly implementing Vorbach in the context of GlobalTrack, “a plurality of connections may now be established and used simultaneously.” *Id.* at 15:34–35.

One embodiment is shown in Figure 5, which we reproduce below:

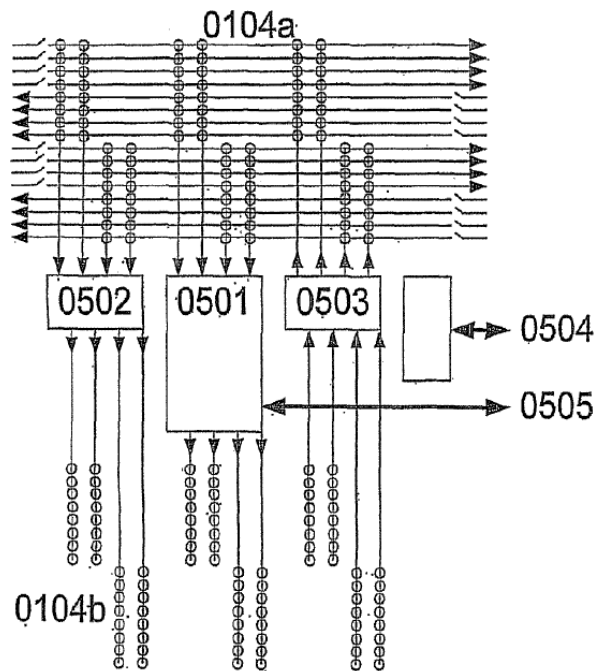


Fig. 5

Figure 5 of the ’631 patent, above, depicts “a possible embodiment of a PAE.” Ex. 1003, 26:42. Data processing unit 501 connects to both first bus

system 104a (for input) and second bus system 104b (for output). *Id.* at 26:42–45. There is also a separate connection to dedicated global bus 0505, which allows either direct connections from PAE 0501 to a different PAE, or from PAE 0501 to an external interface module. *Id.* at 26:56–64.

During prosecution, the applicant argued that each “bus 104 further comprises switches, illustrated in . . . Fig. 5, dividing bus 104 into segments for *each* data processing unit 501–503.” Ex. 1004, 931. Thus, “[e]ach segment may be selectively connected to other segments by the illustrated switches under control of [configuration unit] 504 . . . so that multiple data paths might be provided to each data processing unit 501–503.” *Id.* (citing Ex. 1003, 26:42–55). Based on Figure 5 and on the context of the applicant’s explanation, we understand that the switches in Figure 5 are located at the left and right edges of bus lines 104a.

These switches are also shown in Figure 6, reproduced below:

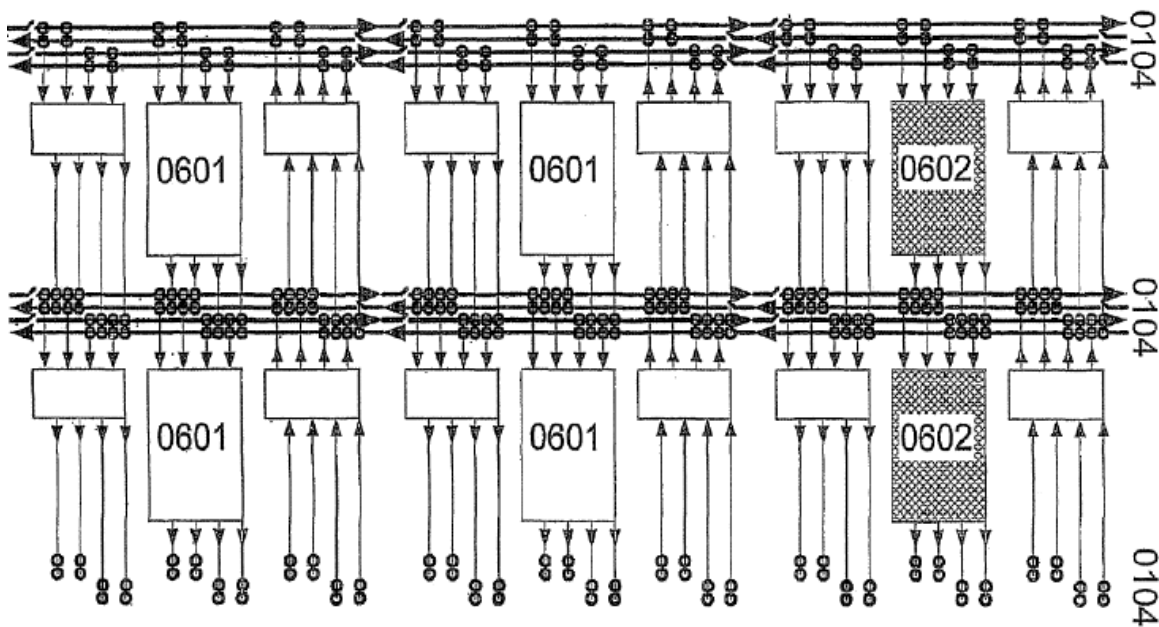


Fig. 6

Figure 6, above, “shows an example of a wiring connection of ALU-PAEs (0601) and RAM-PAEs (0602) via a bus system 0104.” Ex. 1003, 27:32–35. For each bus 0104 there are three PAEs (0601 or 0602) corresponding to PAE 0501 in Figure 5, and there are switching structures between each PAE at the equivalent locations shown in Figure 5.²

C. CHALLENGED CLAIM AND ASSERTED GROUNDS OF
UNPATENTABILITY

PACT has disclaimed claims 1–3. *See* Ex. 2002. This means that “the patent is treated as though the disclaimed claims never existed.” *Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1383 (Fed. Cir. 1998) (citing *Guinn v. Kopf*, 96 F.3d 1419, 1422 (Fed. Cir. 1996)). However, in addressing the patentability of claim 4, we must also address the limitations of claims 1–3, since claim 4 depends, successively, from each of these other claims. *See* Ex. 1003, 34:20–43.

Independent claim 1 is as follows:

1. A bus system for transferring data between parts of a multiprocessor system, the bus system comprising:
 - [a] a plurality of bus segments for each processor of the multiprocessor system comprising a plurality of flexible data channels to each processor of the multiprocessor system according to algorithms to be executed, wherein a plurality of algorithms may executed in parallel;

² In its Reply, Intel agrees that the structures dividing buses 104 in Figure 6 (also shown at either end of bus 104a in Figure 5) are switches that separate buses 104 into segments for each processing unit. *See* Pet. Reply 19–20 (citing Ex. 1003, Fig. 6; Ex. 1004, 931).

- [b] wherein a communication between a sender and a receiver is established in accordance with a data transfer for an executed algorithm; and
- [c] at least one identifier is transmitted with the data for at least one of: identifying a source of the data transfer; and selecting a target of the data transfer.

Ex. 1003, 34:20–33 (Intel’s reference letters added). Claim 2 depends from claim 1, and adds “wherein at least one of the parts of the multiprocessor system is a cache memory.” *Id.* at 34:34–35. Claim 3 depends from claim 2 and adds “wherein the cache memory comprises a plurality of cache cores.” *Id.* at 34:36–37. Claim 4 depends from claim 3, as follows:

- [a] 4. The bus system of claim 3, wherein the cache cores are connected to the bus system such that for the data transfer one of the cache cores is selected according to an address transferred via the bus system;
- [b] wherein at least some of the plurality of cache cores are combined to form a large cache.

Id. at 34:38–43 (Intel’s reference letters added).

Intel argues two grounds for *inter partes* review that involve claim 4, as summarized in the following table:

Claim Challenged	35 U.S.C. §	References
4	103 ³	King, ⁴ Pan, ⁵ Arimilli ⁶
4	103	Budzinski, ⁷ Pan, Arimilli

Pet. 4. For the first ground, Intel alleges that claim 4 is unpatentable under § 103 as obvious “in view of King in combination with Arimilli or, in the alternative, the combination of King, Pan, and Arimilli.” *Id.* For the second ground, Intel alleges that claim 4 is unpatentable under § 103 as obvious “in view of Budzinski in combination with Arimilli or, in the alternative, the combination of Budzinski, Pan, and Arimilli.” *Id.*

D. EXPERT TESTIMONY

For its Petition and Reply, Intel relies on two declarations by Professor Pinaki Mazumder. Exs. 1001, 1053. For its Response and Sur-reply, PACT relies on a declaration by Professor Murali Annavaram. Ex. 2023. We find them both qualified, based on their education and experience, to offer testimony on the subject matter of their respective declarations. Fed. R. Evidence 702(a); *see* Ex. 1001 ¶¶ 5–33; Ex. 1002 (Professor Mazumder’s

³ 35 U.S.C. § 103(a) (2006), *amended by* Leahy–Smith America Invents Act, Pub. L. No. 112-29 § 103, sec. (n)(1), 125 Stat. 284, 287, 293 (2011) (effective Mar. 16, 2013). *See* Pet. 3 n.1 (“Cites to 35 U.S.C. § 102 and § 103 are to the pre-AIA version applicable here.”).

⁴ King et al., US 5,761,455 (issued June 2, 1998) (Ex. 1005).

⁵ Pan et al., *Efficient and Scalable Quicksort on a Linear Array with a Reconfigurable Pipelined Bus System*, 13 Future Generation Computer Sys. 501 (1998) (Ex. 1008).

⁶ Arimilli et al., US 5,893,163 (issued Apr. 6, 1999) (Ex. 1006).

⁷ Budzinski et al., EP 0 071 727 A1 (published Feb. 16, 1983) (Ex. 1007).

curriculum vitae); Ex. 2023 ¶¶ 1–6; Ex. 2028 (Professor Annavaram’s curriculum vitae).

III. GROUNDS OF THE PETITION

For the reasons below, we determine that Intel has *not* shown, by a preponderance of the evidence, that claim 4 is unpatentable under § 103. Before analyzing the Petition’s asserted grounds in detail, we address two matters that will underlie our analysis: the level of ordinary skill in the art, and the claim construction we will apply to the claim terms.

A. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the pertinent art at the time of the invention is one of the factual considerations relevant to obviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). It is also relevant to how we construe the patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). To assess the level of ordinary skill, we construct a hypothetical “person of ordinary skill in the art,” from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct “presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Professor Mazumder opines that a person of ordinary skill in the art “would have had at least a [Master of Science] degree in electrical engineering (or equivalent experience), and at least three years of experience

with processor design and memory architecture.” Ex. 1001 ¶ 68.⁸ Professor Mazumder testifies that this “was the typical level of experience of persons working with multiprocessor systems, including the design of processor, cache, memory, and bus architectures, at the time of the alleged invention.” Ex. 1001 ¶ 68.

Professor Annavaram adopts Professor Mazumder’s formulation, with the understanding that the master’s degree would “include related fields such as computer engineering.” Ex. 2023 ¶ 20.

Based on Professor Mazumder’s uncontested declaratory testimony, which we find consistent with the technical level of the ’631 patent disclosure and asserted prior art references, we adopt Professor Mazumder’s formulation of the level of ordinary skill for this decision.

B. CLAIM CONSTRUCTION

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2020). This includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.* The ordinary and customary meaning of a claim term “is its meaning to the ordinary artisan after reading the entire patent,” and “as of the effective filing date of

⁸ The formulation that Intel expresses in its Petition differs slightly from Professor Mazumder’s formulation. *See* Pet. 14 (“at least an M.S. degree in electrical engineering, and at least three years of experience with multiprocessor systems design”).

the patent application.” *Phillips*, 415 F.3d at 1313, 1321. In construing a claim, we consider “[a]ny prior claim construction determination concerning a term of the claim in a civil action . . . that is timely made of record” in this proceeding. 37 C.F.R. § 42.100(b).

1. “*A Plurality of Bus Segments for Each Processor*”

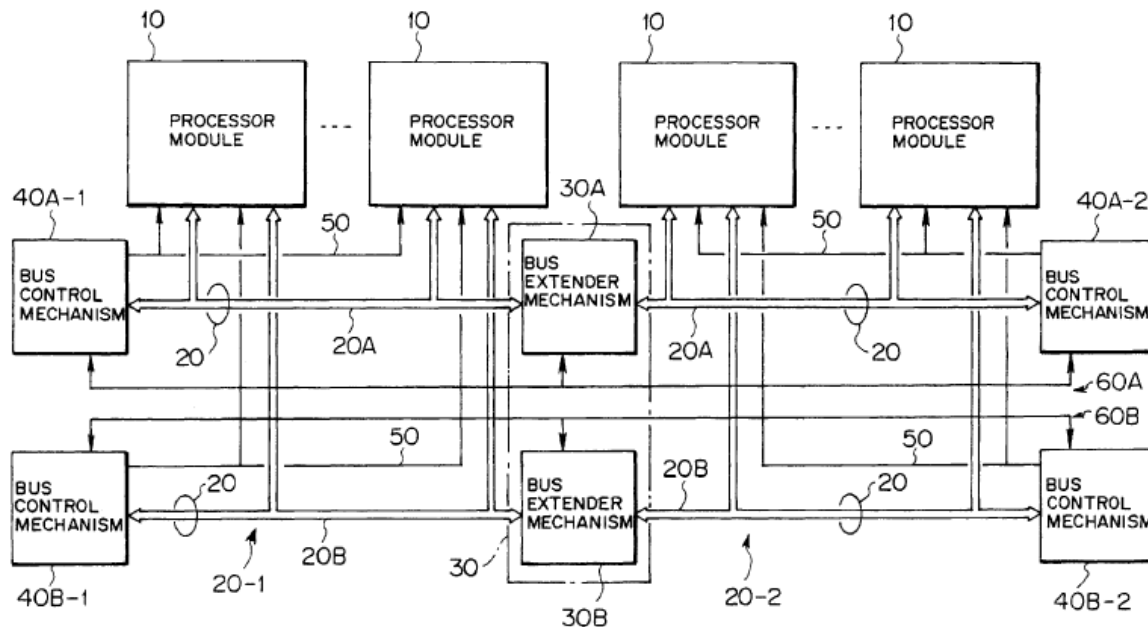
Intel informs us that in the co-pending litigation, the district court construed the term “a plurality of bus segments for each processor of the multiprocessor system” as having its plain and ordinary meaning. Pet. Reply 13–14 (citing Ex. 1050, 11). The parties agree now that this construction should apply in this case. *See id.*; PO Sur-reply 3.

But in the co-pending litigation, Intel proposed construing the term to require that “each bus segment [is] connected to only one of the processors,” because in Intel’s view, the applicant had disclaimed the term’s full ordinary and customary scope during prosecution by distinguishing Takahashi et al., US 5,905,875, issued May 18, 1999 (Ex. 1013). *See* Pet. 5.

Takahashi describes a multiprocessor system “made up of a plurality of processor modules connected together through a duplicated system bus. The duplicated system bus is divided into a plurality of segments, and these segments are coupled together by at least one bus extender mechanism.” Ex. 1013, code (57).

Figure 1 of Takahashi is reproduced below:

FIG. I



Takahashi's Figure 1, above, depicts a plurality of processor modules 10, which are coupled together by system bus 20, which comprises main bus 20A and spare bus 20B. Ex. 1013, 7:43–47. Bus system 20 has two segments (20-1 and 20-2) which “are coupled together by a bus extender mechanism 30.” *Id.* at 7:48–51. Since bus 20 has two parts 20A and 20B, there are two corresponding extender mechanisms 30A and 30B. *Id.* at 7:51–54.

During prosecution, the applicant distinguished the claimed invention from Takahashi by arguing that Takahashi and two secondary references fail to disclose “a plurality of bus segments *for each* processor,” which the applicant argued was a “novel feature.” Ex. 1004, 933–34. In the co-pending litigation, Intel argued that this was a disavowal of claim scope, since the applicant's argument “demonstrates that each bus segment can connect only to a single processor.” Ex. 1050, 11. The district court rejected Intel's

argument, because there were at least two reasonable ways to interpret the term “a plurality of bus segments for each processor of the multiprocessor system” consistently with the applicant’s arguments distinguishing Takahashi. *See id.* at 11–13. Because of this ambiguity in how to interpret the applicant’s argument, the court held that there was no clear disavowal of claim scope. *Id.* at 12–13.

Now, Intel agrees with PACT that the term “a plurality of bus segments for each processor” should be construed to have its full plain and ordinary scope. *See* PO Reply 13–14. We agree with the parties, for the reasons expressed by the district court. Ex. 1050, 11–13. However, the parties still disagree as to the scope of that ordinary meaning. *See* PO Resp. 15–26; Pet. Reply 17–19; PO Sur-reply 3–6. The district court did not resolve this issue. *See* Ex. 1050, 12–13.

To be clear, we do not consider Intel’s proposed construction in the co-pending litigation to be a viable option for the term’s ordinary and customary meaning. Intel’s construction, in which “each bus segment [is] connected to only one of the processors” (Ex. 1050, 11), would exclude the embodiment in Figure 6 of the ’631 patent, which shows bus segments (the three segments between the four switches in the middle row of buses 0104) directly connected to two different processors 0601 or 0602 (above and below middle bus 0104). *See* Ex. 1003, Fig. 6. A person of ordinary skill in the art, upon reading the ’631 patent, would not have understood the term to exclude the principal embodiment of the ’631 patent. Nor is there anything in the claim itself suggesting that each bus segments cannot connect to a plurality of processors, such as in Figure 6.

PACT argues that the claim’s ordinary and customary meaning “requires a plurality of bus segments connected *directly* to each processor, and not simply accessible by the processor.” PO Resp. 26. In support, PACT cites Figures 5 and 6 of the ’631 patent, and related text in the specification, which according to PACT describe “multiple bus segments connected to processing elements 501” to allow, for example, simultaneous access to a plurality of senders or receivers to one memory. *Id.* (citing Ex. 1003, 27:1–13, Figs. 5–6). PACT also argues that during prosecution of the ’631 patent, the applicant explained to the Examiner that in Figure 501, “each bus, 104, has two *sets* of connections to each of the data processing units 501–503. In addition, bus 104 further comprises switches, illustrated in . . . Fig. 5, dividing bus 104 into segments for *each* data processing unit 501–503.” *Id.* (citing Ex. 1004, 931).

Intel makes two arguments in response. First, Intel argues that PACT’s construction, requiring a “direct” connection, “clearly deviates from the plain meaning.” Pet. Reply 17–18 (citing Ex. 1051, 597 (a dictionary definition of the word *for* as meaning “intended to reach; directed or belonging to”); Ex. 1052, 174 (another dictionary definition of *for* as “meant to be used by someone or something; meant to belong to someone; meant to be given to someone”)). Intel contends that PACT’s only support for its proposed construction are “exemplary embodiments: Figures 5 and 6 and descriptions of those figures in the specification and file history,” and “PACT’s cited evidence sheds little light on the phrase ‘for each’ and attributes no importance to direct connections.” *Id.* at 18 (citing PO Response 26; Ex. 1003, 2:60–61, 26:42–43, 27:32–34; Ex. 1004, 931–32).

In response, PACT argues that construing “a plurality of bus segments for each processor” to allow a bus segment to connect indirectly to its processor “renders the phrase ‘for each processor’ meaningless in the context of the claim.” PO Sur-reply 5. According to PACT, this is because claim 1 “already specifies that the plurality of bus segments ‘compris[es] a plurality of flexible data channels to each processor of the multiprocessor system.’” *Id.* Thus, “[i]n order to render ‘for each processor’ distinct from the ‘plurality of flexible data channels,’ it must be understood to require a plurality of bus segments *connected to* each processor.” *Id.* at 5–6.

PACT also argues that Intel’s “cited non-technical dictionaries cannot overcome the plain claim language.” PO Sur-reply 6 (citing *Phillips*, 15 F.3d at 1318 (extrinsic evidence is generally less reliable for claim construction than the patent and its prosecution history)). But even under those definitions, PACT argues that the word *for* connotes an idea of “belonging to.” *Id.* So according to PACT, “a bus segment that is ‘for’ a processor does not refer to a remote bus segment that may be indirectly accessible as part of a larger bus segment.” *Id.* Rather, “it refers to the bus segments intended for or belonging to that processor.” *Id.*

Based on the intrinsic evidence, we find PACT’s argument persuasive that the term “a plurality of bus segments for each processor” does not include bus segments that are only indirectly accessible to a processor through, for example, a switch or another bus segment. We agree that if a bus segment can be “for” a processor simply by being a remote part of a larger bus system that is ultimately accessible by the processor, this would effectively make the phrase “for each processor” redundant to the phrase

“comprising a plurality of flexible data channels to each processor.” *See* Ex. 1003, 34:22–24.

Statements made during the prosecution of the ’631 patent corroborate this understanding of the claim, because the applicant indicated that the switches in Figure 5 “divid[e] bus 104 into segments for *each* data processing unit 501–503,” and “[e]ach segment may be selectively connected to other segments by the illustrated switches . . . so that multiple data paths might be provided to each data processing unit 501–503.”

Ex. 1004, 931. We are persuaded that upon reading this, a person of ordinary skill in the art at the time of the claimed invention would have understood that the applicant intended bus segment 104a to be “for” processing unit 501 because it is directly accessible to the processing unit, rather than being remotely accessible through a switched path involving other segments.

Second, Intel argues that PACT’s proposed construction is undermined by its position in the co-pending litigation that no explicit construction is necessary, and that during prosecution, the applicant argued that “that every bus segment is connected to every processor.” Pet. Reply 19 (Ex. 1049, 35). According to Intel, “[t]hat understanding directly contradicts PACT’s construction here,” because in Figures 5 and 6 of the ’631 patent, the only way that every bus segment is connected to every processor is indirectly (through the switches separating individual bus segments in 0104). *Id.*

In its Sur-reply, PACT contends that its position in district court was not inconsistent with its position here because, as PACT’s counsel explained during the claim construction hearing, PACT did not mean, by “every bus segment,” to include bus segments connected indirectly, such as through bus

extenders, since these extensions do not create flexible data channels. *See* PO Sur-reply 4–5 (citing Ex. 2026, 74:8–11, 75:5–10, 75:21–23, 81:6–19 (claim construction hearing transcript); Ex. 2027, 73–74 (slides for the hearing)).⁹ PACT’s arguments during the claim construction hearing appear to diminish the apparent inconsistency between PACT’s argument here and its argument in the co-pending litigation, and we find PACT’s current argument persuasive.

Thus, we conclude, based on the claim language, the ’631 patent specification, and the prosecution history, that the ordinary and customary meaning of the term “a plurality of bus segments for each processor” means that each bus segment is directly accessible to its corresponding processor or processors.

2. *“A Plurality of Flexible Data Channels to Each Processor”*

In its Response, PACT seems to implicitly argue that in the context of a processor connected to a memory, the phrase “bus segments . . . comprising a plurality of flexible data channels to each processor” means that the bus segments must “provide alternative, parallel paths between a processor and memory.” PO Resp. 27 (citing Ex. 1003, 27:8–12 (“[A] memory [PAE] may have a plurality, in particular, more than two bus connections to 0104a and/or 0104b to allow access of a plurality of

⁹ Under our rules, a sur-reply “may not be accompanied by new evidence other than deposition transcripts of the cross-examination of any reply witness.” 37 C.F.R. § 42.23(b) (2020). However, Intel did not object to Exhibits 2026 and 2027 on the record, and did not file a motion to exclude or strike the exhibits.

senders/receivers to one memory, for example. Accesses may preferably also take place simultaneously (multi-port).”)).

In its Reply, Intel argues that PACT’s construction of “a plurality of flexible data channels to each processor” fails, because “[n]othing in the claim suggests that the data channels must be ‘parallel’ nor that they must specifically connect ‘a processor and memory.’” Pet. Reply 20–21. Intel also argues that the cited language in the specification describes a preference rather than a requirement. *See id.* (citing Ex. 1003, 27:12–13).

In its Sur-reply, PACT stated that it “is not offering a construction of [the term ‘a plurality of flexible data channels to each processor’] beyond its plain meaning.” PO Sur-reply 17 n.2. According to PACT, it “merely recognizes that the term imposes three requirements on the claimed data channels: (1) they must be flexible; (2) there must be a plurality of them; and (3) there must be a plurality ‘to each processor.’” *Id.*

Because PACT stated that it did not intend to propose an explicit claim construction for the term “a plurality of flexible data channels to each processor,” and neither does Intel propose an explicit construction, we do not need to explicitly construe this term for our decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. GROUND BASED ON KING, PAN, AND ARIMILLI

For the first ground, Intel alleges that claim 4 is unpatentable under 35 U.S.C. § 103 as obvious over King in view of Arimilli, or alternatively over the combination of King, Pan, and Arimilli. Pet. 4.

A claim is unpatentable under § 103 for obviousness if the differences between the claimed subject matter and the prior art are “such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). For a combination of references, we consider “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *Id.* at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). A successful petition must “articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (citing *KSR*, 550 U.S. at 418); *see also* 35 U.S.C. § 322(a)(3); 37 C.F.R. §§ 42.22(a)(2), 42.104(b)(4) (2020).

We base our obviousness inquiry on factual considerations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) any objective indicia of obviousness or non-obviousness that may be in evidence. *See Graham*, 383 U.S. at 17–18.

Based on these factors,¹⁰ we determine that Intel has not shown, by a preponderance of the evidence, that claim 4 is unpatentable as obvious over

¹⁰ Neither party has presented evidence of objective indicia of obviousness or non-obviousness, so this does not factor into our decision. *See Ex. 1003*

King in view of Arimilli, with or without the teachings of Pan, for the reasons below.

1. Overview of King

King describes a parallel processing system with multiple processors and multiple memories, with bus units coupling the processors and memories. Ex. 1005, code (57). Each “bus unit provides a pathway between one processor and the bus unit’s respective memory,” and “[t]he coupling of processors to memories can change, dynamically, each bus cycle.” *Id.*

¶ 202 (Professor Mazumder stating that he is not aware of any evidence of objective indicia).

Figure 1, reproduced below, is a block diagram illustrating the system:

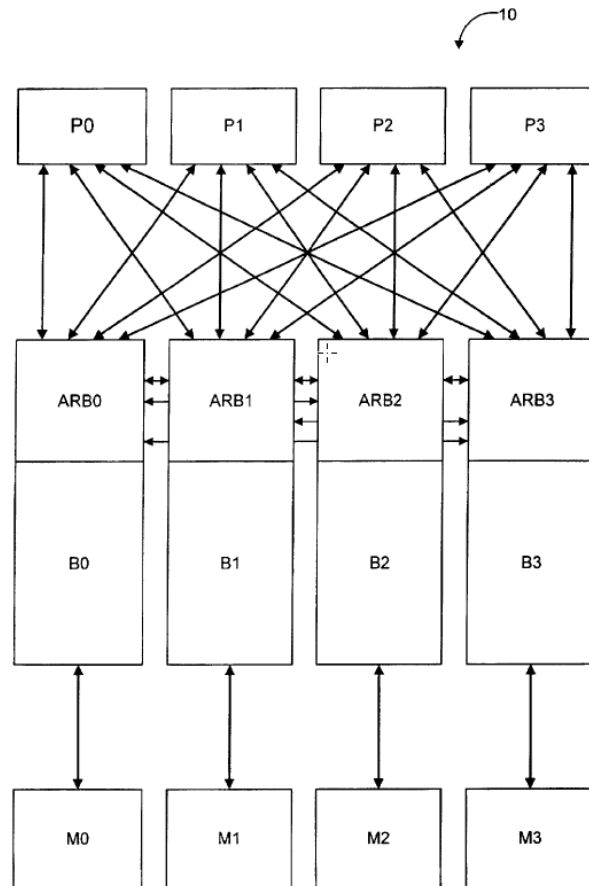


Fig. 1

Figure 1, above, depicts parallel processing system 10, with four processors P0–P3 and four memories M1–M3. Ex. 1005, 2:47–49. Between the processors and memories are four arbitration units ARB0–ARB3 and four bus units B0–B3. *Id.* at 2:49–51. Figure 1 “shows each of the four processors connected to each of the four bus units, resulting in sixteen processor busses,” represented in the figure as arrows. *Id.* at 2:59–61.

King describes using variable bus widths to the shared memory, in order to allow the system to adapt to a tradeoff known in the art: “If the shared memory is set up with a narrow port width, too much contention occurs between the processors for the memory,” but on the other hand, “if

the memory has too large a port width, then much of the available bandwidth to memory is wasted if each processor only needs a portion of the width to access memory.” Ex. 1005, 1:29–35. King’s proposed solution is to make “each processor’s bus width to memory variable, [so that] multiple accesses can occur in a single bus cycle, and memory is easily shared, without a delay for bus setup.” *Id.* at 2:28–31.

King also provides an example of arbitrating different pathways between processors and memories, based on the needs of a particular algorithm: “[S]ince the bus reconfiguration is dynamic, the parallel processing system 10 . . . is easily capable of switching between a SIMD mode and a MIMD mode without any intervening clock cycles for setup.” Ex. 1005, 5:42–56. According to King, SIMD mode is “where each processor operates using the same instructions, but operates on different data. Finite element analysis is an example application.” *Id.* at 5:32–35. MIMD mode is where “each processor runs an independent set of instructions on independent sets of data.” *Id.* at 5:39–40.

2. *Overview of Pan*

Pan describes a method for performing the quicksort algorithm on a “linear array with a reconfigurable pipelined bus system (LARPBS).” Ex. 1008, 501. A LARPBS model includes an array of processors connected to each other through transmitting and receiving buses controlled by switches. *Id.* at 504, Fig. 4.

According to Pan, “different algorithms require different communication patterns,” and “[s]ome algorithms may even need different communication patterns during different phases of the same computation.” *Id.* at 502. Thus, Pan proposes that the pipelined bus of an LARPBS array

“can be reconfigured dynamically under program control to suit communication needs,” so that the time complexity of the quicksort algorithm “compares favorably with [algorithms] implemented on arrays with traditional reconfigurable electronic buses.” *Id.* at 502.

3. Overview of Arimilli

Arimilli discloses a “system for allocating data among cache memories within a symmetric multiprocessor data-processing system.” Ex. 1006, code (57). “[E]ach of the processing units has a cache memory.” *Id.* Figure 1, reproduced below, depicts an example of this system:

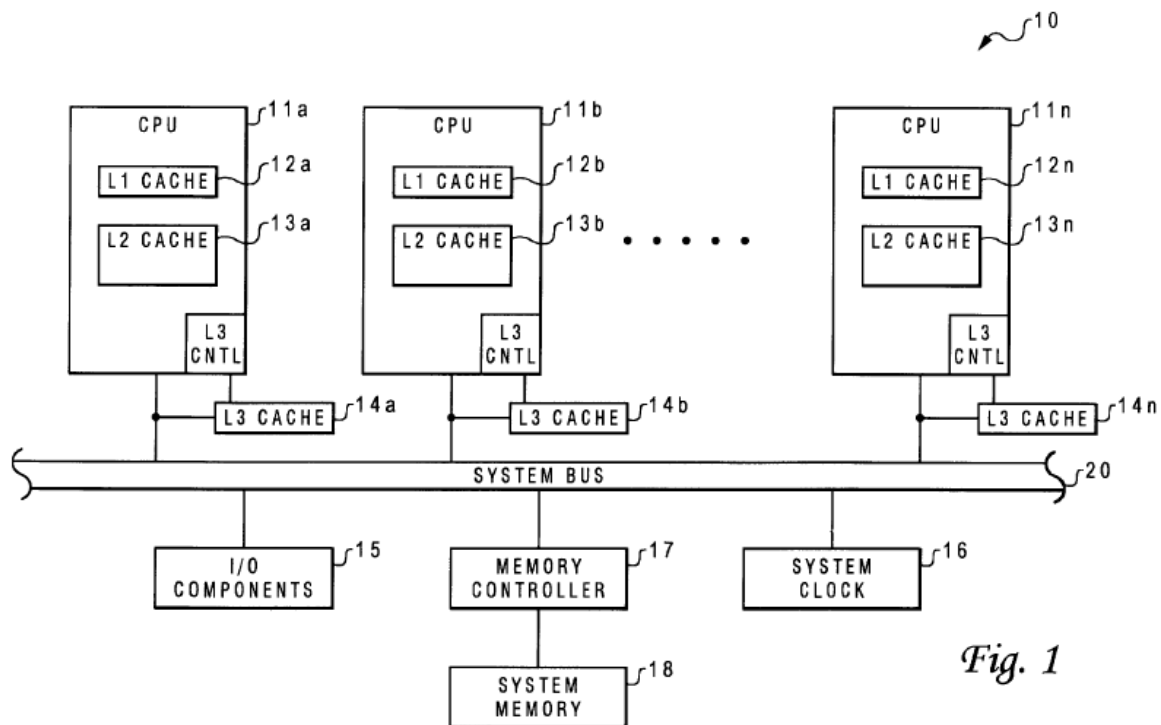


Fig. 1

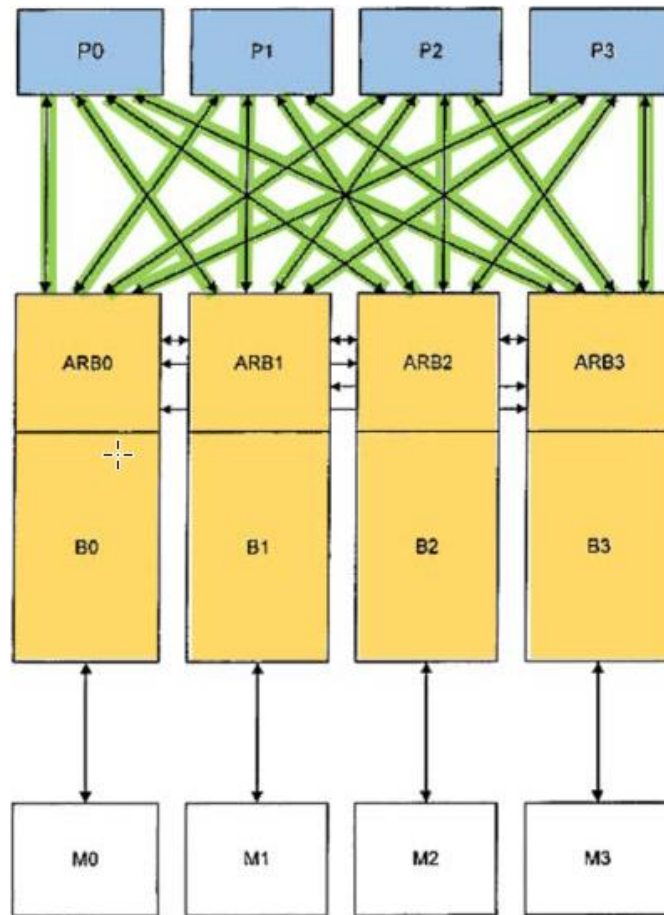
Arimilli’s Figure 1, above, depicts data-processing system 10, which includes multiple CPUs 11a–11n, each of which contains at least one level of local cache. Ex. 1006, 2:65–3:3. In particular, each CPU 11a–11n includes L3 caches 14a–14n, which the figure depicts as being connected to system bus 20. *See id.* at 3:7–10.

Arimilli teaches that “the latency associated with system memory access [is] generally quite large” compared to cache memory, so this latency can be avoided by “maintain[ing] as much useful data in at least one of the cache memories as possible,” and then allowing the system to perform “intervention,” defined as “[t]he process of transferring data from one processing unit to another processing unit on a system bus without going through a system memory.” Ex. 1006, 1:51–64. This can be done by operating the L3 caches in “shared mode,” in which “all L3 caches within the SMP data-processing system are combined, each L3 cache representing different segments of the system memory.” *Id.* at 4:64–66.

4. *Independent claim 1*

Although claims 1–3 have been disclaimed, claim 4 depends from claim 3, which depends from claim 2, which depends from claim 1. *See* Ex. 1003, 34:20–43. So we first address the limitations of independent claim 1. According to Intel, King discloses each of these limitations. Pet. 21–35. PACT does not specifically contest Intel’s arguments in this regard. For the reasons below, we find that Intel has shown, by a preponderance of the evidence, that King discloses every limitation of claim 1 and that King teaches every limitation of claim 1 in light of Pan.

To aid in its presentation, Intel provides an annotated version of King’s Figure 1, with color coding to indicate the different parts of the system, which we reproduce below:



Pet. 23. Intel’s annotated Figure 1, above, depicts processors P0–P3 in blue, the arrows representing the 16 buses in green, bus units B0–B3 and their respective arbitration units ARB0–ARB3 in yellow, and memory units M0–M3 are uncolored. *See* Pet. 22.

(a) Preamble

For the preamble, Intel argues that King discloses “[a] bus system for transferring data between parts of a multiprocessor system.” Pet. 21–23 (citing Ex. 1005, 1:46–50, 1:57–63, 2:4–10, 2:37–3:10, 7:6–8:4 (claim 13),

Fig. 1; Ex. 1001 ¶ 92). We find this persuasive, as it is evident from Figure 1 and the associated text in the '631 patent.¹¹

(b) Limitation 1[a]

Intel divides limitation 1[a] into three parts. Pet. 23–32. The first part is “a plurality of bus segments for each processor of the multiprocessor system.” Pet. 23; Ex. 1003, 34:22–23. Intel argues that the bus segments are the 16 arrows shown in green in annotated Figure 1 (reproduced above). Pet. 23–24. Intel argues that in Figure 1, there are multiple bus segments for each processor since every processor is connected by a distinct bus to every other memory unit, thus meeting this aspect of limitation 1[a]. *Id.* (citing Ex. 1005, 1:55–63, 2:37–3:10, Fig. 1; Ex. 1001 ¶¶ 94–96).

The second part of the limitation is “comprising a plurality of flexible data channels to each processor of the multiprocessor system according to algorithms to be executed.” Pet. 24; Ex. 1003, 34:23–25. Intel argues that in King, bus units B0–B3 create and reconfigure the bus pathways between processors P0–P3 and memory units M0–M3. Pet. 25 (citing Ex. 1005, 3:66–4:6). According to Intel, the pathways are “flexible” because (1) they can connect a processor to a memory unit during each bus cycle, and (2) the bus paths can be of variable width (16, 32, or 64 bits) as needed by the memory type being accessed. *Id.* (citing Ex. 1001 ¶¶ 97–100).

Intel contends that King’s bus segments can be flexibly configured “according to algorithms to be executed,” as recited in the claim, because a person of ordinary skill in the art “would have understood that the memory

¹¹ Because we find this argument persuasive, we do not need to reach any conclusion as to whether the preamble of is limiting.

addresses needed to be read or written by each processor in a given cycle, and the corresponding flexible data channels needed to provide that access, are dependent on the algorithm to be executed by that processor.” Pet. 26 (citing Ex. 1001 ¶¶ 101–103). In addition, Intel argues that King discloses switching flexibly between SIMD and MIMD mode, and that a person of ordinary skill in the art would have chosen SIMD and MIMD depending on the algorithm (for example, choosing SIMD for finite element analysis). *Id.* at 26–28 (citing Ex. 1005, 5:30–46; Ex. 1001 ¶¶ 102–104).

Alternatively, Intel argues that Pan discloses configuring the flexible data channels in a multiprocessor system “according to algorithms to be executed,” because Pan teaches configuring the bus channels of the LARPBS model to increase the efficiency of the quicksort algorithm. Pet. 28–29 (citing Ex. 1008, 502, 506–508, 510). Intel argues that “[i]t would have been obvious in view of Pan to use King’s bus system such that it provides flexible data channels according to algorithms to be executed, as doing so would have improved the efficiency of the algorithms being executed.” *Id.* at 29 (citing Ex. 1001 ¶¶ 107–112); *see also id.* at 29–31 (arguing that the King and Pan are analogous to the claimed invention, and that a person of ordinary skill in the art would have had a reasonable expectation of success).

The third and final part of limitation 1[a] is “wherein a plurality of algorithms may [be] executed in parallel.” Pet. 31; Ex. 1003, 34:26–27. Intel argues that King’s system operates in parallel, including permitting “multiple **simultaneous** memory accesses [to] occur.” Pet. 31 (alteration in original) (quoting Ex. 1005, 1:4–7) (citing Ex. 1005, 1:53–63, 2:47–51, 5:1–5, 5:27–40, 5:47–52, 6:19–21; Ex. 1001 ¶ 104). Intel also argues that King

discloses “operat[ing] in ‘MIMD parallel processor’ mode in which each processor ‘runs an independent set of instructions on independent data sets.’” *Id.* at 32 (quoting Ex. 1005, 5:38–40) (citing Ex. 1001 ¶ 114).

We find Intel’s uncontested arguments persuasive to show that King discloses or teaches limitation 1[a] for the reasons Intel expresses in its Petition, and we also find persuasive Intel’s rationale for why a person would have combined King with the teachings of Pan.

(c) Limitation 1[b]

Limitation 1[b] recites “wherein a communication between a sender and a receiver is established in accordance with a data transfer for an executed algorithm.” Ex. 1003, 34:28–30. Intel argues that during transfer of data between a processor and memory, “King discloses that the processor ‘signals which . . . memory is being requested, an address, and data if the access is a write access.’” Pet. 32 (quoting Ex. 1005, 1:63–65). Then, the bus unit or units “establish a communication path between the processor and the memory or memories associated with that address.” *Id.* (citing Ex. 1005, code (57), 1:57–65, 3:66–4:18).

We find Intel’s uncontested arguments persuasive to show that King discloses limitation 1[b], for the reasons Intel expresses in its Petition.

(d) Limitation 1[c]

Limitation 1[c] recites “at least one identifier is transmitted with the data for at least one of: identifying a source of the data transfer; and selecting a target of the data transfer.” Ex. 1003, 34:31–33. Intel argues that King discloses memory selection lines and address lines, which identify which memory to access, and the specific location of the memory being

requested. Pet. 32–33 (citing Ex. 1005, code (57), 1:63–65, 2:4–5, 2:54–58, 2:64–67, 3:15–20, 3:23–30, 3:45–53, Fig. 2; Ex. 1001 ¶¶ 118–119).

According to Intel, a person of ordinary skill in the art “would have understood both the information on the memory selection lines and on the address lines to be ‘identifier[s],’ as the memory selection lines identify the memory, and the address identifies the particular area of memory.” Pet. 34 (alteration in original) (citing Ex. 1001 ¶ 119). Intel also argues that King discloses that the memory and address identifiers are “transmitted with the data” as recited in limitation 1[c]. *Id.* at 35 (citing Ex. 1005, 1:63–65; Ex. 1001 ¶ 121).

We find Intel’s uncontested arguments persuasive to show that King discloses limitation 1[c], for the reasons Intel expresses in its Petition. Thus, Intel has shown, by a preponderance of the evidence, that King discloses each limitation of claim 1 and that a person of ordinary skill in the art would have had reason to combine the teachings of King and Pan to achieve claim 1.

5. *Dependent claim 2*

Claim 2 depends from claim 1, and further recites “wherein at least one of the parts of the multiprocessor system is a cache memory.” Ex. 1003, 34:34–35. Intel contends that claim 2 would have been obvious over King in view of Arimilli, or alternatively over King, Pan, and Arimilli. *See* Pet. 35–39. For the reasons below, we find Intel’s arguments persuasive.

For teaching a cache memory, Intel relies on Arimilli’s teaching of a system that includes at least L1 caches 12a–12n and L2 caches 13a–13n. Pet. 35–37 (citing Ex. 1006, code (57), 2:39–40, 2:65–3:29, Fig. 1; Ex. 1001 ¶¶ 123–124).

Intel also argues that it would have been obvious to modify King in view of Arimilli to include a cache. Pet. 35, 37–39. Intel contends that King recognizes the benefits of cache memory, in general, as a solution to the problem that “[i]n the typical processing system, the bottleneck which limits processing speed is the interface between the processor and memory.” *Id.* (quoting Ex. 1005, 1:37–39). Thus, according to Intel, a person of ordinary skill in the art “would have . . . recognized in King’s own teachings that King’s system was ready for improvement with a known technique, cache memory, to yield predictable results.” *Id.* at 37–38 (citing Ex. 1005, 1:39–41, 1:46–50, Ex. 1001 ¶ 129). Intel also argues that Arimilli’s teachings would have motivated an ordinarily skilled artisan to reduce high memory latency by using caches, and that Arimilli’s solution would have improved King’s similar system in a similar way, with the expectation of a predictable result. *See id.* at 38–39 (citing Ex. 1006, 1:54–64, 3:35–48, Ex. 1001 ¶¶ 130–133).

In response, PACT focuses its arguments on claim 4 and Arimilli’s shared L3 caches 14a–14n, and does not specifically address Arimilli’s teachings about L1 and L2 caches. *See* PO Resp. 14–23; PO Sur-reply 6–14. As we discuss below, we agree with PACT’s arguments regarding a shared L3 cache in the context of claim 4. *See infra* part III.C.7. But Arimilli’s L1 and L2 caches also fall within the scope of the “one of the parts of the multiprocessor system [that] is a cache memory,” as recited in claim 2. Ex. 1003, 34:34–35.

Thus, we find Intel’s uncontested arguments as to Arimilli’s L1 and L2 caches, and the cited evidence, persuasive to show that the combination of King and Arimilli teaches all the limitations of claim 2, with or without the teachings of Pan. Intel has also shown a persuasive rationale for why an

ordinarily skilled artisan would have modified King to add L1 or L2 caches according to Arimilli's teachings.

6. *Dependent claim 3*

Claim 3 depends from claim 2 and further recites "wherein the cache memory comprises a plurality of cache cores." *Id.* at 34:36–37. Intel contends that claim 3 would have been obvious over King in view of Arimilli, or alternatively over King, Pan, and Arimilli. *See* Pet. 39–42. For the reasons below, we find Intel's arguments persuasive.

First, Intel argues that in Arimilli, L1 caches 12a–12n are each divided into an instruction portion and a data portion, thus each L1 cache has two cache cores. Pet. 39 (citing Ex. 1006, 3:32–35; Ex. 1001 ¶ 136). Intel argues that it would have been obvious to structure an L1 cache this way in King's system because it would achieve "low latency access by the processor cores." *Id.* at 41 (quoting Ex. 1006, 1:39–40). According to Intel, this division of the L1 cache was "a known technique . . . which was ready for improvement" to yield this predictable result. *Id.* at 41–42 (citing Ex. 1001 ¶ 140).

This part of Intel's analysis is uncontested. PACT's Response focuses its arguments on claim 4 and Arimilli's shared L3 caches 14a–14n, and does not specifically address Arimilli's teachings about L1 caches 12a–12n. *See* PO Resp. 14–23; PO Sur-reply 6–14. As we discuss below, we agree with PACT's arguments regarding a shared L3 cache in the context of claim 4. *See infra* part III.C.7. But Intel has persuasively shown that Arimilli's L1 cache, having two cache cores, falls within the scope of a "cache memory compris[ing] a plurality of cache cores," as recited in claim 3. Ex. 1003, 34:36–37.

Intel also makes an alternative argument for claim 3, based on Arimilli's shared L3 caches. *See* Pet. 39–42. Since we find Intel's first argument persuasive as to claim 3, we leave further discussion about Intel's alternative argument for the discussion below in the context of claim 4. As we discuss below, we do not find Intel's argument persuasive that a person of ordinary skill in the art would have modified King's system by adding Arimilli's shared L3 caches.

Thus, we find Intel's uncontested arguments as to Arimilli's L1 cache, and the cited evidence, persuasive to show that the combination of King and Arimilli teaches all the limitations of claim 3, with or without the teachings of Pan. Intel has also shown a persuasive rationale for why an ordinarily skilled artisan would have combined the references' teachings to achieve the bus system recited in claim 3.

7. *Dependent claim 4*

Claim 4, the challenged claim in this proceeding, depends from claim 3, and adds two limitations, which Intel designates as 4[a] and 4[b]. Pet. 43–47; Ex. 1003, 34:38–43. Intel contends that claim 4 would have been obvious over King in view of Arimilli, or alternatively over King, Pan, and Arimilli. *See* Pet. 43–47. For the reasons below, we do not find Intel's arguments persuasive.

In its alternative argument for claim 3 and for claim 4 in general, Intel argues that Arimilli's system-wide L3 cache includes separate L3 caches ("cache cores," according to Intel) 14a–14n, each associated with one of the processors, and when the system is operating in "shared mode," these cache cores function as a combined cache. *Id.* at 39–40 (citing Ex. 1006, 2:52–54, 4:47–50, 4:64–66, 5:6–8, 5:61–65, 6:22–25; Ex. 1001 ¶¶ 136–138). Intel

argues that interpreting L3 caches 14a–14n as “cache cores” is consistent with the ’631 specification. *Id.* at 40–41 (citing Ex. 1003, 29:53–56 (describing a “collector memory” that “may be segmented into multiple memory areas” where “[e]ach memory area may operate independently in different memory modes,” including as cache)).

According to Intel, a skilled artisan would have recognized that splitting the L3 cache into several individual parts would allow those parts to be “located closer to their respective processors, thus reducing access latency.” Pet. 42 (citing Ex. 1001 ¶ 141). Intel also argues that this arrangement would have promoted parallelism, since “each processor unit L3 cache can be accessed independently of the other.” *Id.* (citing Ex. 1001 ¶ 141). Thus, Intel argues that a person of ordinary skill in the art would have been motivated to achieve these predictable results by incorporating Arimilli’s cache structure in King’s multiprocessing system. *Id.*

PACT contests Intel’s proposed motivations to combine King with Arimilli’s shared cache, and argues that Intel has failed to show that a person of ordinary skill in the art would have had a reasonable expectation of success in this combination. *See* PO Resp. 14–23; PO Sur-reply 6–14. We address PACT’s main arguments below.

First, PACT argues that Intel has not shown that a person of ordinary skill in the art would have modified King by adding a shared cache to the 16 processor buses between processors P0–P3 and arbitration units ARB0–ARB3, colored green in Intel’s annotated version of King’s Figure 1 (reproduced above, *supra* part III.C.4). PO Resp. 14–19. PACT cites testimony of Professor Annavaram that “the proposed combination is not a simple substitution or a trivial modification, and could not be effected

‘without substantial experimentation and modification’ to King or Arimilli.” *Id.* at 15–16 (quoting Ex. 2023 ¶ 43). This is because in King, “no two processors are connected to the same bus,” so “it is impossible to connect Arimilli’s L3 caches to King’s processor buses without modifying the bus,” and Intel has not explained how a person of ordinary skill in the art would have performed that modification, or implemented an alternative cache coherency protocol. *Id.* at 16–17 (citing Ex. 2023 ¶¶ 45, 47). PACT argues that this proposed modification “would require, at the very l[e]ast, additional arbitration logic,” which “would increase latency of the system and contention for the processor buses.” *Id.* at 17 (citing Ex. 2023 ¶ 50).

In response, Intel argues that PACT is, in effect, requiring Intel’s combination to bodily incorporate Arimilli’s bus into King’s system, which Intel denies is necessary. *See* Pet. Reply 3–10. Intel contends that a person of ordinary skill in the art would have regarded King and Arimilli as compatible, because the two references have compatible goals of reducing access time and reducing the need for memory access, and because both King and Arimilli teach the advantage of sharing data between processors. *Id.* at 4 (citing Ex. 1005, 1:37–41, 2:7–10, 5:47–52; Ex. 1006, 1:60–64, 4:25–45, 3:42–48; Ex. 1001 ¶¶ 127–133, 141, 147–148; Ex. 1047, 61:14–62:12, 63:12–64:1; Ex. 1053 ¶ 15).

Specifically, Intel argues that a person of ordinary skill would have modified King to implement Arimilli’s shared cache by using Arimilli’s embodiment of a crossbar switch as King’s modified bus system. Pet. Reply 2 (citing Ex. 3:11–13); *id.* at 5 (citing Ex. 1053 ¶ 10; Ex. 1047, 118:15–24; Ex. 1048, 323; Ex. 2025, 183:13–185:10). Citing cross-examination testimony from PACT’s expert Professor Annavaram, Intel contends that the

16 processor buses shown in King’s Figure 1 are simply a “‘logical construct’ illustrating ‘certain functionality’ without requiring a ‘specific physical implementation.’” *Id.* at 6 (quoting Ex. 1047, 116:7–117:7 (quoting Ex. 1005, 2:60–64)). According to Intel, by using such a crossbar switch, a person of ordinary skill in the art could have chosen any well-known cache-coherency protocol, such as a point-to-point directory-based protocol. *Id.* (citing Ex. 1047, 59:18–60:15, 127:10–21, 173:4–12, 174:18–175:10; Ex. 1048, 450; Ex. 1053 ¶ 15; Ex. 2023 ¶ 47).

As to making the required processor-to-processor connections in King as modified by Arimilli, Intel argues that “arbitration was a well-known bus mechanism,” so a person of ordinary skill in the art “would have recognized ‘the possibility that through the arbitrator, processor-to-processor connections can be made’ such ‘that any processor can go and connect with the L3 each of any other processors.’” Pet. Reply 6 (quoting Ex. 2025, 182:25–183:6 (cross-examination testimony of Professor Mazumder)) (citing Ex. 1001 ¶¶ 49, 146; Ex. 1053 ¶ 11).

In its Sur-reply, PACT disputes that a person of ordinary skill in the art would have modified King by using a crossbar switch. PO Sur-reply 8–12. First, PACT contends that Intel’s Petition does not “propose modifying King’s processor buses to implement them as a crossbar interconnect, or explain why [a person of ordinary skill in the art] would be motivated to modify King’s processor buses in this way.” *Id.* at 8. PACT argues that Intel, to the contrary, expressly relies on King’s disclosure that each processor is connected to four bus units, resulting in 16 processor buses, “to show that King discloses ‘a plurality of bus segments for each processor.’” *Id.* at 9 (citing Pet. 23–24). Thus, PACT contends that we should disregard Intel’s

new theory about a crossbar switch that it first made in its Reply. *Id.* at 9 (citing *Ariosa Diagnostics v. Verinata Health Inc.*, 805 F.3d 1359, 1367 (Fed. Cir. 2015); 37 C.F.R. §§ 42.104(b)(5), 42.23(b)).

Addressing the merits of this argument, PACT argues that “if King’s sixteen processor buses are replaced with a crossbar interconnect, the resulting system no longer includes ‘a plurality of bus segments for each processor.’” *Id.* PACT cites cross-examination testimony by Professor Mazumder that instead of there being a plurality of bus segments for each processor, “if King’s interconnect is replaced with a crossbar or similar interconnect . . . , there will be ‘a single connection coming out of the processor [that] would be able to connect to different bus units, B0, B1, B2, B3.” *Id.* at 9–10 (quoting Ex. 2025, 184:1–4) (citing Ex. 2025, 184:5–185:10; Ex. 2028, 18:21–23:18).

We agree with PACT that Intel’s argument that King’s 16 bus segments could be implemented with a crossbar switch, first made in the Reply, is a new argument that relies on a previously unidentified portion of Arimilli to make a meaningfully distinct contention from what Intel argued in the Petition, and is therefore untimely. *See Ariosa*, 805 F.3d at 1367. We also find this new argument unpersuasive. As discussed above, we interpret the ordinary and customary meaning of the term “a plurality of bus segments for each processor” to exclude configurations in which the plurality of bus segments are only indirectly accessible to its corresponding processor through a switch or other segments. *See supra* part III.B.1. This would exclude a configuration where each of King’s processors is only directly connected to a single bus segment and the processor only has *indirect* access to other bus segments through a switch.

We also find unpersuasive Intel’s initial argument in the Petition, which did not rely on the use of a crossbar switch. As PACT persuasively argues, the combination of King and Arimilli in which a shared cache retains the 16 separate directly-connected bus segments as shown in King’s Figure 1 “requires modification of King’s bus arbitration units to allow for communication between different processor buses—a modification that is not disclosed by King or Arimilli.” PO Sur-reply 8 (citing Ex. 2023 ¶¶ 43–50; Ex. 1005, 1:46–50, 1:57–58). That “arbitration was a well-known bus mechanism” (Pet. Reply 6) is an insufficient rationale for modifying King in this way, because Intel has not specifically explained how a person of ordinary skill in the art would have modified King’s arbitration mechanism, in the context of 16 directly-connected bus segments, to incorporate a shared bus as disclosed in Arimilli. *See* PO Sur-reply 11–12 (citing *KSR*, 550 U.S. at 418–19; *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1351–52 (Fed. Cir. 2014); *In re O’Farrell*, 853 F.2d 894, 903 (Fed. Cir. 1988).

8. *Conclusion as to the Ground Based on King, Pan, and Arimilli*

Based on the evidence and arguments of record, we determine that Intel has not shown, by a preponderance of the evidence, that claim 4 of the ’631 patent would have been obvious over King in view of Arimilli, with or without Pan.

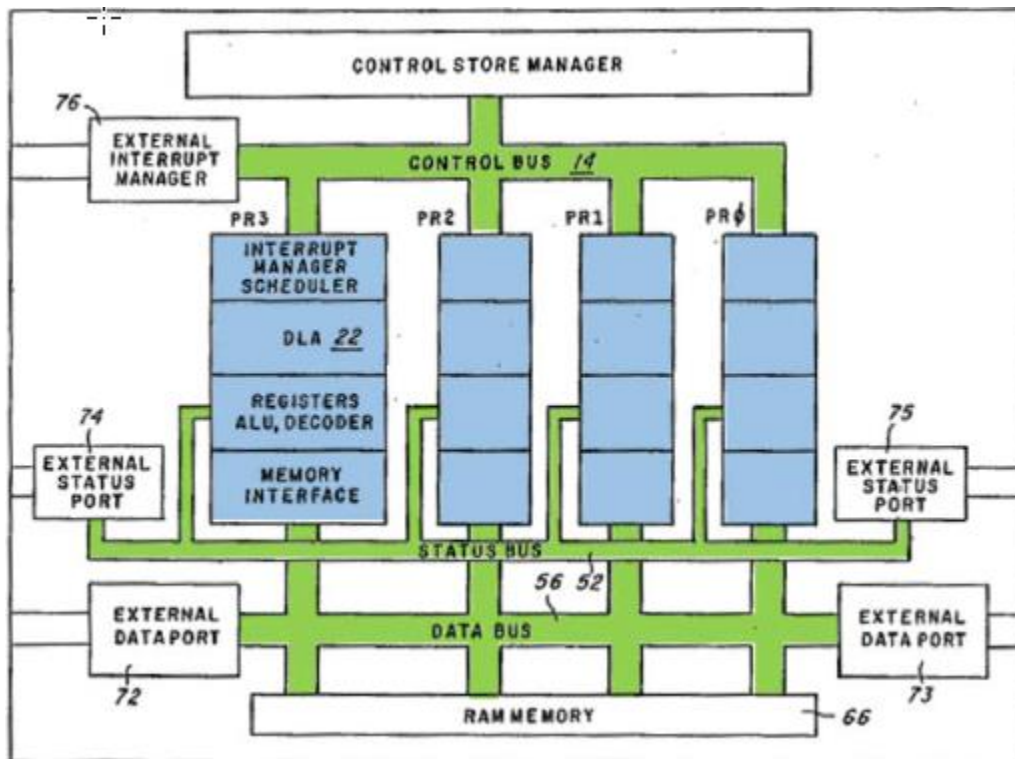
D. GROUND BASED ON BUDZINSKI, PAN, AND ARIMILLI

For the final ground, Intel alleges that claim 4 is unpatentable under § 103 as obvious “in view of Budzinski in combination with Arimilli or, in

the alternative, the combination of Budzinski, Pan, and Arimilli.” Pet. 66. For the reasons below, we determine that Intel has not proven this ground by a preponderance of the evidence. We discuss our findings and conclusions below, after an overview of Budzinski.

1. Overview of Budzinski

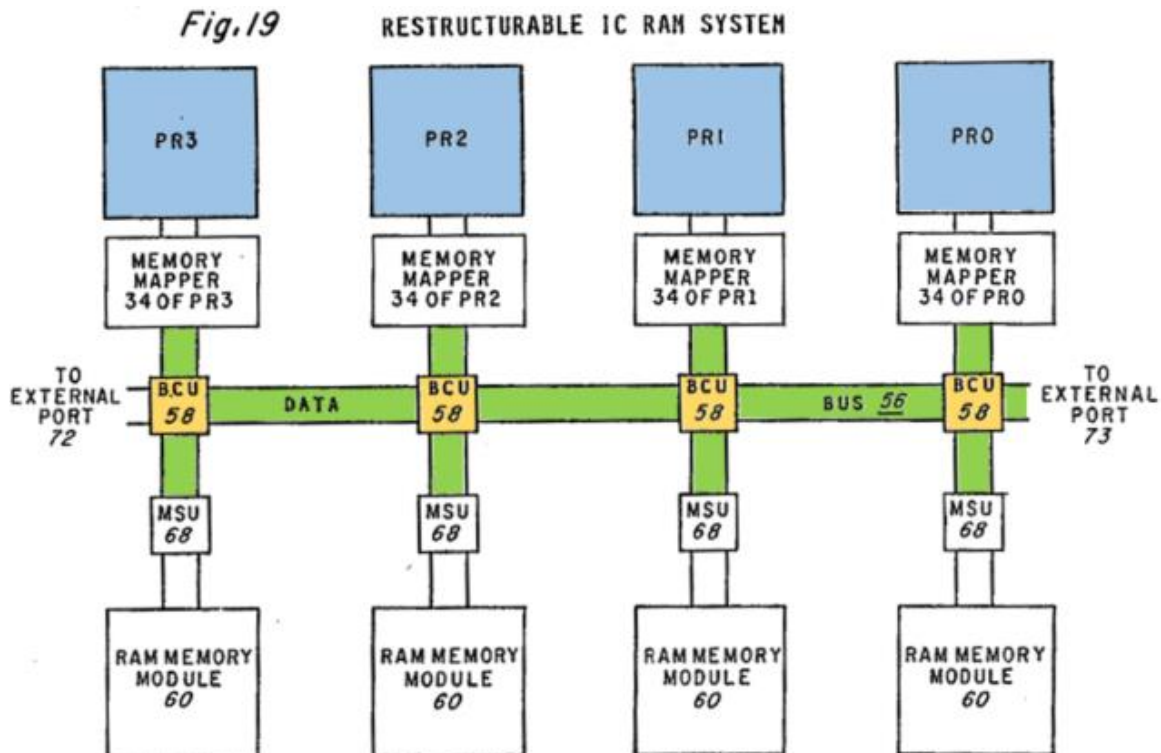
Budzinski describes a “restructurable integrated circuit,” in which all processors “are connected to data, control, and status busses,” and interfaces connected through those busses that “permit reconfigurability among the processors on a chip.” Ex. 1007, code (57). The overall system is shown in Figure 1, which we reproduce below with Intel’s added color-coding:



Pet. 16. Figure 1, above, depicts four processors PR0–PR3 (blue) on a single chip. Ex. 1007, 15:3–4. These processors connect to control bus 14, status bus 52, and data bus 56 (all green). *Id.* at 15:4–5. There are also an on-chip

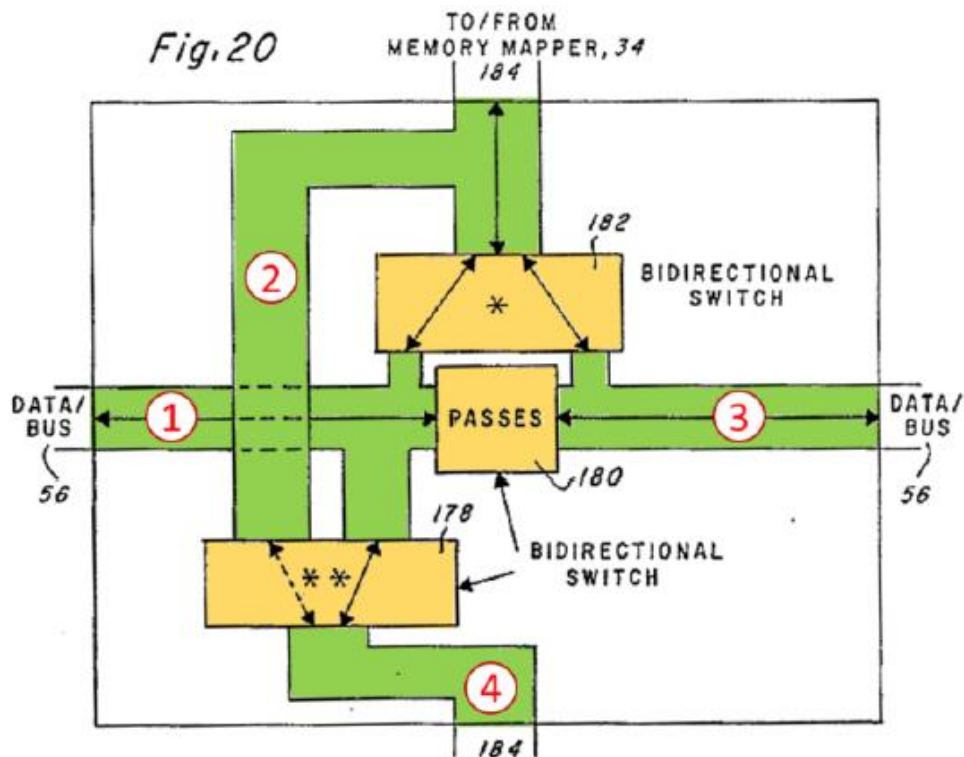
RAM memory 66 and external interfaces 72–76 for each of the buses. *Id.* at 15:5–8.

Budzinski's Figure 19, reproduced below with Intel's added color-coding, shows in more detail how processors PR0–PR3 are connected to memory modules:



Pet. 17. Figure 19, above, shows data bus 56 (horizontal green channels) and processors PR0–PR3 (blue) connected via memory mappers 34 and short busses (upper vertical green channels) to bus control units (BCUs) 58 (yellow), “which provides interface with the data bus 56.” Ex. 1007, 33:17–19. BCUs 58 are also connected by short busses (lower vertical green channels) to memory scheduler units (MSUs) 68 and to memory modules 60. *See* Ex. 1007, 33:15–22.

Budzinski's Figure 20, reproduced below with Intel's annotations and color coding, shows the structure of each BCU 58:



Pet. 18. Figure 20, above, shows that BCU 58 has three bidirectional switches 178, 180, and 182 (all yellow). Ex. 1007, 34:29–31. The buses are shown in green. Short bus 184 connects to memory mapper 34, and another short bus (bottom side)¹² connects via MSUs 68 to memory modules 60. *Id.* at 34:31–35. Bidirectional switches 178, 180, and 182 connect between the various buses as the data bus operates in various modes. *Id.* at 34:35–35:20. Intel includes annotation numerals 1–4 to identify what Intel contends are four separate bus segments. Pet. 16–17, 52.

2. Claim 1

As we discuss above, although claims 1–3 have been disclaimed, claim 4 inherits each of the limitations in claims 1–3 through dependency.

¹² According to Intel, “Figure 20 mislabels ‘short bus 186’ at the bottom of the figure as ‘184.’” Pet. 51 n.6.

See Ex. 1003, 34:20–43. Thus, we begin by addressing the limitations of claim 1. According to Intel, Budzinski, or a combination of Budzinski and Pan, teaches each limitation of claim 1, and a person of ordinary skill in the art would have had reason to combine Budzinski with Pan. *See* Pet. 48–66. For the reasons below, we do not find this persuasive.

(a) Limitation 1[a]

For limitation 1[a], Intel argues that Budzinski discloses that each processor is connected to a plurality of flexible data channels through its associated BCU. Pet. 51 (citing Ex. 1001 ¶¶ 157–158). According to Intel, these segments include the four labeled bus segments in Intel’s annotated version of Figure 20, reproduced above. *Id.* at 52 (citing Ex. 1001 ¶¶ 157–158). Intel further argues that these switches can be configured differently to provide different data paths. *See id.* (citing Ex. 1007, Fig. 21). Intel also argues that each processor is connected to a status bus, which is divided into one segment for each processor. *Id.* at 52–53 (citing Ex. 1001 ¶ 159). Thus, in its Petition, Intel identifies the “plurality of bus segments for each processor” as including the four labeled bus segments in annotated Figure 20, as well as the status bus. *See id.* at 51–54.

In response, PACT argues that Intel has failed to show that all of the four data bus segments Intel has identified in Budzinski’s Figure 20 are “for each processor.” *See* PO Resp. 24–26, 30–31. According to PACT, “the four ‘bus segments’ identified by Petitioner are simply four bus segments that the processor may indirectly access.” *Id.* at 25 (citing Ex. 2023 ¶ 76). Rather, “[o]nly one of the four bus segments identified by Petitioner is connected to a processor—the remaining bus segments are only accessible by the

processor depending on the configuration of the bus control unit (BCU).” *Id.* at 26 (citing Ex. 2023 ¶ 78).

Intel’s response focuses on its proposed construction which allows a bus segment to be “for” a processor even if the processor can only access it indirectly through a BCU switch. *See* Pet. Reply 13–20. As discussed above, we do not find this proposed claim construction persuasive. *See supra* part III.B.1.

For the first time in its Reply, Intel also presents the alternative theory that the bus segment labeled 2 in Intel’s annotated Figure 20 (reproduced above) “could itself be considered three segments. . . . [1] One is a vertical segment where the number 2 is written and [2] the horizontal segment, and then [3] this segment which is between 184 and 182.” Pet. Reply 22 (alterations in original) (quoting Ex. 2025, 156:5–9) (citing Ex. 1053 ¶ 25). Intel contends that this division of bus segments is consistent with Budzinski’s disclosure that segment 184 can connect to two different paths through either switch 178 or 182. *See id.* (citing Ex. 1007, 34:31–35:20; Ex. 1001 ¶¶ 157, 162; Ex. 1053 ¶ 25).

In its Sur-reply, PACT argues that “[t]his is a new argument on Reply and should be given no weight.” PO Sur-reply 15. PACT also argues that the new argument contradicts Intel’s earlier argument in the Petition that in the ’631 patent disclosure, the “bus segments” were “portions of a bus between endpoints—namely, switches.” *Id.* (quoting Ex. 1001 ¶ 94) (citing Pet. 23–24). PACT argues that “[t]he horizontal and vertical portion that make up bus segment ‘2’ are not separated by switches or an equivalent device—they represent a single bus segment.” *Id.* (citing Ex. 2025, 156:1–17 (Professor

Mazumder’s cross-examination testimony that the entirety of segment 2 can be construed as a single bus segment); Ex. 2028, 53:2–9).

We agree with PACT that the new argument Intel made in its Reply about segment 2 being multiple segments is a substantially different contention than what Intel argued in its Petition, and is thus untimely. *See Ariosa*, 805 F.3d at 1367. We also do not find Professor Mazumder’s supporting testimony persuasive, because even if segment 2 were divided into three segments as he proposes, his rationale for this division is that “bus segment 2 includes two separate data paths controlled by two separate switches.” Ex. 1053 ¶ 25. But he does not adequately explain why a person of ordinary skill in the art would have interpreted this as disclosing separate bus segments, rather than as disclosing separate data paths along the same bus segment.

Intel also presents another alternative theory, for the first time in its Reply, that “[d]ata bus segment 2 by itself provides parallel data paths for simultaneous transactions,” because it “can be configured by ‘bidirectional switch 180’ to ‘receive[] a data stream from an earlier stage of operation, and *contemporaneously* provide[] an output stream of data to the following stage of operation,’ thus permitting ‘*parallel transmission* of different streams of data between respective pairs of adjacent processors.’” Pet. Reply 23–24 (alterations in original) (quoting Ex. 1007, 35:10–20; Ex. 1001 ¶¶ 162–163, 165) (citing Ex. 1053 ¶ 30). As further support, Intel contends that Professor Annavaram admitted during cross-examination that data flows to and from each processor simultaneously. *Id.* at 24 (citing Ex. 1047, 153:17–154:1, 154:18–155:5).

In its Sur-reply, PACT argues again that “[t]his is a new argument that should be given no weight.” PO Sur-reply 16. PACT also argues that the new argument “is not supported by the disclosures of Budzinski,” since Budzinski discloses 16-bit processors which are “not capable of both send[ing] and receiving a 16-bit data unit on the same bus segment at one time.” *Id.* 16–17 (citing Ex. 1007, 5:15–20, 7:24–39, 8:37–9:9, 32:6–9, Fig. 16). Rather, PACT contends that in Budzinski’s pipelined mode, “separate processors *sequentially* perform different operations on a single data stream.” *Id.* at 17 (quoting Ex. 1007, 7:26–31). PACT further argues that Intel’s argument refers to multiple data channels, but does not show why, if segment 2 contains multiple data channels, this means that it comprises two bus segments. *See id.* at 16 n.1.

We agree with PACT that the new argument about segment 2 being bidirectional is a substantially distinct from what Intel argued in the Petition, and is thus untimely. *See Ariosa*, 805 F.3d at 1367. We also agree with PACT that Professor Mazumder’s testimony supporting Intel’s new argument does not persuasively show that segment 2 is actually two distinct bus segments, or that the bus segment literally sends and receives data at the same time while in pipeline mode. *See* Ex. 1053 ¶ 30.

Next, PACT argues that the combination of Budzinski’s single connected data bus and the single status bus do not, together, comprise “a plurality of flexible data channels to each processor” as recited in limitation 1[a]. PO Resp. 27. According to PACT, “[t]he data bus and status bus collectively provide one data channel to each processor, which may be used to facilitate a single data transaction at a time.” *Id.* at 27 (citing Ex. 2023 ¶ 80); *id.* at 31. They “do not provide alternative, parallel paths

between a processor and memory, unlike the multiprocessor system described in the '631 Patent.” *Id.* (citing Ex. 1003, 27:8–12; Ex. 1007, 16:20–31). PACT argues that “the status bus is only used to provide certain mode synchronization and control signals when two or more processors are operating in ‘pipelined’ or ‘lockstep’ mode.” *Id.* at 31–32 (citing Ex. 1007, 16:20–31); *see also* Ex. 2023 ¶ 80 (equivalent testimony by Professor Annavaram). PACT also argues that the status bus does not participate in allowing Budzinski’s processors to “select between multiple available paths corresponding to a plurality of senders or receivers.” PO Resp. 32; *see also* Ex. 2023 ¶ 80 (equivalent testimony).

In response, Intel argues that PACT “cites no evidence excluding [synchronization and control] signals from being considered ‘data.’” Pet. Reply 24 (citing Ex. 1001 ¶¶ 155, 163; Ex. 1053 ¶ 32). Intel contends that the status bus comprises a “further flexible data channel [for each processor], as Budzinski uses multiplexers to ‘selectively and programmably connect[] said respective processor through said status bus to adjacent . . . processors,’ . . . and selectively activates and deactivates certain status bus lines depending on a processing mode.” Pet. Reply 16 (second alteration in original) (quoting Ex. 1007, 9:18–33, 38:21–24, Figs. 23–25). Intel disagrees that the claim phrase “comprising a plurality of flexible data channels to each processor” requires “that the data channels must be ‘parallel.’” Pet. Reply 21.

While we agree with Intel that Budzinski’s data and status buses are separate bus segments as recited in limitation 1[a], we disagree with Intel that the data and status buses “comprise a plurality of flexible data channels to each processor.” In his second declaration, Professor Mazumder did not

disagree with Professor Annavaram that Budzinski's status bus provides synchronization and control signals. *See* Ex. 1053 ¶ 32. Instead, he opined that "[t]he term 'data' is broad, and a [person of ordinary skill in the art] would understand it to encompass not just, for example, data stored in memory, but also other types of control and status information." *Id.* While Professor Mazumder states that Professor Annavaram "does not cite anything in the '631 patent limiting the term 'data' to exclude status-type information," neither does Professor Mazumder point to any underlying evidence to support his opinion to the contrary. *See id.*¹³ Thus, we do not find Professor Mazumder's testimony to be more persuasive than that of Professor Annavaram. And as such, Intel has failed to establish, by a preponderance of the evidence, that the combination of Budzinski's data and status bus segments "compris[e] a plurality of flexible data channels to each processor."

(b) Limitations 1[b]–[c] and claim 4

Because we determine that Intel has failed to show that Budzinski, or a combination of Budzinski and Pan, discloses or teaches limitation 1[a], we do not need to consider the other limitations of claim 1. Likewise, we do not need to consider the added limitations of dependent claims 2 and 3, or the limitations of challenged claim 4, since claim 4 inherits limitation 1[a]. *See*

¹³ Professor Annavaram does point to a passage in the '631 patent describing the embodiment of Figure 5 as being capable of allowing *simultaneous* access to memory over a plurality of bus segments. *See* Ex. 2023 ¶ 80 (citing Ex. 1003, 27:8–12 ("For example, a memory may have a plurality, in particular, more than two bus connections to 0104 *a* and/or 0104 *b* to allow access to a plurality of senders/receivers to one memory, for example. Accesses may preferably also take place simultaneously (multi-port).")).

In re Fine, 837 F.2d 1071, 1076 (Fed. Cir. 1988) (“Dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.”).

3. *Conclusion as to the Ground Based on Budzinski, Pan, and Arimilli*

Based on the evidence and arguments of record, we determine that Intel has not shown, by a preponderance of the evidence, that claim 4 of the ’631 patent is unpatentable over Budzinski in view of Arimilli, with or without Pan.

IV. CONCLUSION

For the reasons above, Intel has not shown by a preponderance of the evidence that the challenged claim of the ’631 patent is unpatentable, as summarized in the following table:

Claim	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
4	103(a)	King, Pan, Arimilli		4
4	103(a)	Budzinski, Pan, Arimilli		4
Overall Outcome				4

V. ORDER

In consideration of the foregoing, it is

ORDERED that claim 4 of the ’631 patent has *not* been shown to be unpatentable;

FURTHER ORDERED that parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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