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Paper 33
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00535
Patent 8,312,301 B2

Before KEN B. BARRETT, CHARLES J. BOUDREAU, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges.*

BOUDREAU, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 3, 6–10, 12–19, 23–26, 30, 32, 35, and 36 (the "challenged claims") of U.S. Patent Number 8,312,301 (Ex. 1003, "the '301 patent"). Pet. 1. PACT XPP Schweiz AG ("Patent Owner") filed a Preliminary Response. Paper 6. With our authorization, Petitioner filed a Reply and Patent Owner filed a Sur-reply further addressing certain issues raised in the Preliminary Response. Paper 7; Paper 9. After reviewing these papers, we determined that Petitioner had demonstrated a reasonable likelihood of success in proving that the challenged claims are unpatentable, and we instituted an *inter partes* review of all challenged claims on the grounds set forth in the Petition. Paper 11 ("Institution Decision" or "Inst. Dec.").

After institution, Patent Owner filed a Response (Paper 19, "PO Resp."), Petitioner filed a Reply (Paper 22, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 27, "PO Sur-reply"). An oral hearing in this proceeding was held on May 21, 2021, and a transcript of the hearing is included in the record (Paper 32, "Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, we conclude that Petitioner has shown by a preponderance of the evidence that claims 3, 6, 7, 10, 12, 23, and 24 of the '301 patent are unpatentable under 35 U.S.C. § 103(a) but has not shown that claims 8, 9, 13–19, 25, 26, 30, 32, 35, and 36 are unpatentable on the grounds asserted with respect thereto.

A. Related Matters

The parties report that the '301 patent is the subject of ongoing district court litigation in *PACT XPP Schweiz AG v. Intel Corp.*, Civil Action No. 19-1006 (D. Del. May 30, 2019). Paper 4, 2; Paper 26, 2.

B. The '301 Patent

The '301 patent, titled "Methods and Devices for Treating and Processing Data," issued November 13, 2012, from U.S. Patent Application No. 12/570,984, filed September 30, 2009. Ex. 1003, codes (21), (22), (45), (54).

The '301 patent is directed to multiprocessor systems that include a plurality of processing elements and methods for thermal and power management and optimization in the operation of such systems. Ex. 1003, 1:26–29, 2:36–40. In certain embodiments, the methods include operating different logic cells using different clocking. *Id.* at 2:49–50. To achieve optimum data processing results with respect to time and power consumption, according to the '301 patent, "it is suggested that clocking takes place depending on the state, which means that no clock is preselected jointly for all cells based on a certain state, but rather an appropriate clock is assigned to each cell based on the state." *Id.* at 2:52–59.

By way of background, the '301 patent explains that a processor that is operated at a higher clock frequency requires more power and that the cooling requirements in modern processors increase substantially as the clock frequency increases. Ex. 1003, 2:20–23. The '301 patent further explains that "[s]emiconductor processes typically allow higher clock frequencies when they are operated at higher operating voltages," but that "this causes substantially higher power consumption and may also reduce

the service life of a semiconductor." *Id.* at 10:49–52. According to the '301 patent, "[a]n optimum compromise may be achieved in that the voltage supply is made dependent on the clock frequency. Low clock frequencies may be operated at a low supply voltage, for example. With increasing clock frequencies, the supply voltage is also increased." *Id.* at 10:53–57.

The '301 patent describes that various conditions may determine different clock frequencies for different data processing elements, including, for example, supply voltage, temperature, and prioritization of computations. The '301 patent explains, for example, that "[c]locking may be reduced overall in the case of a drop in supply voltage, in particular in mobile applications." Ex. 1003, 4:50–53, 7:48–53. The '301 patent describes an example of configuring clock frequencies so that "at a drop in the supply voltage, the entire frequency is reduced to a critical value U1; all cells are subsequently clocked slower by one half." *Id.* at 12:67–13:4. "[D]epending on the prioritization, different slowdowns according to the importance of the task are assigned to the respective groups at a voltage drop or under other circumstances." *Id.* at 13:8–11. With respect to temperature, the '301 patent discloses that the operating clock may be reduced if the operating temperature reaches certain threshold values. *Id.* at 7:8–9. According to the '301 patent, "[t]he reduction may take place selectively by initially operating those [processing array elements] on a lower clock which represent the most irrelevant performance loss." *Id.* at 7:9–12. With respect to prioritizing computations, the '301 patent describes an example of configuring multiple sequencers "involved in processing a data packet, requiring a different number of operations for data packet processing." Ex. 1003, 6:25–40. To obtain an optimum operation/power consumption ratio, the sequencer

requiring the most operations is clocked at the maximum operating frequencies, while the other sequencers are clocked proportionally according to their required operations. *See id.* at 6:41–47.

C. Illustrative Claims

Of the challenged claims, claims 3, 6, 8, 10, 12, 23, and 24 are independent. Claims 3, 8, 10, and 12 are illustrative and are reproduced below:

> 3. A method of operating a system having a plurality of data processing elements adapted for programmably processing sequences, to which tasks are assigned, and which are operable at different clock frequencies, the method comprising:
>
> grouping, by execution of software for managing distribution of code, a plurality of subsets of processing elements into processing element groups;
>
> effecting a plurality of temperature measurements in different regions of the system; and
>
> based on the temperature measurement, a control circuit modifying clock rates of the plurality of subsets of processing elements, wherein the clock rates set in the modifying step are set on a processing element group basis.
>
> 8. A processor device, comprising:
>
> a plurality of data processing elements adapted for programmably processing sequences and to which tasks are assigned, each of the data processing elements having at least one Arithmetic Logic Unit; and
>
> at least one bus system at least one of (a) interconnecting at least some of the data processing elements and (b) connecting at least some of the data processing elements with at least one of peripherals and external memory;
>
> wherein:
>
> each of at least some of the data processing elements is capable of operating at a clock frequency

different than at least one other of the data processing elements; and

the processor device is adapted for reducing clock frequencies of the data processing elements in response to a determination that a power reserve of a battery is below a predetermined threshold.

10. A processor device, comprising:

a plurality of data processing elements; and

a software adapted to be executed to (a) manage distribution of code sections, each code section to be executed by a respective group of a subset of the plurality of data processing elements, and (b) assign to each of the code sections a respective clock frequency, the group of data processing elements executing the respective code sections at the respective clock frequencies.

12. A processor device, comprising:

a plurality of data processing elements adapted for programmably processing sequences and to which tasks are assigned, each of the data processing elements having at least one Arithmetic Logic Unit; and

at least one bus system at least one of (a) interconnecting at least some of the data processing elements and (b) connecting at least some of the data processing elements with at least one of peripherals and external memory;

wherein:

each of at least some of the data processing elements is capable of operating at a clock frequency different than at least one other of the data processing elements;

the clock frequency of each of the data processing elements is at least determinable by a state of the processing device; and

the clock frequency for at least some of the data processing elements is set in accordance with a supply voltage.

Ex. 1003, 15:21–34, 15:59–16:9, 16:13–22, 16:27–45.

D. Asserted Grounds of Unpatentability

Petitioner asserted four grounds of unpatentability in the Petition:

Claim(s) Challenged	35 U.S.C. §[1]	Reference(s)/Basis
3, 6–9, 13–19, 25, 26, 30, 32, 35, 36	103(a)	Nicol,[2] Bhatia[3]
10, 12, 23, 24	103(a)	Nicol
10, 12, 23, 24	103(a)	Nicol, DeHon[4]
3, 6–9, 13–19, 25, 26, 30, 32, 35, 36	103(a)	Nicol, Bhatia, DeHon

Pet. 3–5. In its Reply, Petitioner states that the third and fourth grounds, based on the combination of Nicol and DeHon and the combination of Nicol, Bhatia, and DeHon, respectively, are "no longer at issue." Pet. Reply 23; *see also* Tr. 41:19–23 ("[T]here are only two grounds remaining of the initial four. Grounds 3 and 4 address the claim construction issue that neither party is advancing any longer and so we have streamlined that and focused now on Ground 1 and Ground 2, which are Nicol and Bhatia.").[5] Based on that

[1] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the '301 patent issued from an application filed before March 16, 2013, we apply the pre-AIA version of the statutory basis for unpatentability.

[2] Nicol et al., US 6,141,762, issued October 31, 2000 (Ex. 1006).

[3] Bhatia et al., US 6,535,798 B1, issued March 18, 2003 (Ex. 1007).

[4] DeHon et al., US 6,052,773, issued April 18, 2000 (Ex. 1008).

[5] We understand from the Petition and the parties' representations that the third and fourth asserted grounds were contingent on the adoption by the Board of Petitioner's proposed construction from the parallel district court litigation of the "data processing element[s]" terms recited in challenged claims 3, 6, 8, 10, 12, 23, and 24. *See* Pet. 68–77. As explained below,

representation, we address in this Decision only the first and second asserted grounds, based on the combination of Nicol and Bhatia and on Nicol alone, respectively.

Petitioner also relies on the Declarations of Carl Sechen, Ph.D., filed as Exhibits 1001 and 1050. Patent Owner relies on the Declaration of William Henry Mangione-Smith, Ph.D., filed as Exhibit 2022.

II. DISCUSSION

A. Claim Construction

In *inter partes* review proceedings filed on or after November 13, 2018, we apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. *See* 37 C.F.R. § 42.100(b) (2019); Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,341 (Oct. 11, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

In the Petition, Petitioner identified the phrase "data processing elements [adapted for programmably processing sequences]," as recited in each of claims 3, 6, 8, 10, 12, 23, and 24, as being the subject of the only

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neither the district court nor the Board concluded that such construction was warranted. *See infra* § II.A.

claim construction dispute with respect to the '301 patent in the co-pending district court litigation. Pet. 10. Regardless, Petitioner argued, that "the Board does not need to construe any claim term for purposes of evaluating the prior art in this Petition," because the prior art renders the challenged claims obvious under either construction proposed in the co-pending litigation. *Id.* at 11. Specifically, Petitioner alleged that claims 3, 6–9, 13–19, 25, 26, 30, 32, 35, and 36 are unpatentable over the combination of Nicol and Bhatia under Patent Owner's construction, whereas those claims are unpatentable over the combination of Nicol, Bhatia, and DeHon under Petitioner's proposed construction; and, similarly, that claims 10, 12, 23, and 24 are unpatentable over Nicol alone under Patent Owner's construction, whereas those claims are unpatentable over the combination of Nicol and DeHon under Petitioner's construction. *Id.* at 10–11.

In the Institution Decision, we noted that Patent Owner did not respond in the Preliminary Response to Petitioner's contentions regarding claim construction and did not propose construction of any other term, and we agreed with Petitioner that no express construction was necessary for purposes of determining whether to institute *inter partes* review. Inst. Dec. 18.

In its Response, Patent Owner represents that the "data processing elements" term is no longer in dispute in the district court litigation "as the Court has determined that the terms shall be construed according to their plain and ordinary meaning and that no construction is necessary." PO Resp. 5–6. The parties do not otherwise provide any further briefing regarding claim construction in their post-institution papers, and we

maintain our earlier conclusion that no express construction is necessary. *See generally* PO Resp.; Pet. Reply.

B. Legal Framework

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;[6] and (4) when in evidence, objective evidence of obviousness or nonobviousness, i.e., secondary considerations.[7] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). "To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements" but "must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness." *In re Magnum Oil Tools Int'l, Ltd*., 829 F.3d 1364, 1380 (Fed. Cir. 2016). One

[6] Relying on the testimony of Dr. Sechen, Petitioner proposes a definition of a person of ordinary skill in the art of the '301 patent as "a person having at least a Master's degree in Electrical Engineering (or equivalent experience), and at least three years of experience with processor design and memory architecture." Pet. 9–10 (citing Ex. 1001 ¶¶ 106–108). Patent Owner adopted Petitioner's proposed definition for its Response. PO Resp. 11. We agree that Petitioner's proposed level appears reasonable in light of the Specification and the prior art, and we, accordingly, also adopt Petitioner's proposal to the extent necessary for the purposes of this Decision.

[7] The record does not include allegations or evidence of objective indicia of obviousness or nonobviousness.

seeking to establish obviousness based on more than one reference also must articulate sufficient reasoning with rational underpinnings to combine teachings. *See KSR*, 550 U.S. at 418. We analyze the asserted grounds with the principles stated above in mind.

C. Obviousness of Claims 3, 6–9, 13–19, 25, 26, 30, 32, 35, and 36 over Nicol and Bhatia

1. Overview of Nicol

Nicol, titled "Power Reduction in a Multiprocessor Digital Signal Processor Based on Processor Load," relates to dynamically controlling processing load of multi-processor chips by controlling tasks, clock frequency, and supply voltage. Ex. 1006, codes (54), (57), 2:18–22.

Nicol illustrates an embodiment of a multi-processor chip in Figure 2, reproduced below.

FIG. 2

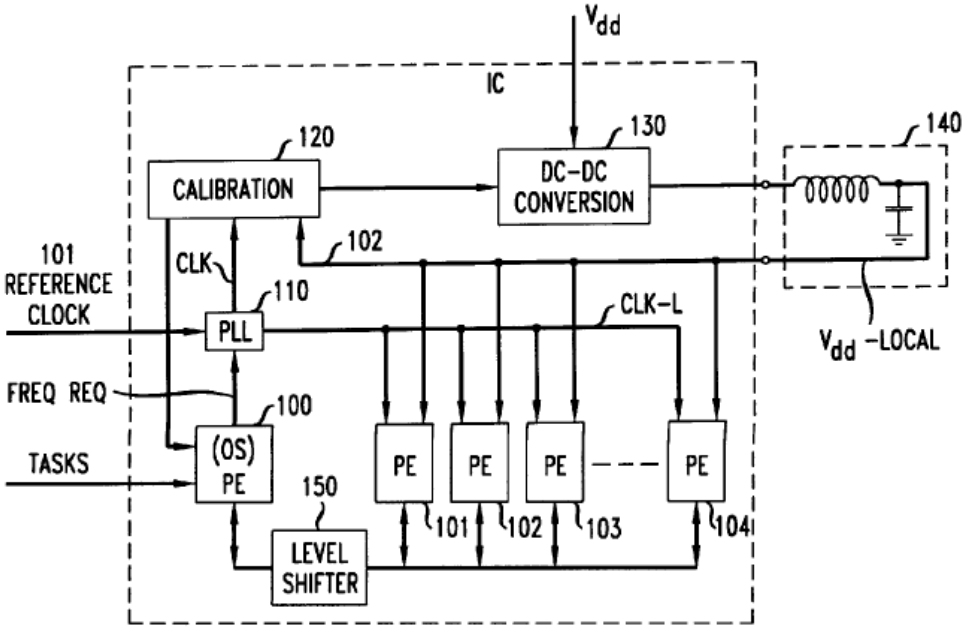


Figure 2 of Nicol, above, is a block diagram of a multi-processor chip with Supply Voltage control. Ex. 1006, 2:37–39.

With reference to Figure 2, Nicol explains that the multi-processor chip contains multiple processing elements (PEs). Ex. 1006, 2:50–53. Nicol discloses "[a] real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications." *Id.* at 2:53–56. Nicol discloses:

> The FIG. 2 system uses the operating system to react to variations in the system load. As more tasks are entered into the "to-do" list, the operating system of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors. It then computes the required operating frequency.

Id. at 5:23–28.

Nicol's Figure 4, reproduced below, illustrates another embodiment of a multi-processor chip.

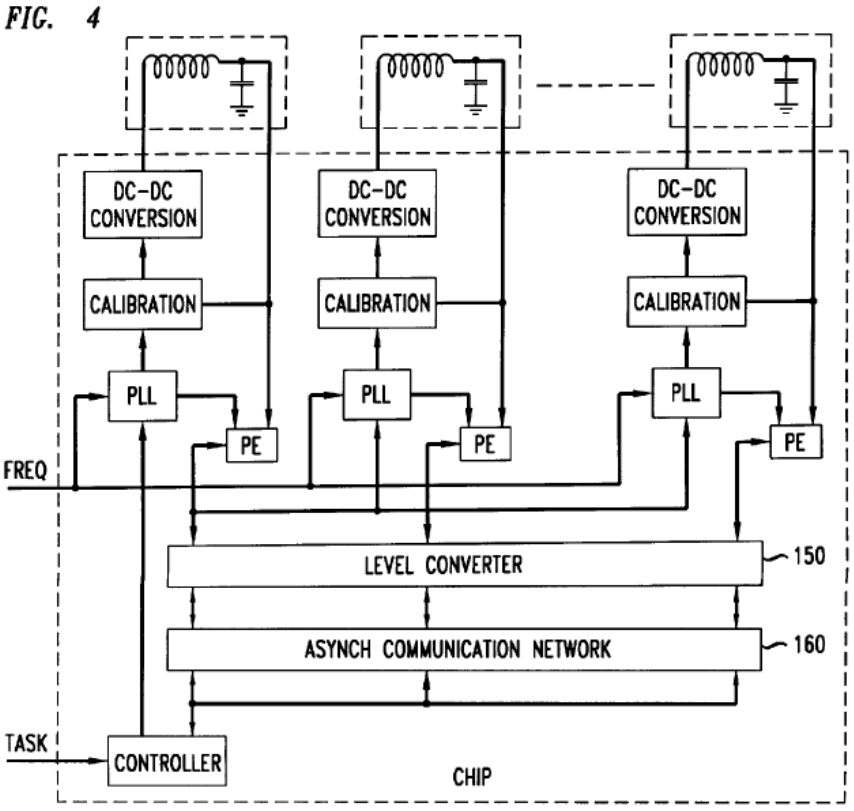


Figure 4 of Nicol, above, is a block diagram of a multi-processor chip with supply voltage control that is individual to each of the processing elements. Ex. 1006, 2:45–47.

Nicol explains that "[t]he notion of adjusting operating frequency to load and adjusting supply voltage to track the operating frequency can be extended to allow each PE to have its own supply voltage." Ex. 1006, 5:52–56. With reference to Figure 4, Nicol discloses an arrangement wherein a separate power supply for each PE in a chip allows the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. *Id.* at 5:66–6:3. With reference to Figure 4, Nicol discloses,

> all of the controllers are embodied in [] single controller 200 . . . . Each processing element also requires a calibration circuit like circuit 120, and a voltage converter circuit like circuits 130 and 140. It also has [] PE 200 that assigns the tasks given to the multi-processor chip of FIG. 4 among the PEs.

Id. at 6:6–13.

Nicol explains the issue of synchronizing differing frequencies "at which the individual PEs operate differ from one another and from other elements within the system where the multiprocessor chip is employed." Ex. 1006 at 6:14–28. "To effect such synchronization, each PE within the FIG. 4 arrangement is connection to an arrangement comprising elements 150 and 160." *Id.* at 6:29–31. "Level converter 150 converts the variable voltage swings of the PEs to a fixed level swing, and network 160 resolves the issue of different clock domains." *Id.* at 6:31–33.

Nicol discloses that "[t]he principles disclosed above for a multiprocessor [are] extendible to other system arrangements," including

"systems with a plurality of separate processor elements that operate at different frequencies and operating voltages, as well as components that are not typically thought of as processor elements." Ex. 1006, 6:34–39. Moreover, Nicol discloses that "the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage." *Id.* at 6:66–7:3.

Nicol illustrates the relationship between clock frequency and voltage in Figure 3, reproduced below.

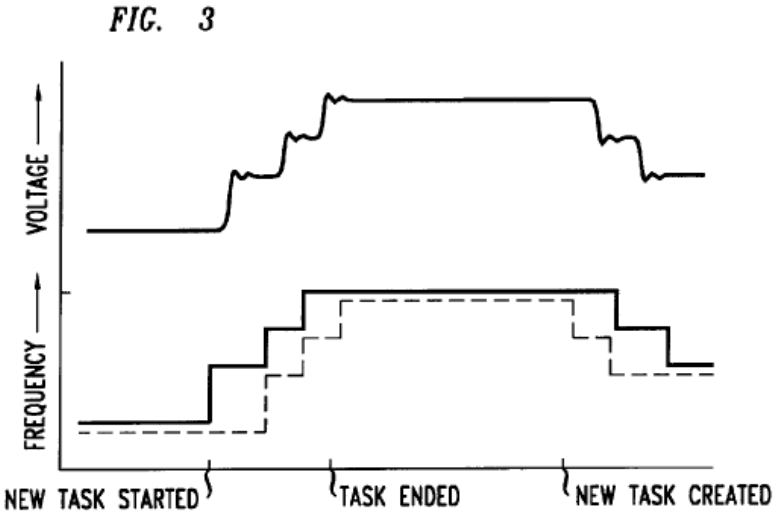


Figure 3 of Nicol, above, shows the relationship between the voltage control clock, CLK, of FIG. 2, the clock applied to the processing elements of FIG. 2, CLK-L, and the Supply Voltage applied to the processing elements, V_{dd}-local.[8] Ex. 1006, 2:40–44.

[8] Petitioner contends that Figure 3 of Nicol includes obvious errors, in that "NEW TASK STARTED" should state "TASK CREATED"; "TASK ENDED" should state "TASK STARTED"; and "NEW TASK CREATED" should state "TASK ENDED." *See* Pet. 13 n.4. Patent Owner does not dispute that contention.

With reference to Figure 3, Nicol describes:

> the timing associated with increasing Clk, Clk-L and V_{dd}-local when a new task is created and the load on the multiprocessor is thus increased, and the timing associated with decreasing Clk, Clk-L and V_{dd}-local when the load on the multiprocessor is decreased. Specifically, it shows the system operating at 70 MHz from a 1.8V supply when the load is increased in three steps to 140 MHz. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution. Some time thereafter according to FIG. 3, a task completes, which reduces the load on the multiprocessor. The reduced load permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V. This, too, is accommodated in steps (two steps, this time), with Clk-L preceding Clk to insure, again, that the PEs continue to operate properly while the supply voltage is decreased.

Id. at 4:54–5:2.

2. Overview of Bhatia

Bhatia, titled "Thermal Management in a System," relates to a system including "a component having a clock and a thermal management controller adapted to vary the component between performance states including a lower performance state when the controller detects a first condition, the controller adapted to throttle the clock while the component is in the lower performance state." Ex. 1007, codes (54), (57), 1:53–59.

Bhatia explains that "[d]ifferent types of power and thermal management techniques have been implemented in systems." Ex. 1007, 1:6–7. An example of a known technique "is defined by the Advanced Configuration and Power Interface (ACPI) Specification, Rev. 1.0, published on Dec. 22, 1996, that provides an interface between the operating system of a system and hardware devices to implement power and thermal management." *Id*. at 1:13–18. Bhatia explains that the ACPI specification

defines two execution states for a CPU: a full-speed state and a throttled state in which the CPU clocks are active only for a programmed percentage of the time. *Id.* at 1:39–42.

Bhatia further discloses "a thermal management scheme in which one or more system components are switched between different levels (two or more) of performance states in response to over-temperature conditions or other conditions." Ex. 1007, 2:24–28. The components may include "general or special-purpose processors such as microprocessors, microcontrollers, application specific integrated circuits (ASICs), programmable gate arrays (PGAs), peripheral device controllers, and other types of devices" including multi-processor systems. *Id.* at 2:32–36, 3:24–28.

Bhatia explains "[a] performance state may be characterized by component core and bus clock speeds and component supply voltage levels," and may include a high performance ("HP") state and low performance ("LP") state. Ex. 1007, 2:38–44. "In the HP state, a processor's (or other component's) core clock frequency and voltage level may be at one setting, while in the LP state, the processor's core clock frequency and voltage level may be at a lower setting." *Id.* at 2:45–48. Bhatia discloses cycling between the HP and LP states when an over-temperature condition exists. *Id.* at 2:51–55. In particular, according to Bhatia, "[t]he processor (or other component) spends a programmed percentage of time in the LP state (throttled or non-throttled) and the rest of the time in the HP state." *Id.* at 2:51–53. Alternatively, Bhatia explains, "if more than two performance states are available, the processor may be transitioned among the different

performance states, with throttling being performed from any of the performance states if necessary." *Id.* at 3:11–14.

Bhatia's Figure 6, reproduced below, illustrates power dissipation P_y as a processor is throttled from the LP state. Ex. 1007, 9:41–45.

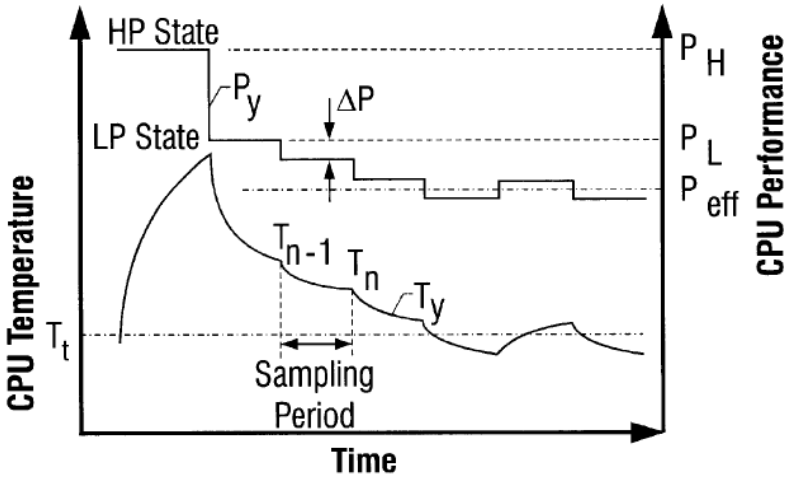


FIG. 6

Figure 6 of Bhatia, above, is a graph of power dissipation levels and temperatures when performing thermal management according to an embodiment of Bhatia's invention. *Id.* at 2:2–5.

Bhatia discloses one or more temperature sensing units that monitor system temperature in corresponding temperature zones. Ex. 1007, 3:33–46. The temperature sensing units are "each capable of issuing an interrupt, e.g., a system management interrupt (SMI), a system controller interrupt (SCI), or some other notification when a sensed temperature rises above a preset target temperature T_t, or falls below the target temperature T_t." *Id.* at 3:34–39. Bhatia discloses that thermal management may be performed independently for multiple thermal zones. *Id.* at 3:64–65.

In addition to thermal management, Bhatia teaches a power management module to control performance state transitions. Ex. 1007, 12:26–32. "The power management module determines [] if a performance

state change is required in response to a received event, indicating a thermal event, power supply transition, docking/undocking, a user command, or other event has occurred." *Id.* at 12:32–36. The power management module may indicate a new performance state by writing a predefined value to a control register. *Id.* at 12:38–44. Bhatia teaches that

> programming of the control register may be defined under the ACPI specification. Thus, in one embodiment, one or more ACPI objects may be created to indicate to the operating system that the computer is capable of transitioning between or among different performance states and to denote the resources that may be used by the operating system to perform the transitions. The location and structure of the control register may be defined under an ACPI object. Further, one or more ACPI objects may define the number of performance states available, the core clock frequencies and supply voltage levels to be used in the performance states, the expected power consumption in each performance state, and other information.

Id. at 12:44–57. Bhatia discloses that "[n]ext, the power management module places [] the processor [] into a low activity state," such as a "deep sleep state," in which "no activity is performed by the processor except maintenance of the stored data in the processor's internal cache," or a "stop grant state," in which the processor performs only minimal activity. *Id.* at 12:58–67.

3. Motivation to Combine Nicol and Bhatia

Citing the testimony of Dr. Sechen, as well as Nicol's and Bhatia's respective disclosures, Petitioner argues that a person of ordinary skill in the art would have been motivated to combine the teachings of Nicol and Bhatia for several reasons. Pet. 18–21 (citing Ex. 1001 ¶¶ 138–152; Ex. 1006,

code (54), 2:18–27, 3:13–18; Ex. 1007, code (54), 1:6–8, 1:57–59, 2:18–31, 3:9–20, 3:24–28, 3:33–46, 4:11–13, 12:26–37, 12:58–64[9]).

First, according to Petitioner, Nicol and Bhatia "both are directed to interrelated thermal and power management aspects that are critical and ubiquitous in processor-based systems." Pet. 18.

Second, "Nicol and Bhatia both describe a flexible multiprocessor architecture in which software residing in a controller is programmed to selectively control the power supply of each processor . . . by dynamically adjusting the processor's clock frequency during operation." Pet. 19. Petitioner contends that "[a]lthough Bhatia is primarily directed to thermal management, its controller software also performs power management functions." *Id.* (citing Ex. 1007, 12:26–37). Citing Dr. Sechen's testimony, Petitioner argues that a person of ordinary skill in the art "would have found it obvious to program Nicol's controller to handle the additional software functionalities discussed in Bhatia, yielding an improvement with predictable results." *Id.* (citing Ex. 1001 ¶¶ 138–152).

Third, Petitioner contends, "Nicol is focused on minimizing power consumption and does not discuss over-temperature protection," but "over-temperature protection is critical for high-performance systems such as Nicol's multiprocessor system and [system-on-a-chip (SoC) systems]," and a person of ordinary skill in the art seeking to improve Nicol therefore "would have been motivated to consult Bhatia, which discusses well-known

[9] Because Petitioner's arguments at pages 18–21 of the Petition relate to Nicol (Exhibit 1006) and Bhatia (Exhibit 1007), rather than to DeHon (Exhibit 1008), we understand each of Petitioner's citations to Exhibit 1008 in the cited portion of the Petition to refer instead to Exhibit 1007.

techniques of providing over-temperature protection, as well as additional improvements." Pet. 20 (citing Ex. 1001 ¶¶ 138–152).

Finally, Petitioner argues, "Bhatia describes in detail '***low-activity state[s]*** . . . commonly used by power management systems to reduce power," and a person of ordinary skill in the art "would have been motivated to consult Bhatia and implement those low activity states in Nicol's system as additional means to further minimize power consumption" with "a reasonable expectation of success . . . because those low activity states were commonly used in the industry." *Id.* at 20–21 (citing Ex. 1001 ¶¶ 138–152; Ex. 1007, 12:58–64).

In its Response, Patent Owner argues that Petitioner's proffered motivations amount only to a suggestion that it would have been beneficial to combine aspects of a computer system managed by Nicol and Bhatia, which, according to Patent Owner, is "plainly insufficient" "without any showing of actual motivation" and "evidences application of impermissible hindsight bias." PO Resp. 27–28 (citing Pet. 18–21; Ex. 2022 ¶ 56; *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068 (Fed. Cir. 2018)). Further, according to Patent Owner, "Petitioner makes no attempt to explain how a system combining Nicol and Bhatia would function, likely due to the fact that managing a plurality of metrics to create an efficient processing system is extremely difficult." *Id.* at 28 (citing Ex. 2022 ¶ 57). Citing Dr. Mangione-Smith's testimony, Patent Owner contends that a person of ordinary skill in the art "might spend their entire career developing intricate systems for managing processor temperature and clock frequency among a plurality of processors, and Petitioner dismisses it as a mere triviality." *Id.* (citing Ex. 2022 ¶ 57). Lastly, Patent Owner contends that "combining

Nicol and Bhatia would frustrate the purpose of each," as "Nicol is designed to minimize power consumption by lowering the clock frequency and therefore the voltage demanded by the processors," while "Bhatia is designed to maintain a system operating at a high performance, characterized by a high frequency . . . without exceeding over-temperature thresholds." *Id.* at 28–29 (emphasis omitted) (citing Ex. 1006, code (57), 2:22–27; Ex. 1007, 1:47–49, 3:14–23, 6:41–51; Ex. 2022 ¶ 58).

Petitioner replies that Patent Owner's arguments against combining Nicol and Bhatia are meritless and contradicted by Patent Owner's expert's testimony. Pet. Reply 15–19. First, Petitioner contends, Patent Owner is incorrect that the Petition merely describes the "benefits" of combining Nicol and Bhatia without showing actual motivation to combine. *Id.* at 16. According to Petitioner, the Petition explains, for example, that "a [person of ordinary skill in the art ('POSITA')] seeking to improve Nicol would have been motivated to consult Bhatia, which discusses well-known techniques of providing over-temperature protection" and "low activity states . . . to further minimize power consumption." *Id.* at 16–17 (quoting Pet. 20, 21) (citing PO Resp. 27). Petitioner contends that Patent Owner failed to address these reasons and that, in fact, Patent Owner's expert testified that Nicol explicitly contemplates the need for and ability to address thermal management. *Id.* at 17 (citing Ex. 1049, 134:16–135:9).

Moreover, Petitioner argues, "[t]he Petition and Dr. Sechen explain how Bhatia discloses well-known techniques and thermal sensors to protect against over-temperature and thus addresses the exact thermal-management need undisputedly called for in Nicol." Pet. Reply 17 (citing Pet. 20; Ex. 1001 ¶¶ 138–152). Petitioner also argues that "there is no dispute that a

POSITA understood how to use such thermal sensors to manage temperature in Nicol's multiprocessor," as Patent Owner's expert "*admitted* that a POSITA 'concerned about overheating' Nicol's system would 'know of ways that he could do temperature management using a temperature sensor.'" *Id.* (quoting Ex. 1049, 129:23–130:9). According to Petitioner, "[t]he well-known benefits of combining the teachings of Nicol and Bhatia explained in the Petition, which stand unrebutted, provide ample reasons to combine." *Id.*

Responding to Patent Owner's contentions that the Petition does not "explain how a system combining Nicol and Bhatia would function" and that the combination would "frustrate the purpose of each" reference (PO Resp. 28–29), Petitioner argues:

> Not so. Bhatia's over-temperature protection system would not interfere with Nicol's task scheduling under normal operation, and a POSITA would have understood that Nicol's task scheduling would need to be altered or suspended when the multiprocessor system overheats, in which case Bhatia's software would take control to avoid device failure."

Pet. Reply 18–19 (citing Ex. 1050 ¶ 35).

In its Sur-reply, Patent Owner argues that the proposed combination of Nicol and Bhatia would not work and that a person of ordinary skill would not have had a reasonable expectation of success. PO Sur-reply 11. According to Patent Owner, Nicol "describes a relatively simplistic system" in which a task is not started until a specific clock frequency is reached and the clock frequency remains constant until the task is completed without any adjustment during the execution of the task, whereas Bhatia "rel[ies] on a discrete set of states . . . which have different clock frequencies and cycles between them." *Id.* at 11–12 (citing Ex. 1001 ¶¶ 120–121; Ex. 2025, 95:2–

96:2, 109:7–21, 115:17–116:8, 116:19–24). In response to Petitioner's argument that Nicol's task scheduling would be free from interference under normal operation and that Bhatia would take over once the overtemperature condition is met (Pet. Reply 18–19), Patent Owner alleges that "Nicol's task scheduling does not take into account any potential interruptions due to overtemperature, or for any other reason," and requires "a constant, single value of the clock frequency needed to ensure completion of a task during the required completion time, assuming no interruptions." PO Sur-reply 12. According to Patent Owner, a person of ordinary skill in the art "would not be motivated to combine Nicol and Bhatia in a way that failed to achieve Nicol's goal of completing tasks within a required completion time." *Id.* at 12–13.

Patent Owner further contends that "Petitioner's described system combining Nicol and Bhatia only works if we make assumptions counter to the stated motivation to combine." PO Sur-reply 13. In particular, according to Patent Owner, "[t]he only way the combined system would work properly is if the overtemperature condition were not met and Nicol's task scheduling could proceed without any alteration or interference," "[b]ut if the overtemperature condition were guaranteed not to be met, there would no longer be a need to combine Nicol with Bhatia." *Id.* Still further, Patent Owner contends, the "reality of power management is that there are many factors to consider" and that "need of tradeoffs" involved in selecting one combination over another in order to create a system with a reasonable expectation of success "was well known at the time." *Id.* at 13–14 (citing Ex. 1014, 8-145; Ex. 2025, 97:20–98:7). Accordingly, Patent Owner repeats from its Response, a person of ordinary skill in the art "might spend their

entire career developing systems for managing processor temperature and clock frequency among a plurality of processors." *Id.* at 14 (citing Ex. 2022 ¶ 57); *see also* PO Resp. 28 (same).

Having fully considered the parties' contentions, we are persuaded that Petitioner has articulated sufficient and persuasive reasoning, with rational underpinnings, to establish that a person of ordinary skill in the art would have been motivated to combine Nicol and Bhatia in the manner proposed by Petitioner and would have had a reasonable expectation of success in doing so. As Petitioner points out, Nicol expressly contemplates that temperature tracking would be desirable in its power management system (*see, e.g.*, Ex. 1006, 4:11–13 (explaining that "the operating system can reduce the supply voltage even further by tracking temperature and process variations"); *see also* Ex. 1049, 134:25–135:9 (Patent Owner's expert recognizing the same)) but does not itself provide any detail, and we credit Dr. Sechen's logical, clear and reasoned testimony, relied upon by Petitioner and supported by the record evidence, that a person of ordinary skill in the art would have been motivated to consult Bhatia and implement the disclosed low activity states in Nicol's system (*see* Ex. 1001 ¶¶ 149–152). *See, e.g.*, *KSR*, 550 U.S. at 420 ("[A]ny need or problem known in the field . . . can provide a reason for combining the elements in the manner claimed."). We also find persuasive Petitioner's argument that it is undisputed that a person of ordinary skill in the art would have understood how to manage temperature in Nicol's multiprocessor system. *See* Pet. Reply 17 (citing Ex. 1049, 128:20–130:9 (Patent Owner's expert agreeing that a person of ordinary skill in the art would have known of ways to use a

temperature sensor in implementing Nicol "[a]t least to the extent that the Pentium disclosed it, for example")).

Despite Patent Owner's arguments to the contrary (*see* PO Resp. 19–20), we are not persuaded that Nicol and Bhatia are incompatible in any relevant way. *See MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015) ("[T]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference." (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)); *Lear Siegler, Inc. v. Aeroquip Corp.*, 733 F.2d 881, 889 (Fed. Cir. 1984) (The ordinary artisan is not "compelled to adopt every single aspect of [a reference's] teaching without the exercise of independent judgment."). Contrary to Patent Owner's arguments, we do not understand Petitioner to contend that implementation of the low activity states of Bhatia would entail cycling between states with different clock frequencies in the normal operation of Nicol's system, but rather that such cycling would occur, if at all, only when the multiprocessor system is determined to be overheating. *See* PO Sur-reply 12. As Patent Owner acknowledges, Petitioner contends that "Bhatia's over-temperature protection system would not interfere with Nicol's task scheduling under normal operation" and that "Nicol's task scheduling would need to be altered or suspended" only "when the multiprocessor system overheats." PO Sur-reply 18–19. That contention is fully consistent with Dr. Sechen's testimony cited by Patent Owner that "[i]f there's no heating . . . Bhatia's additional performance states would . . . not interfere with the normal operation of Nicol." Ex. 2025, 11:6–25.

Further, we disagree with Patent Owner's contentions either that Nicol's failure to "take into account any potential interruptions due to

overtemperature, or for any other reason" or that "if there were an overtemperature condition, the combined system would not complete tasks within the required times" would have dissuaded a person of ordinary skill in the art from combining Nicol and Bhatia. *See* PO Sur-reply 12–13. Notwithstanding Patent Owner's arguments, it is not credible that a person of ordinary skill in the art would have understood Nicol to prefer device failure over any alteration or suspension of task scheduling, even if the latter potentially would result in tasks not being completed "within the required times" as Patent Owner's arguments appear to suggest. Rather, we credit Dr. Sechen's testimony, relied upon by Petitioner, that a person of ordinary skill in the art would have understood that Nicol's task scheduling would need to be altered or suspended to avoid chip failure due to overheating. Ex. 1050 ¶ 35; *see* Pet. Reply 18–19.

Finally, notwithstanding Patent Owner's expert testimony that a person of ordinary skill in the art "might spend their entire career developing systems for managing processor temperature and clock frequency among a plurality of processors" (Ex. 2022 ¶ 57), the challenged claims recite only modifying clock rates based on temperature measurement, not a perfect optimization of such parameters. Accordingly, we are not persuaded by Patent Owner's arguments based on that testimony that a person of ordinary skill in the art would not have had a reasonable expectation of success in implementing the proffered combination or that the combination would have required undue experimentation and would not have yielded predictable results. *See* PO Resp. 28; PO Sur-reply 14. As the Federal Circuit has explained, "[t]he reasonable expectation of success requirement refers to the likelihood of success in combining references to meet the limitations of the

claimed invention." *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016). In light of Petitioner's arguments regarding the teachings of Bhatia, as well as Petitioner's further argument that Nicol itself discloses the use of thermal sensors to track temperature in a multiprocessor chip (*see id.* at 31 (citing Ex. 1006, 1:41–48, 4:11–13)), supported by the testimony of Dr. Sechen (*see, e.g.*, Ex. 1001 ¶¶ 138–150, 207–214), we are persuaded that a person of ordinary skill in the art would have had a reasonable expectation of success in combining Nicol's and Bhatia's teachings.

4. Independent Claim 3

Petitioner contends that Nicol teaches all limitations of independent claim 3, with the exception of "effecting a plurality of temperature measurements in different regions of the system; and based on the temperature measurement, a control circuit modifying clock rates of the plurality of subsets of processing elements," for which limitations Petitioner additionally relies on Bhatia. Pet. 21–33. Petitioner's contentions are supported by citations to the evidence of record, including the testimony of Dr. Sechen and evidence cited therein. *See id.* (citing Ex. 1001 ¶¶ 153–156, 162–164, 172–181, 184–195, 198–199, 202–221, 311–312; Ex. 1006, 1:41–48, 2:44, 2:50–56, 3:11–13, 4:3–5, 4:11–13, 5:23–28, 5:42–44, 5:66–6:2, 6:6–18, 6:26–28, 6:40–41, 6:63–7:3, Figs. 2, 4;[10] Ex. 1007, code (57), 1:6–

[10] Because Petitioner's arguments at pages 21–28 of the Petition relate to Nicol (Exhibit 1006), rather than to the '301 patent (Exhibit 1003), we understand each of Petitioner's citations to Exhibit 1003 in the cited portion of the Petition to refer instead to Exhibit 1006.

17, 2:24–28, 3:28–39, 3:64–65, 4:34–37, 12:5–10;[11] Ex. 1010, 290, 491–93, Fig. 3.14; Ex. 1013, 37, 45, Fig. 1; Ex. 1018, Fig. 4). For the reasons that follow, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claim 3 is unpatentable over the combination of Nicol and Bhatia. We address each element of claim 3 in turn.

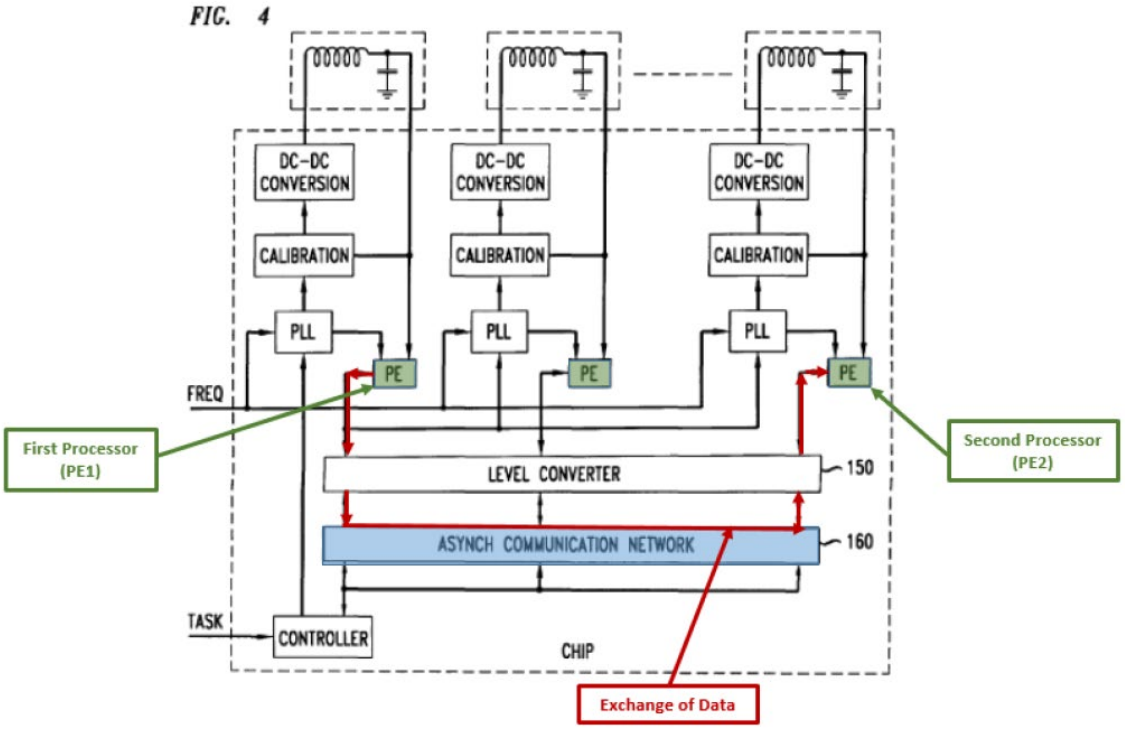
a) *"A method of operating a system having a plurality of data processing elements adapted for programmably processing sequences, to which tasks are assigned, and which are operable at different clock frequencies, the method comprising:"*

In the Petition, Petitioner contends that "Nicol discloses 'a plurality of data processing elements adapted for programmably processing sequences, to which tasks are assigned,'" as recited in the preamble of claim 3, under "Patent Owner's construction as plain meaning." Pet. 21 (citing Ex. 1001 ¶ 153). First, Petitioner contends, Nicol discloses a multiprocessor chip that "contains a plurality of processing elements (PEs) . . . that are data processing elements because they process data." Pet. 21–22 (citing Ex. 1006, 2:50–53, Figs. 2, 4). Second, Petitioner contends, Nicol's plurality of PEs are assigned tasks. *Id.* at 22 (citing Ex. 1001 ¶¶ 162–164). According to Petitioner, Nicol's "multiprocessor chip also includes a controller . . . that is a PE 'that assigns the tasks given to the multiprocessor chip among the PEs.'" *Id.* (citing Ex. 1006, 6:6–13). More particularly, Petitioner contends, "Nicol explains that the 'real-time operating system' in

[11] Because Petitioner's arguments in the first two textual paragraphs of page 32 of the Petition relate to Bhatia (Exhibit 1007), rather than to Nicol (Exhibit 1006), we understand each of Petitioner's citations to Exhibit 1006 in the cited portion of the Petition to refer instead to Exhibit 1007.

the controller PE . . . 'allocates tasks to the other PEs . . . from a mix of many digital signal processing applications,' i.e., the operating system assigns tasks to the different PEs," and "[e]ach PE contains 'a central processing unit (CPU)' that executes programmed instructions and 'a local cache memory' that stores instructions and data, as was well-known to a POSITA." *Id.* (emphasis omitted) (citing Ex. 1006, 2:51–56).

Third, Petitioner contends, "to the extent programmably processing sequences includes *data*," Nicol specifically "discloses its plurality of PEs are adapted for programmably processing sequences" by virtue of its teaching with respect to synchronizing the exchange of data of the PEs through an asynchronous communication network. Pet. 23 (citing Ex. 1006, 6:14–18, 6:26–28, Figure 4; Ex. 1001 ¶¶ 172–177). In support of that contention, Petitioner provides the following annotated version of Nicol's Figure 4.



Annotated Figure 4, above, highlights asynchronous communication network 160 and PEs of Nicol's Figure 4 in blue and green, respectively; calls out two of the highlighted PEs as "First Processor (PE1)" and "Second Processor (PE2)"; and labels certain data flows between network 160 and PE1 and PE2 via level converter 150 in red as "Exchange of Data." *Id.* at 24.

With reference to annotated Figure 4, Petitioner contends that Nicol "depicts the exchange of data (red) from PE1 (green) through the asynchronous communication network (blue) to PE2 (green) for further processing." *Id.* at 23 (citing Ex. 1001 ¶¶ 172–177; Ex. 1006, Fig. 4). Further, Petitioner contends, "[t]he exchange of data among the PEs over the asynchronous communication network of Nicol enables a source PE to pass its results to destination PE(s) to be processed by the destination PE(s), i.e., programmably processing sequences." *Id.* at 24. Indeed, Petitioner argues, such a network would have been unnecessary and Nicol's multiprocessor system would have been of little practical use if one PE could not pass its results to other PEs for further processing. *Id.* at 24–25 (citing Ex. 1001 ¶¶ 178–181).

Citing Dr. Sechen's testimony, Petitioner further contends that digital signal processing ("DSP") applications such as those Nicol's multiprocessor system is intended to handle "typically involve complex operations performed in a pipeline fashion, whereby partial results from one PE are passed to another PE, i.e., programmably process sequences, of the pipeline for further processing." *Id.* at 25–26 (citing Ex. 1001 ¶¶ 184–188; Ex. 1006, 2:55–56). Still further, Petitioner argues that a person of ordinary skill in the art would have known that the PEs in Nicol's system could be configured to

programmably process sequences in a manner similar to well-known "systolic architecture[s]." *Id.* at 26 (citing Ex. 1001 ¶¶ 309–312).

Still further, to the extent "programmably processing sequences" includes instructions, as opposed to data, Petitioner contends, Nicol also discloses its plurality of PEs are adapted therefor. *Id.* at 27 (citing Ex. 1003, 2:53–56, 4:3–5; Ex. 1001 ¶¶ 193–195).

Finally, Petitioner contends, Nicol discloses its PEs are operable at different clock frequencies, quoting disclosure in Nicol that "the frequencies at which the individual PEs operate [can] differ from one another and from other elements within the system." *Id.* at 28 (citing Ex. 1006, 6:14–16, 6:63–66; Ex. 1001 ¶¶ 198–199).

Patent Owner contends in its Response that the combination of Nicol and Bhatia does not disclose "programmably processing sequences." PO Resp. 16–23. Referring specifically to Petitioner's arguments (1) that Nicol's asynchronous communication network "would have been unnecessary" if Nicol's PEs were not configured to pass results of their tasks to other processors (Pet. 24), (2) that "DSP applications typically involve . . . a pipeline" process whereby PEs pass data from one to the next in a sequence (*id.* at 25), and (3) that the PEs in Nicol's multiprocessor system "could be configured . . . similar to . . . [a] systolic architecture" (*id.* at 26), Patent Owner argues that Petitioner presents a "flawed" "three step analysis" that "rests on mere possibilities" that "do not support the contention that a POSITA would assume an [asynchronous communication network ("ACN")] implies programmable processing sequences" (PO Resp. 16 (citing Pet. 25–28; Ex. 2022 ¶ 42)).

First, Patent Owner argues, Petitioner's evidence does not show that a person of ordinary skill in the art would understand an ACN to imply passing of data or instructions between processors, as the supporting evidence relied upon by Dr. Sechen describes a configuration in which a processor and a coprocessor communicate directly within a CPU, in contrast with Nicol's multi-processor system. *Id.* at 16–20 (citing Ex. 1006, 2:51–53; Ex. 1010, Fig. 3.14; Ex. 2022 ¶¶ 43–46). According to Patent Owner, "[b]ecause the microprocessor and co-processor communicate directly and are unlikely to communicate across the bus, a POSITA would not assume that a bus connected to multiple processors (as in Nicol) implies it is used by the processors to share data between them." *Id.* at 20 (citing Ex. 2022 ¶ 46).

Second, Patent Owner argues, Nicol's DSP does not require a pipeline process with PEs passing data in a sequence. PO Resp. 20–21 (citing Ex. 2022 ¶ 47). According to Patent Owner, "there are a multitude of architectures for performing digital signal processing," not all of which are performed using a chain of processors. *Id.* at 20 (citing Ex. 2022 ¶ 47).

Finally, Patent Owner argues, a person of ordinary skill in the art would not understand that Nicol's multiprocessor system "would not and could not be operated as a systolic architecture." PO Resp. 21 (citing Ex. 2022 ¶ 48). According to Patent Owner, Nicol's architecture includes processors connected in parallel, as shown in Nicol's Figure 4, whereas systolic architectures are processors hardwired in series. *Id.* at 21–22 (citing Ex. 2022 ¶ 48). Further, Patent Owner contends, "[t]he fundamental defining aspect of a systolic architecture is that the individual processors share a 'beat' like a heart, and pass data among themselves based on this unified shared global heartbeat," whereas each of Nicol's PEs "has its own

clock frequency (heart beat) and cannot rely upon any other PE having the same heart rate." *Id.* at 22 (citing Ex. 2022 ¶ 48). Accordingly, Patent Owner argues, "if Nicol operated as a systolic architecture, it would not disclose 'programmably processing sequences.'" *Id.* at 23 (citing Ex. 2022 ¶ 48).

In its Reply, Petitioner argues that "[t]he Petition provides three independent reasons for why a POSITA would understand Nicol to disclose, or at least render obvious, 'programmably processing sequences' where this term refers to programmably processing sequences of ***data***." Pet. Reply. 6 (citing Pet. 21–29). According to Petitioner, "[w]hile Patent Owner mischaracterizes these multiple independent grounds as being part of a 'three step analysis,' no such effort is necessary: as explained in the Petition, Nicol discloses that sequences of data can be programmably processed in one PE and then passed to another PE, thus meeting this element." *Id.* at 6–7 (citing PO Resp. 16; Pet. 23–24). With reference to the annotated version of Nicol's Figure 4 from the Petition, Petitioner argues that "Nicol discloses this functionality via its synchronization schema that allows for data to be communicated between PEs over its PE-to-PE communication network, thus allowing PEs to programmably process sequences of data that are passed between PEs." *Id.* at 7 (citing Pet. 23–24; Ex. 1006, 6:18–21, 6:25–33, Fig. 4). Petitioner contends that Patent Owner's argument that Nicol's network does not allow for PE-to-PE communication but only communication between the PEs and the controller "was eviscerated" by the admissions of Patent Owner's expert, Dr. Mangione-Smith, who, Petitioner argues, "agrees that not only does Nicol 'envision[]' such a PE-to-PE arrangement, but it specifically discloses

a structure that does so." *Id.* at 8 (citing Ex. 1049, 107:14–108:1, 110:21–25).

Further, Petitioner points out, the Patent Owner Response "does not dispute that Nicol also discloses programmably processing sequences of ***instructions***, *i.e.*, sequential ***instruction*** processing," which, Petitioner contends, Patent Owner's expert Dr. Mangione-Smith recognized "***certainly*** could" be "sequences" as that term is used in claim 3. Pet. Reply 9 (quoting Ex. 1049, 82:20–83:4). Indeed, Petitioner contends, Dr. Mangione-Smith "further concedes that '[t]he PEs in Nicol could be . . . a standard sort of microprocessor or a core processor ***that executes instructions in sequence to complete tasks***' and 'a person of ordinary skill in the art looking at Nicol would understand that it ***certainly could be that***,' *i.e.*, processing sequences of instructions." *Id.* at 9–10 (quoting Ex. 1049, 87:20–88:10).

In its Sur-reply, Patent Owner responds that the Petition does not provide three independent reasons for this element being disclosed by Nicol, as alleged in Petitioner's Reply, but instead focuses only on the asynchronous communication network of Nicol. PO Sur-reply 6 & n.2 (citing Pet. 21–22; Pet. Reply 6). With respect to Nicol's network, Patent Owner contends, the statements relied upon by Petitioner "show no more than an ability to communicate between PEs, and fall short of Petitioner's claim that Nicol shows that data output from one PE is passed to another PE." *Id.* at 7 (citing Ex. 1006, 6:18–21, 6:27–28).

Having fully considered the parties' respective arguments and cited evidence, we are persuaded by Petitioner's contentions that Nicol teaches or suggests "a plurality of data processing elements adapted for programmably processing elements, to which tasks are assigned," as recited in the preamble

of claim 3.[12] Notwithstanding Patent Owner's contention in its Sur-reply that Nicol's statements "fall short of Petitioner's claim that Nicol shows that data output from one PE is passed to another PE" (Sur-reply 7), we do not understand claim 3 to require that data output from one PE be passed to another PE. As noted above, Patent Owner argued in related district court litigation *against* a construction of the claim phrase "data processing elements adapted for programmably processing sequences" that would have required "the data results from processor [to be] fed to another, for each processor to perform a separate computation," advocating instead that the term has its plain and ordinary meaning and needs no explicit construction. *See* Ex. 1012, 14. We further understand that the district court agreed with Patent Owner and that both parties now agree that the plain and ordinary meaning should apply in this proceeding and that no explicit construction is necessary. PO Resp. 5–6. In this regard, we agree with Petitioner that it is sufficient that Nicol discloses, for example, that the "real-time operating system" in the controller of Figure 4 "allocates tasks to the other PEs" and that "a synchronization schema must be implemented" for "synchronizing the exchange of data among the PEs of a multiprocessor chip." *See* Pet. 27–28 (citing Ex. 1006, 2:53–56, 4:3–5; Ex. 1001 ¶¶ 193–195); *see also id.* at 22–23 (citing Ex. 1006, 2:51–56, 6:14–18, 6:26–28, Fig. 4; Ex. 1001 ¶¶ 162–164).

[12] The parties did not address whether the preamble of claim 3 is limiting in their briefing, and when asked during oral argument, counsel for Petitioner represented that the parties had contested the construction of the "programmably processing sequences" recitation in the district court and appear to have conceded that it is limiting. Tr. 57:26–58:11.

We also are persuaded by Petitioner's contentions that Nicol teaches that the PEs "are operable at different clock frequencies," as further recited in the preamble of claim 3. *See* Pet. 28 (citing Ex. 1006, 6:14–16, 6:63–66; Ex. 1001 ¶¶ 198–199). Patent Owner does not dispute Petitioner's contentions with respect to this recitation, and Petitioner's assertions are supported by the cited evidence.

Accordingly, we are persuaded by a preponderance of the evidence that the preamble of claim 3 is taught or suggested by the asserted prior art.

b) "grouping, by execution of software for managing distribution of code, a plurality of subsets of processing elements into processing element groups;"

Pointing to the disclosure in Nicol that "the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own power supply," Petitioner contends that Nicol discloses that its PEs may be grouped into different processing element groups. Pet. 29 (quoting Ex. 1006, 6:66–7:3). Petitioner further contends that Nicol's controller, through its "real-time operating system" (i.e., software for managing distribution of code), "allocates tasks to the other PEs . . . from a mix of many digital signal processing applications," and thereby assigns tasks to groups of PEs (i.e., a "plurality of subsets of processing elements," in the parlance of claim 3) for processing applications. *Id.* at 29–30 (quoting Ex. 1006, 2:53–56, 6:40–41, Fig. 2; Ex. 1001 ¶¶ 202–206).

Patent Owner contends in its Response that Nicol does not disclose the recited "grouping" limitation. PO Resp. 11–15. According to Patent Owner, "Petitioner emphasizes Nicol's grouping of PEs, while ignoring the nature of the groups described." *Id.* at 12. More particularly, Patent Owner contends that "Nicol groups PEs '**to operate from [the group's] own**

controlled supply voltage,'" but "does not group PEs 'by execution of Software for managing distribution of code . . . into processing element groups.'" *Id.* (bracketing in original) (citing Ex. 1006, 6:66–7:3; Ex. 2022 ¶ 37). Citing the testimony of Dr. Mangione-Smith, Patent Owner alleges that a person of ordinary skill in the art would understand Nicol's "intention for grouping processing elements to be sharing a common voltage." *Id.* (citing Ex. 2022 ¶ 37).

Further, Patent Owner argues, "the grouping of PEs is described as a 'middle ground' between 'PEs in a multi-processor chip [being] subjected to a single controlled supply voltage' and 'each of the PEs in a multi-processor chip [being] subjected to its own, individually controlled, supply voltage.'" PO Resp. 12–13 (bracketing in original) (citing Ex. 1006, 6:62–65, 6:67; Ex. 2022 ¶ 37). According to Patent Owner, "[m]erely providing a common power supply does not suggest that Nicol's PEs are grouped, by execution of software for managing distribution of code, into processing element groups." *Id.* at 13 (citing Ex. 2022 ¶ 37). Pointing to Figures 2 and 4 of Nicol, Patent Owner further contends that the power supplies illustrated in the former "are hardwired to the individual processors – not grouped by execution of software," whereas those in the latter "each have their own power supply, and so cannot be described as grouped in the manner described in Nicol." *Id.*

Patent Owner further contends that Petitioner misrepresents Nicol by suggesting that Nicol discloses an operating system that assigns tasks to groups of PEs. PO Resp. 14 (citing Ex. 1022 ¶ 38). According to Patent Owner, Nicol's description of an operating system on a first PE "allocat[ing] tasks to the other PEs" is not a grouping of processors by execution of

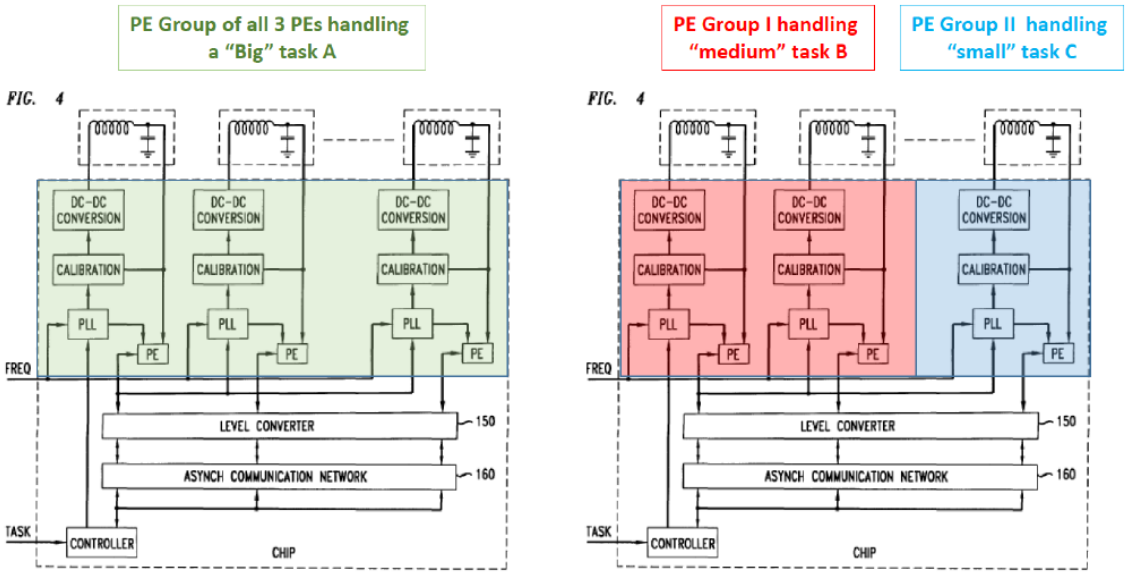
software for managing distribution of code, but merely describes the fact that a processor is necessary to allocate tasks. *Id.* (citing Ex. 1006, 2:53–56; Ex. 2022 ¶ 38).

Further, Patent Owner argues, "Nicol is explicit in how tasks are allocated: 'divide the collection of tasks as evenly as possible (in terms of needed processing time).'" PO Resp. 14–15 (quoting Ex. 1006, 3:66–4:1) (citing Ex. 2022 ¶ 39). According to Patent Owner, "[g]rouping processors during operation under software control is inconsistent with attempting to evenly distribute tasks among all available processors" and "would cause certain tasks to be distributed among members of a processing element group and exclude those processors not within the group, thereby preventing the distribution of tasks amongst all processors as required in Nicol." *Id.* at 15 (citing Ex. 2022 ¶ 39)

Finally, Patent Owner contends that Petitioner's interpretation of Nicol is inconsistent with Nicol's purpose of reducing power consumption on a chip because grouping would result in higher processing load—and consequently a higher operating frequency and higher power consumption—for individual processors. PO Resp. 15 (citing Ex. 2022 ¶ 40).

In its Reply, Petitioner responds that Patent Owner focuses on Nicol's hardware-based grouping while ignoring that the Petition relies on Nicol's further disclosure that "applications that need to be processed are . . . under [the] control of real time operating system (RTOS)" that is executed on the controller PE and "allocates tasks to the other PEs." Pet. Reply 1–2 (quoting Ex. 1006, 3:11–13, 2:53–56) (citing Pet. 29–30). As detailed in the Petition, Petitioner contends, "Nicol's Figure 4 illustrates a system in which the controller PE has the flexibility to program the supply voltage and frequency

of each individual PE." *Id.* at 3 (citing Pet. 29–30; Ex. 1006, 5:66–6:2). According to Petitioner, although the controller PE can divide up a large task among all available PEs and program the same supply voltage and frequency to all PEs, in which case the PEs would operate in unison as in Nicol's Figure 2 (hardwired) embodiment, the controller PE can also group the PEs into different groups tailored to the tasks in its "to-do" list. *Id.* at 3–4 (citing Ex. 1006, 5:24–27; Ex. 1050 ¶¶ 8–9). In that manner, the controller PE can assign a first task to a first group of PEs programmed to operate at one supply voltage and frequency and assign a second task to one or more other PEs programmed to operate at a different supply voltage and frequency setting. *Id.* at 4 (citing Ex. 1006, 5:60–64; Ex. 1050 ¶ 10). Petitioner provides the following annotated versions of Nicol's Figure 4 to illustrate the two scenarios described:



The annotated figures above illustrate Petitioner's exemplary grouping of the three PEs and connected components of Nicol's Figure 4 in a single group, highlighted in green (left figure), and Petitioner's exemplary grouping of the

same PEs and components into two groups, highlighted in red and blue, respectively (right figure). *Id.* at 3.

Further, Petitioner contends, "[t]he same PE groupings under RTOS software control also apply to the 'middle ground' architecture of Nicol discussed in the Petition." Pet. Reply 5 (citing Ex. 1006, 6:66–7:3; Pet. 29). In that architecture, "the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage." Ex. 1006, 6:66–7:3. Petitioner argues, "in this middle ground architecture, PEs are hardwired into clusters of PEs . . . , with all the PEs of each cluster sharing the same DC-DC converter and PLL. Pet. Reply 5 (citing Ex. 1050 ¶¶ 12–13). According to Petitioner, although the controller RTOS in this architecture "cannot program each PE's voltage and frequency individually and must program them by PE cluster," the RTOS can "[n]evertheless . . . assign 'heavy' tasks to one cluster of PEs . . . —or to a select few PE clusters—and 'lighter' tasks to another cluster of PEs . . . , thereby grouping those PEs clusters into PE groups by execution of software for managing the distribution of code." *Id.* (citing Ex. 1006, 5:60–61, 3:39–41; Ex. 1049, 72:13–16; Ex. 1050, ¶13).

In its Sur-reply, Patent Owner argues that the groupings referenced in Petitioner's Reply are not illustrated either in the Petition or in Nicol itself. PO Sur-reply 3–4. According to Patent Owner, "Petitioner alleges that the shadings represent groups that the real-time operating system (RTOS) in Nicol is 'capable of' creating, but these groups are not described in Nicol," and "[b]ecause none of this is disclosed by Nicol, Petitioner relies on permissive language ('can', 'capable of') when describing these creations." *Id.* at 3–4, 4 n.1. According to Patent Owner, "Nicol does not describe the

groupings illustrated by Petitioner in any embodiment." *Id.* at 4. In particular, Patent Owner contends:

> In the Figure 2 embodiment, there is only one clock frequency to determine because a single voltage supply powers all the PEs. Even if the collection of all PEs were deemed a group, the grouping is not determined by software (the system is hard-wired) and not during execution, as this grouping cannot change during operation. There isn't a mechanism to form subsets of PEs, as all the PEs operate at the same voltage and frequency. In the Figure 4 embodiment, the "divide the collection of tasks" language does not apply, as Nicol states the controller "does not divide tasks among PEs." Ex. 1006 (Nicol) at 6:5–6. Instead, each PE handles its own tasks, because the "operating system … independently program[s] the lowest operating frequency … for each PE." *Id.* at 5:67–6:2. The shaded "groupings" are simply a creation of Petitioner's that Nicol never envisioned. This is not enough to show obviousness.
>
> . . . . Lastly, Petitioner constructs a hypothetical according to the '301 claim language but attempts to justify it by tying it to Nicol's "middle ground" embodiment. This is a new interpretation not found in the original Petition. Petitioner acknowledges the disclosure in Nicol regarding the middle ground that was cited in the original Petition describes hardware[.] *See* Reply at 5 ("PEs are hardwired into clusters of PEs . . . ").

Id. at 4–5; *see also id.* at 22–23 (arguing that Petitioner's "new arguments on Reply for this limitation should be disregarded").

Having reviewed the parties' respective arguments and cited evidence, we are persuaded that the recited "grouping" limitation would have been obvious in view of Nicol. As cited in the Petition, Nicol expressly discloses that "the PEs of the multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage." Ex. 1006, 6:66–7:3 (cited at Pet. 29). Although the second clause

of the quoted sentence (i.e., "each group of PEs can be arranged to operate from its own controlled supply voltage") suggests that the disclosed groups *can* be implemented via hardware, we do not find in that permissive language any teaching away from the groups instead being implemented by Nicol's real-time operating system (i.e., "by execution of software," in the parlance of claim 3), as proposed by Petitioner. *See* Pet. 29–30; Ex. 1006, 2:53–56, 6:40–41, Fig. 4.

Further, while we recognize that Nicol does not provide an express recitation of an embodiment in which the PEs of Figure 4 are grouped by execution of Nicol's real-time operating system, we find Dr. Sechen's testimony (*see, e.g.*, Ex. 1001 ¶¶ 21, 110, 200–206; Ex. 1050 ¶¶ 6–13, 32) credible and persuasive with respect the teachings of the prior art and the level of skill in the art, and we are persuaded that resolving these details would have been well within the skill of a person of ordinary skill in the art, who has ordinary creativity and is not an automaton. *See KSR*, 550 U.S. at 421. Notably, although Patent Owner disputes that this limitation would have been obvious over Nicol, Patent Owner's expert Dr. Mangione-Smith's testimony does not directly contradict Dr. Sechen's testimony in relevant regard. *See, e.g.*, Ex. 1049, 168:17–169:12 (Dr. Mangione-Smith testifying, with respect to whether grouping PEs in Nicol's "middle-ground" embodiment is "something that a person of ordinary skill could do," that "that complicates the scheduler to a significant extent. So I feel uncomfortable . . . saying doing that would have been obvious. But it's certainly possible.").

c) "effecting a plurality of temperature measurements in different regions of the system;"

Petitioner contends that Bhatia discloses one or more temperature sensor units for monitoring system temperature in one or more corresponding thermal zones, while "Nicol also discloses the use of thermal sensor(s) to track temperature in a multiprocessor chip." Pet. 30–31 (citing Ex. 1006, 1:41–48, 4:11–13; Ex. 1007, 3:28–29). Petitioner further contends that a person of ordinary skill in the art "would have understood that Bhatia's approach of partitioning a system or chip into multiple thermal zones, each monitored by its own thermal sensor, is beneficial to Nicol's multiprocessor chip because the different PEs of the chip can have different workloads and thus different temperature profiles." *Id.* (citing Ex. 1006, 5:42–44). In particular, citing the testimony of Dr. Sechen, Petitioner contends that "[h]aving multiple thermal sensors tracking the temperatures of different thermal zones of a multiprocessor chip would [] improve the accuracy of Nicol's power management system" and that "[i]mplementing this added functionality would not require undue experimentation, has a reasonable expectation of success, and would yield predictable results because the added functionality is primarily add-on software to Nicol's existing controller software." *Id.* at 20, 31 (citing Ex. 1006, 3:9–20, 4:11–13; Ex. 1001 ¶¶ 138–152, 207–214). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of Nicol's and Bhatia's respective teachings with respect to this limitation. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Moreover, for the reasons stated in Section II.C.3 above, we are persuaded that a person of ordinary skill in the art would have been

motivated to combine the teachings of Nicol and Bhatia as proposed by Petitioner. Accordingly, we are persuaded that this limitation is taught by the asserted prior art.

> *d) "based on the temperature measurement, a control circuit modifying clock rates of the plurality of subsets of processing elements, wherein the clock rates set in the modifying step are set on a processing element group basis."*

Petitioner asserts "Nicol in combination with Bhatia discloses a system where based on the temperature measurement, a control circuit modifying clock rates of the plurality of subsets of processing elements, wherein the clock rates set in the modifying step are set on a processing element group basis." Pet. 32 (citing Ex. 1001 ¶ 215). In particular, Petitioner contends "Bhatia discloses modifying clock rates based on temperature management," while "Nicol discloses modifying . . . clock rates based on an element group basis." *Id.* at 32–33 (citing Ex. 1007, 2:24–28, 4:34–37, 12:5–10; Ex. 1006, 6:6–13, 6:66–7:3). Petitioner asserts that "based on Bhatia's modifying clock rates in response to a temperature measurement, Nicol's controller would modify the clock rates for each of the PEs in a particular group and would then set the clock frequency on a group basis." *Id.* at 33 (citing Ex. 1001 ¶¶ 216–221; Ex. 1006, 3:11–13, 5:23–28, 6:66–7:3). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of Nicol's and Bhatia's respective teachings with respect to this limitation. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Moreover, for the reasons stated in Section II.C.3 above, we are persuaded that a person of ordinary skill in the art would have been motivated to combine the teachings of Nicol and Bhatia as proposed by

Petitioner. Accordingly, we are persuaded that this limitation is taught by the asserted prior art.

e) Conclusion Regarding Claim 3

Based on Petitioner's persuasive arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 3 would have been obvious over Nicol and Bhatia.

5. Independent Claim 6

a) "A processor device, comprising:"

Petitioner contends that Nicol discloses a multiprocessor system integrated on a chip and, thus, discloses "a processor device." Pet. 34 (citing Ex. 1006, 2:44; Ex. 1001 ¶¶ 222–225). Petitioner's contention is supported by the cited evidence and is not challenged by Patent Owner (*see generally* PO Resp.). We are persuaded that this limitation is taught by the asserted prior art.

b) "a plurality of data processing elements adapted for programmably processing sequences and to which tasks are assigned,"

Petitioner contends that Nicol discloses this limitation for the reasons stated with respect to the identical recitation in the preamble of claim 3. Pet. 34 (citing Pet. 21–28; Ex. 1001 ¶ 227). Patent Owner does not specifically address Petitioner's contention with respect to this limitation but asserts that "Petitioner has failed to show that Nicol in view of Bhatia renders claim 6 obvious for at least the same reasons Petitioner has failed to show that Nicol in view of Bhatia renders claim 3 obvious." PO Resp. 29. For the reasons stated in Section II.C.4 above, we conclude that Petitioner's contentions with respect to claim 3 are supported by the cited evidence and

are persuasive. For the same reasons, we conclude that Petitioner has met its burden to show by a preponderance of the evidence that the present limitation is taught by the asserted prior art.

c) "each of the data processing elements having at least one Arithmetic Logic Unit,"

Petitioner contends that Nicol renders this limitation obvious. Pet. 34 (citing Ex. 1001 ¶ 228). Specifically, pointing to the disclosure in Nicol of multi-processor chips containing PEs "each . . . contain[ing] a central processing unit (CPU) and a local cache memory," Petitioner contends that a person of ordinary skill in the art would have understood that a CE having a CPU and cache includes arithmetic logic units ("ALUs") and registers. Pet. 34–35 (quoting Ex. 1003, 2:50–53) (citing Ex. 1001 ¶¶ 229–234). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of the prior art's teaching with respect to this limitation. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Accordingly, we are persuaded that this limitation is taught by the asserted prior art.

d) "and at least some of the data processing elements being adapted to operate at different clock frequencies that are adapted locally depending on a plurality of temperature measurements at different regions of the processor device;"

Petitioner contends that this claim limitation is disclosed by the combination of Nicol and Bhatia, based on Bhatia's teaching of locally adapting clock frequency depending on a plurality of temperature measurements at different regions of a processor device, in combination with Nicol's disclosure contemplating that "the frequencies at which the individual PEs operate [can] differ from one another and from other

elements within the system." Pet. 35–36 (emphasis omitted) (quoting Ex. 1006,[13] 6:14–16) (citing Ex. 1007, Abstract, 3:54–65; Ex. 1001 ¶¶ 136–152, 235). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of Nicol's and Bhatia's respective teachings with respect to this limitation. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Moreover, for the reasons stated in Section II.C.3 above, we are persuaded that a person of ordinary skill in the art would have been motivated to combine the teachings of Nicol and Bhatia as proposed by Petitioner. Accordingly, we are persuaded that this limitation is taught by the asserted prior art.

e) "wherein a plurality of subsets of the data processing elements are grouped, by execution of software for managing distribution of code, into processing element groups,"

Petitioner contends that Nicol discloses this limitation for the reasons stated with respect to the corresponding limitation in claim 3. Pet. 36 (citing Pet. 29–30; Ex. 1001 ¶ 242). Patent Owner likewise relies for this limitation on its arguments with respect to claim 3, asserting that "[s]imilar to claim 3, claim 6 requires 'processing elements . . . grouped, by execution of software for managing distribution of code, into processing elements,'" and that, "[a]ccordingly, Petitioner has failed to show that Nicol in view of Bhatia renders claim 6 obvious for at least the same reasons Petitioner has failed to show that Nicol in view of Bhatia renders claim 3 obvious." PO Resp. 29. For the reasons stated in Section II.C.4 above, we conclude that Petitioner's

[13] Based on the reference to Bhatia and the specific quoted language, we understand Petitioner's citation of "Ex. 1003, at 6:14–16" at page 36 of the Petition to refer instead to Ex. 1006, 6:14–16.

contentions with respect to claim 3 are supported by the cited evidence and are persuasive. For the same reasons, we conclude that Petitioner has met its burden to show by a preponderance of the evidence that the present limitation is taught by the asserted prior art.

> *f) "and the clock frequencies set for the data processing elements responsive to the temperature measurements are set on a processing element group basis, so that, for each of the groups, the clock frequency of the data processing elements of the group are modified in a same manner."*

Petitioner contends that this claim limitation is disclosed by the combination of Nicol and Bhatia. Pet. 37 (citing Ex. 1001 ¶ 244). First, according to Petitioner, Bhatia discloses setting a clock frequency in response to a temperature measurement, citing, for example, disclosure that Bhatia's "thermal management controller varies the component between different performance states . . . when an over-temperature condition is detected." *Id.* (emphasis omitted) (quoting Ex. 1007, Abstract). Relying on the testimony of Dr. Sechen, Petitioner further contends that a person of ordinary skill in the art would have understood that "Bhatia's approach of partitioning a system or chip into multiple thermal zones, each monitored by its own thermal sensor, is beneficial to Nicol's multiprocessor chip because the different PEs of the chip can have different workloads and thus different temperature profiles and more effective[ly] be grouped together and monitored." *Id.* (citing Ex. 1001 ¶¶ 244–246; Ex. 1006, 5:42–44). Further, Petitioner argues, "while Bhatia discloses adding temperature sensors to different regions/groups of a system and adjusting a clock frequency based on those sensors, Nicol discloses grouping PEs into different processing elements groups" and "that the clock frequency of the PEs of the group would be modified in the same manner." *Id.* (citing Ex. 1006, 6:66–7:3;

Ex. 1001 ¶¶ 246–248). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of Nicol's and Bhatia's respective teachings with respect to this limitation. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Moreover, for the reasons stated in Section II.C.3 above, we are persuaded that a person of ordinary skill in the art would have been motivated to combine the teachings of Nicol and Bhatia as proposed by Petitioner. Accordingly, we are persuaded that this limitation is taught by the asserted prior art.

g) Conclusion Regarding Claim 6

Based on Petitioner's persuasive arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 6 would have been obvious over Nicol and Bhatia.

6. Dependent Claim 7

Claim 7 depends from claim 6 and further recites "wherein the processing device is an integrated circuit." Ex. 1003, 15:57–58.

Petitioner has shown by a preponderance of the evidence that this limitation would have been obvious in light of the Nicol-Bhatia combination. *See* Pet. 38–39 (citing Ex. 1006, 6:5–8, 7:17–23, claim 5; Ex. 1001 ¶¶ 252–254). Beyond the arguments addressed above with respect to independent claims 3 and 6, Patent Owner does not contest Petitioner's assertions with respect to claim 7. PO Resp. 29.

Based on Petitioner's persuasive arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that

the subject matter of dependent claim 7 would have been obvious over Nicol and Bhatia.

7. Independent Claim 8

Petitioner contends that Nicol teaches all limitations of independent claim 8, with the exception of the processor device being "adapted for reducing clock frequencies of the data processing elements in response to a determination that a power reserve of a battery is below a predetermined threshold," for which limitation Petitioner additionally relies on Bhatia. Pet. 39–44. With respect to that final limitation, Petitioner contends, first, that Nicol discloses power minimization of a multiprocessor DSP chip, including "by dynamically controlling the processing load of chips and controlling . . . the operating voltages of those chips so as to minimize overall power consumption." *Id.* at 42 (quoting Ex. 1006, 2:18–21) (citing Ex. 1001 ¶¶ 274–275). Further, Petitioner contends, "[w]hile Nicol discloses techniques for power conservations in personal computers," Bhatia explicitly discloses that "[d]ifferent events may be used to trigger performance state transitions" and that "environmental changes in the computer system may trigger a performance state change." *Id.* (quoting Ex. 1007, 12:5–7). Petitioner additionally points out that Bhatia discloses that a change in performance state may be necessary when a laptop computer is undocked, or its power source changes from AC power to battery. *Id.* at 42–43 (citing Ex. 1001 ¶¶ 276–280; Ex. 1007, 4:64–67, 12:14–19, 12:33–36).

Relying on the testimony of Dr. Sechen, Petitioner further contends that, in addition to the previously asserted reasons to combine Bhatia's teachings with those of Nicol, a person of ordinary skill in the art "would

have been further motivated to combine Bhatia and Nicol given Bhatia's teachings of tracking a change in power, with Nicol's disclosure of laptop computers and the different types of events that may trigger a performance state transition." *Id.* at 43–44 (citing Ex. 1001 ¶¶ 284–287). Petitioner thus contends that the combination of Nicol and Bhatia "combines prior art elements according to known methods that would yield predictable results, i.e., tracking a battery level and triggering a performance state transition upon a certain threshold" and "merely applies known techniques—as evidenced by . . . disclosure . . . in Ex. 10[1]6 at 5:11–18 ('detection of a low battery condition')—of monitoring a battery level and employing a triggering event when the battery reaches a certain level, all of which, was well known in the art." *Id.* at 44 (quoting Ex. 1016, 5:11–18[14]) (citing Ex. 1001 ¶¶ 284–287). Thus, Petitioner argues, "based on the teachings of Bhatia, and common knowledge to a POSITA at the time, it would have been obvious to, in addition to tracking the state of the power source, to track the state of a laptop battery, and ultimately lower a clock frequency upon determining a battery level is below a predetermined threshold." *Id.* (citing Ex. 1001 ¶¶ 284–287).

In response to Petitioner's contentions, Patent Owner argues that neither Nicol nor Bhatia discloses "reducing clock frequencies of the data processing elements in response to a determination that a power reserve of a battery is below a predetermined threshold" and that "a POSITA would not

[14] Based on the quoted phrase and citations at pages 42 and 43 of the Petition, we understand Petitioner's citations to "Ex. 1006" at page 44 of the Petition to refer to Cline et al., US 6,704,877 B2 ("Cline," Ex. 1016) rather than to Nicol (Ex. 1006).

understand the references to teach the feature." PO Resp. 23. More particular, according to Patent Owner,

> Nicol discusses reduction of power consumption through the division of tasks in a multi-processor system between all processors such that each of the processors may be run at a lower frequency, which requires a lower voltage. Ex. 1006, 2:22–31; 2:65–3:20; Ex. 2022, ¶52. Nicol does not disclose any other methods for reducing power consumption that is not directly related to the distribution of tasks between processors. *See, e.g[.]*, *id.* at 53–65; Ex. 2022, ¶52. Bhatia, on the other hand, relates to a system that reduces clock frequency of a processor when a thermal zone of a computer system exceeds a temperature threshold. Ex. 1007, 2:36–3:46; Ex. 2022, ¶52. This adaptation is done to ensure that a processor does not overheat while also allowing it to run at a high, efficient frequency. *Id.* at 1:6–30; 1:47–49; Ex. 2022, ¶52. Despite the distinct and complex nature of the inventions disclosed in Nicol and Bhatia and despite the fact that neither reference so much as mentions a power reserve of a battery, Petitioner nonetheless appears to suggest that a POSITA would combine these reference and read them to imply that a clock frequency of a plurality of processors could be predicated on a power reserve of a battery, and specifically checking if it is below a predetermined threshold. Pet., 43–44; Ex. 2022, ¶52. No POSITA would make such a drastic jump to this conclusion. Ex. 2022, ¶52.

Id. at 24.

We agree with Patent Owner. We find no teaching or suggestion in either Nicol or Bhatia of determining the power reserve of a battery, let alone reducing clock frequencies in response to a determination that the power reserve is below a predetermined threshold. We also agree with Patent Owner that Petitioner's reliance on disclosure of "detection of a low battery condition" in Cline is unavailing. PO Resp. 25–26; *see* Pet. 43–44 (quoting Ex. 1016, 5:11–18); *see also supra* note 14. As Patent Owner

points out, Petitioner did not include Cline in the asserted grounds of unpatentability set forth in the Petition and has not persuasively shown either that a person of ordinary skill in the art would have been motivated to combine Cline with Nicol and Bhatia or that Cline would have informed such a person's understanding of the asserted references. *Cf. Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015) (explaining that references outside of an asserted combination "can legitimately serve to document the knowledge that skill artisans would bring to bear in reading the prior art identified as producing obviousness"). Even if we were to consider Cline as providing such knowledge as contemplated by *Ariosa*, moreover, we further agree with Patent Owner that Petitioner does not persuasively explain how that knowledge would have led a person of ordinary skill to reduce clock frequency according to a lower battery state. PO Resp. 26. Although Petitioner quotes Cline as disclosing "detection of a low battery condition" (Ex. 1016, 5:11–18), Petitioner does not identify in Cline any contemplation of modification of clock frequency due to such low battery condition. Nor does Petitioner provide any persuasive evidence that a person of ordinary skill in the art would have analogized a low battery condition to an overtemperature condition, for example, so as to suggest implementing Bhatia's frequency throttling in response to the power reserve being below a predetermined threshold.

In its Reply, Petitioner contends that "the Board need not find a 'motivation to combine' in order to consider Cline as corroborative evidence of Petitioner's showing of the state of the art." Pet. Reply 15 (citing *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019)). Petitioner's argument is not persuasive. In *Realtime Data*, the court

concluded that the Board was not required to make any finding regarding a motivation to combine where a non-asserted prior art reference was used to inform the meaning of a term in the asserted prior art. In the present proceeding, in contrast, despite Petitioner's contention that Cline is used "sole[ly] . . . as describing the state of the art," we find that Cline is relied upon for its teaching of a claim element not taught by either of the asserted references.

Petitioner also contends, for the first time in its Reply, that Bhatia itself "discloses reducing a clock frequency in response to the power reserve of a battery falling below a threshold level," based on disclosure in Bhatia of a "power management module" that "determines [] if a ***performance state change is required in response*** to a received event, indicating a thermal event, ***power supply transition***, docking/undocking, a user command, ***or other event*** has occurred," where the "described 'performance state' transitions 'includ[e] adjusting the processor's core clock frequency and voltage level." Pet. Reply 10–11 (alterations in original) (quoting Ex. 1007, 12:32–36, 11:47–49) (citing Ex. 1007, 4:64–67, 12:67–13:4, Fig. 8).

Despite Petitioner's contentions, we do not find any teaching or suggestion of "a battery [being] below a predetermined threshold" among Bhatia's disclosed list of "received event[s]," i.e., "a thermal event, power supply transition, docking/undocking, a user command, or other event." We agree with Patent Owner, for example, that a "power supply transition . . . is different than moving below a battery threshold." PO Sur-reply 8–9. Indeed, it appears that Bhatia's only references to a "battery" are in its statement that "[t]he main power supply voltages in the system 10 are provided by a power supply circuit 56 that is coupled to a battery 60 and an

external power source outlet 58" and its inclusion of battery 60 in its illustration of the referenced elements in Figure 1. Ex. 1007, 4:64–67, Fig. 1. We find nothing in those references to suggest that Bhatia is concerned with battery 60's power reserve level or otherwise to link battery level with a "power supply transition" or any other "received event" identified by Bhatia. Accordingly, we are not persuaded that the cited disclosures teach or suggest performance state changes in response to "a determination that a power reserve of a battery is below a predetermined threshold," as recited in claim 8.

Petitioner also argues in the Reply that Patent Owner's expert "confirm[ed] that a POSITA would have understood this limitation to be obvious in view of Bhatia's teachings, including the disclosures it incorporates from the well-known [Advanced Configuration and Power Interface ('ACPI')] specification." Pet. Reply 11–12. In particular, Petitioner contends that Dr. Mangione-Smith admitted at his deposition that "at the time of Bhatia, . . . the ACPI specification was already pretty well known by people of ordinary skill and [already] in use" and that the ACPI specification indicates that "the low-level operating system or the user-level operating system [] can monitor the battery capacity.'" *Id.* at 12 (quoting Ex. 1049, 143:19–24, 149:16–23). Petitioner further contends that the Board found that "Bhatia incorporates these known techniques from the ACPI Specification" and that "the '301 patent itself even confirms that battery reserve monitoring was well known: the 'power reserve . . . may be determined based on the existing methods according to the related art[.]'" *Id.* at 12 n.5 (citing Inst. Dec. 24–27), 13 n.6 (quoting Ex. 1003, 7:48–53).

In its Sur-reply, Patent Owner argues that Bhatia's citations to the ACPI specification to low activity states and interrupts, rather than to the battery power management portions of ACPI that Petitioner relies on. PO Sur-reply 9 (citing Ex. 1007, 12:58–67, 13:29–38). According to Patent Owner,

> The various disclosures on battery power management (bullet point in the section 3 Overview and section 3.8 on Battery management) are in a separate section of the ACPI because the battery is a separate part of the system, and is not managed the same way as a processor. A POSITA would not look to the battery power management sections of the ACPI simply because Bhatia references processor power management states of the ACPI. Furthermore, the ACPI specification requires the use of a Smart Battery or an interface called CMBatt in order for a battery to be ACPI-compatible and take advantage of the described states. Ex. 1014 (ACPI) at 3-26. There is no indication in Nicol or Bhatia that such a type of battery was contemplated, as Nicol does not even mention a battery, and Bhatia simply lists a generic battery.
>
> In addition, Petitioner cites yet another section of ACPI, page 3-22 in section 3.4, relating to device power management. This part of ACPI is not cited by Bhatia as it is yet a third section separate from both the processor power management and the battery power management.
>
> Recall that the ground here is Nicol in view of Bhatia, and Petitioner relied on Bhatia's overtemperature functionality as the reason a POSITA would allegedly combine Nicol with Bhatia. This provides no basis that a POSITA would look to Bhatia for battery power management, and then further look to ACPI for additional battery power management disclosure. ACPI itself describes "Performance," "Power consumption and battery life," and "Thermal requirements" as three separate, sometimes paradoxical goals, and it is far from clear all power management systems should include all three. *Id.* at 8-145.

PO Sur-reply 9–10. Still further, in response to Petitioner's argument that the '301 patent admits that monitoring of battery reserve was known, Patent

Owner contends that does not mean that it was obvious to use such monitoring as part of determining clock frequency. *Id.* at 10 (citing Pet. Reply 13 n.6).

We agree with Patent Owner that Petitioner's reply arguments regarding ACPI and alleged admissions in the '301 patent are unavailing. Regardless of whether the ACPI specification was well known at the time of Bhatia, we agree with Patent Owner that Petitioner's arguments with respect to the battery power management and device power management sections of that specification proceed in a new direction of unpatentability than was presented in the Petition and accordingly are untimely. *See* PO Sur-reply 20–21; *see also* Patent Trial and Appeal Board Consolidated Trial Practice Guide 73–75 (Nov. 2019), https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf ("CTPG") ("Generally, a reply or sur-reply may only respond to arguments raised in the preceding brief. . . . 'Respond,' in the context of 37 C.F.R. § 42.23(b), does not mean proceed in a new direction with a new approach as compared to the positions taken in a prior filing. . . . [A] reply . . . . that raises a new issue or belatedly presents evidence may not be considered."). In the Petition, Petitioner cited the ACPI specification only in support of its contention that Bhatia discusses power and thermal management, which in turn is the only context in which Bhatia itself mentions ACPI. *See* Pet. 15–16, 20–21; Ex. 1007, 1:13–46, 3:16–24, 4:8–24, 7:57–65, 11:11–37, 12:44–64, 13:29–40.

Even if Petitioner's belated arguments were properly considered, they are unpersuasive. Contrary to Petitioner's suggestion (*see* Pet. Reply 13 n.6), we did not find in the Institution Decision, and do not now find, that Bhatia incorporates the entirety of the ACPI specification by its reference to

processor power management states disclosed therein. We find no suggestion in the asserted prior art that would have led a person of ordinary skill in the art to look to the ACPI specification for battery power management disclosure when combining the teachings of Nicol and Bhatia.

Accordingly, we conclude that Petitioner has not met its burden to demonstrate that claim 8 is unpatentable over the combination of Nicol and Bhatia.

8. Dependent Claims 9, 13–19, 25, 26, 30, 32, 35, and 36

Claims 9, 13–19, 25, 26, 30, 32, 35, and 36 each depend directly or indirectly from claim 8.[15] For the reasons stated in Section II.C.7 above with respect to claim 8, we conclude that Petitioner has not met its burden to demonstrate that claims 9, 13–19, 25, 26, 30, 32, 35, and 36 are unpatentable over the combination of Nicol and Bhatia.[16]

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[15] We note that claims 13, 14, 16, 17 are written in multiple dependent format, as provided for in pre-AIA 35 U.S.C. § 112 ¶ 3 ("A claim may be written . . . , if the nature of the case admits, in . . . multiple dependent form."). In particular, claims 13 and 14 each depend from "any one of claims 8, 10, and 11," and claims 16 and 17 each depend from "any one of claims 8, 10, 11, 12, and 15." Ex. 1003, 16:46–47, 16:52–53, 16:64–65, 17:1–2. For purposes of our analysis with respect to the asserted ground based on Nicol and Bhatia, we evaluate claims 13, 14, 16, and 17 (as well as claim 30, which depends from claim 13) as including all limitations of claim 8. *See* pre-AIA 35 U.S.C. § 112 ¶ 5 ("A multiple dependent claim shall be construed to incorporate by reference all the limitations of the particular claim in relation to which it is being considered.").

[16] Petitioner contends in a footnote in the Petition that "Petitioner need only prove the invalidity of one claim combination to invalidate claim 14." Pet. 46 n.5; *see also id.* at 49 n.6, 50 n.7 (similar arguments with respect to claims 16 and 17). Notwithstanding a naked cross-reference in that same footnote to "claim 10 at Section X.B.1," Petitioner does not identify any challenge to claims 13, 14, 16, 17, and 30 on the Nicol-only ground on which claims 10 and 12 are challenged. Moreover, the Petition does not

D. Obviousness of Claims 10, 12, 23, and 24 over Nicol

1. Independent Claim 10

a) "A processor device, comprising: a plurality of data processing elements;"

Petitioner contends that Nicol discloses a "processor device" comprising "a plurality of data processing elements" for the reasons stated with respect to the identical limitations of claims 3 and 6. Pet. 55–56 (citing Pet. 21–28, 33–34; Ex. 1001 ¶¶ 346, 347). Petitioner's contention is supported by the cited evidence and is not challenged by Patent Owner (*see generally* PO Resp.), and we are persuaded that this limitation is taught by the asserted prior art.

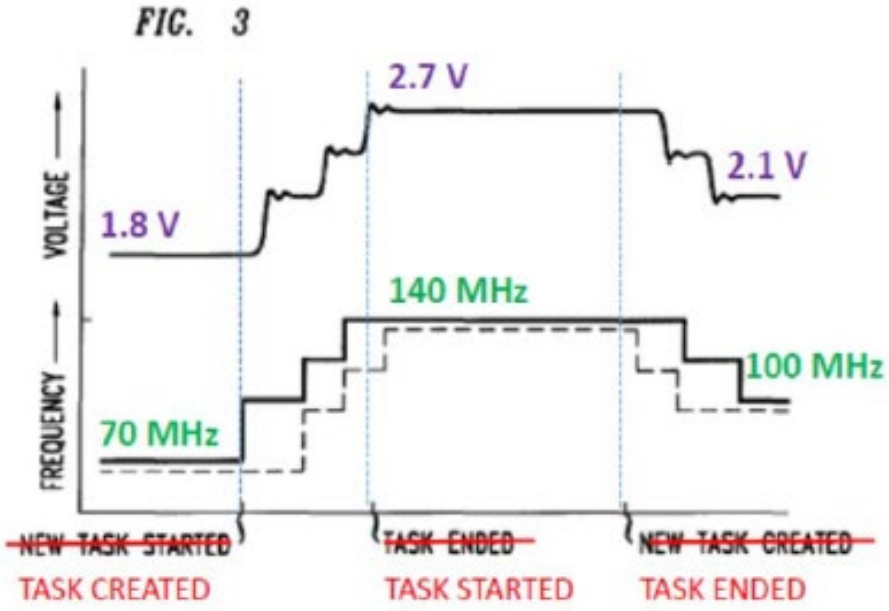
b) "a software adapted to be executed to (a) manage distribution of code sections, each code section to be executed by a respective group of a subset of the plurality of data processing elements, and (b) assign to each of the code sections a respective clock frequency, the group of data processing elements executing the respective code sections at the respective clock frequencies."

Petitioner contends Nicol teaches that the "real-time operating system" software in Nicol's controller assigns tasks to the different PEs, "manages distribution of code sections," and assigns respective clock frequencies to each of the code sections, citing, for example, Nicol's teaching that, based on the "the number of instructions that need to be executed for each task . . . , a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors." Pet. 56–58 (quoting Ex. 1006, 3:13–18) (citing

challenge claim 11, from which each of claims 13, 14, 16, 17, and 30 alternatively depends, on any ground. *See generally* Pet.

Ex. 1001 ¶¶ 348, 350–362; Ex. 1006, 2:53–56, 5:24–28, Fig. 2). According to Petitioner, "the code sections (instructions) are executed by a subset of the plurality of data processing element[s] because the tasks assigned by the operating system are distributed among all the available PEs." *Id.* at 57 (citing Ex. 1006, 3:19–20, 5:56–59, 6:66–7:3).

Additionally, Petitioner contends, Nicol's operating system ascertains the required completion time of tasks, "'consider[s] the PE with the tasks that require the most time to carry out, and adjust[s] the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time,' i.e., supply a respective clock frequency to the PE." Pet. 58 (emphasis omitted) (citing Ex. 1006, 3:66–4:5; Ex. 1001 ¶¶ 357–362). Petitioner contends that Nicol discloses "adjusting the clock frequencies of one or more PEs as 'to do' tasks are created, executed, and then completed" as shown in annotated Figure 3, reproduced below. *Id.* at 58–59.



Petitioner's annotated Figure 3 of Nicol shows the voltage changes in purple, clock frequency in green, and task creation in red. Pet. 13.

With reference to annotated Figure 3, Petitioner contends that "as new 'to do' tasks appear the controller PE determines the required completion time and . . . assigns the code sections to be executed by a group of PEs, and also raises their clock frequency (to 140 MHz), at which point the PEs transition to a high-performance state." Pet. 59 (citing Ex. 1006, 3:13–18, 5:24–28; Ex. 1001 ¶¶ 357–362).

In response, Patent Owner contends that "Nicol does not disclose . . . a subset of data processing elements, much less a subset of data processing elements that execute a code section." PO Resp. 30. Patent Owner argues that this claim element is similar to the "grouping" element of claim 3 discussed in Section II.C.4.b above, and that "[a]ccordingly, Petitioner fails to prove that Nicol renders claim 10 obvious for at least the same reasons that Petitioner fails to show that claim 3 is obvious is view of Nicol and Bhatia." *Id.*

For the reasons stated in Section II.C.4 above, we conclude that Petitioner's contentions with respect to claim 3, including Petitioner's contentions with respect to Nicol's teaching of the "grouping" limitation thereof, are supported by the cited evidence and are persuasive. For the same reasons, we conclude that Petitioner has met its burden to show by a preponderance of the evidence that the present limitation is taught by the asserted prior art.

c) Conclusion Regarding Claim 10

Based on Petitioner's persuasive arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 10 would have been obvious over Nicol.

2. Independent Claim 12

a) "A processor device, comprising:
a plurality of data processing elements adapted for programmably processing sequences and to which tasks are assigned, each of the data processing elements having at least one Arithmetic Logic Unit; and

Petitioner contends that Nicol discloses the preamble and "data processing elements" limitation of claim 12 for the reasons stated with respect to the identical limitations of claim 8, which Petitioner contends are in turn identical to limitations of claims 3 and 6. Pet. 59 (citing Pet. 39; Ex. 1001 ¶ 366); *see also id.* at 21–28, 33–35. Petitioner's contention is supported by the cited evidence and is not challenged by Patent Owner (*see generally* PO Resp.), and we are persuaded that these limitations are taught by the asserted prior art.

b) at least one bus system at least one of (a) interconnecting at least some of the data processing elements and (b) connecting at least some of the data processing elements with at least one of peripherals and external memory;

Petitioner contends that Nicol discloses the recited limitation, citing Nicol's Figure 4 as illustrating a bus system (i.e., Nicol's asynchronous communication network 160) interconnecting data processing elements with each other and with other system elements. Pet. 39–40 (citing Ex. 1006, Fig. 4, 6:18–21, 6:26–33) (cited at Pet. 59). Relying on the testimony of Dr. Sechen, Petitioner alleges that a person of ordinary skill in the art "would have understood that the bus system disclosed in Nicol, which

connects at least some of the PEs 'with other system elements,' would naturally include at least one peripheral and external memory." Pet. 40–41 (citing Ex. 1001 ¶¶ 260–267). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of Nicol's teachings with respect to these limitations. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Accordingly, we are persuaded that these limitations are taught by the asserted prior art.

> *c) wherein: each of at least some of the data processing elements is capable of operating at a clock frequency different than at least one other of the data processing elements;*

Petitioner contends that Nicol discloses this claim element by virtue of its teaching that "the frequencies at which the individual PEs operate [can] differ from one another and from other elements within the system." Pet. 41 (quoting Ex. 1006, 6:14–21) (citing Ex. 1001 ¶¶ 270–272; Ex. 1006, 5:66–6:2, 6:63–66, Fig. 4). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of Nicol's teachings with respect to this limitation. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Accordingly, we are persuaded that this limitation is taught by the asserted prior art.

> *d) "the clock frequency of each of the data processing elements is at least determinable by a state of the processing device;"*

With respect to the limitation "wherein . . . the clock frequency of each of the data processing elements is at least determinable by a state of the processing device," Petitioner contends that Nicol teaches "a range of control strategies in which Nicol determines a clock frequency based on the

state of the device" and thereby teaches this limitation. Pet. 60. According to Petitioner:

> As an initial matter, Nicol teaches that state can be determined selectively for each PE, can be common to a group of PEs, or can be common to all PEs of a chip. Ex. 1008, 6:57–7:3; *see also* Figure 2. . . .
>
> Nicol further teaches that the clock frequency adjustment is made according to a state of the multiprocessor system. Ex. 1001, ¶327–378. For example, as shown in Figure 3 . . . , prior to tasks being created, the multiprocessor system is in a low-activity state or a non-operational state and the controller maintains the clock frequency at a low value (70 MHz illustrated). Ex. 1008, 4:54–62. After task creation, the multiprocessor system transitions to a high-activity operational state and the controller adjusts the clock frequency to a high value (140 MHz illustrated). *Id.*
>
> Additionally, Nicol teaches a control strategy in which the controller PE would "ascertain the required completion time, divide the collection of tasks as evenly as possible . . . consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time." Ex. 1006, 3:66–4:5.

Pet. 60–62 (emphasis omitted).[17] Further, according to Petitioner, Figure 3 illustrates all PEs of the multiprocessor system are in a low-activity state before the controller allocates the tasks, after which the heavily-loaded PE transitions to a higher clock frequency. *See id.* at 62 (citing Ex. 1006, 3:66–4:5, 4:54–62). Petitioner contends that "[t]hus in this control strategy

[17] Because Petitioner's arguments at pages 60–62 of the Petition relate to Nicol (Exhibit 1006), rather than to DeHon (Exhibit 1008), we understand each of Petitioner's citations to Exhibit 1008 in the above quotation to refer instead to Exhibit 1006.

disclosed by Nicol, the clock frequency may be determined based on the state of the processing device." *Id.* (citing Ex. 1001 ¶¶ 327–378).

In response, Patent Owner argues that Nicol does not recite "low activity state," "inactive state," or "high activity state," but that those are merely Petitioner's characterizations of the voltage and frequency levels illustrated in Nicol's Figure 3. PO Resp. 30. According to Patent Owner, "[t]o the extent that these different voltage and frequencies might be considered states within the meaning of claim 12, Nicol does not teach that 'the clock frequency of each of the data processing elements is . . . determinable **by a state of the processing device**,'" but instead that "a frequency established according to time and load limitations drives the state." *Id.* at 31–32 (citing Ex. 1006, 2:56–58, 3:15–18, 4:3–5; Ex. 2022 ¶¶ 62–63). Accordingly, Patent Owner contends, "Nicol discloses the opposite" of the recited limitation. *Id.* at 32 (citing Ex. 2022 ¶ 63).

In its Reply, Petitioner contends that Patent Owner's argument "relies on a misidentification of the identified 'state' in Nicol" and "challenges a strawman argument by contending that Nicol's 'low activity' and 'high activity' states do not determine the clock frequency." Pet. Reply 21. Petitioner argues, "[a]s the Petition explained, Nicol teaches that the clock frequency of the PEs is determined by the load on (*i.e.*, 'state of') the processing device." *Id.* In particular, Petitioner explains, "clock frequency increases 'when a new task is created and the load of the multiprocessor is thus increased' and decreases 'when ***the load*** on the multiprocessor is decreased' because '[t]he ***reduced load*** permits lowering the clock frequency.'" *Id.* at 21–22 (quoting Ex. 1006, 4:54–66) (citing Pet. 61–62; Ex. 1006, 2:65–3:2, 3:67–4:5). Thus, according to Petitioner, "[t]here is no

dispute that this 'state' in Nicol meets the claim element, a point that [Patent Owner's] . . . argument leaves unrebutted." *Id.* at 22. Indeed, Petitioner argues, Patent Owner's expert admitted that "the processing load may be considered a 'state' of a PE." *Id.* (citing Ex. 1049, 159:4–16, 159:21–24).

In its Sur-reply, Patent Owner argues that Petitioner's "identifi[cation of] the processing load as the 'state' for this limitation for the first time on Reply . . . is a new argument that should be disregarded." PO Sur-reply 16, 21–22. Even if Petitioner's new argument is considered, however, Patent Owner further contends that "Petitioner confuses two different concepts as 'load,' only one of which could be understood as a state of the system." *Id.* at 16. In particular, Patent Owner argues, the load that is described in Nicol and relied upon by Petitioner is "anticipated load," as opposed to "actual load." *Id.* at 16–17. According to Patent Owner, "Nicol examines future tasks and determines and sets the clock frequency before starting task execution and actually 'loading' the system." *Id.* (citing Ex. 1001 ¶¶ 120–121; Ex. 1025, 93:1–16, 95:2–20). Thus, Patent Owner contends, "in Nicol the actual load on the system is never part of what determines the clock frequency." *Id.* at 17. With regard to Petitioner's contention that Patent Owner's expert admitted that processing load may be considered a "state" of a PE, Patent Owner argues that Dr. Mangione-Smith further testified that he did not consider the meaning of the term under the claim. *Id.*

We are persuaded that Nicol teaches the recited limitation. As an initial matter, we do not agree with Patent Owner that Petitioner's Reply presents a "new argument" as to how Nicol discloses the recited limitation than that presented in the Petition. Although the discussion of this limitation in the Petition does not expressly use the term "processing load," the

disclosure of Nicol relied on in support of Petitioner's arguments in the Petition that Nicol teaches PE state being determinable by the clock frequency does expressly refer to "the load on the microprocessor." *See, e.g.*, Ex. 1006, 4:54–62 (cited at Pet. 61 in support of contentions that "prior to tasks being created, the multiprocessor system is in a low-activity state or a non-operational state" and that "[a]fter task creation, the multiprocessor system transitions to a high-activity operational state"). The Reply does not introduce any new evidence with respect to this limitation, and we find that, rather than raising new issues, the arguments presented are responsive to those raised in the Patent Owner Response with respect to this limitation. Thus, we find those arguments to be within the scope of permissible reply. *See* CTPG 73–75.

With regard to the substance of the parties' arguments, we find Petitioner's mapping of Nicol's processing loads to the recited "state" to be supported by the cited evidence and persuasive. We also find persuasive Petitioner's evidence that Nicol teaches that PE clock frequency may be driven by the processing load. Further, notwithstanding Patent Owner's assertion of a substantive distinction between "anticipated load" and "actual load" in Nicol (PO Sur-reply 16–17), we find that the portion of Nicol cited by Petitioner nevertheless teaches that PE clock frequency may indeed be driven by actual load. For example, Nicol discloses that completion of a task "reduces the load on the multiprocessor" and that "*[t]he reduced load permits lowering the clock frequency.*" Ex. 1006, 4:62–65 (emphasis added). In view of that disclosure, in contrast, Patent Owner's contentions that "in Nicol the actual load on the system is never part of what determines

the clock frequency" (PO Sur-reply 17) and that the "frequency . . . drives the state" (PO Resp. 32) are unpersuasive.

e) "and the clock frequency for at least some of the data processing elements is set in accordance with a supply voltage."

Petitioner contends Nicol teaches first increasing the supply voltage to accommodate setting a higher clock frequency. Pet. 62–63 (citing Ex. 1006, 4:38–41, 5:3–5; Ex. 1001 ¶¶ 381–387). Patent Owner does not dispute Petitioner's contentions regarding the scope and content of Nicol's teachings with respect to this limitation. *See generally* PO Resp.

Petitioner's assertions are supported by the cited evidence and are persuasive. Accordingly, we are persuaded that this limitation is taught by the asserted prior art.

f) Conclusion Regarding Claim 12

Based on Petitioner's persuasive arguments and evidence, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 12 would have been obvious over Nicol.

3. Independent Claim 23

Independent claim 23 differs from independent claim 12 only insofar as it recites that the clock frequency of at least some of the data processing elements is "determined by a fill level of at least one of an input data buffer and an output data buffer" rather than being "set in accordance with a supply voltage." *Compare* Ex. 1003, 17:33–51, *with id.* at 16:27–45. Petitioner contends that Nicol renders this limitation obvious, citing disclosure in Nicol that the described system "react[s] to variations in the system load," such that "[a]s more tasks are entered into the 'to-do' list, the operating system of PE 100 computes the correct way to balance the additional computational

requirements[,] allocates the tasks to the processors[, and] then computes the required operating frequency." Pet. 65 (emphases omitted) (quoting Ex. 1006, 5:23–29) (citing Ex. 1001 ¶ 391). Further citing Nicol's disclosure that "[i]f the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors" and relying on the testimony of Dr. Sechen, Petitioner argues that the clock frequency of Nicol's PEs may therefore be determined by the number of tasks entered into the "to-do" buffer, which Petitioner contends is an "input data buffer" because it stores tasks for later input to the processor. *Id.* (quoting Ex. 1006, 3:13–18) (citing Ex. 1001 ¶¶ 392–396). In additional support of this contention, Petitioner also cites a statement made by the applicant for the '301 patent, during prosecution of a related patent application, that "one of ordinary skill in the art would understand that the fill level of a data buffer [is] representative of the number of waiting operations or processor load." *Id.* at 65–66 (emphasis omitted) (quoting Ex. 1009, 377 (prosecution history of U.S. Serial No. 13/653,639)). Patent Owner does not challenge Petitioner's contentions with respect to this limitation in its Response, but relies for claim 23 on its arguments made with respect to independent claims 3 and 12. PO Resp. 32; PO Sur-reply 17.

Petitioner's assertions are supported by the cited evidence and are persuasive. For the above reasons and for the reasons previously stated in the discussion of claims 3 and 12 (*see supra* §§ II.C.4, II.D.2), we are persuaded that Petitioner has established by a preponderance of the evidence that claim 23 is unpatentable over Nicol.

4. Independent Claim 24

Independent claim 24 differs from independent claim 12 only insofar as it recites that the clock frequency of at least some of the data processing elements is "set based on whether data is determined to be available" rather than being "set in accordance with a supply voltage." *Compare* Ex. 1003, 17:52–6:3, *with id.* at 16:27–45. Relying again on Nicol's disclosure that when "the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors," along with Nicol's disclosure that a subdivision of an application to be processed in concurrent task streams "allows the clock frequency of the PEs to be reduced," Petitioner contends that a person of ordinary skill in the art would thus have understood that setting a clock frequency may take into account whether and how much data is available for completing tasks to insure that tasks are completed in a timely order. Pet. 67 (emphases omitted) (quoting Ex. 1006, 3:12–18, 4:21–27) (citing Ex. 1001 ¶¶ 406–407). Patent Owner does not challenge Petitioner's contentions with respect to this limitation in its Response, but relies for claim 24 on its arguments made with respect to independent claims 3 and 12. PO Resp. 32; PO Sur-reply 17.

Petitioner's assertions are supported by the cited evidence and are persuasive. For the above reasons and for the reasons previously stated in the discussion of claims 3 and 12 (*see supra* §§ II.C.4, II.D.2), we are persuaded that Petitioner has established by a preponderance of the evidence that claim 24 is unpatentable over Nicol.

III. CONCLUSION[18]

Based on the evidence presented with the Petition, the evidence introduced during the trial, and the parties' respective arguments, Petitioner has shown by a preponderance of the evidence that each of claims 3, 6, 7, 10, 12, 23, and 24 of the '301 patent is unpatentable. Petitioner has not shown by a preponderance of the evidence that the claims 8, 9, 13–19, 25, 26, 30, 32, 35, and 36 are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 3, 6, 7, 10, 12, 23, and 24 of the '301 patent have been shown to be unpatentable;

FURTHER ORDERED that claims 8, 9, 13–19, 25, 26, 30, 32, 35, and 36 of the '301 patent have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

[18] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2) (2020).

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
3, 6–9, 13–19, 25, 26, 30, 32, 35, 36	103(a)	Nicol, Bhatia	3, 6, 7	8, 9, 13–19, 25, 26, 30, 32, 35, 36
10, 12, 23, 24	103(a)	Nicol	10, 12, 23, 24	
10, 12, 23, 24	103(a)	Nicol, DeHon[19]		
3, 6–9, 13–19, 25, 26, 30, 32, 35, 36	103(a)	Nicol, Bhatia, DeHon[20]		
Overall Outcome			3, 6, 7, 10, 12, 23, 24	8, 9, 13–19, 25, 26, 30, 32, 35, 36

[19] As explained above, we do not reach this ground. *See supra* § I.D.

[20] As explained above, we do not reach this ground. *See supra* § I.D.

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