Trials@uspto.gov
571-272-7822

Paper 30
Entered: September 8, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00540
Patent 9,037,807 B2

Before SALLY C. MEDLEY, SCOTT C. MOORE, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges.*

OGDEN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In response to a Petition (Paper 2, "Pet.") by Petitioner Intel Corporation ("Intel"), the Board instituted an *inter partes* review of claims 1–6, 9, 24, 26, 27, 29, 30, 32, 42, 44, 73, and 74 of U.S. Patent No. 9,037,807 B2 (Ex. 1003, "the '807 patent"). Paper 11. Patent Owner PACT XPP Schweiz AG ("PACT") filed a Patent Owner Response (Paper 17, "PO Resp."), Intel filed a Reply to the Patent Owner Response (Paper 21, "Pet. Reply"), and PACT filed a Sur-reply (Paper 23, "PO Sur-reply").

We held an oral hearing on June 16, 2021, and the transcript is entered on the record. Paper 29 ("Tr.").

This is a Final Written Decision under 35 U.S.C. § 318(a) as to whether the claims challenged in the *inter partes* review are patentable. By a preponderance of the evidence on the record before us, Intel has shown that all the challenged claims of the '807 patent are unpatentable.

II. BACKGROUND

A. RELATED PROCEEDING

As related matters, the parties identify *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-00267-RGA (D. Del. terminated Apr. 24, 2019); *PACT XPP Schweiz AG v. Intel Corp.*, No. 6:19-cv-00273-ADA (W.D. Tex. terminated May 30, 2019); *Intel Corp. v. PACT XPP Schweiz AG*, No. 3:19-cv-02241 (N.D. Cal. terminated May 30, 2019); and *PACT XPP Schweiz AG v. Intel Corp.*, No. 1:19-cv-1006-JDW (D. Del. filed May 30, 2019) ("the co-pending litigation"). Paper 27, 2; Paper 18, 1–2.

B. THE '807 PATENT (EX. 1003)

The patent describes a computer multi-processor system with "reconfigurable components," and "the decoupling of data processing" within those components. Ex. 1003, 1:18–24. The system includes processing array elements ("PAEs") arranged in a processing array ("PA"). Ex. 1003, 1:64–66. Each PAE may be a processor, memory, networking cells, I/O, or other components. *See id.* at 1:61–63. The system also has "interface modules" that transmit data between the PA and external memory units. *See id.* at 4:16–25. There is also a "bus system [that] allows data exchange to take place configurably between the interface modules and any PAEs within the PA." *Id.* at 24:17–19.

In describing how the PAEs are connected to each other, the '807 patent refers to, and builds on, a German application by a common inventor (Exs. 1010, 1011 (English translation), "Vorbach" [1]) that discloses a flexible bus system. *See, e.g.*, Ex. 1003, 14:26–32, 14:58–59, 25:63–26:6. According to the '807 patent, Vorbach "describes a method of constructing flexible data channels within a PAE matrix according to the algorithms to be executed," and "[d]ata to be transmitted may be precisely assigned to one source and/or one destination." *Id.* at 14:26–32. Vorbach itself states that it intends to "create a bus system that can transmit data between a plurality of function blocks in such a way that a plurality of data packets can be present on the bus at the same time." Ex. 1011 § 1.3.

[1] Vorbach, DE 197 04 742 A1, published Sept. 24, 1998. *See* Ex. 1010, code (43). Intel contends that Vorbach qualifies as prior art under 35 U.S.C. § 102(b), and PACT does not challenge this assertion. Pet. 12 n.3. However, Intel does not include Vorbach in the grounds of its Petition.

Figure 2 of Vorbach is reproduced below:

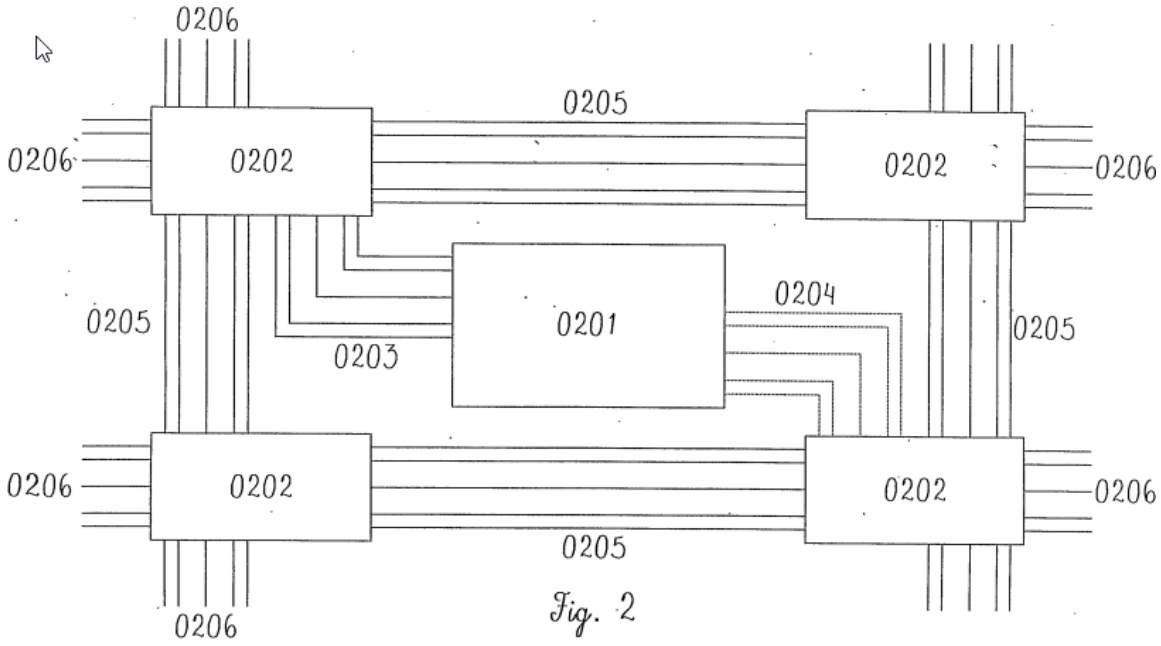


Figure 2, above, illustrates one recurring part of a two-dimensional array of configurable processing cells (PAEs) 0201 and bus control circuits 202. *See* Ex. 1011 §§ 2.1, 5. Each PAE 0201 connect to bus control circuits 0202 through one of two bundles of data lines 0203 or 0204. *Id.* § 5. Bus control circuits 0202 connect to each other through bus segments 0205, and connect externally to other bus control units in the PA through bus segments 0206. *Id.* § 5. "Each bus segment can be used and connected independently of the others, with the interconnection being the responsibility of the nodes." *Id.* § 3.1.

The '807 patent adds to Vorbach's disclosure "additional possibilities . . . (hereinafter referred to jointly as GlobalTrack) that permit flexible allocation and interconnection during run time." Ex. 1003, 14:35–38. In particular, the '807 patent states that by properly implementing Vorbach in the context of GlobalTrack, "a plurality of connections may now be established and used simultaneously." *Id.* at 14:61–63.

For example, Figure 8 of the '807 patent, reproduced below, depicts an embodiment of a structure for connecting interface modules or PAEs, via a dedicated global bus, to external memories:

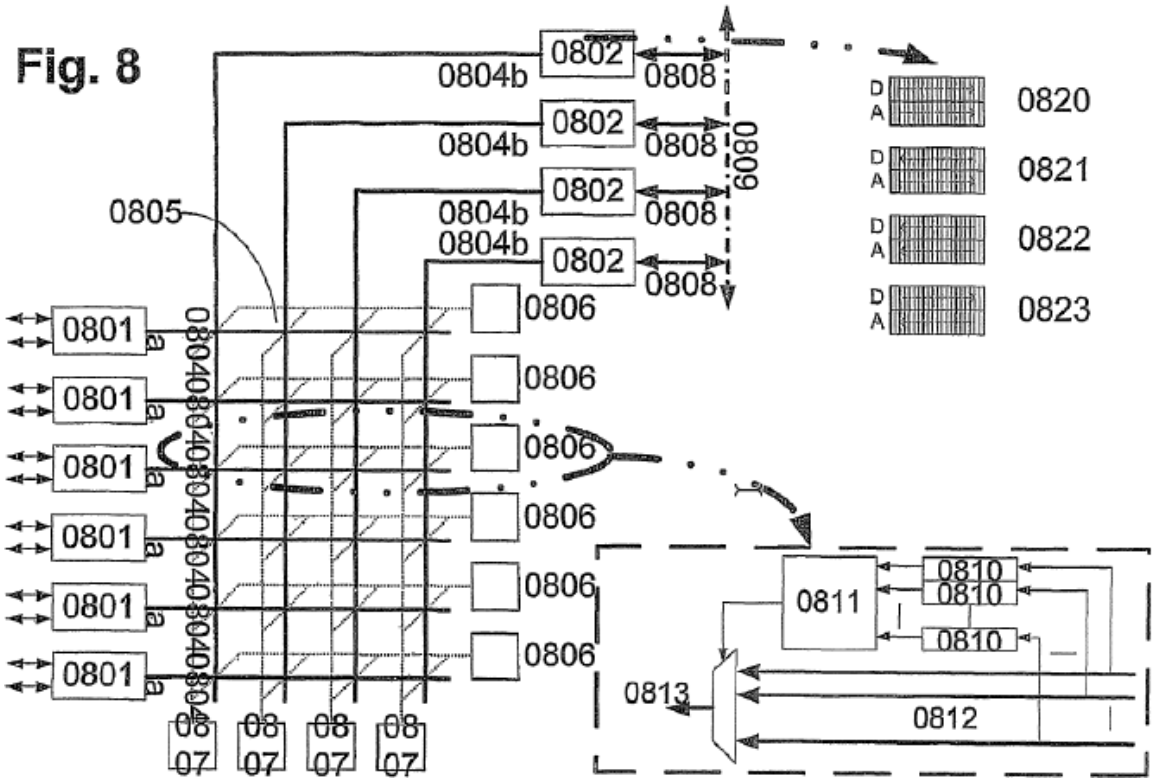


Figure 8, above, is a block diagram showing "a possible connection structure between interface modules and/or PAEs having a dedicated global bus (0801) and protocol converters (0802) to external (main) memories and/or other (peripheral) data streams." Ex. 1003, 26:59–62; *see also id.* at 2:54–55. The connection structure between global bus 0801 and protocol converters 0802 includes data lines 804a and 804b arranged in rows and columns, and interconnected by switches 805 which are designed as transmission gates, tristate buffers, or multiplexers. *Id.* at 26:65–27:5. The rows are connected to dedicated global bus 801, which connects to interface units or PAEs. *See id.* at 26:60–62, 27:5–16. The columns are connected to protocol converters 802, which connect to external (main) memory units. *See id.* Triggering units

806 and 807 trigger the rows and columns, respectively, to control data transfer between global bus 801 and protocol converters 802. *Id.* at 27:5–16.

Another example of bus systems connecting PAEs is shown in Figure 5, which we reproduce below:

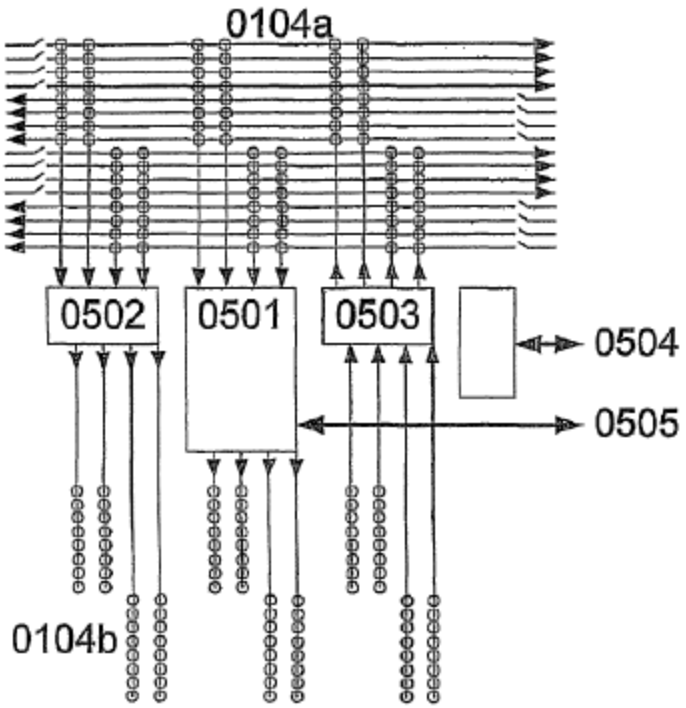


Fig. 5

Figure 5 of the ’807 patent, above, depicts “a possible embodiment of a PAE.” Ex. 1003, 25:49. Data processing unit 501 connects to both first bus system 104a (for input) and second bus system 104b (for output). *Id.* at 25:49–52. There is also a separate connection to dedicated global bus 0505, which allows either direct connections from PAE 0501 to a different PAE, or from PAE 0501 to an external interface module. *Id.* at 25:63–26:4. The ’807 patent states that the bus system described in Vorbach “may be used for such purposes.” *Id.* at 26:4–6.

When multiple units, such as in Figure 5, are joined together in a grid, they can form ring patterns, as shown in Figure 6, reproduced below:

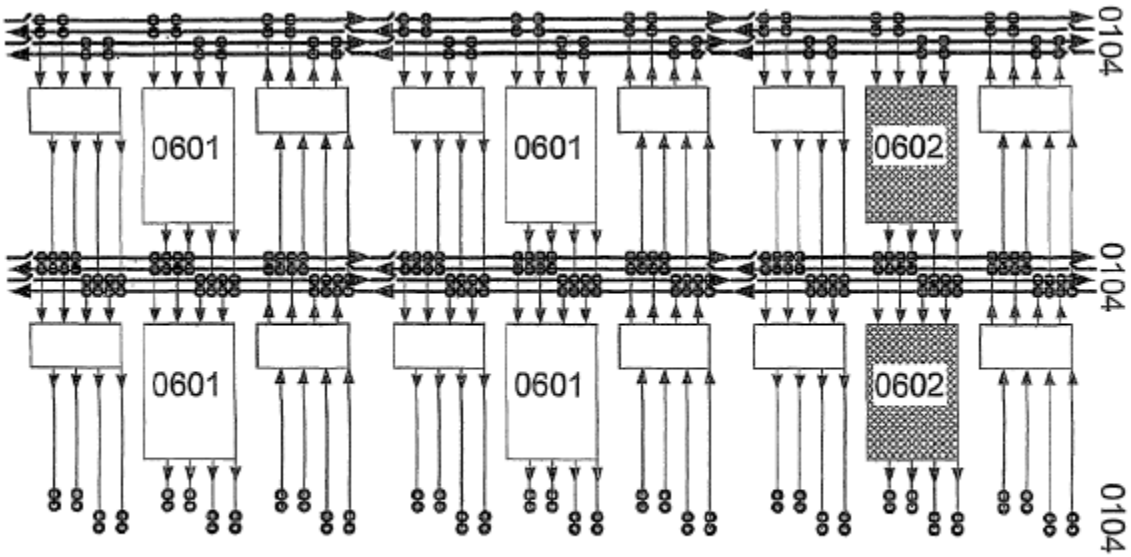


Fig. 6

Figure 6, above, "shows an example of a wiring connection of ALU-PAEs (0601) and RAM-PAEs (0602) via a bus system 0104." Ex. 1003, 26:38–39. For each bus 0104 there are three PAEs (0601 or 0602) corresponding to PAE 0501 in Figure 5. During prosecution, the applicant explained that Figure 6 "clearly shows a bus interconnection of processor array element[s] by a bus system 0104 in a ring formation with a bi-directional connection." Ex. 1004, 537. An example ring, according to the applicant, is a transfer "from the top-right 0602[2] element to a transverse bus line below that directs the data to the left, which data can then be transmitted upwards, for example, to the element to the immediate right of the top-left 0601 element." *Id.* From there, the transfer can go "upwards to the transverse bus line above that

[2] The applicant may have intended this to be 0601, otherwise the resulting formation would not be a closed ring.

directs the data to the right, and then for example, down to the top-right 0601 element." *Id.*

The '807 patent claims a priority date of March 5, 2001, which Intel does not contest in the Petition. Pet. 11; Ex. 1003, code (30), 1:11–14.

C. CHALLENGED CLAIM AND ASSERTED GROUNDS OF UNPATENTABILITY

Claim 3, below, is representative of the challenged claims:

3. A multi-processor system on a chip, comprising:

[a] a plurality of data processing elements that each includes at least one arithmetic-logic unit (ALU) and a plurality of registers adapted for storing data;

[b] a plurality of memory elements that each independently operates as a cache for caching data; and

[c] at least one interface element for providing a connection to a common higher level memory;

[d] wherein each of the data processing elements, each of the memory elements, and each of the at least one interface element are interconnected via a bus system for transferring data at least between (i) at least one of the data processing elements and at least one of the memory elements and (ii) at least one of the memory elements and the at least one interface element;

[e] wherein the bus system is adapted for dynamically establishing and releasing transmission channels between a sending one of the elements and a receiving one of the elements; and

[f] wherein an identification token is assigned to transmitted data for indicating an affiliation of the transmitted data to a process.

Ex. 1003, 32:34–55 (Intel's reference letters added). Claims 1, 4, 5, 9, 19, 26, 27, and 30 are also independent, and claims 2, 6, 24, 32, 42, 44, 73, and 74 depend ultimately from one of the challenged independent claims. *See id.* at 32:8–40:52.

Intel argues three grounds for *inter partes* review, as summarized in the following table:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
I	3, 4, 9, 24, 26, 27, 30, 42, 73, 74	103	Barroso,[3] Alpha Manual[4]
II	1, 5, 32, 44	103	Barroso, Alpha Manual, Godfrey,[5] Nickolls[6]
III	2, 6, 29	103	Barroso, Alpha Manual, Godfrey, Nickolls

Pet. 4. For Ground I, Intel alleges that claims 3, 4, 9, 24, 26, 27, 30, 42, 73, and 74 are unpatentable under § 103 as obvious over Barroso and Alpha Manual. *Id.* For Ground II, Intel alleges that claims 1, 5, 32, and 44 are unpatentable under § 103 as obvious on alternative grounds: "(a) Barroso, Alpha Manual, and Nickolls or, alternatively, (b) Barroso, Alpha Manual, Godfrey, and Nickolls." *Id.* For Ground III, Intel alleges that claims 2, 6, and

[3] Luiz André Barroso et al., *Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing*, Proc. 27th Int'l Symp. on Computer Architecture (June 14, 2000) (Ex. 1005). *See also* Ex. 1021 (Grenier Decl.).

[4] *Alpha AXP Architecture Reference Manual* (Richard L. Sites & Richard T. Witek eds., 2d ed. 1995) (Ex. 1020, "Alpha Manual").

[5] Godfrey et al., US 6,266,797 B1 (issued July 24, 2001) (Ex. 1006).

[6] Nickolls et al., US 5,598,408 (issued Jan. 28, 1997) (Ex. 1012).

29 are unpatentable under § 103 as obvious over Barroso, Alpha Manual, Godfrey, and Nickolls. *Id.*

D. EXPERT TESTIMONY

For its Petition and Reply, Intel relies on two declarations of Dr. Pinaki Mazumder. Exs. 1001, 1050. For its Response and Sur-reply, PACT relies on a declaration by Dr. Andrew Wolfe. Ex. 2026. We find both witnesses qualified, based on their education and experience, to offer expert testimony on the subject matter of their respective declarations. *See* Fed. R. Evid. 702(a); *see* Ex. 1001 ¶¶ 5–33; Ex. 1002 (Dr. Mazumder's curriculum vitae); Ex. 2026 ¶¶ 3–15; Ex. 2027 (Dr. Wolfe's curriculum vitae).

In its Response, PACT contends that we should discount Dr. Mazumder's testimony because allegedly, during cross-examination, (A) he "could not answer basic questions about the '807 patent, Barroso, and Nickolls" without refreshing his recollection, PO Resp. 12–13 (citing Ex. 2028, 20:25–22:11, 41:6–46:6, 82:14–84:14, 100:2–102:4, 129:6–131:12, 133:13–134:22, 143:20–147:16, 164:11–166:24); (B) he admitted that he did not know the answer to certain questions about the structure of elements described in the '807 patent or the cited art, *id.* at 13 (citing Ex. 2028, 41:6–46:6, 56:12–60:25, 71:3–73:19, 74:15–76:2, 82:8–96:19; 126:5–127:2, 143:20–147:16; Ex. 1012, 7:36–39); and (C) he was evasive, *id.* at 14–15 (citing Ex. 2028, 38:15–46:6, 82:8–96:19, 108:9–113:22, 114:7–118:5, 125:17–132:24, 143:20–147:16, 164:11–166:24; Ex. 1005, 291; *10X Genomics, Inc. v. Univ. of Chicago*, IPR2015-01157, Paper 30 at 2 (PTAB 2016)).

In its Reply, Intel argues that PACT mischaracterizes Dr. Mazumder's testimony. Pet. Reply 26. Intel argues that "there is nothing improper about Dr. Mazumder refreshing his recollection—which PACT never objected to—particularly when he submitted his declaration nine months before his deposition." *Id.* Intel also argues that for the cited examples in which PACT describes Dr. Mazumder as "rereading extensive portions" of documents, the transcript "instead shows him identifying relevant passages in response to PACT's questions and explaining them." *Id.* at 26–27. Intel also disputes that Dr. Mazumder was being evasive or avoided answering questions. *Id.* at 27–28 (citing Ex. 2028, 48:11–23, 71:10–73:19, 86:2–87:5, 108:11–110:2, 164:11–166:24).

At least with respect to the portions of Dr. Mazumder's declaration that supports Intel's arguments on which we rely for our decision, and any cross-examination relevant to that testimony, we disagree that Dr. Mazumder was improperly recalcitrant, or demonstrated a lack of knowledge of the subject matter to the extent that it would discredit him as a credible expert witness. Given the circumstances, we also do not fault Dr. Mazumder for refreshing his recollection during cross-examination. Thus, we do not agree with PACT that we should, as a general proposition, disregard or give less credit to Dr. Mazumder's testimony for these reasons.

III. GROUNDS OF THE PETITION

For the reasons below, we determine that Intel has shown, by a preponderance of the evidence, that claims 1–6, 9, 24, 26, 27, 29, 30, 32, 42, 44, 73, and 74 of the '807 patent are unpatentable under § 103. Before analyzing the Petition's asserted grounds in detail, we address two matters

that will underlie our analysis: the level of ordinary skill in the art, and the construction we will apply to the claim terms.

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the time of the invention is one of the factual considerations relevant to obviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). It is also relevant to how we construe the patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). To assess the level of ordinary skill, we construct a hypothetical "person of ordinary skill in the art," from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct "presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan." *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Intel argues that a person of ordinary skill in the art "would have had at least an M.S. degree in electrical engineering, and at least three years of experience with multiprocessor systems design." Pet. 14 (citing Ex. 1001 ¶ 72). Dr. Mazumder testifies that this level of skill "was the typical level of experience of persons working with multiprocessor systems, including the design of processor, cache, memory, and bus architectures, at the time of the alleged invention." Ex. 1001 ¶ 72.

Dr. Wolfe does not disagree, and in his declaration he applies Dr. Mazumder's proposed articulation of the level of ordinary skill. *See* Ex. 2026 ¶ 40.

For this decision, we adopt Dr. Mazumder's uncontested declaratory testimony, which we find consistent with the level of technical expertise assumed by the '807 patent disclosure and the asserted prior art references.

B. CLAIM CONSTRUCTION

In an *inter partes* review, we construe a patent claim "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2020). This includes "construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." *Id.* The ordinary and customary meaning of a claim term "is its meaning to the ordinary artisan after reading the entire patent," and "as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313, 1321. We also consider "[a]ny prior claim construction determination concerning a term of the claim in a civil action . . . that is timely made of record" in this proceeding. 37 C.F.R. § 42.100(b) (2020).

Neither Intel nor PACT argues that any claim terms need an explicit construction. *See* Pet. 5 ("Intel does not believe any terms need to be construed to resolve the prior art issues presented in this Petition."). However, according to Intel, in the co-pending litigation the parties "stipulated that the preambles are not limiting" for all independent claims challenged in the Petition. *Id.* (citing Ex. 1014). PACT does not challenge this statement, and whether the preambles are limiting does not appear to be material to Intel's contentions in the Petition.

Absent a controversy, we do not need to explicitly construe any terms for our decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). To the extent that our decision involves interpreting claim language, we discuss that language below in our analysis of the claim limitations.

C. GROUND I (BARROSO, ALPHA MANUAL)

For Ground I, Intel alleges that claims 3, 4, 9, 24, 26, 27, 30, 42, 73, and 74 are unpatentable under 35 U.S.C. § 103 as obvious over Barroso in view of Alpha Manual. Pet. 4.

A claim is unpatentable under § 103 for obviousness if the differences between the claimed subject matter and the prior art are "such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). For a combination of known elements that are not explicitly found together in the prior art, we consider "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). A successful petition must "articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (citing *KSR*, 550 U.S.

at 418); *see also* 35 U.S.C. § 322(a)(3); 37 C.F.R. §§ 42.22(a)(2), 42.104(b)(4) (2020).

We base our obviousness inquiry on factual considerations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) any objective indicia of obviousness or non-obviousness that may be in evidence. *See Graham*, 383 U.S. at 17–18.

Based on these factors,[7] Intel has shown that claims 3, 4, 9, 24, 26, 27, 30, 42, 73, and 74 are unpatentable under 35 U.S.C. § 103 as obvious over Barroso in view of Alpha Manual. We present our findings and conclusions below.

1. Cited Prior Art

We may institute an *inter partes* review "only on the basis of prior art consisting of patents or printed publications." 35 U.S.C. § 311(b). PACT contends that Barroso does not fall within the scope of permissible prior art because it is allegedly not a printed publication. *See* PO Resp. 41–47. After providing an overview of Barroso, we address whether it is a printed publication below. Then we also provide a brief overview of Alpha Manual.

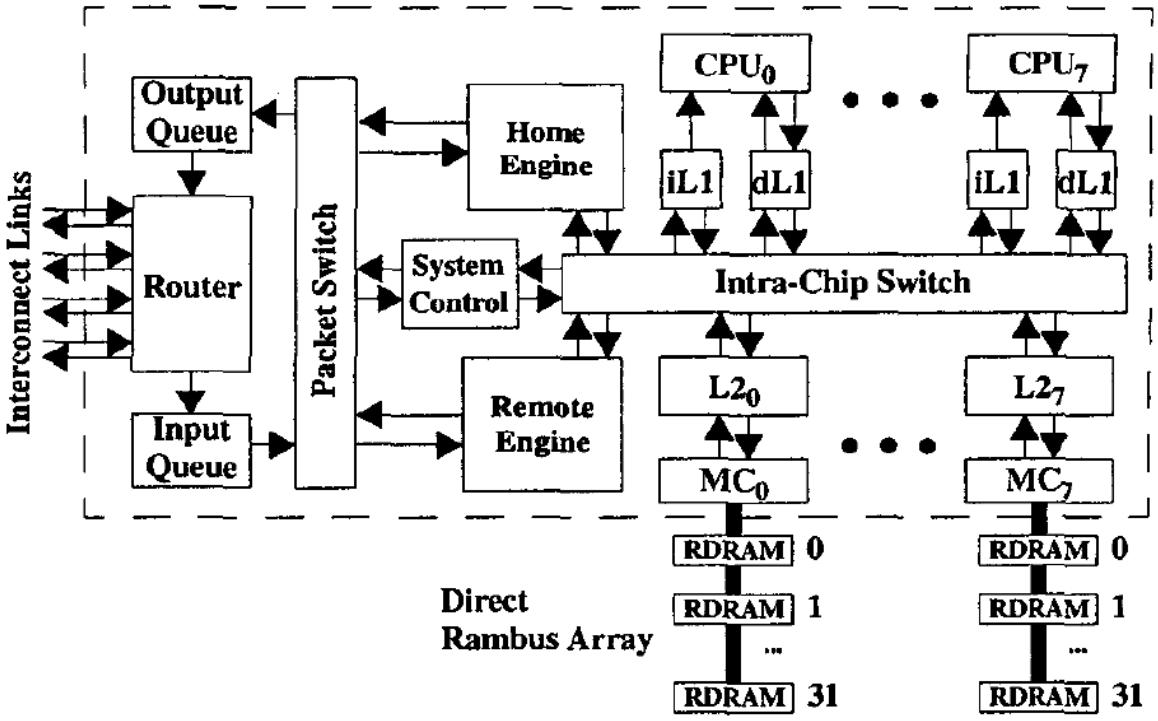
(a) Overview of Barroso

Barroso "describes the *Piranha* system, a research prototype . . . that aggressively exploits chip multiprocessing by integrating eight simple Alpha

[7] Neither party has identified any objective indicia of obviousness or non-obviousness, so this does not factor into our decision. *See* Ex. 1001 ¶ 206 (Dr. Mazumder stating that he is not aware of any objective indicia); PO Resp. (not contending that any objective indicia are present).

processor cores along with a two-level cache hierarchy onto a single chip." Ex. 1005, 282.

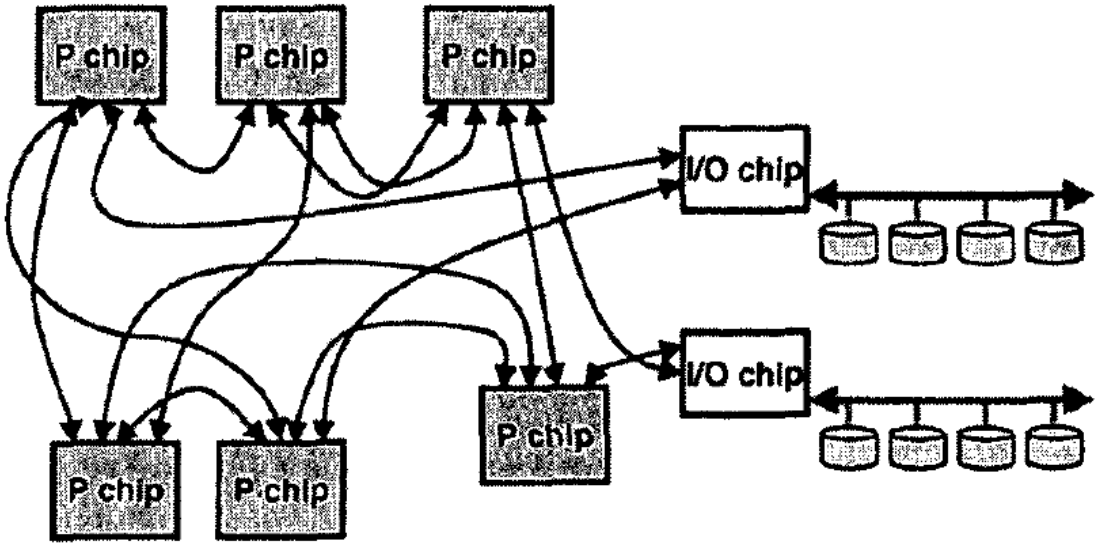
Figure 1, reproduced below, is a block diagram illustrating a single-chip processing node within the Piranha system:



Ex. 1005, 283. Barroso's Figure 1 is a block diagram depicting Alpha processor cores CPU_0–CPU_7, each directly connected to dedicated level-one cache modules iL1 (for instructions) and dL1 (for data). *Id.* "These first-level caches interface to other modules through the *Intra-Chip Switch (ICS)*," shown below the first-level caches. *Id.* Below the ICS are level-two cache modules $L2_0$–$L2_7$, each of which attaches, respectively, to memory controllers MC_0–MC_7, which directly interface to a bank of up to 32 RDRAM chips within a memory array. *Id.* "Also connected to the ICS are two protocol engines, the *Home Engine (HE)* and the *Remote Engine (RE)*, which support shared memory across multiple Piranha chips." *Id.* Input and

output functions take place through a connection to a separate I/O node, which is similar to Figure 1 but has only one processor and one memory bank. *Id.* at 284; *see also id.* Figs. 2, 3.

Barroso's Figure 3, reproduced below, depicts an example configuration for a Piranha system with multiple chips:



Ex. 1005, 284. Figure 3, above, depicts six processing chips (each identified as "P chip" and containing eight CPUs each, as shown above in Figure 1) and two I/O chips, with connections between all eight of the chips indicated with arrows. *Id.* Figure 3 also shows four I/O devices connected to each I/O chip. Barroso states that "the Piranha router supports arbitrary network topologies and allows for dynamic reconfigurability," and the system "treat[s] I/O in a uniform manner as a full-fledged member of the interconnect," to create "a single switching fabric that forms a global resource which can be dynamically utilized for both memory and I/O traffic." *Id.*

(b) Whether Barroso is a Prior Art Printed Publication

Barroso is a conference paper, and according to Intel, it was "published June 14, 2000" and "is prior art under at least § 102(a), (b)." Pet. 3. Intel submits a declaration of Gerard P. Grenier, the Senior Director of Content Management of the IEEE, who testifies that "[t]he article and abstract from [IEEE's web server] shows the date of publication," and that the web server "populates this information using the metadata associated with the publication." Ex. 1021 ¶ 10. He states that the article "was published in the Proceedings of the 27th International Symposium on Computer Architecture," which was "held on June 14, 2000." *Id.* ¶ 11. He states, "Copies of the conference proceedings were made available no later than on the day of the conference." *Id.*

PACT argues that Intel "fails to establish that Barroso is a prior art publication." PO Resp. 41. First, PACT acknowledges that "Barroso's front page bears certain indicia that may correspond to publication, including a copyright date and a reference to an ACM symposium," but PACT argues that Intel and Mr. Grenier's declaration "fail to offer any detail regarding public accessibility, including what happened during the conference and who had access to the conference." *Id.* at 43 (citing *Hulu, LLC v. Sound View Innovations*, LLC, IPR2018-01039, Paper 29 at 11 (PTAB Dec. 20, 2019) (precedential); *In-Depth Geophysical v. ConocoPhillips Co.*, IPR2019-00849, Paper 14 at 9–10 (Sept. 6, 2019) (informative) (denying institution when the document in question had a copyright notice indicating the same year as the priority date of the patent, but with no month or day, and no further indication of what the date represented)).

Second, PACT argues that Mr. Grenier "fails to explain how Barroso was available or publicly accessible to 'interested persons,'" or how those 'ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.'" PO Resp. 44–45 (quoting *Hulu*, IPR2018-01039, Paper 29 at 10–11) (citing *Argentum v. Research Corp.*, IPR2016-00204, Paper 19 at 12 (May 23, 2016) (informative)). In particular, PACT argues that only paragraph 11 of Mr. Grenier's declaration relates to Barroso's availability at or after the conference. *Id.* at 44 (citing Ex. 1021 ¶ 9). And according to PACT, "there is no evidence showing that the declarant had *personal* knowledge of the availability of Barroso as of the date of the ACM symposium," and there is no explanation "as to how Barroso was distributed at or after the symposium." *Id.* PACT also compares Mr. Grenier's testimony in this case with his testimony submitted in a different case for which the Board held that two references were not printed publications, *Smart Microwave Sensors Gmbh v. Wavetronix LLC*, IPR2016-00488, Paper 57 at 27–29 (PTAB July 17, 2017), arguing that "the same rationale applies here." *Id.* at 45–47.

In its Reply, Intel submits declarations that, according to Intel, "show[] that physical copies of Barroso were publicly available at the University of Wisconsin and University of Texas libraries as early as June and August 2000, respectively." Pet. Reply 28 (citing Exs. 1053, 1054). Intel also submits "a declaration from ISCA[8] 2000 steering committee member Robert Colwell." *Id.* at 28–29 (citing Ex. 1055). According to Intel, ISCA 2000 was "the IEEE-sponsored conference where Barroso was presented,"

[8] According to Dr. Colwell, ISCA stands for the "International Symposium on Computer Architecture." Ex. 1055 ¶ 4.

and according to Intel, Dr. Colwell testifies that the conference "was attended by 'about 230 people,' that the 'standard practice was to give a physical, bound copy of the proceedings to each attendee when they checked into the conference,' and that Barroso is a 'well-known paper' in the field of multi-processors.'" *Id.* (quoting Ex. 1055).

Intel also submits cross-examination testimony from a related *inter partes* review in which PACT's expert for that case, Dr. Murali Annavaram, testified about ISCA. Pet. Reply 29 (citing Exs. 1051, 1056). According to Intel, Dr. Annavaram is "an ISCA reviewer," and he "described ISCA as a 'top-of-the-line conference[]' and confirmed that 'at the time of the conference, the attendees get to read [the conference proceedings] either in a physical binder format or electronically.'" *Id.* (alteration in original) (quoting Ex. 1051, 163:7–164:11, 164:22–166:5) (citing Ex. 1056 (a document that appears to be Dr. Annavaram's curriculum vitae)[9]).

In its Sur-reply, PACT contends that Intel's "new evidence regarding the public availability of Barroso is not admissible." PO Sur-reply 20–21. But PACT does not assert any particular ground for inadmissibility in its Sur-reply, and although PACT filed timely objections to the new evidence (Paper 22), PACT did not file a motion to exclude. Thus, PACT has not preserved these objections. *See* 37 C.F.R. § 42.64(c) ("A motion to exclude evidence must be filed to preserve any objection.").

Whether a reference is a printed publication "involves a case-by-case inquiry into the facts and circumstances surrounding the reference's disclosure to members of the public." *Hulu*, IPR2018-01039, Paper 29 at 9

[9] In its objections to Exhibit 1056, PACT acknowledges that the document is Dr. Annavaram's curriculum vitae, as filed in related case IPR2020-00531.

(quoting *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018)). Indicia on the face of the reference, such as a copyright date or ISBN number, "are considered as part of the totality of evidence." *Id.* at 17–18 (citing *Nobel Biocare Servs. AG v. Instradent USA, Inc.*, 903 F.3d 1365, 1377 (Fed. Cir. 2018)).

Based on the evidence as a whole, Intel has shown persuasively that the IEEE published the Barroso article in 2000 as part of a physical volume accessible to researchers in the field. In addition to having a copyright notice dated 2000, Barroso is part of a non-consecutively paginated article, bearing the ISBN number "1-58113-232-8." Ex. 1005, 282. The document also provides instructions for copying and republication, and specifies a copying fee of $5.00. *See id.* We also find it credible that Mr. Grenier would be familiar with the publication practices of the IEEE in 2000, and the IEEE's practices with respect to maintaining publication metadata for articles such as Barroso.

Although we would reach this conclusion without the new evidence that Intel submitted with its Reply, this new evidence also supports our finding. We find credible the librarian testimony that copies of Barroso were publicly available in two university libraries before the earliest priority date of the '087 patent. *See* Exs. 1053, 1054. We also find credible the testimony of Dr. Colwell that Barroso was well-known in the field, and that it is standard practice to submit a physical, bound copy of proceedings at the ISCA conference. Ex. 1055 ¶ 10. So the evidence suggests that about 230 people would have received a bound copy of Barroso at that time. *See id.* ¶ 9. Dr. Annavaram's testimony, as a witness appearing on behalf of PACT in another case, corroborates this, although according to him, attendees to

the ISCA conferences might have received an electronic copy rather than a bound copy. *See* Ex. 1051, 165:6–166:5.

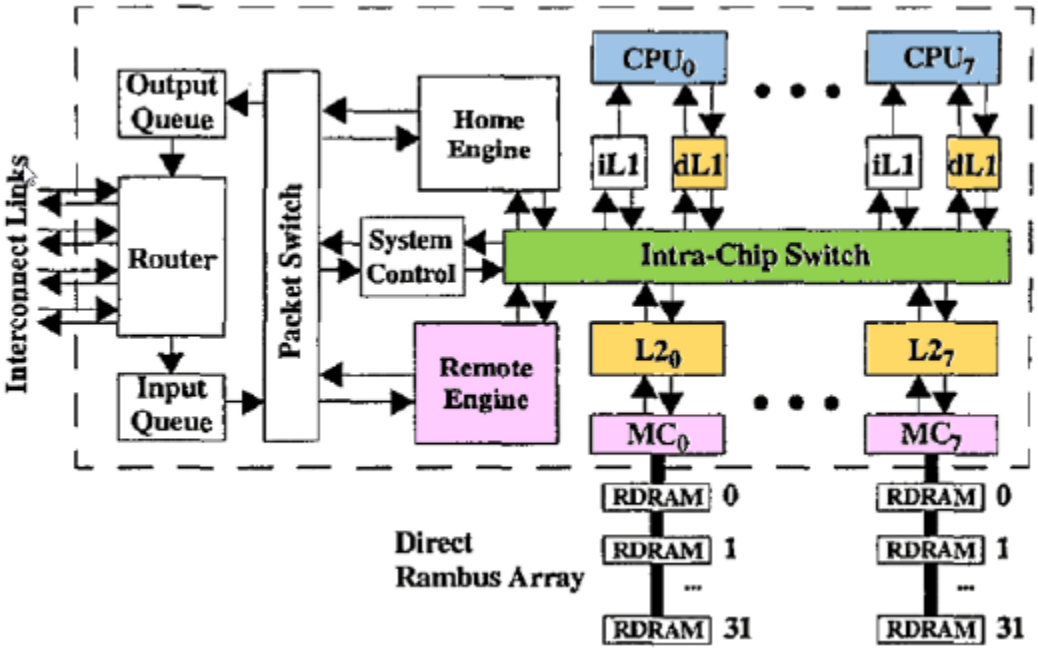
Thus, we find that Barroso was a printed publication at the time of the claimed invention.

(c) Overview of Alpha Manual

Alpha Manual is a reference manual describing the architecture of the Alpha processor. Ex. 1020, Preface to the First Edition. Intel cites Alpha Manual mainly with respect to limitation 3[a] and corresponding limitations in other claims, as we discuss below. *See infra* part III.C.2(b). PACT does not challenge Intel's contentions regarding Alpha Manual.

2. Independent claim 3

To illustrate its contentions regarding claim 3, Intel provides a colorized version of Barroso's Figure 1, which we reproduce below:



Pet. 30. Intel's colorized version of Figure 1, above, uses the following colors to identify the portions of the figure that Intel regards as elements of claim 3, as follows: blue for "data processing elements" (3[a]) CPU_0–CPU_7; yellow for "memory elements" (3[b]) dL1 and $L2_0$–$L2_7$; pink for "at least one interface element" (3[c]) MC_0–MC_7 and Remote Engine; and green for "bus system" (3[d]) including Intra-Chip Switch. Pet. 20–30.

(a) Preamble

Intel states that in the co-pending litigation, "[t]he parties have stipulated that the preamble is not limiting." Pet. 19 (citing Ex. 1014); *see also id.* at 5. PACT does not dispute that characterization. In any event, Barroso clearly describes a single-chip system with multiple processors. *See* Ex. 1005, Fig. 1. Since the matter is not in dispute, and is not material to our decision, we do not need to decide whether the preamble is limiting. *See Nidec*, 868 F.3d at 1017.

(b) Limitation 3[a]

Limitation 3[a] recites "a plurality of data processing elements that each includes at least one arithmetic-logic unit (ALU) and a plurality of registers adapted for storing data." Ex. 1003, 32:35–37. Intel argues that Barroso teaches this limitation, because each of the single-chip processing nodes in the Piranha system contains a plurality of data processing elements, which Intel identifies as CPU_0–CPU_7 in Barroso's Figure 1 (blue in Intel's colorized Figure 1, *supra* part III.C.2). Pet. 19–20 (citing Ex. 1005, 282–83, 282, 291, Figs. 1, 9). According to Intel, each of the Alpha CPUs includes five ALUs. *Id.* at 21 (citing Ex. 1005, 284).

Intel cites Alpha Manual as evidence that each of the Alpha CPUs in Barroso contains "a plurality of registers adapted for storing data." Pet. 21 (citing Ex. 1020, 1-1, 1-4, 1-6, 3-1–3-4, 5-10; Ex. 1001 ¶ 93). Intel argues that "Barroso expressly cites the Alpha Manual when describing Piranha's use of the Alpha processing core," so a person of ordinary skill in the art "would have looked to the Alpha Manual to better understand the Alpha processor core's structure and functionality." *Id.* at 22. According to Intel, "implement[ing] Barroso's processor cores using a plurality of data-storing registers, as disclosed by the Alpha Manual . . . would have taken advantage of the full processing capabilities of Barroso's Alpha processor cores, and would have further provided for low-latency mechanisms for storing data for manipulation during data processing." *Id.* at 23–24 (citing Ex. 1001 ¶ 99).

PACT does not contest Intel's contentions about limitation 3[a]. For the reasons given in the Petition, we find Intel's uncontested arguments persuasive in showing that Barroso discloses or teaches limitation 3[a] in light of the additional teachings of Alpha Manual.

(c) Limitation 3[b]

Limitation 3[b] recites "a plurality of memory elements that each independently operates as a cache for caching data." Ex. 1003, 32:38–39. As these memory elements, Intel identifies level-one data caches dL1 and level-two caches $L2_0$–$L2_7$ of Barroso's Figure 1 (yellow in Intel's colorized Figure 1, *supra* part III.C.2). Pet. 24. According to Intel, Barroso "discloses that each memory element operates independently as a cache for caching data." *Id.*; *see also id.* at 24–25 (citing Ex. 1005, 283–85, Fig. 1; Ex. 1001 ¶ 102) (identifying examples in Barroso where, according to Intel, the caches operate independently).

PACT does not contest Intel's arguments about limitation 3[b]. For the reasons given in the Petition, we find Intel's uncontested arguments persuasive in showing that Barroso discloses limitation 3[b].

(d) Limitation 3[c]

Limitation 3[c] recites "at least one interface element for providing a connection to a common higher level memory." Ex. 1003, 32:40–41. As relevant to PACT's arguments regarding this limitation, we also note that limitation 3[d] (which we discuss in more detail below, *infra* part III.C.2(e)) requires that the interface elements are interconnected to cache memory "via a bus system for transferring data." *Id.* at 32:43–45.

In its Petition, Intel argues that Barroso discloses limitation 3[c], and identifies memory controllers MC_0–MC_7 and the Remote Engine in Barroso's Figure 1 (pink in Intel's colorized Figure 1, *supra* part III.C.2) as the "at least one interface element." Pet. 25–28 (citing Ex. 1005, 283–84, Fig. 1; Ex. 1001 ¶¶ 105–106). According to Intel, the memory controllers interface to "common higher level memory" because "requests from any core can be routed to any memory controller," and the RDRAM memory "represents a third level in the memory hierarchy (after L1 and L2)." *Id.* at 26–27 (citing Ex. 1005, 285; Ex. 1001 ¶¶ 105–106). Intel argues that the Remote Engine connects to common higher level memory by interfacing with shared memory on other Piranha chips. *Id.* at 27–28 (citing Ex. 1005, 284–86, Fig. 3; Ex. 1001 ¶ 107).

In its Response, PACT first argues that Barroso's memory controllers MC_0–MC_7 "lack the necessary connections to the claimed 'bus system.'" PO Resp. 30. PACT argues that the "connection to a common higher level memory," recited in limitation 3[c] must take place through the recited "bus

system" of limitation 3[d]. *Id.* But according to PACT, "Barroso's memory controllers are not connected to the ICS, which [Intel] identifies as the 'bus system' . . . ; they are connected to a respective L2 cache." *Id.* at 31 (citing Ex. 1005, Fig. 1; Ex. 2026 ¶ 61).

In its Reply, Intel counters that claim 3 "does not require a direct connection" to the common higher level memory, but even if it did, the bus system as Intel identifies it (which includes not just the ICS but other connections between components in Barroso's Figure 1) directly connects to memory controllers MC_0–MC_7. *See* Pet. Reply 15 (citing Ex. 1005, Fig. 1; Ex. 1001 ¶ 111); *see also id.* at 17 (citing Ex. 1049, 59:12–19[10]) (arguing that Dr. Wolfe admitted on cross-examination that "use of the term 'connection' allows for 'intervening elements'").

In its Sur-reply, PACT cites Dr. Wolfe's testimony to the effect that a person of ordinary skill in the art "would not consider the separate connections between Barroso's caches and their respective memory controllers to be part of a single bus system with the ICS." PO Sur-reply 12 (citing Ex. 2026 ¶ 46).

We find Intel's argument persuasive, and we disagree with PACT that Barroso's memory controllers MC_0–MC_7 lack a sufficient connection to Barroso's bus system. Claim 3 requires a connection "via a bus system for transferring data at least between . . . at least one of the memory elements and the at least one interface element," the interface element having the function of "providing a connection to a common higher level memory." *See* Ex. 1003, 32:14–19, 32:21–22. But claim 3 does not require a *direct*

[10] The cited lines appear to be incorrect, and apparently should be 65:2–9.

connection. *See id.* We find Dr. Mazumder's opinion that an ordinarily skilled artisan "would have understood that the [ICS], together with direct connections between elements, comprise the claimed 'bus system,'" Ex. 1001 ¶ 111, more credible than Dr. Wolfe's opinion to the contrary, Ex. 2026 ¶ 46, because as we discuss below in the context of the global interconnection system recited in limitation 9[d], there is nothing in claim 3 that requires connections through the bus system to be *direct* connections. *See infra* part III.C.4(a).

PACT also argues, in its Response, that Barroso's Remote Engine is, "at best, . . . an interface to other chips in the system," rather than an interface to "common higher level memory." PO Resp. 31 (citing Ex. 1005, 286; Ex. 2026 ¶ 60). According to PACT, memory controllers on the *other* Piranha chips perform the function of accessing the other chips' higher level memories. *Id.* (citing Ex. 2026 ¶ 60).

In its Reply, Intel counters that Barroso "expressly discloses that 'the *remote engine* imports memory whose home is remote,' i.e., it provides a connection to off-chip memory." Pet. Reply 16 (quoting Ex. 1005, 285–86). According to Intel, "[t]his memory is common because it is 'shared' between multiple CPUS and chips," and "it is higher level because, as even Dr. Wolfe admits, it is at a higher level than Barroso's caches." *Id.* at 6 & n.5 (citing Ex. 1005, 283, 285; Ex. 1049, 50:15–19, 58:22–59:5, 60:2–5; Ex. 1001 ¶¶ 107–109; Ex. 2026 ¶ 61).

In its Sur-reply, PACT argues that "[t]he mere fact that other chips in the system have their own respective memories does not lend itself to the conclusion that these memories are accessed through Barroso's remote engine." PO Sur-reply 13. For example, PACT contends that "Barroso's

remote engine may access data from other chips without ever accessing those chips' higher level memories . . . if the requested data is stored in the remote chip's caches." *Id.* Citing Dr. Wolfe, PACT argues that "Barroso's Remote Engine merely provides access to a protocol engine on another chip, enabling sharing of data—not sharing of memory." *Id.* (citing Ex. 1049, 60:2–5; Ex. 2026 ¶ 60).

Having considered the arguments and evidence, we find Intel's arguments persuasive. We also disagree with PACT's argument that claim 3 requires that any connection between the interface element and the common higher level memory take place over the "bus system" recited in limitation 3[d]. Limitation 3[d] requires an interconnection through the bus system between the interface element and the *cache* memory, but does not require a similar connection to the *common higher level* memory. *See* Ex. 1003, 32:16–19, 32:21–22.

We also disagree with PACT that "providing a connection to a common higher level memory," as recited in limitation 3[c], requires an unmediated connection, or an ownership relation, to memory on another chip. Rather, we find persuasive Intel's argument that Barroso meets this limitation because the Remote Engine (the "interface element") has a data path to access memory on Barroso's remote chips. Also, in the context of claim 3, we find no meaningful distinction between "sharing of memory" and "sharing of data" stored in the memory, because the '807 patent makes no such distinction in this context. *See, e.g.*, Ex. 1003, 26:59–62 (stating that Figure 8 of the '807 patent shows a connection structure "to external (main) memories and/or *other . . . data streams*" (emphasis added)); *see also id.* at 32:44–45, 32:47–48 (limitation 3[d], requiring that cache memory is

"interconnected via a bus system for *transferring data* . . . between . . . at least one of the memory elements and the at least one interface element" (emphasis added)).

And although the data stream to or from the common higher level memory in another chip may have been cached, or may pass through a protocol engine, we disagree that these interposing structures mean that there is no "connection" as recited in limitation 3[c]. Ultimately, there is a connection to the remote memory via the cache or the protocol engine. *See, e.g.*, Ex. 1003, Fig. 8 (showing an example, in the '807 patent, of protocol converters 0802 interposed between interface modules (via global bus 0801) and external memories), Fig. 10 (same).

Thus, we find that Intel has shown persuasively that Barroso discloses limitation 3[c].

(e) Limitation 3[d]

Limitation 3[d] recites

> wherein each of the data processing elements, each of the memory elements, and each of the at least one interface element are *interconnected via a bus system* for transferring data at least between (i) at least one of the data processing elements and at least one of the memory elements and (ii) at least one of the memory elements and the at least one interface element

Ex. 1003, 32:42–48 (emphasis added). Intel argues that Barroso's intra-chip switch (ICS) (green in Intel's colorized Figure 1, *supra* part III.C.2), in combination with all the connections between elements (i.e., the connections shown as arrows in Barroso's Figure 2), is the recited bus system, and that it interconnects the processing elements, memory elements, and interface elements. Pet. 28–29 (citing Ex. 1005, 283–84; Ex. 1001 ¶¶ 108–117). Intel

also explains how it believes Barroso's ICS is arranged to transfer data between the three elements as recited in limitation 3[d]. *Id.* at 30–32 (citing Ex. 1005, 283–85, Fig. 1; Ex. 1001 ¶¶ 112–116).

In its Response, PACT first argues that Intel "does not cite any disclosure in Barroso that describes the ICS—alone or in combination with connections between other elements—as a bus system. At best, Barroso describes that [the] ICS is '[c]onceptually' a 'crossbar.'" PO Resp. 16 (alteration in original) (quoting Ex. 1005, 284); PO Sur-reply 3. Thus, according to PACT, Barroso's ICS "does not necessarily bear any similarity to Figure 8 of the '807 patent in implementation." PO Resp. 19 (citing Ex. 1005, 284). Moreover, PACT cites Dr. Wolfe as testifying that "switches may be used in many different applications, and not every switch is a bus system." *Id.* (citing Ex. 2026 ¶ 49)

But according to PACT, "[n]either the Petition nor the expert declaration provides any explanation as to why Barroso's ICS would constitute a 'bus system,' or why one of ordinary skill would view Barroso's ICS *combined with* separate direct connections between elements as a single bus system." PO Resp. 17 (citing *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9 at 13–14 (Oct. 16, 2018) (informative)); PO Sur-reply 3. PACT argues that Dr. Mazumder's testimony on this issue is conclusory, and that during cross-examination he provided no further explanation on how Barroso's ICS is implemented, and was allegedly evasive when counsel asked him questions attempting to distinguish Barroso's ICS from a bus. PO Resp. 17–19 (citing Ex. 1001 ¶ 111; Ex. 2028, 71:3–73:19, 74:15–76:2, 82:8–96:19; Ex. 37 C.F.R. § 42.65(a); *10X Genomics*, IPR2015-01157, Paper 30).

PACT also argues that "Barroso itself distinguishes its ICS from a bus, explaining that the Piranha chips disclosed therein have 'a high-speed switch *instead of* a bus to connect the on-chip cores.'" PO Resp. 17 (quoting Ex. 1005, 291) (citing Ex. 2026 ¶¶ 48–49); PO Sur-reply 4. And according to PACT, "[t]he references cited on the face of the '807 patent similarly indicate that bus systems and crossbar systems are not the same." PO Resp. 17 (citing Ex. 2012 ("Bauman"[11]), 2:24–67).

In its Reply, Intel counters that, "as Dr. Wolfe admits, a 'bus system' includes a '*plurality of busses* whether or not switches are also included.'" Pet. Reply 3 (quoting Ex. 2026 ¶ 49). According to Intel, "[n]o reasonable dispute exists that Barroso discloses a plurality of buses," and Barroso's ICS is implemented as "a set of eight internal datapaths." *Id.* (quoting Ex. 1005, 284–85). Intel contends that "Dr. Wolfe admitted [that] a bus is just a wire, *i.e.*, a datapath." *Id.* (citing Ex. 1049, 16:13–18 (Dr. Wolfe stating that in the context of the '807 patent, a bus "would generally be one or more wires that are capable of communicating data from one place to another such that there are multiple potential sources of that data"); Ex. 2028, 87:2–19 (Dr. Mazumder's cross-examination testimony equating a datapath with a "data bus")). Thus, according to Intel, since Barroso's ICS contains datapaths, as do the connections from the various components to the ICS, these are all buses which, together, constitute the bus system of Barroso's Piranha chip. *See id.* (citing Ex. 1005, 283; Ex. 2028, 75:8–17; Ex. 1001 ¶ 111).

Intel also argues that "a crossbar was a well-understood type of bus system by 2001, as evidenced by an IEEE article that Dr. Wolfe wrote in

[11] Bauman, US 6,480,927 B1 (issued Nov. 12, 2002) (Ex. 2012).

1996, stating that "[a]ll basic crossbar designs rely on switching signals from horizontal input busses to vertical output busses. In the simplest scheme, a single transmission gate connects the horizontal and vertical busses." Pet. Reply 3–4 (alteration in original) (emphasis omitted) (quoting Ex. 1048, 46) (citing Ex. 1051, 171:15–172:6). According to Intel, Dr. Wolfe admitted that the switching structure in Figure 8 of the '087 patent has all the elements of a crossbar as Dr. Wolfe described it in his article. *See id.* at 4–5 (citing Ex. 1049, 17:17–19:8; Ex. 1003, 26:59–27:4, Fig. 8).

Intel also disagrees with PACT that Barroso distinguishes its ICS from a bus by stating that the Piranha chip uses "a high speed switch instead of a bus to connect the on-chip cores" (Ex. 1005, 291), because the claims require a bus *system*, not just a single bus. Pet. Reply 5. According to Intel, Barroso's "ICS is not a single bus, but a crossbar comprising a set of buses." *Id.*

In its Sur-reply, PACT argues that Intel's additional explanation of why Barroso's ICS is part of a bus system is untimely. PO Sur-reply 3–4 (citing *Ariosa Diagnostics v. Verinata Health Inc.*, 805 F.3d 1359, 1367 (Fed. Cir. 2015); 37 C.F.R. §§ 42.104(b)(5), 42.23(b)). PACT also contends that "Barroso does not disclose that its ICS is a conventional crossbar, and the Petition does not propos[e] modifying Barroso to replace the ICS with a conventional crossbar." PACT clarifies that it "does not contend that a crossbar can *never* be a bus system—only that [Intel] has not shown that Barroso's ICS is a bus system—or even a crossbar." *Id.* at 4. As to the nature of a crossbar, PACT also points out that Dr. Wolfe testified, on cross-examination, that the statement in his 1996 article, about the components of a crossbar design, was incorrect. *Id.* at 4–5 n.1 (citing Ex. 1049, 22:3–22).

Having considered the arguments and evidence, we find Intel's arguments persuasive in showing that Barroso discloses limitation 3[d]. First, although Barroso does not describe its ICS in great detail, and thus neither did Intel in its Petition or Dr. Mazumder in his testimony, we agree with Intel that Barroso describes the ICS well enough that a person of ordinary skill in the art would have understood that it is part of a bus system.[12] Barroso's statement that the ICS is "[c]onceptually . . . a crossbar that interconnects most of the modules on a Piranha chip" (Ex. 1005, 284) indicates that it at the very least *functions* the way that a person of ordinary skill in the art would have understood a crossbar to function. Whether this means it is a "conventional" crossbar or some modified crossbar or similar switching structure, it still "interconnects . . . modules on a Piranha chip," it is involved in "data transfer," and it has "two independent 64-bit datapaths . . . for sending and receiving data" and "eight internal datapaths." *Id.* at 285–85. It is also a "high-speed switch." *Id.* at 291. Thus, we do not agree with PACT's argument that Intel would need to show that the ICS is, precisely, a conventional crossbar or that it has the same structure as the switch illustrated in Figure 8 of the '807 patent.

[12] We disagree with PACT's argument (PO Sur-reply 3–4) that Intel's additional arguments about limitation 1[d], made in its Reply, are untimely. Like Intel's Reply, its Petition argued that Barroso's ICS is part of the "bus system" recited in limitation 3[d], and the Reply simply responds to PACT's arguments to the contrary. *See Anacor Pharm., Inc. v. Iancu*, 889 F.3d 1372, 1380–81 (Fed. Cir. 2018) ("[T]he petitioner in an inter partes review proceeding may introduce new evidence after the petition stage if the evidence is a legitimate reply to evidence introduced by the patent owner . . . .").

We also disagree with PACT's argument that Barroso distinguishes its ICS (a "high-speed switch") from a "bus," and do not credit Dr. Wolfe's testimony supporting that argument. PO Resp. 17. Rather, we find more persuasive Intel's explanation, and supporting testimony by Dr. Mazumder, that there is a difference between a "bus" and a "bus system," and that Barroso only distinguished the latter. Pet. Reply 5; Ex. 1050 ¶ 4 (Dr. Mazumder's supporting testimony). And although we find Dr. Wolfe's testimony persuasive that "not every switch is a bus system" in every context (Ex. 2026 ¶ 26), in this case we agree with Intel that Barroso's ICS is both a switch and part of a bus system which, itself, comprises a set of buses. Pet. Reply 5.

This is consistent with Dr. Wolfe's admission, which we find credible, that a bus system can include a "plurality of busses whether or not switches are also included." Ex. 2026 ¶ 49. It is also consistent with the statements in Dr. Wolfe's 1996 article that a "basic crossbar design" relies on "switching signals from horizontal input busses to vertical output busses." Ex. 1048, 46.[13] So, at the very least, the evidence of record shows that Barroso's ICS comprises buses and is part of a bus system.

We also take into consideration the similarity between Barroso's ICS, which functions as a crossbar, and the crossbar structure in Figure 8 of the '087 patent, which is described as a "bus system" and as a "preferred embodiment." Ex. 1003, 26:65–27:16. We disagree with PACT that Bauman (a reference cited in the '087 patent) distinguishes between a crossbar

[13] We do not credit Dr. Wolfe's statement on cross-examination, which he did not fully explain, that the statement in his 1996 article was false. Ex. 1049, 22:3–22.

system and a "bus system." PO Resp. 17. Rather, Bauman distinguishes between a "crossbar system" and "multiple buses" (with no mention of an included crossbar). Ex. 2021, 2:24–67. Nothing in Bauman is inconsistent with Intel's argument that a person of ordinary skill in the art would have understood that a crossbar structure such as in Figure 8 of the '807 patent, which switches data between horizontal and vertical buses, can be part of a "bus system" as recited in limitation 1[d]. Moreover, as Intel correctly states in its Reply, "Bauman does not override the '807 patent's disclosure of Figure 8" of a 'bus system' that is a crossbar." Pet. Reply 5.

Thus, we find that Intel has shown persuasively that Barroso discloses limitation 3[d].

(f) Limitation 3[e]

Limitation 3[e] recites "wherein the bus system is adapted for dynamically establishing and releasing transmission channels between a sending one of the elements and a receiving one of the elements." Ex. 1003, 32:49–52. Intel argues that Barroso discloses this limitation, and explains a rationale for how the ICS establishes and releases transmission channels between the connected elements. *See* Pet. 33.

PACT does not contest Intel's arguments about limitation 3[e]. For the reasons given in the Petition, we find Intel's uncontested arguments persuasive in showing that Barroso discloses limitation 3[e].

(g) Limitation 3[f]

Limitation 3[f] recites "wherein an identification token is assigned to transmitted data for indicating an affiliation of the transmitted data to a process." Ex. 1003, 32:53–55.

Intel argues that on each new transaction in Barroso's Piranha chip, "the protocol engine allocates an entry from the transaction state register file (TSRF) that represents the state of [the currently executing] thread (*e.g.*, addresses, program counter, timer, state variables, etc.)." Pet. 33–34 (alteration in original) (quoting Ex. 1005, 286). Thus, "a transaction address (the claimed 'identification token') is assigned to a response (the claimed 'transmitted data') for indicating an affiliation of the transmitted data to a thread (the claimed 'process')." *Id.* (citing Ex. 1001 ¶ 122). Intel also contends that "Barroso's transaction address is used in the same way as an application identification ("APID") described by the '807 patent and by the Applicant in the prosecution history." *Id.* (citing Ex. 1004, 538).

According to PACT's Response, Intel's argument ignores the '807 patent's discussion of "identifiers," which the applicant equated to an "identification token" during the prosecution history. PO Resp. 27 (citing Ex. 1004, 538). PACT argues that the '807 patent disclosure "repeatedly and consistently describes 'identifiers' as information assigned to data that is transmitted *in addition to* an address." *Id.* at 27–28 (citing Ex. 1003, 9:66–10:9, 22:39–41, 22:44–51, 28:8–33, 29:67–30:5); *see also id.* at 29–30 (citing *GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1370 (Fed. Cir. 2016) ("[W]hen a patent 'repeatedly and consistently' characterizes a claim term in a particular way, it is proper to construe the claim term in accordance with that characterization."). PACT disagrees that an identification token can refer merely to an address associated with the data transfer. *Id.* at 28 (citing Ex. 2026 ¶ 64).

PACT also argues that Barroso's transaction address "is included in a data transfer to indicate the memory location where the data is located, not

to indicate an affiliation of the data with a process" as recited in limitation 1[f]. PO Resp. 28–29 (citing Ex. 2026 ¶¶ 64–65). Thus, PACT disagrees that Barroso's transaction address is like the APIDs described in the '807 patent, which are transmitted *along with* the addresses.

In its Reply, Intel responds that "nothing in the claims precludes an identification token from being an address. Nor is there any evidence of disclaimer or disavowal of plain meaning." Pet. Reply 13–14 (citations omitted) (citing Ex. 1051, 109:25–110:20 (PACT's expert from a related *inter partes* review)). And Intel points to an example in which it argues that "the '807 patent equates addresses to identifiers." *Id.* at 14 (citing Ex. 1003, 28:8–11 ("Addresses (preferably identifiers, e.g., with IOIDs and/or APIDs) are transmitted . . . .")).

Intel also disagrees with PACT's argument that Barroso's transaction address is not "for indicating an affiliation of the transmitted data to a process" as recited in limitation 3[f], because PACT "does not dispute that the transaction address will be 'associated with a process' for purposes of accessing off-chip memory, which is sufficient to meet the claim." Pet. Reply 14 (citing PO Resp. 28–29; Ex. 2026 ¶ 65).

We find Intel's argument persuasive that Barosso's transaction address is "an identification token . . . for indicating an affiliation of the transmitted data to a process" as recited in limitation 3[f]. We disagree with PACT that being an address is incompatible with also being an "identification token" as recited in the claim, so long as it serves the function of "indicating an affiliation of the transmitted data to a process." Ex. 1003, 32:53–55. We find that Barroso's transaction address serves both functions, including the function of identifying a particular thread in Barroso's TSRF. *See* Ex. 1005,

286 ("A thread that is waiting for a response from a local or remote note has its TSRF entry set to a waiting state, and the incoming response is later matched with this entry based on the transaction address."). We also find persuasive Intel's argument that, in at least one example, the '807 patent refers to "identifiers" such as APIDs as "[a]ddresses." *See* Ex. 1003, 28:8–11.

Thus, we find that Intel has shown persuasively that Barroso discloses limitation 3[f].

(h) Conclusion for claim 3

For the above reasons, we find that Intel has shown persuasively that Barroso discloses or teaches each limitation of claim 3 in light of Alpha Manual. Intel has also shown a persuasive rationale for why a person of ordinary skill in the art would have combined the teachings of Barroso and Alpha Manual. Therefore, considering all of the evidence of record, we conclude Intel has shown by a preponderance of the evidence that claim 3 is unpatentable as obvious over Barroso in light of Alpha Manual.

3. Claim 4

Claim 4 is also independent, and has limitations essentially the same as those of claim 3, except for limitation 3[f]. *Compare* Ex. 1003, 32:56–33:10, *with id.* at 32:56–33:11. Whereas limitation 3[f] recites "wherein an identification token is assigned to transmitted data for indicating an affiliation of the transmitted data to a process," the corresponding limitation in claim 4 recites "wherein an identification token is assigned to data transferred via the interface element for indicating an affiliation of the transferred data to a process." *Id.* at 32:53–55, 33:8–10. Thus, claim 4 uses

the word "transferred" rather than "transmitted," and requires that the transfer take place "via the interface element."

Intel relies on the same arguments as for claim 3. Pet. 35. Intel also argues that in Barroso, "the transmitted data associated with a transaction includes 'data transferred via the interface element," the interface element in this case being Barroso's Remote Engine. Pet. 35–36 (citing Ex. 1005, 285–86; Ex. 1001 ¶ 126).

PACT does not contest Intel's specific contention regarding claim 4, and we find it persuasive. As discussed above, we also find Intel's arguments for claim 3 persuasive, and likewise, this these arguments and evidence are persuasive in the context of claim 4. *See supra* part III.C.2. Thus, we conclude that claim 4 is unpatentable as obvious over Barroso in light of Alpha Manual.

4. Claim 9

Independent claim 9 is generally similar to claim 3. *Compare* Ex. 1003, 34:4–35, *with id.* at 32:34–55. In the Petition, Intel numbers the limitations as 9[a]–9[h] and compares these limitations to the combination of Barroso and Alpha Manual in much the same way as with claim 3. *See* Pet. 36–48.

As Intel notes, the preamble of claim 9 and limitations 9[a]–[c] are the same as the preamble of claim 3 and limitations 3[a]–[c]. Pet. 36; *compare* Ex. 1003, 34:4–11, *with id.* at 32:34–41. We address the preamble and these limitations above in the context of claim 3, and we likewise find Intel's arguments persuasive in the context of claim 9. *See supra* parts III.C.2(a)–(d). We address limitations 9[d]–[h] below.

(a) Limitation 9[d]

Limitation 9[d] recites "at least one global interconnection system adapted for interconnecting the plurality of data processing elements, the plurality of memory elements, and the at least one interface element." Ex. 1003, 34:12–15. Intel contends that in Barroso, the "global interconnection system" includes the "ICS and the interconnections leading to the ICS." Pet. 38 (citing Ex. 1001 ¶ 131). According to Intel, the '807 patent describes a "global bus" as a bus that "permits communication with external components." *Id.* (citing Ex. 1003, 23:64–65 ("[T]he RAM-PAEs have dedicated connections to an external bus system (e.g., global bus) . . . ."), 24:44–46, 25:63–67). According to Intel, Barroso discloses such a global interconnection system because its "ICS is likewise adapted for communicating with external memory, such as shared memory across multiple Piranha chips' accessed through the 'Remote Engine,' or 'DRAM chips' accessed through the 'memory controller[s].'" *Id.* (alteration in original) (quoting Ex. 1005, 283).

In its Response, PACT argues that Intel "offers no explanation as to how Barroso's ICS is a global interconnect system," because "Barroso's ICS . . . does not provide *direct* access to external memory or peripherals, which are accessed via the memory controller or a separate I/O chip, respectively." PO Resp. 20–21 (emphasis added) (citing Ex. 1003, 25:63–67; Ex. 1005, 283–84; Ex. 2026 ¶ 52). And according to PACT, Barroso's ICS "is not an external bus system, as it resides internal to a single Piranha chip and solely interconnects internal components such as the L1 caches, L2 caches, and protocol engines." *Id.* (citing Ex. 1003, 23:64–65; Ex. 1005, 284, Fig. 1; Ex. 2026 ¶ 53). PACT also contends that "the '807 patent consistently

distinguishes between internal bus systems and the 'global bus' or 'GlobalTrack,' and indicates that these are separate interconnects between different elements." *Id.* at 24.

In its Reply, Intel argues that claim 9 "recite[s] '[a] multi-processor system on a chip, comprising . . . ,' permitting the global interconnection system to be internal to the chip; and . . . do[es] not require direct connections." Pet. Reply 6 (second and third alterations and omissions in original). Intel also contends that "claim 9 expressly permits the 'global interconnection system' to connect *indirectly* to external components *through* an 'interface element.'" *Id.* (citing Ex. 1003, 34:32–35). Intel contends that "Barroso's ICS is part of a 'global interconnection system' because it is adapted for communicating with (1) external memory through interface elements—the 'Remote Engine (RE)' or 'memory controller[s] (MC)' and, (2) external components, also through the [Remote Engine], which Dr. Wolfe admits 'provide[s] an interface to . . . I/O chips.'" *Id.* (alterations in original) (citation omitted) (citing Pet. 37–38; Ex. 1005, 283; Ex. 2026 ¶ 59; Ex. 1005, 284).

To the extent that the '807 patent describes *direct* connections or connections to *external* components, Intel characterizes these as non-limiting examples or embodiments. Pet. Reply 6–7 (citing Ex. 1003, 25:63–67, 23:53–67; *Dealtrack, Inc. v. Huber*, 674 F.3d 1315, 1327 (Fed. Cir. 2012)). Intel also points to a passage in the '807 patent defining the word "external" to include components of a "system on a chip" that are on the chip, but "outside of the VPU architecture." *Id.* at 7 n.1 (citing Ex. 1003, 23:37–52).

In its Sur-reply, PACT concedes that a global interconnect system "can be internal to the chip," but argues that it must "allow[] the processing

elements on the chip to communicate with other elements external to the chip, such as external memory and peripheral units." PO Sur-reply 6 (citing Ex. 1003, 25:63–67). PACT also argues that "[t]he issue is not whether the global bus or global interconnect uses an interface to provide access to external components—rather, it is whether that interface provides direct access to the external components." *Id.* According to PACT, "Barroso's ICS does not provide any such direct communication with global or external components. Instead, access to external components must pass through a series of components and transactions, including a packet switch, a queue, a router, and external interconnect links." *Id.* at 6–7 (citing Ex. 1003, 25:63–67; Ex. 1005, 284, Fig. 2; Ex. 2026 ¶¶ 52–53).

Considering the evidence presented by both sides, we find Intel's arguments persuasive. The "global interconnection system" in claim 9 plays the same role, and has the same meaning in claim 9 as the "bus system" in claim 3, except that it is explicitly "global." But we find that Intel has persuasively shown that Barroso's bus system is global, because it can access remote memory on other Piranha chips through its Remote Engine.

While Barroso's ICS does not *directly* connect to external components, we disagree with PACT that claim 9 requires a direct connection. The '807 patent describes the "global interconnection system" of claim 9 (e.g., a "GlobalTrack"), as a "bus system." *E.g.*, Ex. 1003, 23:65, 24:45–46, 26:4–6, 26:32–34. Like the "bus system" recited in claim 3, the global bus system of claim 9 may have multiple interposing elements. For example, as Intel persuasively argues, limitation 9[h] requires that the global interconnect system connects with an external peripheral *indirectly*, through an interface element. *See* Pet. Reply 6; Ex. 1003, 34:32–35. Figure 8 of the

'807 patent also describes a "dedicated global bus" (0801) connecting to external peripherals through a crossbar switch (0804a, 0804b, 0805), protocol converters (0802), and an internal bus system (0104). *See* Ex. 1003, 26:59–27:3, Fig. 8. We disagree with PACT that a connection through an interface element as recited in limitation 9[h], or through the interposing elements in the Figure 8 embodiment, are more "direct," in any relevant way, than a connection through a packet switch, a queue, a router, or external interconnect links.

We also disagree with PACT that Intel has not shown that Barroso's bus system is "global," because as Intel persuasively argues, Barroso's ICS accesses external, shared memory on other chips through its Remote Engine." *See* Pet. 38. We also find persuasive Intel's arguments that Barroso's global interconnection system includes "the interconnections leading to the ICS." *Id.* Even if these parts of the system are not, themselves, "global," that does not mean that the bus system, as a whole, is not a global interconnection system, via the Remote Engine.

Second, PACT argues that Intel's "identification of Barroso's ICS as *both* the claimed bus system (*e.g.*, in claim 3) *and* the claimed global interconnect system (e.g., in claim 9) ignores the express teachings of the '807 patent, which repeatedly describe the 'global bus' as a separate interconnect *in addition to* the bus system." PO Resp. 21–23 (citing Ex. 1003, 25:63–26:6, 31:59–65, Figs. 5, 15; Ex. 2026 ¶ 51).

In its Reply, Intel argues (1) that claim 9 "do[es] not require a 'bus system' in addition to the 'global interconnection system'"; (2) "the '807 specification indicates a 'global bus' is part of a 'bus system'"; and (3) "Dr. Wolfe admitted that 'the global interconnection system can be a bus

system.'" Pet. Reply 7 (citing Ex. 1003, 26:28–34, 25:67–26:6; Ex. 1049, 27:10–12).

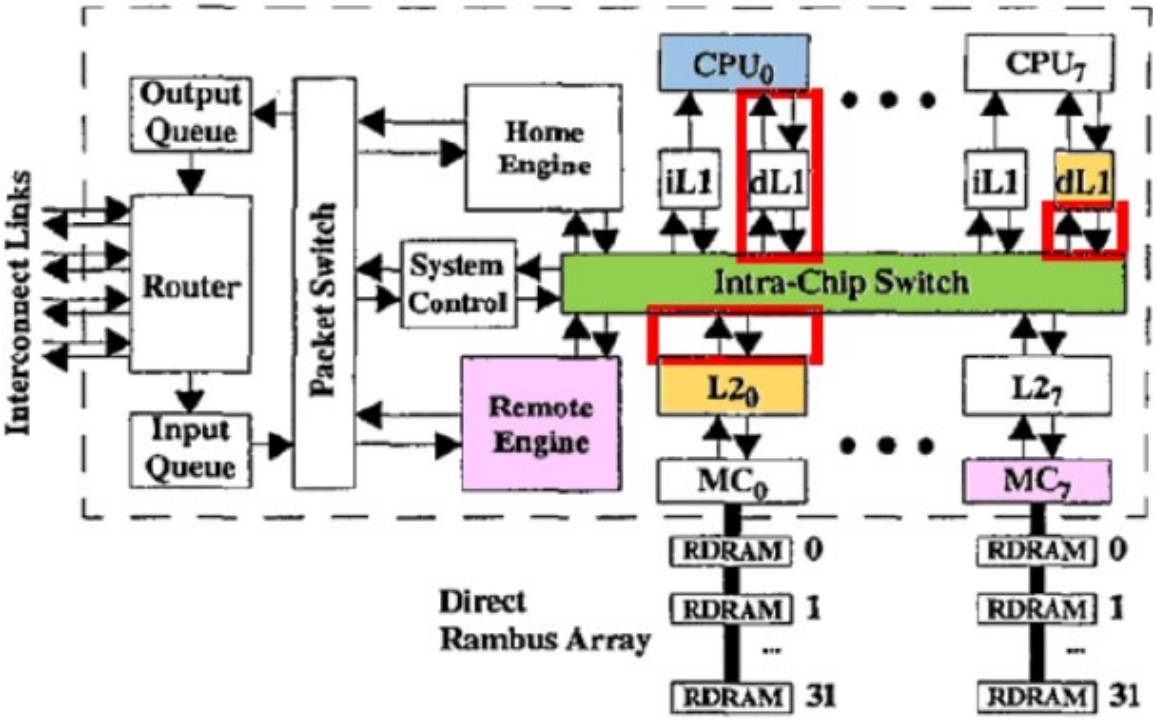
We find Intel's arguments persuasive that claim 9 does not require any bus system other than the recited "global interconnection system." Although the '807 patent describes embodiments in which it refers to the global bus separately from an internal bus, we agree with Intel that claim 9 does not require two distinct bus systems, or that its bus system be explicitly divisible into global and local parts. *See Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1346–47 (Fed. Cir. 2015) (cautioning against "limiting the claimed invention to preferred embodiments or specific examples in the specification." (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1328 (Fed. Cir. 2002)).

(b) Limitation 9[e]

Limitation 9[e] requires that "the at least one global interconnection system is accessible by each of the data processing elements and memory elements via a respective dedicated bus interface node, and permits flexible allocation and interconnection during run time." *Id.* at 34:16–20.

We address Intel's arguments that Barroso discloses a "global interconnection system" above. *See supra* part III.C.4(a). Intel argues that Barroso's bus system permits flexible allocation and interconnection during run time because the "ICS is implemented by using a set of eight internal datapaths that run along the center of the Piranha chip," which flexibly allows various modules to initiate connections for data transfer at run time. Pet. 39–40 (citing Ex. 1005, 284–85; Ex. 1001 ¶ 134). PACT does not contest this argument.

As to the requirement that the global interconnection system "is accessible by each of the data processing elements and memory elements by a respective dedicated bus interface node," Intel provides an annotated version of Barroso's Figure 1, which we reproduce below:



Pet. 39. Figure 1, above, is the same as the colorized version of Figure 1 that we reproduce above in our discussion of claim 3 (*supra* part III.C.2), except that it contains red boxes indicating alleged "dedicated bus interface nodes" connecting (1) the ICS with CPU_0 via its cache dL1; (2) the ICS directly to the dL1 cache for CPU_7; and (3) the ICS with level-two cache $L2_0$. *See* Pet. 39. According to Intel, "the ports for CPU_0 are not shared with any other CPUs, and the ports for dL1 of CPU_7 and $L2_0$ are similarly not shared." *Id.* (citing Ex. 1001 ¶ 133).

In its Response, PACT argues that Intel "appears to selectively identify some of Barroso's CPUs as processing elements (but not others),

and to selectively identify some of Barroso's L1 caches as memory elements (but not others)." PO Resp. 26. Also, according to PACT, Intel "contends that the L1 cache for CPU2 has a 'dedicated connection to the ICS (disregarding the CPU that is attached to the cache)." *Id.* But PACT disagrees that Intel can "plausibly contend that for Barroso's eight identical CPUs with identical data caches, the connection to the ICS is sometimes a 'dedicated' connection to the CPU, but other times a 'dedicated' connection to the cache." *Id.*

In its Reply, Intel counters that each of the identified ports "is 'dedicated'—it is permanently pre-assigned to the component(s) connected to that port. The ports are not arbitrated at transaction time." Pet. Reply 12 (citing Ex. 1005, 284). According to Intel, "nothing in the claims precludes a bus interface node from being dedicated to multiple components. And, regardless, each CPU has its own bus interface to its L1 cache—which is an interface to the global interconnection system." *Id.* at 13. Intel also notes in the context of limitation 9[g] (which we discuss below, *infra* part III.C.4(d)) that Barroso's Figure 1 discloses a plurality of connections to the CPUs and a separate plurality of connections to the level 2 caches, so its argument does not hinge on whether the L1 caches have their own dedicated bus interface nodes independently of the CPUs. *See* Pet. Reply 8–10; *id.* at 13 (referring to Intel's arguments regarding limitation 9[g]).

In its Sur-reply, PACT notes that the claim language requires there to be a "*respective* dedicated bus interface node," where the word "'[r]espective' indicates that each data processing element and each memory

element has its own dedicated bus interface node, not that multiple elements can share a single bus interface node." PO Sur-reply 12.[14]

We agree with Intel that a bus interface node is "dedicated" if it is permanently pre-assigned to the component. PACT does not dispute that interpretation in its Sur-reply, and it reflects the ordinary and customary meaning of that term. It is also consistent with the use of the word "dedicated" in the '087 patent. *See, e.g.*, Ex. 1003, 26:28–29. Thus, we find Intel's argument persuasive that a plurality of data processing elements (i.e., the CPUs) and a plurality of memory elements (e.g., the L2 caches) have dedicated bus interface nodes to Barroso's ICS, in the sense that these nodes are permanently assigned to the components. We find this persuasive, even though the bus interface nodes corresponding to the CPUs connect to the CPUs via the L1 caches. Claim 9 requires the dedicated bus interface nodes to be *respective*, but there is no requirement in claim 9 that the interface nodes are *direct* connections without an interposing cache.

That Intel's contention does not include all the processing elements and all the memory elements in Barroso's Figure 1 does not matter, because as Intel correctly argues in the context of the "separately connected" limitation 9[g], claim 9 only requires a *plurality* of processing elements and a *plurality* of memory elements. It does not necessarily require that the limitations apply to *all* processing elements and *all* memory elements in the

[14] PACT also contends that Intel's argument in the Reply is untimely because it represents an abandonment of Intel's original theory. PO Sur-reply 11. We disagree. Intel's argument is a reply to PACT's argument in its Response, providing further explanation for Intel's original position that the interfaces it identified in its annotated version of Barroso's Figure 1 (marked in red) are dedicated bus interface nodes.

claimed multi-processor system. Pet. Reply 8 (citing Ex. 1001 ¶¶ 132, 140–141).

We also find persuasive Intel's argument that the portions of Barroso's bus system directly connecting the CPUs to their respective dL1 caches each constitutes a respective dedicated bus interface node, accessible by the global interconnection system. In its Sur-reply, PACT argues that this argument is untimely, and that it "fails because the connections between the CPUs and the L1 caches are still shared by both elements." PO Sur-reply 12 n.5. We disagree that the argument is untimely, because this is one of the two ports that Intel identified (by a red box in its annotated version of Barroso's Figure 1) as comprising the bus interface node corresponding to CPU_0. *See* Pet. 39. We also disagree that the argument fails because this port is shared between CPU_0 and its corresponding dL1, because Intel does not need to rely on the dL1 caches to find a plurality of memory elements meeting limitation 9[e].

For the above reasons, including our additional discussion, below, regarding limitation 9[g] (*infra* part III.C.4(d)), we find that Intel has shown persuasively that Barroso discloses limitation 9[e].

(c) Limitation 9[f]

Limitation 9[f] recites "transmitters and receivers of the data processing, memory and interface elements are adapted for being connected via the global interconnection system in an addressed manner to permit individual data transfer." Ex. 1003, 34:21–24.

Intel contends that Barroso discloses this limitation because the "processor cores, first level caches, second level caches, memory controllers, and Remote Engine all individually" transmit and receive data, as recited in

limitation 9[f]. Pet. 40–42 (citing Ex. 1005, 283–85, 287–88, Fig. 1; Ex. 1001 ¶ 137).

Other than its contention that Barroso does not disclose a "global interconnection system," which we address above (*supra* part III.C.4(a)), PACT does not contest Intel's specific arguments about limitation 9[f]. For the reasons given in the Petition, we find Intel's uncontested arguments persuasive that Barroso discloses limitation 9[f].

(d) Limitation 9[g]

Limitation 9[g] requires that

> each of the data processing elements, memory elements, and at least one interface element are *separately connected to the global interconnection system* for transferring data between (i) at least one of the data processing elements and at least one of the memory elements, and (ii) at least one of the memory elements and the at least one interface element.

Ex. 1003, 34:25–31 (emphasis added).

Limitation 9[g] is similar to limitation 3[d], except that the global interconnection system must be "separately connected" to each of the data processing, memory, and interface elements. *Compare id.*, *with* Ex. 1003, 32:42–48. Other than for this limitation, Intel's arguments are essentially the same as for limitation 3[d], and we find Intel's arguments persuasive for the same reasons we find them persuasive in the context of claim 3. *Compare* Pet. 42–45, *with* Pet. 28–32; *see supra* part III.C.2(e).

For the "separately connected" issue, Intel argues that Barroso's ICS is separately connected to processors CPU_0–CPU_7, level-one caches dL1, level-two caches $L2_0$–$L2_7$, and memory controllers MC_0–MC_7 because there are separate connection paths to each of the components as shown by red

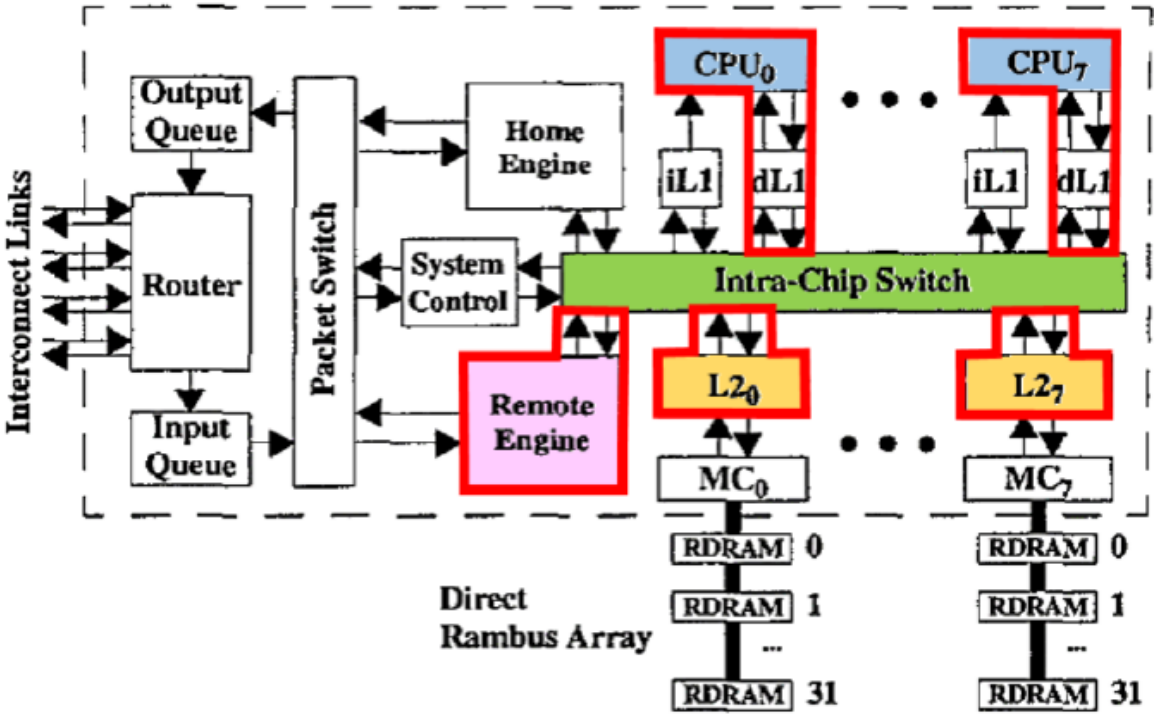
boxes in Intel's annotated version of Figure 1 (reproduced above in part III.C.4(b)).

PACT argues that Figure 1 "demonstrates the opposite is true." PO Resp. 25. According to PACT, CPU_0 (a processing unit) and dL2 (a memory element) are not connected to the ICS 'separately and independently' of each other—rather, as is clearly shown, CPU_0 is connected to the ICS through the same datapath as dL1." *Id.* (citing Ex. 2026 ¶ 56; Ex. 2028, 112:22–113:22). As with the "dedicated bus interface node" issue in limitation 9[e], addressed above in part III.C.4(b), PACT argues that Intel "appears to selectively identify some of Barroso's CPUs as processing elements (but not others), and to selectively identify some of Barroso's L1 caches as memory elements (but not others)." *Id.* at 26.

In its Reply, Intel points out that its contention is that "Barroso's 'global interconnection system' . . . include[s] the interconnections leading to the ICS. So Barroso's CPUs are, in fact, directly connected." Pet. Reply 7–8 (citation omitted). As we discuss above in the context of limitation 9[e], Intel points out that the claim language only requires that a *plurality* of data processing elements and *plurality* of memory elements are separately connected—not all of them in the system. *Id.* at 8 (citing Ex. 1001 ¶¶ 132, 140–141; *ResQNet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1382 (Fed. Cir. 2003) ("'[E]ach of a plurality of fields' means 'each of at least two fields.'")).

Intel also presents, in its Reply, a combination of elements in Barroso's Figure 1 that does not include any dL1 caches, and includes a plurality of connections to the CPUs and a separate plurality of connections

to the level 2 caches, as shown in a second annotated version of Figure 1, which we reproduce below:



Pet. Reply 9. Intel's second annotated Figure 1, above, is the same as Intel's colorized version of Figure 1 (*supra* part III.C.2), adding red boxes to indicate each alleged way in which components are "separately connected": (1) two connections between the ICS and each of CPU_0 and CPU_7 via their respective caches dL1; (2) two connections between the ICS and each of $L2_0$ and $L2_7$; and (3) one connection to the Remote Engine. *See id.* at 8–9 (citing Ex. 1005, Fig. 1; Ex. 1001 ¶ 139).

Intel argues that on cross-examination, "Dr. Wolfe admitted that Intel need only show *two* data processing elements, *two* memory elements, and *one* interface element separately connected to the ICS." Pet. Reply (citing Ex. 1049, 34:7–35:9). According to Intel, he also agreed that "$L2_0$ and $L2_7$ together are a plurality of memory elements," "CPU_0 and CPU_7 together are

a plurality of data processing elements," that the Remote Engine "is an interface element," and that Remote Engine, $L2_0$, and $L2_7$ are "separately connected to the ICS." *Id.* at 10 (citing Ex. 1049, 37:12–27, 38:10–39:2, 39:6–20).

In its Sur-reply, PACT argues that Barroso's CPUs cannot be "separately connected" from their respective dL1 caches, because they share a connection to the global interconnection system with their dL1 caches. PO Sur-reply 7–8.

PACT also argues that Intel's new argument in the Reply based on its second annotated version of Barroso's Figure 1, is untimely because it raises new claim construction issues. PO Sur-reply 8. And in any event, PACT disagrees that Intel only needs to show that two processing elements and two memory elements are separately connected, since the claim states that "*each of the* data processing elements, memory elements, and at least one interface element are separately connected." *Id.* at 9 (quoting Ex. 1003, 34:25–27). Thus, according to PACT, "while the claims only require at least two data processing elements and at least two memory elements, *all* of those data processing elements and memory elements must be separately connected." *Id.* PACT disagrees that Dr. Wolfe admitted to the contrary, because according to PACT, his testimony is consistent with PACT's position when taken in its proper context. *See id.*

We find Intel's arguments persuasive, and we disagree with PACT's proposed claim interpretation. While limitation 9[g] states that "*each of the* data processing elements [and] memory elements . . . are separately connected," Ex. 1003, 34:25–27, it uses the article "the," which refers to the antecedents "a plurality of data processing elements" and "a plurality of

memory elements" in limitations 9[a] and 9[b]. Since claim 9 is a "comprising" claim, each of these "pluralities" do not need to include every data processing element or every memory element in the multi-processor system. Thus, on its face, the claim language supports Intel's interpretation and does not support PACT's proposed interpretation.

We also do not agree with PACT that Intel's argument, in its Reply, is a new claim construction argument or is otherwise untimely. Intel's argument relies on the plain and ordinary meaning of claim 9, consistently with how Intel interpreted the claim in the Petition, and does not introduce any new evidence. Although Intel included a different combination of data processing elements and memory elements for its argument in the Reply (i.e., CPU_0, CPU_7, $L2_0$ and $L2_7$), the Petition *did* originally include a plurality of Barroso's CPUs and L2 caches (specifically, CPU_0, CPU_1, $L2_0$ and $L2_1$) as part of the pluralities of data processing and memory elements. *See* Pet. 36, 43. The selection of CPU_7 and $L2_7$ in the Reply, rather than CPU_1 and $L2_1$ in the Petition, is not a materially different argument, and is understandable given that Figure 1 does not explicitly show CPU_1 or $L2_1$. Barroso expresses no material difference between CPU_1, CPU_7, or $L2_1$ and $L2_7$. *See* Ex. 1005, 283–285.

For the above reasons, including our additional discussion above regarding 9[e] (*supra* part III.C.4(b)), we find that Intel has shown persuasively that Barroso discloses limitation 9[g].

(e) Limitation 9[h]

Limitation 9[h] recites, "wherein at least one interface element is adapted to connect to an external peripheral and the global interconnect

system is adapted to transfer data to and from said external peripheral." Ex. 1003, 34:32–35.

Intel argues that "it would have been obvious to use Barroso's Remote Engine to connect to input/output (I/O) devices, which a [person of ordinary skill in the art] would understand is [a] type of external peripheral," because Barroso discloses that Piranha I/O chips "interface to various I/O devices," as shown in Figure 3. Pet. 46 (quoting Ex. 1005, 284) (citing Ex. 1005, 284, Fig. 3; Ex. 1001 ¶ 144). Intel also contends that it would have been obvious that this connection would take place through the Remote Engine for handling input and the Home Engine for handling output, since there are only a finite number of devices on the processing chip, and "a [person of ordinary skill in the art] would have recognized that it would be obvious to try the protocol engines, including the Remote Engine, for importing and exporting information from an I/O device, as doing so would be an efficient way to leverage pre-existing, known functionality, with a reasonable expectation of success." Pet. 47–48 (citing Ex. 1005, 285–88; Ex. 1001 ¶ 146).

In response, PACT argues that Barroso's processor chip cannot connect to I/O devices (external peripherals) because "Barroso expressly teaches that a separate I/O chip is required for this task." PO Resp. 33 (citing Ex. 1005, 284 (stating that the Piranha processing chip "does not have any I/O capability"); Ex. 2026 ¶ 69). PACT also contends that Barroso's ICS "is designed to transfer data between internal components of a Piranha chip—not to and from external peripherals," and that "[o]ff-chip communications are performed using a separate point-to-point' interconnect between chips." *Id.* at 34 (citing Ex. 1005, 287; Ex. 2026 ¶ 70).

In its Reply, Intel argues that during cross-examination, Dr. Wolfe admitted that the "Remote Engine . . . provide[s] an interface to . . . I/O chips." Pet. Reply 17 (alterations in original) (quoting Ex. 2026 ¶ 59). Intel also argues that PACT's argument "ignores that the ICS connects to the Remote and Home Engines, whose purpose is to transfer data to or from external components." *Id.* at 18–19 (citing Ex. 1005, 283–87, Fig. 4; Ex. 1001 ¶ 145).

We find Intel's arguments persuasive that it would have been obvious to a person of ordinary skill in the art to use the Remote Engine and Home Engine on a Piranha processor chip to communicate with connected Piranha I/O chips. Barroso clearly discloses, and PACT does not dispute, that Barroso's separate I/O chips connect with external peripherals to send and receive information from them. *See* Ex. 1005, 284; PO Resp. 33 (acknowledging that the separate Piranha I/O chip is required for communicating with external peripherals). There is no explicit requirement in claim 9 that the interface element is adapted to connect *directly* to an external peripheral, and we find no such requirement in the '807 disclosure. *See* Ex. 1003, 34:33–35; Ex. 1050 ¶ 24 (Dr. Mazumder testifying that "[t]o the extent Dr. Wolfe is contending that the claims require a direct connection between the 'interface element' and 'external peripheral,' I disagree, as there is nothing in the claims imposing such a requirement.").

We also credit Dr. Mazumder's testimony that a person of ordinary skill in the art would have considered the Remote Engine and the Home Engine as the obvious and natural structures by which the Piranha processing chip communicates with the I/O chips and, ultimately, the external peripherals. *See* Ex. 1001 ¶¶ 146–148. Although Dr. Wolfe

disagreed with Dr. Mazumder on the general point that Barroso's protocol engines are adapted to connect to external I/O devices, *see* Ex. 2026 ¶ 69, he testified that "[t]he Protocol Engines in Barroso (which includes the Remote Engine and the Home Engine) provide an interface to . . . I/O chips . . . ."), Ex. 2026 ¶ 59; *see also* Ex. 1050 ¶ 24 (Dr. Mazumder's testimony recognizing Dr. Wolfe's agreement on this point).

Thus, crediting the testimony of Dr. Mazumder, we find that Barroso suggests to a person of ordinary skill in the art that the Pirahna processing chips communicate via the global interconnection system with external peripherals via the Piranha I/O chips. We also find that there are only a limited number of components by which the Piranha processing chips could communicate with the external peripherals, and a person of ordinary skill in the art would have had reason to select the Remote Engine and the Home Engine for this purpose. In addition, we find that adapting the Remote Engine and the Home Engine for communicating with the external peripherals via the global interconnection system (which includes the inter-chip connections) would have been within the level of ordinary skill in the art at the time of the claimed invention, which in this case is relatively high. Thus, we find that Intel has shown persuasively that a person of ordinary skill in the art would have implemented limitation 9[h] in Barroso.

(f) Conclusion for claim 9

For the above reasons, we find that Intel has shown persuasively that Barroso discloses or teaches each limitation of claim 9 in light of Alpha Manual. Intel has also shown a persuasive rationale for why a person of ordinary skill in the art would have combined the teachings of Barroso and Alpha Manual, and otherwise modified the teachings of Barroso in an

obvious manner. Therefore, considering all of the evidence of record, we conclude Intel has shown by a preponderance of the evidence that claim 9 is unpatentable as obvious over Barroso in light of Alpha Manual.

5. Claim 24

Claim 24 depends from claim 9, and further recites method steps in which (a) a first data processing element transfers an address to a first memory element, "the address not corresponding to a memory location included in the first memory element"; (b) the first memory element forwards the address to a second memory element "based on the lack of correspondence of its included memory locations to the address"; and (c) "responsive to the receipt of the address, the second memory element transfers data conditional upon its inclusion of a memory allocation that corresponds to the address." *See* Ex. 1003, 35:28–40.

Intel contends that Barroso discloses these additional limitations. Pet. 48–52. To illustrate, Intel identifies CPU_0 as the first data processing element, $L2_0$ as the first memory element, and the dL1 cache of CPU_7 as the second memory. *See id.* Intel contends that when CPU_0 requests memory, the request first goes to its L1 cache (dL1) and, if there is a cache miss, the request goes to $L2_0$ (if the memory is not already in the dL1 corresponding to CPU_0), and if there is an L2 cache miss (i.e., the address does not correspond to a memory location included in the first memory element as recited in claim 24), the request (including the address) is forwarded to the dL1 cache of another CPU core (e.g., CPU_7), and if that dL1 contains the memory, it transfers the data. *See id.* (citing Ex. 1005, 283, 285–86, Fig. 1; Ex. 1001 ¶¶ 147–154).

PACT does not separately contest Intel's specific arguments about claim 24. Based on Intel's arguments and evidence, which we find persuasive, and our analysis of parent claim 9 (*supra* part III.C.4), we determine that claim 24 is unpatentable as obvious over Barroso in light of Alpha Manual.

6. Claims 26 and 27

Claims 26 and 27 are independent, and recite combinations of limitations that are largely the same as those of claim 9. *Compare* Ex. 1003, 35:44–36:38, *with id.* at 34:4–35. However, unlike claim 9, claims 26 and 27 do not explicitly require that the components are "separately connected," and are thus broader than claim 9 in that respect. *See* Pet. 52–53 (citing Ex. 1003, 35:64–36:3); Ex. 1003, 36:28–35. Claim 26 also includes a limitation corresponding to limitation 3[f], and claim 27 includes a limitation corresponding to limitation 4[f], both of which we address above. *See supra* parts III.C.2(g), III.C.3.

Intel relies on the same arguments it made for the corresponding limitations in claims 3, 4, and 9. *See* Pet. 52–54. We find these arguments persuasive, and PACT does not separately contest these arguments as they relate to claims 26 and 27. Thus, we determine that claims 26 and 27 are unpatentable as obvious over Barroso in light of Alpha Manual.

7. Claims 30, 42, 73, and 74

Claim 30 is independent, and includes a combination of limitations that include limitations corresponding to limitations 9[a]–[c], 3[d], the "separately connected" aspect of 9[g], and 9[h]. *Compare* Ex. 1003, 37:24–46, *with id.* at 32:42–48, *and id.* at 34:4–11, 34:25–27, 34:32–35. Intel relies

on its same arguments for claims 3 and 9. *See* Pet. 54–57 (citing Ex. 1001 ¶¶ 159, 163–164).

Claim 42 depends from claim 30, and also includes a limitation corresponding to limitation 3[e]. *Compare* Ex. 1003, 38:18–21, *with id.* at 32:49–52. Intel relies on its arguments for claim 30 and limitation 3[e]. Pet. 58 (citing Ex. 1001 ¶ 165).

Claim 73 depends from claim 30, and further recites "wherein an address is transferred via the bus system and from one of the plurality of data processing elements to one of the plurality of memory elements, which responsively transfers data conditional upon its inclusion of a memory location that corresponds to the transferred address." *See* Ex. 1003, 40:34–38. Intel argues that Barroso discloses this limitation, based on essentially the same argument outlined above for claim 24. *See* Pet. 58–60 (citing Ex. 1001 ¶¶ 166–168).

Claim 74 is the same as claim 24, but depends from claim 30 rather than claim 9. *Compare* Ex. 1003, 40:39–52, *with id.* at 35:28–40. Intel relies on its arguments for claims 9, 24, and 30. Pet. 60.

We find these arguments persuasive, and PACT does not separately contest these arguments as they relate to claims 30, 42, 73, and 74. Thus, we determine that claims 30, 42, 73, and 74 are unpatentable as obvious over Barroso in light of Alpha Manual.

D. GROUNDS II AND III (BARROSO, ALPHA MANUAL, GODFREY, NICKOLLS)

For Ground II, Intel alleges that claims 1, 5, 32, and 44 are unpatentable under § 103 as obvious on alternative grounds: "(a) Barroso, Alpha Manual, and Nickolls or, alternatively, (b) Barroso, Alpha Manual,

Godfrey, and Nickolls." Pet. 4. For Ground III, Intel alleges that claims 2, 6, and 29 are unpatentable under § 103 as obvious over Barroso, Alpha Manual, Godfrey, and Nickolls. *Id.*

Based on the *Graham* factors, we determine that Intel has shown that claims 1, 2, 5, 6, 29, 32, and 44 are unpatentable under 35 U.S.C. § 103 as obvious over Barroso in view of Alpha Manual, Godfrey, and Nicolls. We present our findings and conclusions below.

1. Overview of Godfrey

Godfrey describes "[a] computer chip including a data transfer network." Ex. 1006, code (57). This is illustrated in Figure 2A:

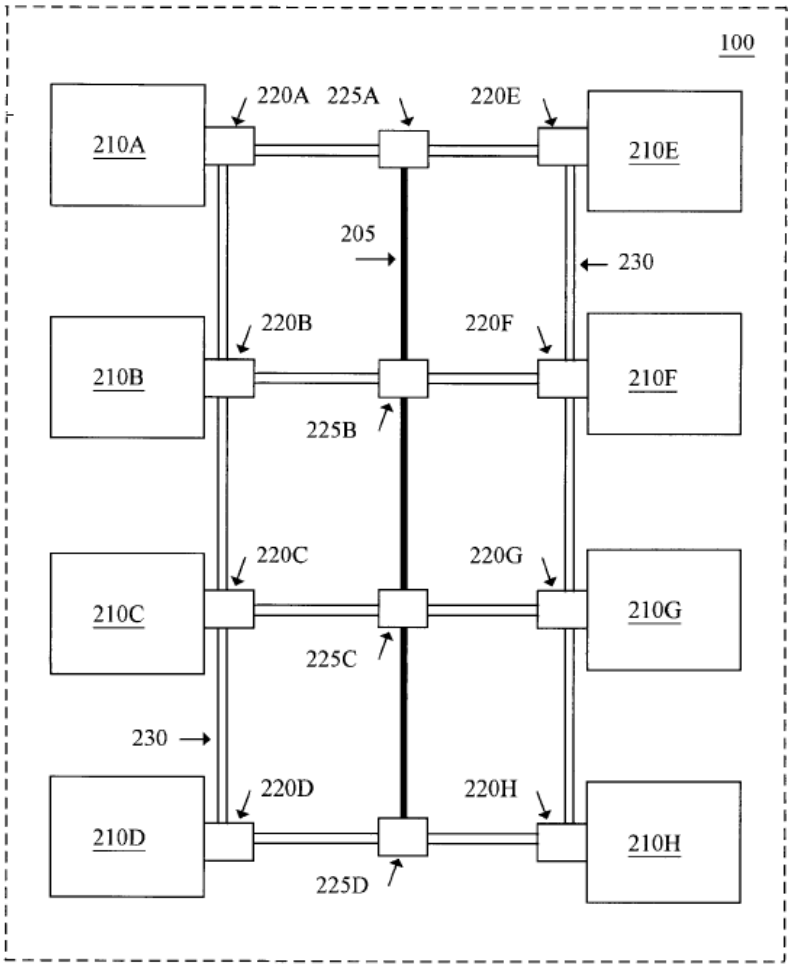


FIG. 2A

Figure 2A of Godfrey shows "computer chip 100 with an on-chip data transfer network for interconnecting a plurality of devices or modules 210A–210H linked by a plurality of communication ports 220A–220H." *Id.* at 3:67–4:3. The data transfer network also includes circular bus 230 coupled to communication ports 220A–220H, and also coupled to backbone bus 205 which has a plurality of communication ports 225A–225D. *Id.* at 4:17–21.

Godfrey's Figure 3B, reproduce below, shows ports 220 in more detail:

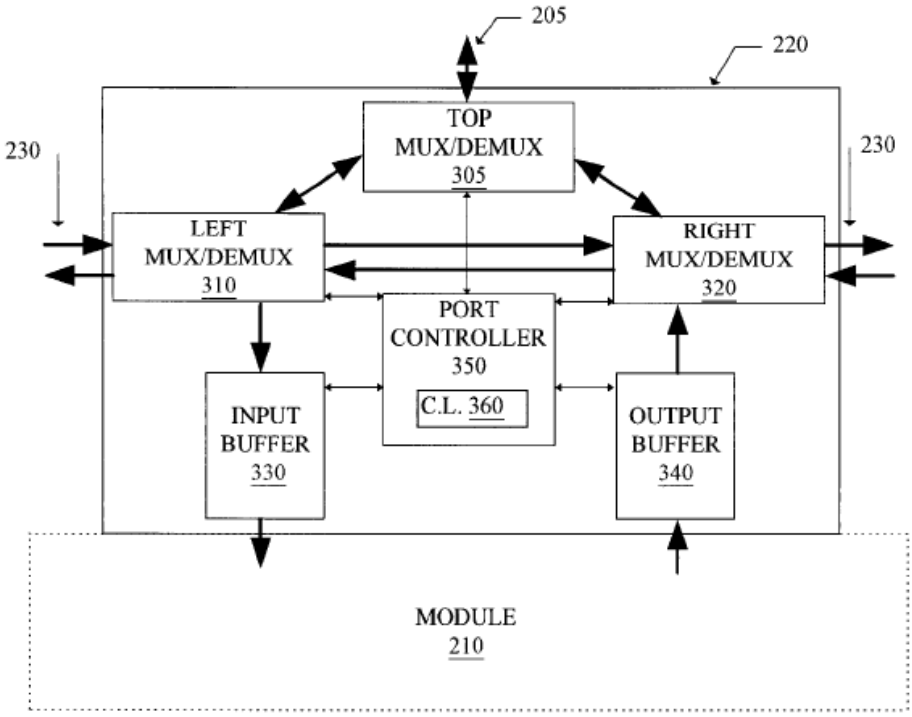


FIG. 3B

Godfrey's Figure 3B, above, is "an embodiment . . . of communications port 220." Ex. 1006, 8:63–64. Transfers along circular bus 230 take place from the left MUX/DEMUX 310 and right MUX/DEMUX 320, whereas data passes between circular bus 230 and module 210 via input buffer 330 and output buffer 340. *See id.* at 8:63–9:2. Port controller 350 routes data among the various buses, including circular bus 230 and backbone bus 205. *Id.* at 8:4–9. There is also a top MUX/DEMUX (305) that connects to backbone bus 205. *Id.* at Fig. 3B.

2. Overview of Nickolls

Nickolls describes "[a] massively parallel computer system . . . having a global router network in which pipeline registers are spatially distributed to increase the messaging speed of the global router network." Ex. 1012, code (57). In particular, Nickolls describes "partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message." *Id.* at 6:10–14. According to Nickolls, this arrangement leads to increased messaging speed and higher data flow rates through the routing path. *Id.* at 6:21–33.

3. Claim 1

Claim 1 is independent, and includes limitations that correspond to limitations 3[a]–[e]. *Compare* Ex. 1003, 32:8–26, *with id.* at 32:34–52. For these limitations, Intel relies on its arguments for claim 3. *See* Pet. 60.

Claim 1 also includes an additional limitation: "wherein the bus system is adapted for forming at least one ring via interconnection elements that include pipeline-registers." Ex. 1003, 32:27–29. For the aspect of this limitation in which the bus system is "adapted for forming at least one ring," Intel contends that this would have been obvious over Barroso in view of Godfrey. *See* Pet. 63. In particular, Intel argues that it would have been an obvious substitution to replace Godfrey's circular bus 230 (*see* Figure 2A, reproduced above in part III.D.1) for Barroso's ICS, because the resulting combination would "improve information routing between the different modules on the chip." Pet. 67 (citing Ex. 1001 ¶¶ 184–187); *see also* Pet.

67–70 (citing Ex. 1005, Abstract, 283–84; Ex. 1006, 1:27–31, 1:53–61, 3:57–61, 7:13–19; Ex. 1001 ¶¶ 185–187).

Intel relies on Nickolls to teach the use of pipeline registers. *See* Pet. 70. Intel argues that Nicolls "discloses that its routing path provides a 'substantial increase' in messaging speed, indeed 'many times larger . . . than that of a similar routing path not having the pipeline registers.'" Pet. 62–63 (alteration in original) (citing Ex. 1012, 6:21–33). According to Intel, a person of ordinary skill in the art "would have been motivated to incorporate pipeline registers in route-selecting stages of an interconnection network—such as in Godfrey's communication ports—as a means of maximizing data flow rates over the bus, as taught by Nickolls. Pet. 70 (citing Ex. 1001 ¶ 188). In particular, according to Intel, "Nickolls teaches that additional benefits are achieved by providing pipeline registers 'at each division point in a partitioned path to couple one segment to the next,'" and an ordinarily skilled artisan "would have recognized such an opportunity in Godfrey, where each communication port serves to divide the circular bus into segments." Pet. 70–71 (quoting Ex. 1012, 6:38–45) (citing Ex. 1006, Fig. 2B; Ex. 1001 ¶ 188). Also, Intel contends that since pipeline registers were well-known hardware, a person of ordinary skill in the art "would have been able to incorporate pipeline[ ]registers with a reasonable expectation of success." Pet. 71 (citing Ex. 1001 ¶ 188).

In its Response, PACT argues that the pipeline register system in Nickolls has "limited applicability" that does not include modification of Godfrey's communication ports. PO Resp. 40. According to PACT, Nickolls solves the problem that in massively parallel computing systems organized as multi-stage interconnect network ("MIN"), the per-path transmission time

grows in an un-scalable way as the size of the network increases, by "partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message." *See id.* at 38–39 (quoting Ex. 1012, 6:12–20) (citing Ex. 1012, 5:2–9, 5:21–36). But PACT argues that such MINs "are fundamentally different from Godfrey's small, compact data transfer network." *Id.* at 40 (citing Ex. 2026 ¶ 80). Also, PACT contends that "Nickolls teaches that pipeline registers add a time penalty that is only advantageous if it can be offset by increased data rate from shorter bus segments." *Id.* (citing Ex. 2026 ¶ 80).

Alternatively, PACT argues that there is no need to add pipeline registers in Godfrey "because Godfrey already discloses that buffers can be placed at the inputs and outputs of the communication ports," and Intel "does not offer any reason why [a person of ordinary skill in the art] would be motivated to ignore this teaching in Godfrey, and to instead use pipeline registers," since Nickolls's benefit comes from segmenting routes into shorter paths, and not specifically from the use of pipeline registers. PO Resp. 40–41 (citing Ex. 1006, 8:36–41; Ex. 2026 ¶ 81).

In its Reply, Intel argues that Nickolls is not directed exclusively to a MIN structure, but addresses other structures as well. Pet. Reply 24 (citing Ex. 1012, 1:34–5:67, 8:18–67); *id.* at 25. Intel also contends that Nickolls teaches that pipeline registers achieve their benefit "by reducing corruption caused by 'cross-coupling' between wires on a bus," and a person of ordinary skill in the art would have recognized in Godfrey an additional opportunity to improve performance by using Nickolls's pipelining,

particularly with larger ring sizes. *Id.* at 26 (citing Ex. 2028, 155:19–157:13).

Intel acknowledges that Nickolls's pipeline registers create a "slight time penalty," but argues that "the penalty is only temporary and quickly outweighed by a significant benefit—'*once the pipeline is primed . . . a substantial increase is observed in the messaging speed*'—so a [person of ordinary skill in the art] would have had ample motivation to apply Nickolls's technique." Pet. Reply 25 (quoting Ex. 1012, 6:21–28).

Having considered the arguments and the evidence on both sides, we find that Intel has shown persuasively that a person of ordinary skill in the art would have reason to substitute Godfrey's circular bus structure for Barroso's ICS, and also to improve Godfrey's performance by adding pipeline registers. We disagree with PACT that Nickolls teaches away from, or is inapplicable to, use in a bus like that of Godfrey, because PACT has not pointed to anything in Nicholls that criticizes, discredits, or otherwise discourages the use of pipeline registers in systems other than a MIN. We also credit Dr. Mazumder's testimony that a person of ordinary skill in the art would have expected benefits from using pipeline registers in Godfreys' bus. *See* Ex. 1001 ¶ 188; Ex. 1050 ¶¶ 27, 36–41; Ex. 2028, 155:19–157:13.

Although, as Nickolls teaches, there is a tradeoff to using pipeline registers, we disagree with PACT that this tradeoff would have dissuaded a person of ordinary skill in the art from seeking the advantages from the use of pipeline registers, for the reasons Intel expresses in its Reply. *See Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) ("[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.").

For the above reasons, we determine that Intel has shown, by a preponderance of the evidence, that claim 1 would have been obvious over the combination of Barroso, Alpha Manual, Godfrey, and Nickolls, and is thus unpatentable.

4. Claim 5

Independent claim 5 is essentially the same as claim 1, except that unlike claim 1, it does not include a limitation corresponding to limitation 3[e]. *Compare* Ex. 1003, 33:12–29, *with id.* at 32:8–29. Thus, Intel correctly asserts that claim 5 is broader than claim 1, and the same arguments are applicable. *See* Pet. 71.

Thus, for the same reasons as claim 1, we conclude that claim 5 is unpatentable as obvious over the combination of Barroso, Alpha Manual, Godfrey, and Nickolls.

5. Claims 32 and 44

Claim 32 depends from claim 30, and further recites "wherein the bus system is adapted for simultaneously transferring data by a plurality of connects." Ex. 1003, 37:49–51. Intel contends that Barroso discloses this limitation because each port of Barroso's ICS includes "two independent 64-bit datapaths . . . for sending and receiving data," and that the ICS can issue a grant to one initiator to transfer data, while concurrently, "the destination receives a request signal that identifies the initiator and type of transfer." Pet. 72–73 (alteration in original) (quoting Ex. 1005, 284) (citing Ex. 1001 ¶ 192).

Alternatively, Intel argues that Godfrey's bus system teaches this limitation because is segments may transmit simultaneously, and "[i]t would

have been obvious to modify Barroso to use Godfrey's ring bus with the ability to transfer data simultaneously as disclosed by Godfrey, with a reasonable expectation of success, for the reasons discussed . . . with respect to claim 1." Pet. 73–74 (citing Ex. 1006, 4:10–12, 6:2–9, 6:23–37, 7:13–19, 7:42–46, 7:58–65, claim 12, Fig. 2A; Ex. 1001 ¶¶ 193–194).

Claim 44 is the same as claim 32, except that it depends from claim 42, rather than claim 30. *Compare* Ex. 1003, 38:24–26, *with id.* at 37:49–51. Intel relies on its same arguments as for claim 32. Pet. 74–75 (citing Ex. 1001 ¶ 196).

PACT does not separately contest Intel's specific arguments about claims 32 or 44. Based on Intel's arguments and evidence, which we find persuasive, we determine that claims 32 and 44 are obvious over the combination of Barroso, Alpha Manual, Godfrey, and Nickolls, and is thus unpatentable.

6. Claim 2, 6, and 29

Claim 2 depends from claim 1 and further recites "wherein the ring is adapted for transmitting data in two directions using separate respective interconnection elements for each direction." Ex. 1003, 32:30–33. Claim 6 includes the same limitation, but it depends from claim 5. *See id.* at 33:30–33. Claim 29 is independent and is essentially the same as claim 1, except that similarly to claim 2, it further recites "wherein the bus system is adapted for transmitting data in at least two directions and comprises separate and independent structures for each of the data transmission directions." *Id.* at 37:17–20; *compare id.* at 37:1–16, 37:21–23, *with id.* at 32:8–29. Thus, claims 2, 6, and 29 include substantially the same limitation.

Regarding this limitation,[15] Intel argues that "[i]n Godfrey's system, *separate* communication ports 220 (the claimed 'interconnection element') are adapted for transmitting data on the circular bus 230 (forming the claimed 'ring') in different directions." Pet. 75 (citing Ex. 1001 ¶ 199). According to Intel, Godfrey's ports 220 are adapted for communication in either direction via their left or right MUX/DEMUX 310 or 320. Pet. 75–77 (citing Ex. 1006, 2:11–13, 2:35–40, 7:58–65, 9:19–35, Figs. 2A, 3B; Ex. 1001 ¶ 201). Thus, according to Intel, "Godfrey's system is configured such that two (or more) different communication ports 220 transmit data in opposite directions, depending on the data path needed for each respective communication." Pet. 77.

In its Reply, PACT argues that since Godfrey's communication ports are bidirectional, "it is clear that the different communication parts that [Intel] relies on are not separate interconnection elements for transmitting data in different *directions*—they are simply elements that define two different paths that data may take." PO Resp. 35–36 (citing Ex. 1006, code (57), 2:11–13, 2:35–40, Fig. 2A; Ex. 2026 ¶¶ 87–89; Ex. 2028, 162:14–163:8 (Dr. Mazumder acknowledging that along any particular segment of Godfrey's circular bus 230 between ports 220, data does not move in both directions in parallel)). PACT contrasts this with the Figure 5 embodiment of the '807 patent, in which there are separate structures in each bus segment for transferring data in opposite directions along the same path. *Id.* at 36–37 (citing Ex. 1003, 25:52–54; Ex. 2026 ¶¶ 88–89).

[15] Intel makes essentially the same arguments for claims 2, 6, and 29. *See* Pet. 77–79. PACT makes no substantive distinction between the claims in its arguments. *See* PO Resp. 34–37; PO Sur-reply 15–17.

In its Reply, Intel disagrees that according to the claim limitation, "each separate interconnection element/structure must *exclusively* transmit data in one direction." Pet. Reply 22 (quoting PO Resp. 36). Intel contends that PACT's argument is based on only a single exemplary embodiment (that of Figure 5), which should not be imported into the claim. *See id.* at 22–23.

In its Sur-reply, PACT disputes that its argument is based on a single example in the '807, and contends that it is "based on the claim language itself, which . . . clearly requires separate elements for transmitting data in different directions, and not merely multiple elements that can form separate paths." PO Sur-reply 16.

We find Intel's argument persuasive, and disagree with PACT's proposed interpretation of the claim limitation. Claims 2 and 6 require that the bi-directional transmission "us[es] separate respective interconnection elements for each direction." Ex. 1003, 32:32–33, 33:32–33. And, similarly, claim 29 requires that the bi-directional transmission "comprises separate and independent structures for each of the data transmission directions." *Id.* at 37:18–20. But the claims do not require that the interconnection elements or structures are *dedicated* to transmission in a single direction on a permanent basis, only that they be "adapted for" such transmission. Thus, a bus structure, such as that in Godfrey, meets this limitation if can be "adapted," either temporarily or permanently, such that separate and independent structures (e.g., two different ports 220 in Godfrey's Figure 2A) perform transmission in opposite directions.

For the above reasons, we determine that Intel has shown, by a preponderance of the evidence, that claims 2, 6, and 29 would have been

obvious over the combination of Barroso, Alpha Manual, Godfrey, and Nickolls, and are thus unpatentable.

IV. CONCLUSION[16]

Considering all of the evidence of record, for the reasons discussed above, Intel has shown by a preponderance of the evidence that 1–6, 9, 24, 26, 27, 29, 30, 32, 42, 44, 73, and 74 of the '807 patent are unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
3, 4, 9, 24, 26, 27, 30, 42, 73, 74	103(a)	Barroso, Alpha Manual	3, 4, 9, 24, 26, 27, 30, 42, 73, 74	
1, 5, 32, 44	103(a)	Barroso, Alpha Manual, Godfrey, Nickolls	1, 5, 32, 44	
2, 6, 29	103(a)	Barroso, Alpha Manual, Godfrey, Nickolls	2, 6, 29	
Overall Outcome			1–6, 9, 24, 26, 27, 29, 30, 32, 42, 44, 73, 74	

[16] Should PACT wish to pursue amendment of claims in a reissue or reexamination proceeding after this decision, we draw PACT's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If PACT chooses to file a reissue application or a request for reexamination of the challenged patent, we remind PACT of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2) (2020).

V. ORDER

In consideration of the foregoing, it is

ORDERED that claims 1–6, 9, 24, 26, 27, 29, 30, 32, 42, 44, 73, and 74 of the '807 patent are unpatentable;

FURTHER ORDERED that parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

For PETITIONER:

Kevin Bendix
Robert A. Appleby
Gregory S. Arovas
KIRKLAND & ELLIS LLP
kevin.bendix@kirkland.com
robert.appleby@kirkland.com
greg.arovas@kirkland.com

For PATENT OWNER:

Ziyong Li
Nima Hefazi
Joseph M. Paunovich
QUINN EMANUEL URQUHART & SULLIVAN LLP
seanli@quinnemanuel.com
nimahefazi@quinnemanuel.com
joepaunovich@quinnemanuel.com