

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.,
Petitioner,

v.

IMPINJ, INC.,
Patent Owner.

IPR2020-00544
Patent 8,344,857 B1

Before BRIAN J. McNAMARA, ROBERT J. WEINSCHENK, and
KEVIN C. TROCK, *Administrative Patent Judges*.

WEINSCHENK, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Granting-in-Part and Denying-in-Part
Patent Owner's Motion to Amend
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

NXP USA, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–15 (“the challenged claims”) of U.S. Patent No. 8,344,857 B1 (Ex. 1001, “the ’857 patent”). Impinj, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”) to the Petition. We instituted an *inter partes* review of the challenged claims on September 1, 2020. Paper 8 (“Dec. on Inst.”), 38.

After institution, Patent Owner did not file a Response to the Petition, but filed a non-contingent Motion to Amend requesting that we cancel original claims 1–15 and add proposed substitute claims 16–30. Paper 20 (“Mot. Amend”), 1. Petitioner filed an Opposition (Paper 23, “Pet. Opp.”) to the Motion to Amend. Pursuant to Patent Owner’s request (Mot. Amend 4), we provided Preliminary Guidance on the Motion to Amend. Paper 25. Patent Owner then filed a Reply (Paper 26, “PO Reply”) to the Opposition, and Petitioner filed a Sur-reply (Paper 31, “Pet. Sur-reply”) to the Reply. We held an oral hearing on June 2, 2021, and a transcript of the hearing is included in the record. Paper 35 (“Tr.”).

For the reasons set forth below, we grant Patent Owner’s request to cancel original claims 1–15, but we deny Patent Owner’s request to add proposed substitute claims 16–30.

B. Real Parties in Interest

Petitioner identifies the following real parties in interest: 1) NXP USA, Inc.; 2) NXP Semiconductors N.V.; 3) NXP B.V.; and 4) Freescale Semiconductor Holdings V, Inc. Pet. 120. Patent Owner identifies itself as the only real party in interest. Paper 4, 2.

C. Related Matters

The parties indicate that the '857 patent is the subject of the following district court case: *Impinj, Inc. v. NXP USA, Inc.*, No. 4:19-cv-03161 (N.D. Cal.). Pet. 120; Paper 4, 2–3. Patent Owner identifies several other petitions for *inter partes* review that involve related patents. Paper 4, 3–4.

D. The '857 Patent

The '857 patent relates to a power rectifier for a Radio Frequency Identification (“RFID”) tag. Ex. 1001, 2:11–13. The '857 patent explains that an RFID system typically includes an RFID reader and an RFID tag. *Id.* at 1:20–21. In general, an RFID reader transmits a Radio Frequency (“RF”) wave, and an RFID tag senses the RF wave and responds by transmitting back another RF wave. *Id.* at 1:29–35.

Early RFID tags included an energy storage device, such as a battery. *Id.* at 1:50–52. But “[a]dvances in semiconductor technology have miniaturized the electronics so much that an RFID tag can be powered solely by the RF signal it receives.” *Id.* at 1:53–56. This type of RFID tag is known as a passive RFID tag. *Id.* at 1:56–57. According to the '857 patent, “[h]arvesting sufficient power” for a passive RFID tag “can be difficult since the voltage of the RF signal is in the range of approximately 200 millivolts, and a typical supply voltage for circuits of the RFID tag is one volt.” *Id.* at 1:58–61. Thus, a passive RFID tag typically includes a power rectifier with a charge pump “to increase the output [direct current (“DC”)] voltage.” *Id.* at 1:64–67.

The '857 patent describes a “power rectifier system” that “maximizes the energy harvest efficiency of the RFID tag circuit.” *Id.* at 2:20–21.

Figure 8A depicts one embodiment of a synchronous power rectifier for an RFID tag and is reproduced below. *Id.* at 7:16–18, Fig. 8A.

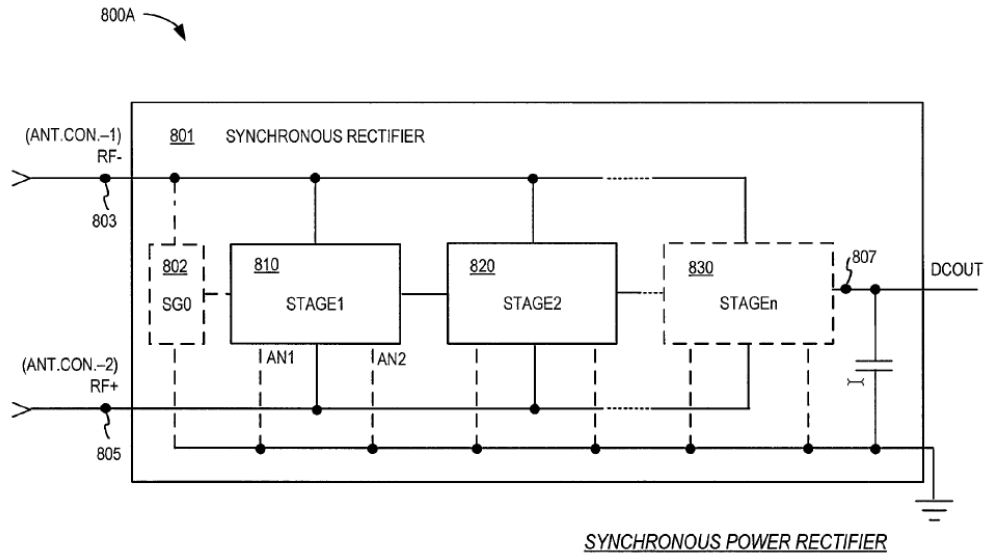


FIG. 8A

Figure 8A shows a synchronous power rectifier comprising “[a] number of synchronous rectifier stages . . . [that] are coupled serially.” *Id.* at 7:16–18, 7:23–25. Figure 8B depicts a synchronous rectifier stage and is reproduced below. *Id.* at 7:34–36, Fig. 8B.

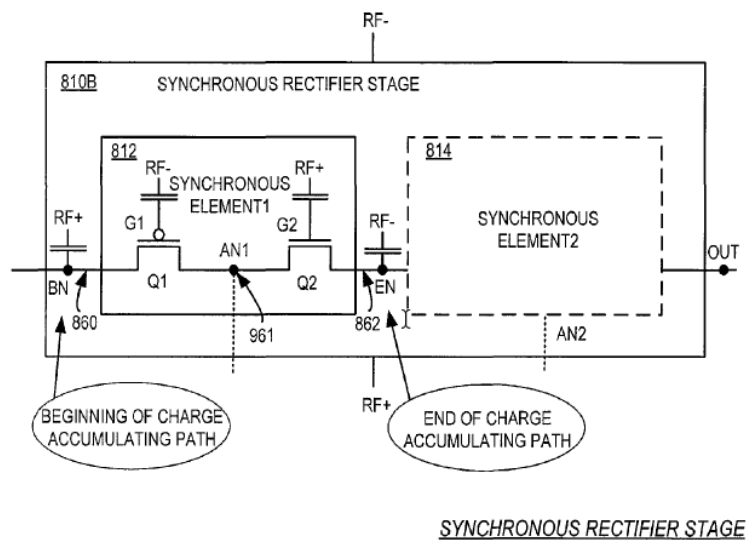


FIG. 8B

Figure 8B shows a synchronous rectifier stage comprising “synchronous [e]lement 812 and synchronous [e]lement[] 814” that “are coupled serially.” *Id.* at 7:36–38. Synchronous element 812 includes transistor Q1 and transistor Q2. *Id.* at 7:41–42. The output of transistor Q1 is connected to the input of transistor Q2 at averaging node AN1. *Id.* at 7:47–49.

E. Illustrative Claim

Proposed substitute claims 16, 21, and 26 replace original independent claims 1, 6, and 11, respectively. Mot. Amend, Appx. A. Proposed substitute claims 17–20, 22–25, and 27–30 replace original dependent claims 2–5, 7–10, and 12–15, respectively. *Id.* Proposed substitute claim 16 is illustrative of the proposed amendments and is reproduced below with additions to original claim 1 shown in underline and deletions shown with strikethrough.

16. A rectifier for a Radio Frequency Identification tag, comprising:

a first antenna input,

a second antenna input,

first, second, third, and fourth capacitors,

a first transistor including an input terminal, an output terminal, and a gate, and

a second transistor of a type complementary to the first transistor and including an input terminal, an output terminal, and a gate, wherein,

the input terminal of the first transistor is coupled to a beginning node,

the output terminal of the first transistor is coupled to an averaging node,

the input terminal of the second transistor is coupled to the averaging node,

the output terminal of the second transistor is coupled to an ending node,

the first antenna input is coupled to the gate of the first transistor and to the ending node,

the second antenna input is coupled to the gate of the second transistor and to the beginning node,

the first antenna input is coupled to the ending node via the first capacitor,

the second antenna input is coupled to the beginning node via the second capacitor,

the first antenna input is coupled to the gate of the first transistor via the third capacitor, ~~and~~

the second antenna input is coupled to the gate of the second transistor via the fourth capacitor,

a first, controllable DC bias voltage is coupled between the gate of the first transistor and the averaging node,

a second, controllable DC bias voltage is coupled between the gate of the second transistor and the averaging node, and

the first and second DC bias voltages are functions of and controlled based on an amplitude of an RF signal on the first and second antenna inputs.

Mot. Amend, Appx. A, 1–2.

F. Evidence

Petitioner submits the following evidence:

Evidence	Exhibit No.
Soumyajit Mandal, <i>Far Field RF Power Extraction Circuits and Systems</i> (June 2004) (“Mandal Thesis”)	1003
Mandal, US 8,045,947 B2, issued Oct. 25, 2011 (“Mandal ’947 patent”)	1004
Declaration of Maria P. Garcia (“Garcia Declaration”)	1005
Declaration of Daniel van der Weide, Ph.D. (“van der Weide Declaration”)	1006

Evidence	Exhibit No.
Supplemental Declaration of Daniel van der Weide, Ph.D. (“Supp. van der Weide Declaration”)	1009
Oliver, US 2006/0197668 A1, published Sept. 7, 2006 (“Oliver”)	1010
Kotani, JP 2008-11584, published Jan. 17, 2008 (“Kotani”)	1011

Patent Owner submits the Declaration of Gregory Durgin, Ph.D.
Ex. 2007 (“Durgin Declaration”).

G. Asserted Grounds

Petitioner asserts that the original claims and proposed substitute claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–15	103 ¹	Mandal Thesis
1–15	102(a), (e)	Mandal ’947 patent
16–30	103	Mandal Thesis
16–30	103	Mandal Thesis, Oliver
16–30	103	Mandal ’947 patent, Oliver
16–30	103	Mandal Thesis, Kotani
16–30	103	Mandal ’947 patent, Kotani
16–30	103	Kotani
16–30	112	Lack of enablement

II. ANALYSIS

A. Legal Standards

In an *inter partes* review, amended claims are not added to a patent as of right, but rather must be proposed as a part of a motion to amend.
35 U.S.C. § 316(d) (2018). We must assess the patentability of proposed

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103, 112. Because the ’857 patent has an effective filing date before the effective date of the relevant amendment, the pre-AIA versions of §§ 102, 103, 112 apply.

substitute claims “without placing the burden of persuasion on the patent owner.” *Aqua Prods., Inc. v. Matal*, 872 F.3d 1290, 1328 (Fed. Cir. 2017) (en banc); *see also Lectrosonics, Inc. v. Zaxcom, Inc.*, IPR2018-001129, Paper 15 at 3–4 (PTAB Feb. 25, 2019) (precedential). Subsequent to the issuance of *Aqua Products*, the Federal Circuit issued a decision in *Bosch Automotive Service Solutions, LLC v. Matal*, 878 F.3d 1027 (Fed. Cir. 2017) (“*Bosch*”), as well as a follow-up Order amending that decision on rehearing. *See Bosch Auto. Serv. Sols., LLC v. Iancu*, No. 2015-1928 (Fed. Cir. Mar. 15, 2018) (Order on Petition for Panel Rehearing).

In accordance with *Aqua Products*, *Bosch*, and *Lectrosonics*, a patent owner does not bear the burden of persuasion to demonstrate the patentability of the substitute claims presented in the motion to amend. Rather, ordinarily, “the petitioner bears the burden of proving that the proposed amended claims are unpatentable by a preponderance of the evidence.” *Bosch*, 878 F.3d at 1040 (as amended on rehearing); *see Lectrosonics*, Paper 15 at 3–4. In determining whether a petitioner has proven unpatentability of the substitute claims, we focus on “arguments and theories raised by the petitioner in its petition or opposition to the motion to amend.” *Nike, Inc. v. Adidas AG*, 955 F.3d 45, 51 (Fed. Cir. 2020).

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including 1) the scope and content of the prior art;

2) any differences between the claimed subject matter and the prior art; 3) the level of ordinary skill in the art; and 4) any objective indicia of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art “would have had a bachelor’s degree in electrical engineering or physics and three years of experience with circuit design (or equivalent degree and experience).” Pet. 7 (citing Ex. 1006 ¶¶ 39–40). Petitioner’s description of the level of ordinary skill in the art is supported by the testimony of Petitioner’s declarant, Dr. Daniel van der Weide. Ex. 1006 ¶¶ 39–40. Patent Owner does not dispute Petitioner’s description. Mot. Amend 21. Therefore, we adopt Petitioner’s description of the level of ordinary skill in the art.

C. Claim Construction

In an *inter partes* review proceeding, a claim of a patent, or a claim proposed in a motion to amend, is construed using the same standard used in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of the claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b) (2019). Neither party proposes an express construction for any claim terms. Pet. 8–9; Mot. Amend 21; Pet. Opp. 1. We determine that no claim terms require an express construction to resolve the parties’ disputes regarding the asserted grounds of unpatentability. *See* Sections II.E.1–II.E.3.

D. Original Claims 1–15

Patent Owner’s Motion to Amend includes a non-contingent request to cancel original claims 1–15. Mot. Amend 1, 3, Appx. A. Petitioner does

not oppose Patent Owner's request. Therefore, we grant Patent Owner's non-contingent request to cancel original claims 1–15.

E. Proposed Substitute Claims 16–30

Patent Owner's Motion to Amend requests that we add proposed substitute claims 16–30. Mot. Amend 3–4, Appx. A. Petitioner argues that proposed substitute claims 16–30 are unpatentable based on several asserted grounds. Pet. Opp. 2. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that proposed substitute claims 16–30 are unpatentable.² Therefore, we deny Patent Owner's request to add proposed substitute claims 16–30.

1. Obviousness of Proposed Substitute Claims 16–30 over the Mandal '947 Patent and Oliver

Petitioner argues that proposed substitute claims 16–30 would have been obvious over the Mandal '947 patent³ and Oliver. Pet. 64–120; Pet. Opp. 6–14. For the reasons discussed below, Petitioner has shown by a

² Because Petitioner has shown that proposed substitute claims 16–30 would have been obvious, we need not decide whether Patent Owner's Motion to Amend complies with the other applicable statutory and regulatory requirements.

³ Patent Owner argued in its Preliminary Response that the Mandal '947 patent is not prior art because the inventors of the '857 patent conceived of the claimed invention prior to the filing date of the Mandal '947 patent and diligently reduced it to practice. Prelim. Resp. 57–64. We did not find that argument persuasive and instead determined that Petitioner had shown sufficiently that the Mandal '947 patent was prior art based on the evidence of record at that stage of the proceeding. Dec. on Inst. 26–28. Specifically, we noted that the Mandal '947 patent was filed on December 11, 2006, and published on April 19, 2007, both of which are prior to the filing date of the '857 patent. *Id.* at 26 (citing Pet. 8). Patent Owner does not dispute that the Mandal '947 patent is prior art in its Motion to Amend or Reply.

preponderance of the evidence that proposed substitute claims 16–30 would have been obvious over the Mandal '947 patent and Oliver.

a. Overview of the Mandal '947 Patent and Oliver

The Mandal '947 patent describes a multi-stage rectifier that “increases the output DC voltage that can be generated from a given input RF signal.” Ex. 1004, 11:44–46, 11:57–61. The Mandal '947 patent's Figure 18 is reproduced below. *Id.* at Fig. 18.

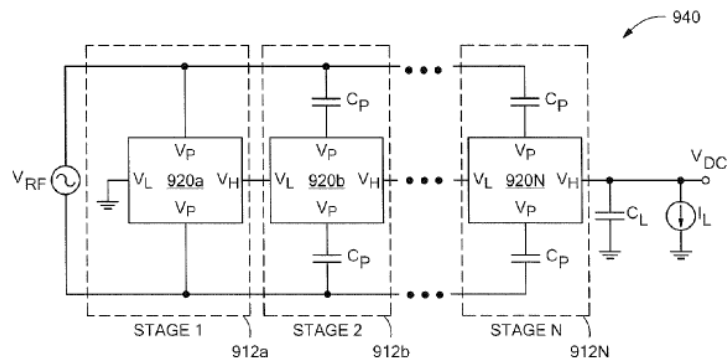


FIG. 18

Figure 18 is a circuit diagram for a multi-stage rectifier having N stages. *Id.* at 11:44–46. Each stage of the rectifier includes a rectifier cell, and each rectifier cell may be formed using “diodes, transistors, varactors, or other nonlinear elements or any combination thereof.” *Id.* at 11:47–51. One example of a rectifier cell is shown in Figure 25 and is reproduced below. *Id.* at 13:31–32, Fig. 25.

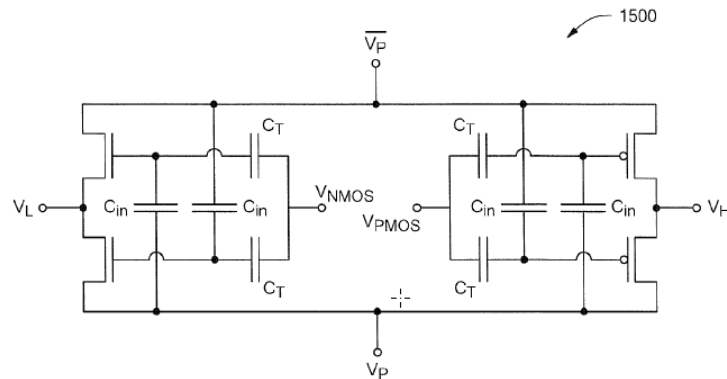


FIG. 25

Figure 25 depicts “a floating gate version of [a] four-transistor rectifier cell.” *Id.* at 13:31–32.

Oliver describes a voltage bias source coupled to the gate of a transistor in a rectifier. Ex. 1010 ¶ 53. Oliver teaches that the voltage bias source reduces the need for the voltage of an RF input signal to drive the gate of the transistor to its threshold voltage, thereby improving efficiency. *Id.* According to Oliver, the voltage bias source is adjustable, and, thus, “enable[s] the bias voltage applied to the gate of a transistor to be adjusted to optimize operation.” *Id.* ¶ 56. For example, the bias voltage may be “adjusted based on the maximum amplitude of the PHASE1 and PHASE2 signals” so that the bias voltage is “increased in response to higher amplitude PHASE1 and PHASE2 signals.” *Id.* ¶ 64.

b. Proposed Substitute Claim 16

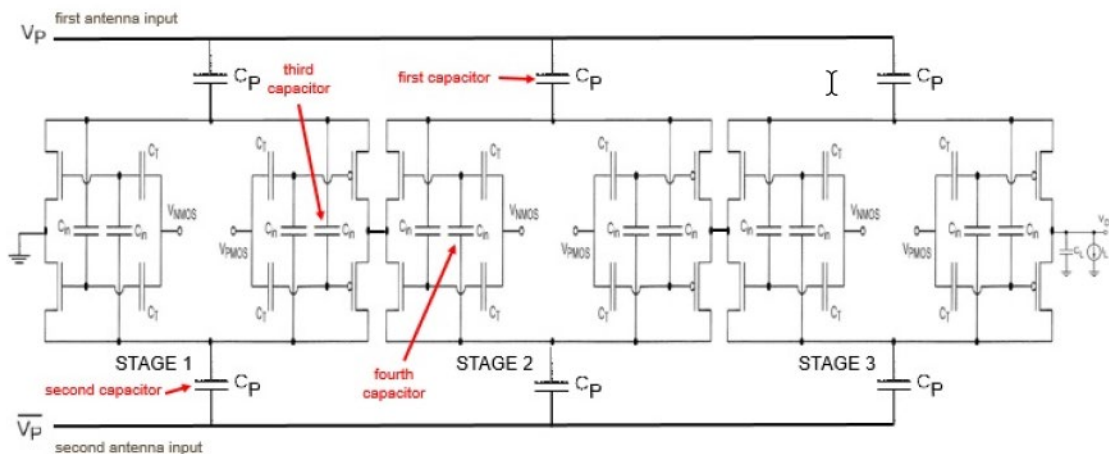
Proposed substitute claim 16 recites “[a] rectifier for a Radio Frequency Identification tag.”⁴ Mot. Amend, Appx. A at 1. The Mandal

⁴ Because we determine that the prior art teaches the recitations in the preamble of each independent claim, we need not decide whether the preamble in any of the independent claims is limiting.

'947 patent teaches a rectifier for an RFID tag. Pet. 64–68; Ex. 1004, 1:16–18, 1:22–26, 2:4–11. Patent Owner does not dispute that the Mandal '947 patent teaches the preamble of proposed substitute claim 16.

Proposed substitute claim 16 recites “a first antenna input” and “a second antenna input.” Mot. Amend, Appx. A at 1. The Mandal '947 patent teaches a first antenna input and a second antenna input. Pet. 68–74; Ex. 1004, 9:24–28, 10:6–10, 10:34–36, Figs. 13–14. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “first, second, third, and fourth capacitors.” Mot. Amend, Appx. A at 1. The Mandal '947 patent's Figure 18 teaches a multiple stage rectifier with several cells in series, and the Mandal '947 patent's Figure 25 teaches a floating gate version of a four transistor cell. Pet. 70–72; Ex. 1004, 11:44–49, 13:31–32, Figs. 18, 25. The evidence of record indicates that the transistor cell in Figure 25 can be inserted into each stage of the rectifier in Figure 18. Pet. 72–75; Ex. 1006 ¶¶ 161, 163, 167–168. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 77.



The above figure shows a rectifier comprising first, second, third, and fourth capacitors. *Id.*; Ex. 1006 ¶ 170. Although the capacitor identified as the second capacitor in the above figure is not shown in the Mandal '947 patent's Figure 18, the Mandal '947 patent teaches that the rectifier may include that capacitor. Pet. 72–73; Ex. 1004, 6:53–56, 11:51–56, 13:34–37; Ex. 1006 ¶¶ 161, 163.

Patent Owner responds that the capacitor Petitioner relies on to show the claimed “second capacitor” is “neither shown, nor described, in the relied upon Mandal figures.” PO Reply 9. Patent Owner argues that Petitioner “provides a series of quotations related to Fig[ure] 18 of the Mandal '947 [p]atent without any explanations regarding the significance of those quotations.” *Id.* at 11 (citing Pet. 70, 74–77). According to Patent Owner, “those quotations explicitly point to Fig[ure] 18 of the Mandal '947

[p]atent, which **does not** include pump capacitors connected to Stage 1, but clearly shows pump capacitors connected to all other stages.”⁵ *Id.*

Patent Owner’s argument is unavailing. The Mandal ’947 patent’s Figure 18 is reproduced below. Ex. 1004, Fig. 18.

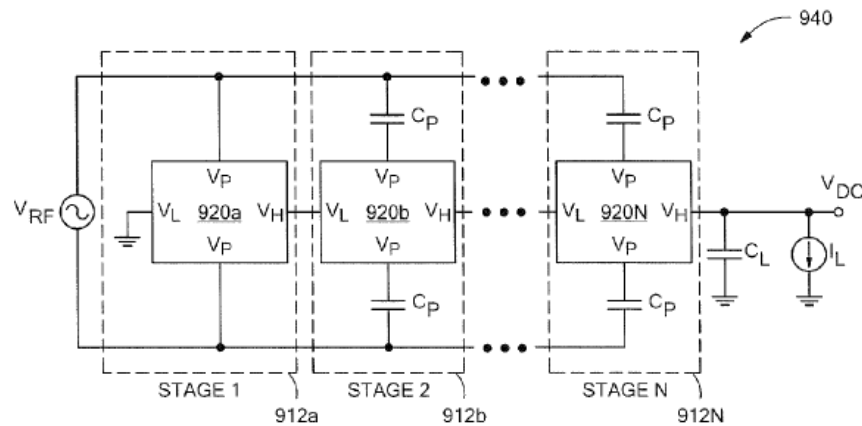


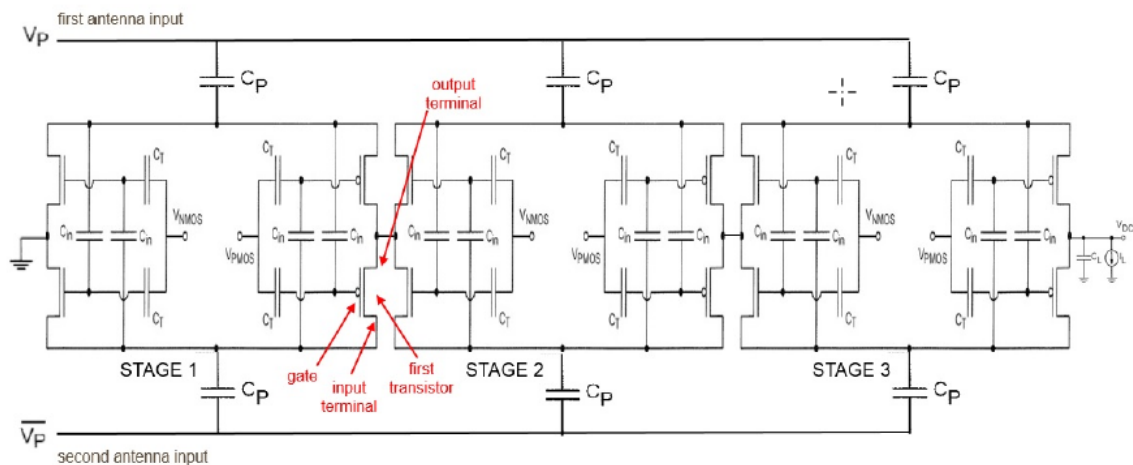
FIG. 18

Figure 18 is a circuit diagram for a multi-stage rectifier having N stages. *Id.* at 11:44–46. Although Figure 18 does not show a pump capacitor coupled between V_{RF} and V_P for Stage 1 of the rectifier, the Mandal ’947 patent states that “[t]he input RF signal V_{RF} is fed in parallel to *each of the stages* 912a–912N (*directly or through pump capacitors C_P , e.g., pump capacitors 50*). *Id.* at 11:51–56 (emphasis added). Thus, the Mandal ’947 patent teaches that each stage, including first stage 912a, in Figure 18 may include a pump capacitor between V_{RF} and V_P . *Id.*; Ex. 1006 ¶ 163. Further, in

⁵ Patent Owner argued at the oral hearing that Kotani also teaches omitting a pump capacitor for the first stage of its rectifier, and, thus, Kotani confirms that the Mandal ’947 patent intended to omit such a capacitor. Tr. 34:15–20. We disagree. Although Kotani’s Figure 9 does not include a coupling capacitor between the AC signal and TA1 (or TA2) for the first stage of its rectifier, Kotani teaches that a coupling capacitor may be included for the first stage. Pet. Opp. 15; Ex. 1009 ¶ 94; Ex. 1011 ¶ 139, Fig. 9.

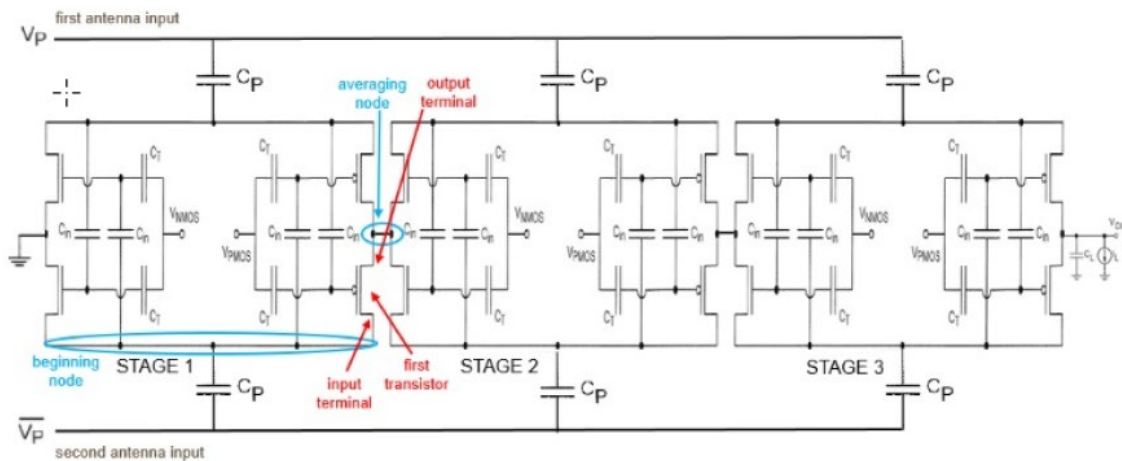
describing the cell used for each stage of the rectifier, the Mandal '947 patent confirms that each individual cell may include a pump capacitor between V_{RF} and V_P . Ex. 1004, 13:31–37, Fig. 25; Ex. 1006 ¶ 161.

Proposed substitute claim 16 recites “a first transistor including an input terminal, an output terminal, and a gate.” Mot. Amend, Appx. A at 1. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 77–78.



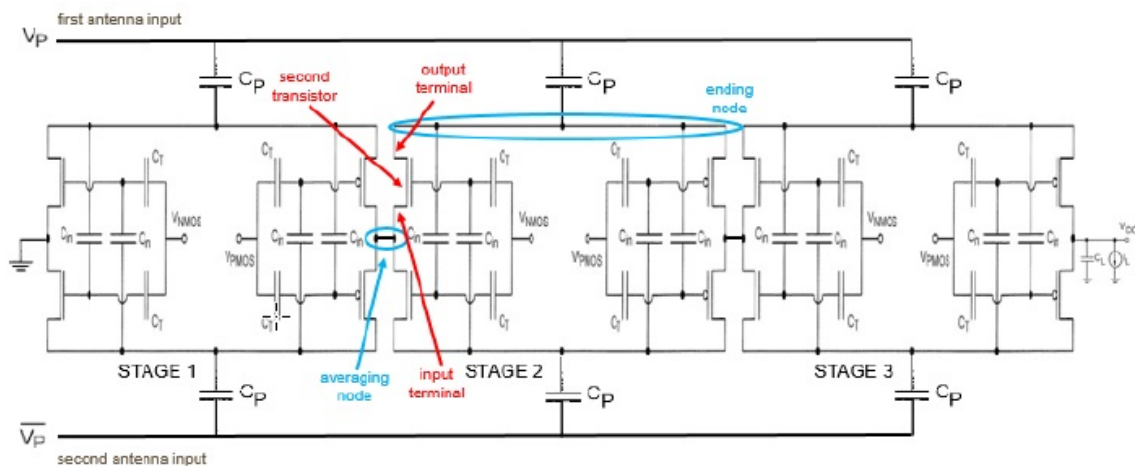
The above figure shows a rectifier comprising a first transistor with an input terminal, an output terminal, and a gate. *Id.*; Ex. 1006 ¶ 172. The evidence of record indicates that the first transistor is a p-channel metal oxide semiconductor (“PMOS”) transistor. Pet. 79–80; Ex. 1006 ¶ 174. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “a second transistor of a type complementary to the first transistor and including an input terminal, an output terminal, and a gate.” Mot. Amend, Appx. A at 1. Petitioner presents



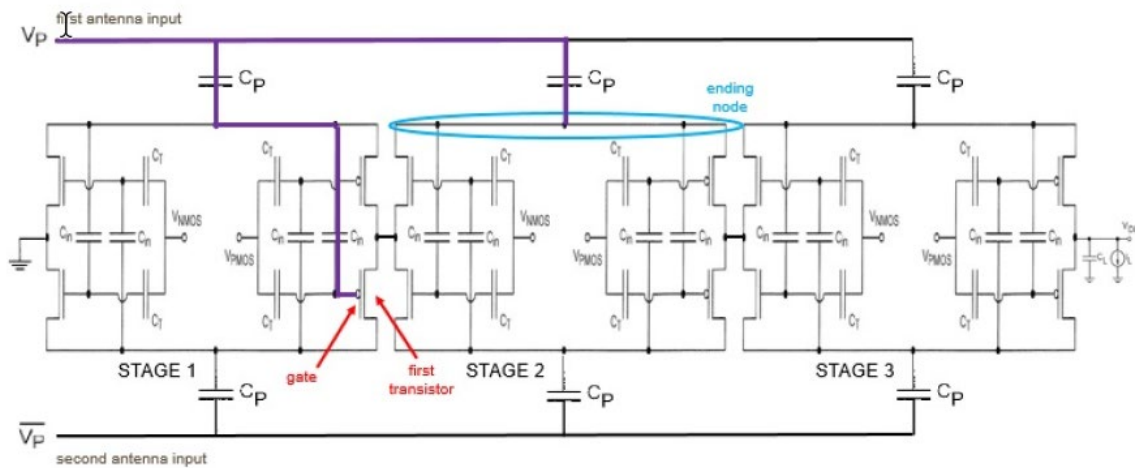
The above figure shows the input terminal of the first transistor coupled to a beginning node and the output terminal of the first transistor coupled to an averaging node. *Id.*; Ex. 1006 ¶ 176. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “the input terminal of the second transistor is coupled to the averaging node,” and “the output terminal of the second transistor is coupled to an ending node.” Mot. Amend, Appx. A at 1. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 82.



The above figure shows the input terminal of the second transistor coupled to the averaging node and the output terminal of the second transistor coupled to an ending node. *Id.*; Ex. 1006 ¶ 177. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

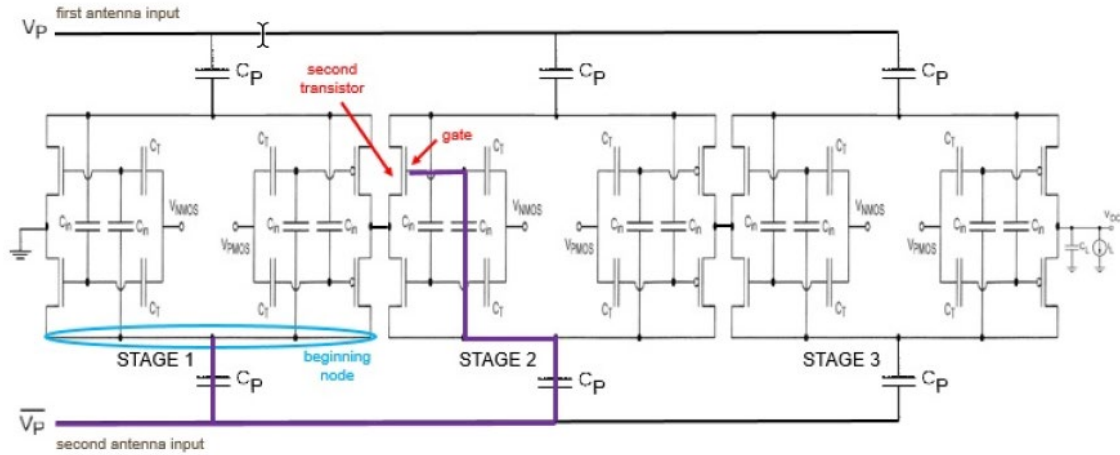
Proposed substitute claim 16 recites “the first antenna input is coupled to the gate of the first transistor and to the ending node.” Mot. Amend, Appx. A at 1. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 83.



The above figure shows the first antenna input coupled to the gate of the first transistor and to the ending node. *Id.*; Ex. 1006 ¶ 181. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

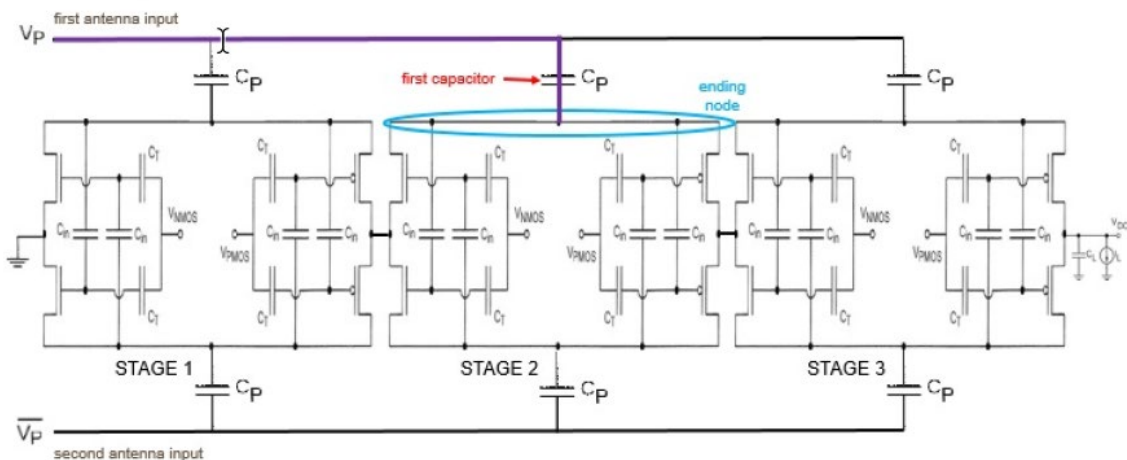
Proposed substitute claim 16 recites “the second antenna input is coupled to the gate of the second transistor and to the beginning node.” Mot. Amend, Appx. A at 1. Petitioner presents the following annotated

figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 84.



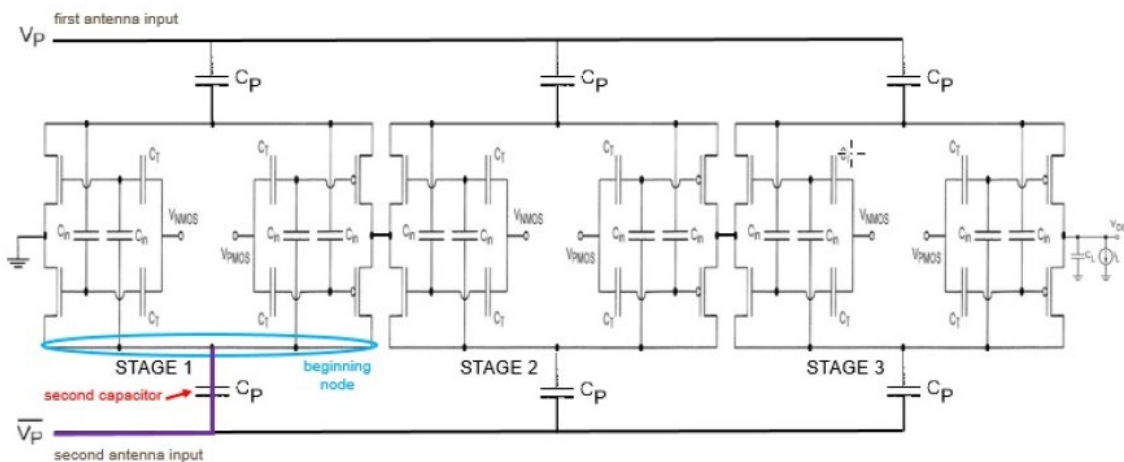
The above figure shows the second antenna input coupled to the gate of the second transistor and to the beginning node. *Id.*; Ex. 1006 ¶ 183. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “the first antenna input is coupled to the ending node via the first capacitor.” Mot. Amend, Appx. A at 2. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 85.



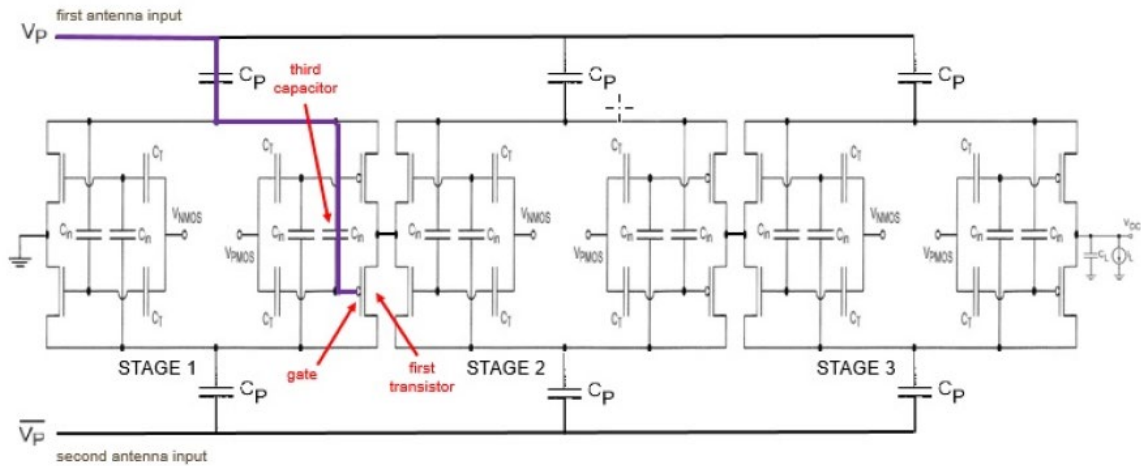
The above figure shows the first antenna input coupled to the ending node via the first capacitor. *Id.*; Ex. 1006 ¶ 184. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “the second antenna input is coupled to the beginning node via the second capacitor.” Mot. Amend, Appx. A at 2. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 86.



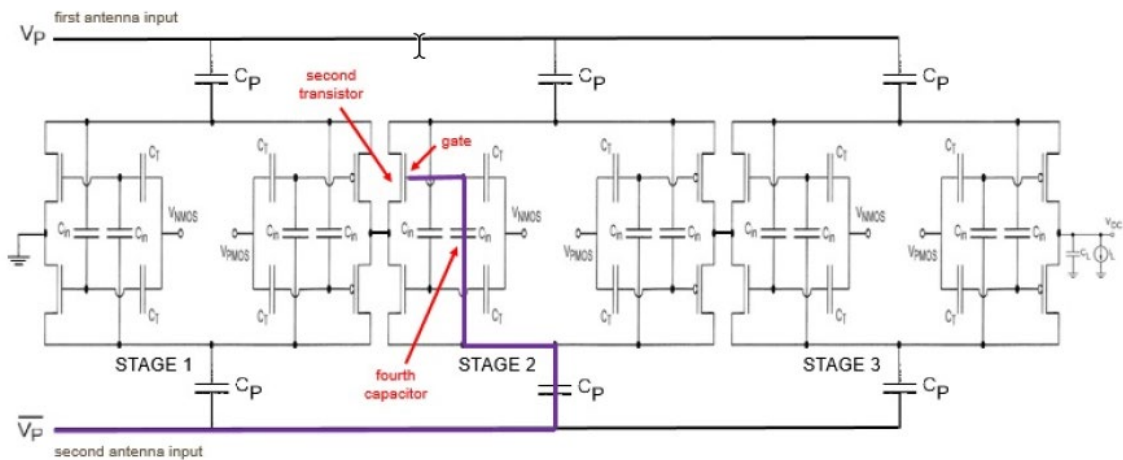
The above figure shows the second antenna input coupled to the beginning node via the second capacitor. *Id.*; Ex. 1006 ¶ 185. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “the first antenna input is coupled to the gate of the first transistor via the third capacitor.” Mot. Amend, Appx. A at 2. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 87.



The above figure shows the first antenna input coupled to the gate of the first transistor via the third capacitor. *Id.*; Ex. 1006 ¶ 186. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “the second antenna input is coupled to the gate of the second transistor via the fourth capacitor.” Mot. Amend, Appx. A at 2. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 88.



The above figure shows the second antenna input coupled to the gate of the second transistor via the fourth capacitor. *Id.*; Ex. 1006 ¶ 188. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 16.

Proposed substitute claim 16 recites “a first, controllable DC bias voltage is coupled between the gate of the first transistor and the averaging node.” Mot. Amend, Appx. A at 2. Oliver teaches a controllable DC bias voltage coupled to the gate of a transistor. Pet. Opp. 6–7; Ex. 1009 ¶¶ 55–57; Ex. 1010 ¶¶ 64–71. As discussed in more detail below, it would have been obvious to a person of ordinary skill in the art to combine the cited teachings of the Mandal '947 patent and Oliver so that Oliver's controllable DC bias voltage is coupled between the gate of the Mandal '947 patent's first transistor and the averaging node. Pet. Opp. 13–14; Ex. 1009 ¶¶ 81–83.

Proposed substitute claim 16 recites “a second, controllable DC bias voltage is coupled between the gate of the second transistor and the averaging node.” Mot. Amend, Appx. A at 2. As discussed above, Oliver teaches a controllable DC bias voltage coupled to the gate of a transistor. Pet. Opp. 6–7; Ex. 1009 ¶¶ 55–57; Ex. 1010 ¶¶ 64–71. As discussed in more detail below, it would have been obvious to a person of ordinary skill in the art to combine the cited teachings of the Mandal '947 patent and Oliver so that Oliver's controllable DC bias voltage is coupled between the gate of the Mandal '947 patent's second transistor and the averaging node. Pet. Opp. 13–14; Ex. 1009 ¶¶ 81–83.

Proposed substitute claim 16 recites “the first and second DC bias voltages are functions of and controlled based on an amplitude of an RF signal on the first and second antenna inputs.” Mot. Amend, Appx. A at 2.

Oliver teaches that the controllable DC bias voltages are adjusted “based on the maximum amplitude of the PHASE1 and PHASE2 signals” that “represent the induced AC voltage in the antenna.” Pet. Opp. 7; Ex. 1009 ¶ 65; Ex. 1010 ¶¶ 47, 64. As discussed in more detail below, it would have been obvious to a person of ordinary skill in the art to combine the cited teachings of the Mandal ’947 patent and Oliver so that Oliver’s controllable DC bias voltages are functions of and controlled based on an amplitude of the RF signal on the Mandal ’947 patent’s first and second antenna inputs. Pet. Opp. 14; Ex. 1009 ¶¶ 84–87.

Patent Owner argues that “the ’857 Patent already describes biasing schemes similar to Oliver in connection with Fig[ures] 7B and 11C, and the line identified as 1403 in Fig[ure] 14.” PO Reply 8 (citing Ex. 1001, 7:8–15, 9:54–57, 10:27–38; Ex. 2007 ¶¶ 68–71). In particular, Patent Owner’s declarant, Dr. Gregory Durgin, states that Oliver’s DC bias voltages “exhibit[] a flat control voltage” similar to “the line labeled PRIOR ART 1403” in the ’857 patent’s Figure 14. Ex. 2007 ¶ 71. Thus, according to Dr. Durgin, Oliver’s DC bias voltages are not “a function of the RF signal amplitude” or “controlled based on that amplitude.” *Id.*

Patent Owner’s argument is unavailing. As discussed above, Oliver teaches that the controllable DC bias voltages are adjusted “*based on the maximum amplitude* of the PHASE1 and PHASE2 signals” that “represent the induced AC voltage in the antenna.” Ex. 1010 ¶¶ 47, 64 (emphasis added). Oliver explains that “the bias voltages . . . are increased in response to higher amplitude PHASE1 and PHASE2 signals,” and, thus, “[w]here the maximum amplitude for the PHASE1 and PHASE2 [signals] continues to increase, the bias currents may eventually be great enough to generate a bias

voltage in excess of the V_t of the transistors.” *Id.* ¶ 64. Thus, Oliver’s controllable DC bias voltages are not flat voltages, but, rather, increase as the maximum amplitude of an RF signal increases. *Id.*; Ex. 1009 ¶¶ 65, 85.

Patent Owner also argues that, “in Oliver, the gate-to-drain voltage does not modulate based on the RF signal.” PO Reply 8 (citing Ex. 2007 ¶¶ 70–71). Specifically, Patent Owner’s declarant, Dr. Durgin, states that Oliver “discusses bias currents that can be adjusted . . . based on a maximum value of Phase 1 and Phase 2,” but “having a dependency based on a maximum value does not account for changes in the RF input . . . that includes *modulations and transitions*.” Ex. 2007 ¶ 70 (emphasis added). According to Patent Owner, “[a] substantially constant biasing voltage would not have accommodated the *abrupt transitions* in the RF signal amplitude and would have been detrimental to optimum performance of the rectifier circuit.” PO Reply 9 (citing Ex. 2007 ¶¶ 44–55) (emphasis added).

Patent Owner’s argument is unavailing. Proposed substitute claim 16 only recites that the controllable DC bias voltages are functions of and controlled “based on an amplitude of an RF signal.” Mot. Amend, Appx. A at 2. Proposed substitute claim 16 does not recite that the controllable DC bias voltages account for modulations and transitions in an RF signal. *See id.* Further, neither Patent Owner nor Dr. Durgin identify any specific portion of the ’857 patent that describes the controllable DC bias voltages as

accounting for modulations and transitions in an RF signal.⁶ *See* Mot. Amend 7–8; PO Reply 8–9 (citing Ex. 1001, 2:1–3, 4:4–13); Ex. 2007 ¶¶ 44–55. For example, Dr. Durgin asserts that the ’857 patent describes controllable DC bias voltages that “detect[] short-term changes in the RF envelope,” but Dr. Durgin does not identify any specific portion of the ’857 patent to support that assertion. Ex. 2007 ¶ 50.

For the foregoing reasons, Petitioner shows sufficiently that the Mandal ’947 patent and Oliver combination teaches the limitations of proposed substitute claim 16.

c. Proposed Substitute Claim 17

Proposed substitute claim 17 depends from proposed substitute claim 16, and recites “an averaging-node capacitor coupling the averaging node to at least one of a ground, a substrate, and another averaging node.” Mot. Amend, Appx. A at 2. As discussed above, the rectifier formed by combining Figures 18 and 25 of the Mandal ’947 patent includes a node where the output of the first transistor is coupled to the input of the second transistor (i.e., the averaging node). Pet. 81–82; Ex. 1006 ¶¶ 176–177. The Mandal ’947 patent teaches that there are “parasitic capacitances to ground” at the rectifier’s nodes. Pet. 101; Ex. 1004, 7:8–13. Thus, the evidence of

⁶ The ’857 patent states that the controllable DC bias voltages “are functions of an amplitude of the RF signal and may be controlled such that the DC output current of the Power Rectifier is substantially maximized for a given RF input power.” Ex. 1001, 7:59–62; *see id.* at 9:64–67. But Patent Owner acknowledged at the oral hearing that proposed substitute claim 16 is not limited to controllable DC bias voltages that are substantially maximized for a given RF input power. Tr. 41:9–16 (“That would be one example of it.”).

record indicates that there is a parasitic capacitance to ground at the averaging node. Pet. 101; Ex. 1006 ¶ 190.

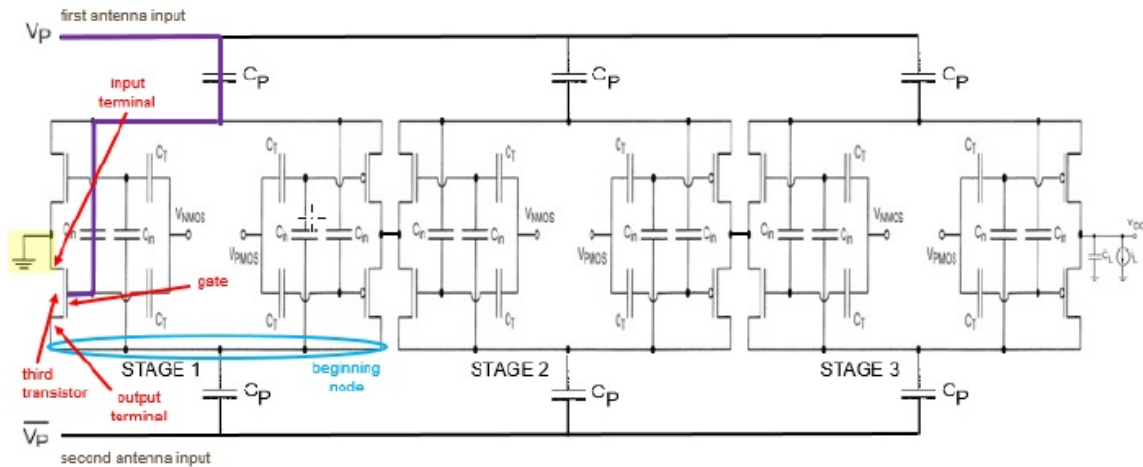
Patent Owner argues that “(1) none of the relied upon circuits in the Mandal references show such a capacitor, (2) [Petitioner’s] conclusory statement, even if presumed true, indicates that such a capacitance *may*, and therefore, *may not* be present, and (3) NXP does not provide a rationale as to why such a capacitance would be present at the claimed location, or why it be would connected to the *ground*.” PO Reply 12 (citing Ex. 2007 ¶¶ 72–75). Patent Owner’s argument is unavailing. The ’857 patent describes the averaging-node capacitor as a parasitic capacitance that couples the averaging node to a ground.⁷ Ex. 1001, Fig. 9B. The Mandal ’947 patent likewise teaches that there are “parasitic capacitances” that couple the rectifier’s nodes (e.g., the averaging node) “*to ground*.” Ex. 1004, 7:8–13 (emphasis added). Thus, the evidence of record indicates that the Mandal ’947 patent’s rectifier includes a parasitic capacitance that couples the averaging node to ground. Ex. 1006 ¶ 190.

d. Proposed Substitute Claim 18

Proposed substitute claim 18 depends from proposed substitute claim 16, and recites “a third transistor including an input terminal, an output terminal, and a gate, wherein the input terminal of the third transistor is coupled to a ground node, the output terminal of the third transistor is coupled to the beginning node, and the gate of the third transistor is coupled to the first antenna input.” Mot. Amend, Appx. A at 2–3. Petitioner

⁷ Patent Owner does not dispute that the claimed “averaging-node capacitor” can be a parasitic capacitance. See PO Reply 12.

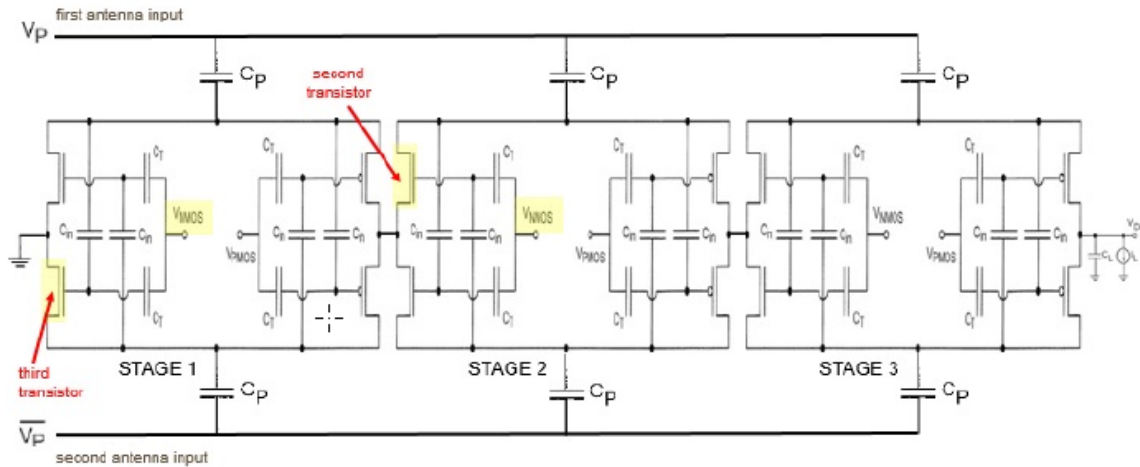
presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 102–103.



The above figure shows a rectifier comprising a third transistor with an input terminal, an output terminal, and a gate. *Id.*; Ex. 1006 ¶ 191. The above figure also shows the input terminal of the third transistor coupled to a ground node, the output terminal of the third transistor coupled to the beginning node, and the gate of the third transistor coupled to the first antenna input. Pet. 102–103; Ex. 1006 ¶ 191. Patent Owner does not dispute that the Mandal '947 patent teaches the limitations of proposed substitute claim 18.

e. Proposed Substitute Claim 19

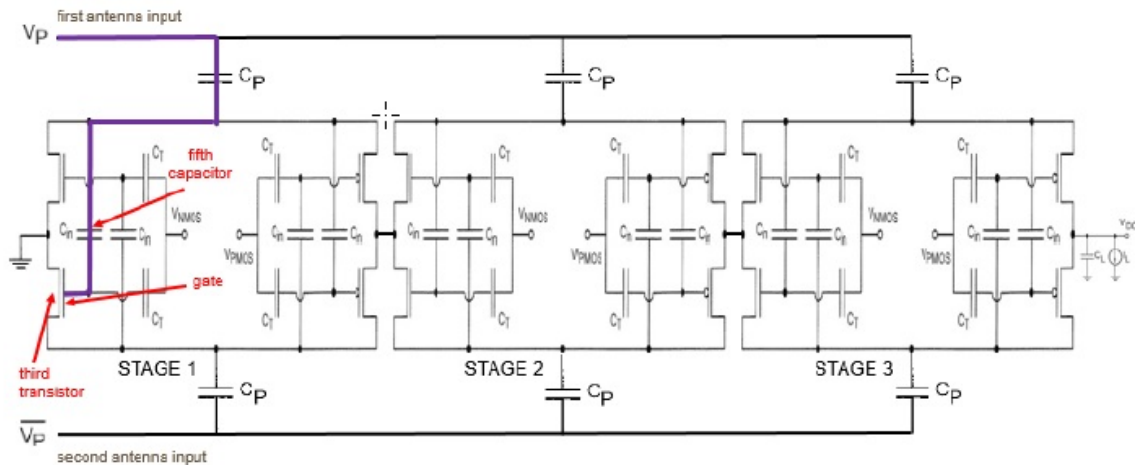
Proposed substitute claim 19 depends from proposed substitute claim 18, and recites “wherein the second and third transistors are of the same type.” Mot. Amend, Appx. A at 3. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 104.



The above figure shows the second transistor and the third transistor. *Id.*; Ex. 1006 ¶ 193. The evidence of record indicates that the second transistor and the third transistor are NMOS transistors, and, thus, the second transistor and the third transistor are of the same type. Pet. 104; Ex. 1006 ¶ 193. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 19.

f. Proposed Substitute Claim 20

Proposed substitute claim 20 depends from proposed substitute claim 18, and recites “a fifth capacitor coupling the first antenna input to the gate of the third transistor.” Mot. Amend, Appx. A at 3. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 105.



The above figure shows a rectifier comprising a fifth capacitor coupling the first antenna input to the gate of the third transistor. *Id.*; Ex. 1006 ¶ 194. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claim 20.

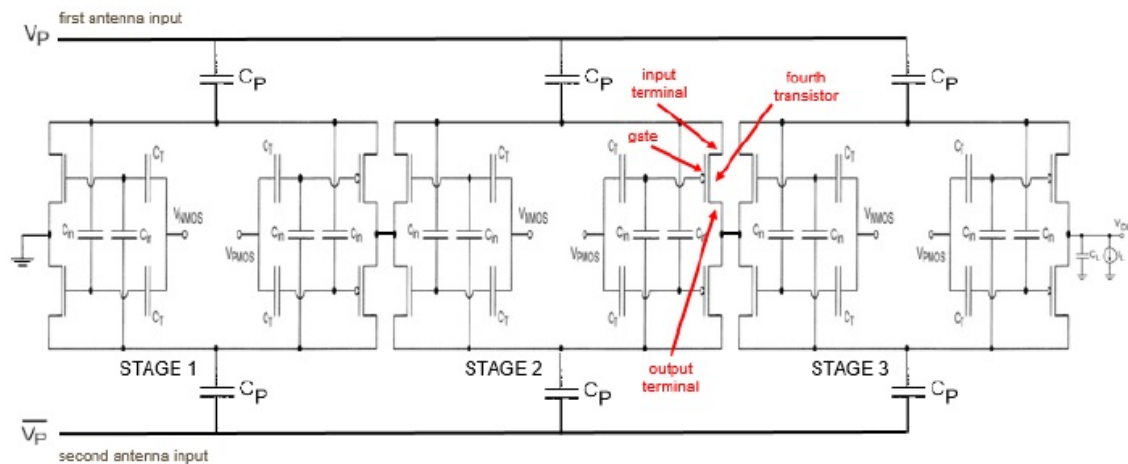
g. Proposed Substitute Claims 21 and 26

Proposed substitute claims 21 and 26 recite limitations similar to those discussed above for proposed substitute claims 16, 18, and 20. Mot. Amend, Appx. A at 3–8. For the same reasons discussed above for proposed substitute claims 16, 18, and 20, Petitioner shows sufficiently that the Mandal '947 patent and Oliver combination teaches the limitations of proposed substitute claims 21 and 26. Pet. 89–101; Pet. Opp. 6–14. Other than the arguments discussed above, Patent Owner does not separately dispute that the Mandal '947 patent and Oliver combination teaches the limitations of proposed substitute claims 21 and 26.

h. Proposed Substitute Claims 22 and 27

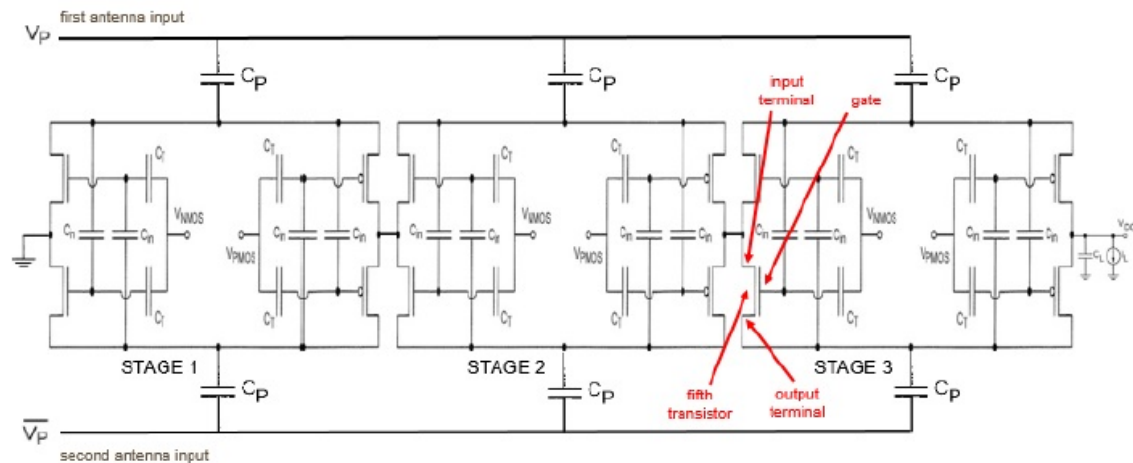
Proposed substitute claim 22 depends from proposed substitute claim 21, and recites “a fourth transistor including an input terminal, an output terminal, and a gate.” Mot. Amend, Appx. A at 5. Proposed substitute

claim 27 depends from proposed substitute claim 26, and recites a similar limitation. *Id.* at 8. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 106–107.



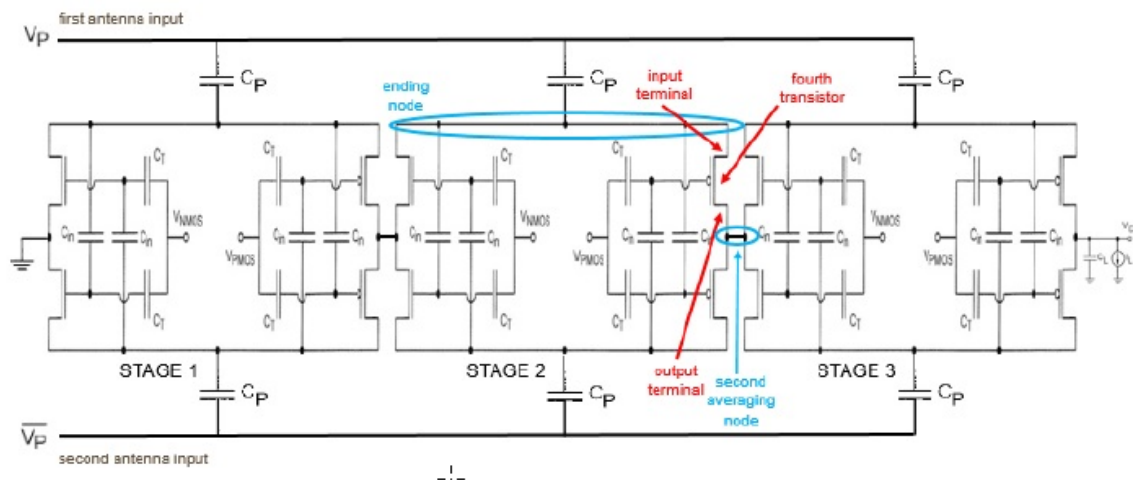
The above figure shows a rectifier comprising a fourth transistor with an input terminal, an output terminal, and a gate. *Id.*; Ex. 1006 ¶ 196. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 22 and 27.

Proposed substitute claim 22 recites “a fifth transistor of a complementary type to the fourth transistor and the first transistor, and including an input terminal, an output terminal, and a gate.” Mot. Amend, Appx. A at 5. Proposed substitute claim 27 recites a similar limitation. *Id.* at 8. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 107–108.



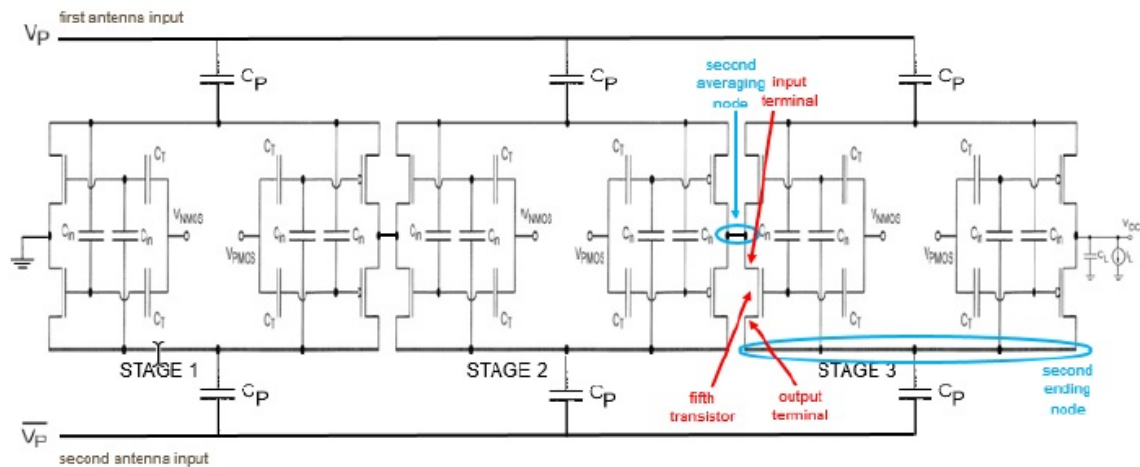
The above figure shows a rectifier comprising a fifth transistor with an input terminal, an output terminal, and a gate. *Id.*; Ex. 1006 ¶ 197. The evidence of record indicates that the fifth transistor is an NMOS transistor and the first and fourth transistors are PMOS transistors, and, thus, the fifth transistor is of a complementary type to the first and fourth transistors. Pet. 108–109; Ex. 1006 ¶ 198. Patent Owner does not dispute that the Mandal ’947 patent teaches this limitation of proposed substitute claims 22 and 27.

Proposed substitute claim 22 recites “the input terminal of the fourth transistor is coupled to the ending node,” and “the output terminal of the fourth transistor is coupled to a second averaging node.” Mot. Amend, Appx. A at 5. Proposed substitute claim 27 recites a similar limitation. *Id.* at 8–9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal ’947 patent. Pet. 110.



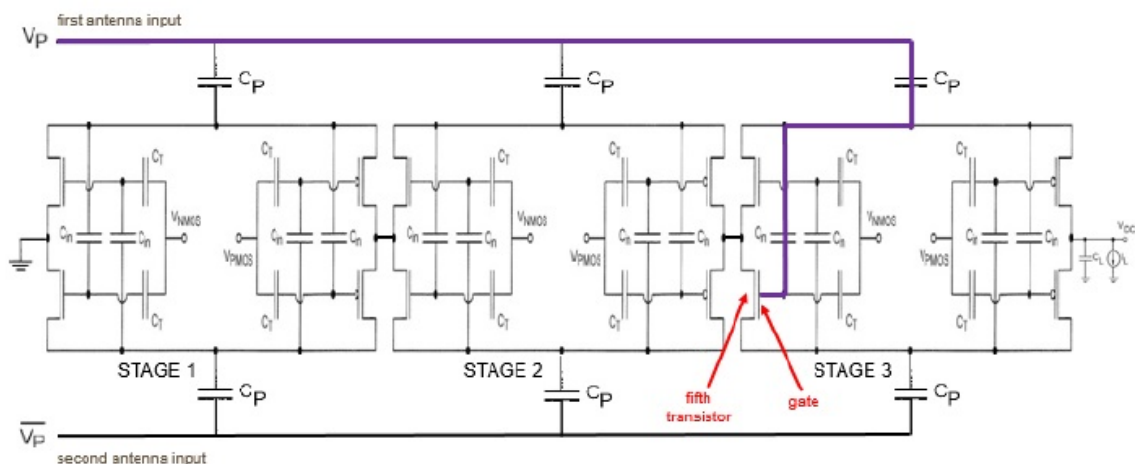
The above figure shows the input terminal of the fourth transistor coupled to the ending node and the output terminal of the fourth transistor coupled to a second averaging node. *Id.*; Ex. 1006 ¶ 199. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 22 and 27.

Proposed substitute claim 22 recites “the input terminal of the fifth transistor is coupled to the second averaging node,” and “the output terminal of the fifth transistor is coupled to a second ending node.” Mot. Amend, Appx. A at 5. Proposed substitute claim 27 recites a similar limitation. *Id.* at 9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 111.



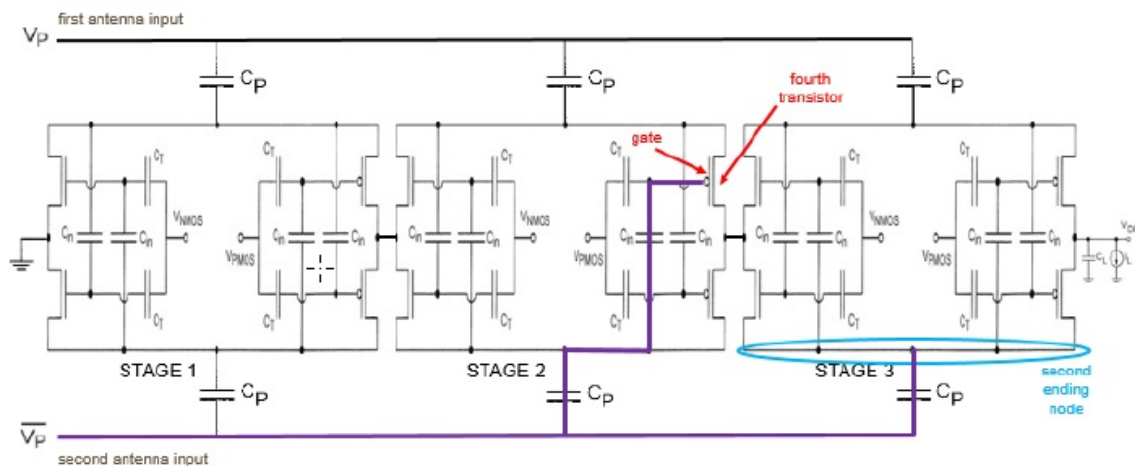
The above figure shows the input terminal of the fifth transistor coupled to the second averaging node and the output terminal of the fifth transistor coupled to a second ending node. *Id.*; Ex. 1006 ¶ 200. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 22 and 27.

Proposed substitute claim 22 recites “the first antenna input is further coupled to the gate of the fifth transistor.” Mot. Amend, Appx. A at 5. Proposed substitute claim 27 recites a similar limitation. *Id.* at 9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 112.



The above figure shows the first antenna input coupled to the gate of the fifth transistor. *Id.*; Ex. 1006 ¶ 201. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 22 and 27.

Proposed substitute claim 22 recites “the second antenna input is further coupled to the gate of the fourth transistor and the second ending node.” Mot. Amend, Appx. A at 5. Proposed substitute claim 27 recites a similar limitation. *Id.* at 9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 113.

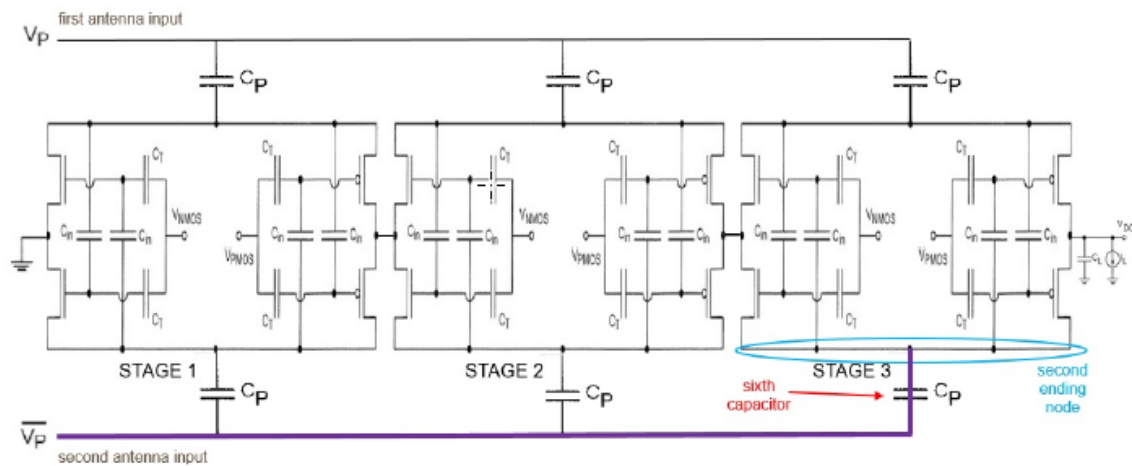


The above figure shows the second antenna input coupled to the gate of the fourth transistor and the second ending node. *Id.*; Ex. 1006 ¶ 202. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 22 and 27.

i. Proposed Substitute Claims 23 and 28

Proposed substitute claim 23 depends from proposed substitute claim 22, and recites “a sixth capacitor coupling the second antenna input to the second ending node.” Mot. Amend, Appx. A at 6. Proposed substitute

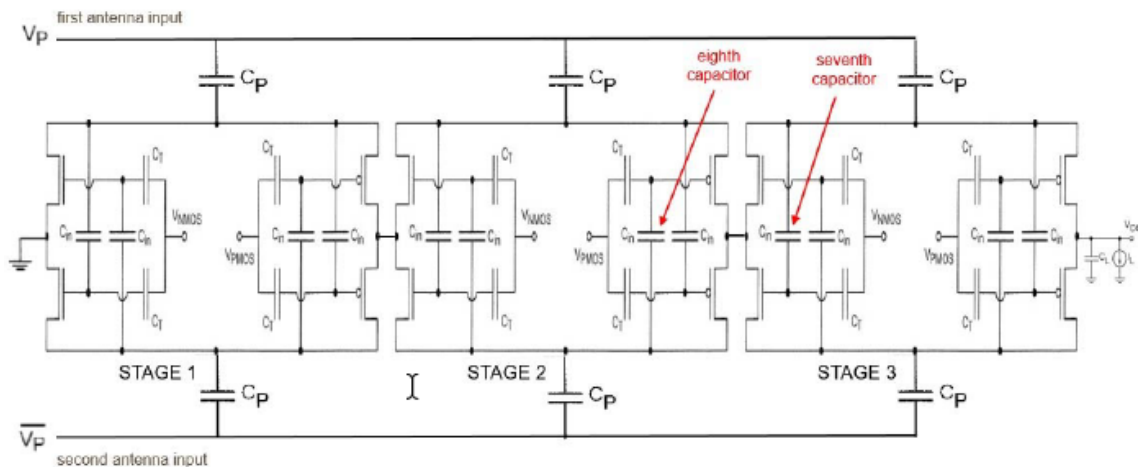
claim 28 depends from proposed substitute claim 27, and recites a similar limitation. *Id.* at 9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 114.



The above figure shows a rectifier comprising a sixth capacitor coupling the second antenna input to the second ending node. *Id.*; Ex. 1006 ¶ 204. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 23 and 28.

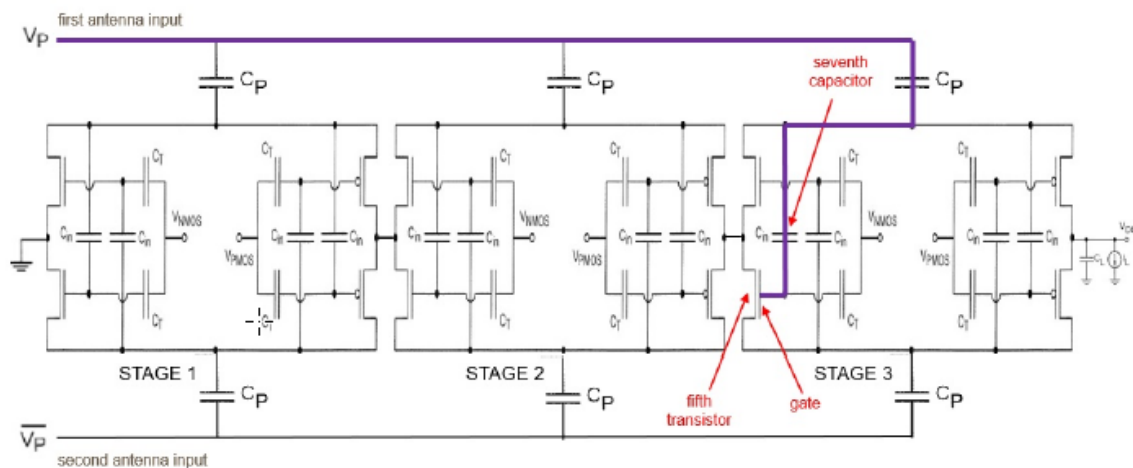
j. Proposed Substitute Claims 24 and 29

Proposed substitute claim 24 depends from proposed substitute claim 23, and recites “seventh and eighth capacitors.” Mot. Amend, Appx. A at 6. Proposed substitute claim 29 depends from proposed substitute claim 28, and recites a similar limitation. *Id.* at 9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 115–116.



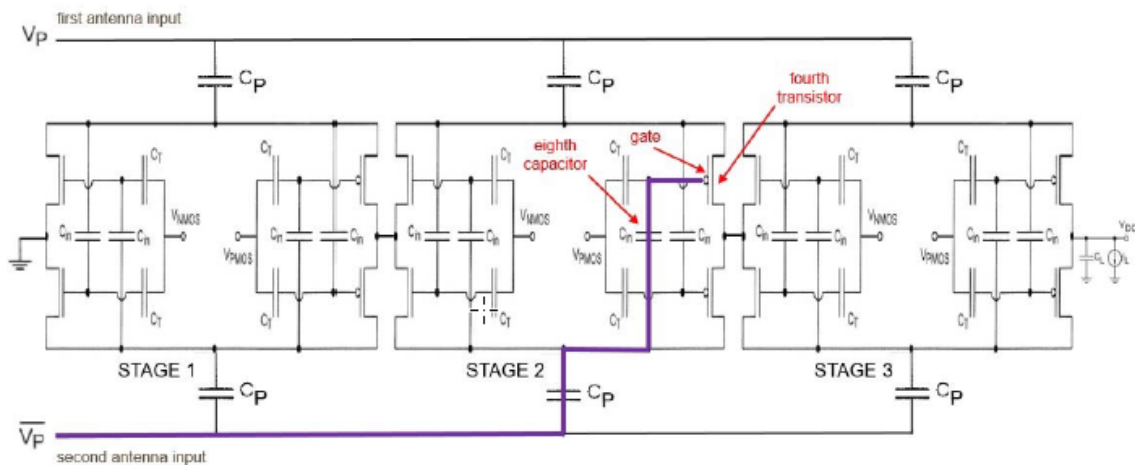
The above figure shows a rectifier comprising seventh and eighth capacitors. *Id.*; Ex. 1006 ¶ 206. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 24 and 29.

Proposed substitute claim 24 recites “the first antenna input is coupled to the gate of the fifth transistor via the seventh capacitor.” Mot. Amend, Appx. A at 6. Proposed substitute claim 29 recites a similar limitation. *Id.* at 9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 116–117.



The above figure shows the first antenna input coupled to the gate of the fifth transistor via the seventh capacitor. *Id.*; Ex. 1006 ¶ 207. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 24 and 29.

Proposed substitute claim 24 recites “the second antenna input is coupled to the gate of the fourth transistor via the eighth capacitor.” Mot. Amend, Appx. A at 6. Proposed substitute claim 29 recites a similar limitation. *Id.* at 9. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 18 and 25 of the Mandal '947 patent. Pet. 117–118.



The above figure shows the second antenna input coupled to the gate of the fourth transistor via the eighth capacitor. *Id.*; Ex. 1006 ¶ 208. Patent Owner does not dispute that the Mandal '947 patent teaches this limitation of proposed substitute claims 24 and 29.

k. Proposed Substitute Claims 25 and 30

Proposed substitute claim 25 depends from proposed substitute claim 22, and recites “a second averaging node capacitor coupling the second averaging node to at least one of a ground, a substrate, and a different

averaging node.” Mot. Amend, Appx. A at 6. Proposed substitute claim 30 depends from proposed substitute claim 26, and recites a similar limitation. *Id.* at 9–10. As discussed above, the rectifier formed by combining Figures 18 and 25 of the Mandal ’947 patent includes a node where the output of the fourth transistor is coupled to the input of the fifth transistor (i.e., the second averaging node). Pet. 110–111; Ex. 1006 ¶¶ 199–200. The Mandal ’947 patent teaches that there are “parasitic capacitances to ground” at the rectifier’s nodes. Pet. 118–119; Ex. 1004, 7:8–13. Thus, the evidence of record indicates that there is a parasitic capacitance to ground at the second averaging node. Pet. 119; Ex. 1006 ¶ 210.

Patent Owner responds with the same argument discussed above for proposed substitute claim 17. PO Reply 12; *see* Section II.E.1.c. Patent Owner’s argument is unavailing for the same reasons discussed above for proposed substitute claim 17. *See* Section II.E.1.c.

l. Reasons for Combining the Mandal ’947 Patent and Oliver

Petitioner presents evidence that a person of ordinary skill in the art would have had reason to combine the cited teachings of the Mandal ’947 patent and Oliver. Pet. Opp. 9–14 (citing Ex. 1009 ¶¶ 71–89). We agree with Petitioner’s rationale. Specifically, the Mandal ’947 patent and Oliver relate to the same field of endeavor as the ’875 patent, namely, using a multi-stage rectifier for an RFID tag. Pet. 1–2, 12–13; Pet. Opp. 6, 10; Ex. 1001, 1:14–16, 7:16–18, Fig. 8A; Ex. 1004, 1:22–26, 11:44–46, Fig. 18; Ex. 1009 ¶ 73; Ex. 1010 ¶¶ 2, 47, Fig. 5. Further, it would have been obvious to incorporate Oliver’s controllable DC bias voltage into the Mandal ’947 patent’s rectifier because doing so would have improved the Mandal ’947 patent’s rectifier. Pet. Opp. 10; Ex. 1009 ¶¶ 71–73. Specifically, the

Mandal '947 patent states that “for a particular rectifier topology, there exists an optimum threshold voltage” that “increases with the RF amplitude.” Ex. 1004, 13:54–58. Oliver teaches that its controllable DC bias voltage “enable[s] the bias voltage applied to the gate of a transistor to be adjusted to optimize operation,” for example, by increasing the bias voltage as the maximum amplitude of the RF input increases. Ex. 1010 ¶¶ 56, 64. Thus, Oliver’s controllable DC bias voltage would have improved the Mandal '947 patent’s rectifier by enabling adjustment of the bias voltage to improve efficiency and optimize operation. Ex. 1009 ¶ 73.

Petitioner also presents evidence showing how a person of ordinary skill in the art would have combined the cited teachings of the Mandal '947 patent and Oliver. Pet. Opp. 13–14; Ex. 1009 ¶¶ 81–87. Specifically, it would have been obvious to combine the Mandal '947 patent and Oliver so that 1) a controllable DC bias voltage is coupled between the gate of the Mandal '947 patent’s first transistor and the averaging node; and 2) a controllable DC bias voltage is coupled between the gate of the Mandal '947 patent’s second transistor and the averaging node. Pet. Opp. 13–14; Ex. 1009 ¶¶ 81–82. Doing so would have been obvious because coupling the DC bias voltages to the gates of the first and second transistors provides control over the biasing of those transistors, and coupling the DC bias voltages to the averaging node is convenient because the averaging node is located between the first and second transistors. Pet. Opp. 14; Ex. 1009 ¶ 82.

It also would have been obvious to a person of ordinary skill in the art to combine the cited teachings of the Mandal '947 patent and Oliver so that Oliver’s controllable DC bias voltages are functions of and controlled based

on an amplitude of the RF signal on the Mandal '947 patent's first and second antenna inputs. Pet. Opp. 14; Ex. 1009 ¶¶ 84–87. Doing so would have been obvious because Oliver teaches this specific arrangement. Pet. Opp. 14; Ex. 1009 ¶¶ 85–87. As discussed above, Oliver teaches that the controllable DC bias voltages are adjusted “based on the maximum amplitude of the PHASE1 and PHASE2 signals” that “represent the induced AC voltage in the antenna.” Ex. 1009 ¶ 85; Ex. 1010 ¶¶ 47, 64.

Patent Owner argues that a person of ordinary skill in the art would not have had a reason to combine the cited teachings of the Mandal '947 patent and Oliver. PO Reply 6–8. Specifically, Patent Owner contends that the Mandal '947 patent already describes a procedure for “making adjustments to threshold voltages in very specific ways, and thus a [person of ordinary skill in the art] would not have found further tweaking of the threshold voltages a reason for combination with Oliver.” *Id.* at 7–8 (citing Ex. 2007 ¶¶ 62–67). For example, according to Patent Owner, the Mandal '947 patent describes using “one-time programming voltages” and “the uphill simplex method” to find the optimum threshold voltage.⁸ *Id.* at 7 (citing Ex. 1004, 14:4–32).

⁸ Patent Owner also argues that a different reference—the Mandal Thesis—“disparages tweaking the threshold voltages as not being too robust.” PO Reply 6–7 (citing Ex. 1003, 93). We disagree. The Mandal Thesis states that “further gains in performance (which may not be too robust) are expected if one continues to tweak threshold voltages about the optimum point.” Ex. 1003, 93. In other words, the Mandal Thesis acknowledges that tweaking threshold voltages can be expected to improve a rectifier's performance to at least some degree. *Id.* Thus, we are not persuaded that the Mandal Thesis teaches away from tweaking threshold voltages.

Patent Owner's argument is unavailing. The portion of the Mandal '947 patent cited by Patent Owner describes a process for "find[ing] the optimum threshold voltage for the rectifier." Ex. 1004, 14:4–32. But that portion of the Mandal '947 patent does not describe adjusting a bias voltage as the RF input changes. *See id.* On the other hand, Oliver teaches a controllable DC bias voltage that adjusts the bias voltage when the maximum amplitude of the RF input changes, for example, by increasing the bias voltage when the maximum amplitude of the RF input increases. Ex. 1010 ¶ 64. As discussed above, Oliver's controllable DC bias voltage would have improved the Mandal '947 patent's rectifier by enabling adjustment of the bias voltage to improve efficiency and optimize operation when the maximum amplitude of the RF input changes. Ex. 1009 ¶ 73.

Patent Owner also argues that Petitioner does not explain how a person of ordinary skill in the art would have combined the cited teachings of the Mandal '947 patent and Oliver. PO Reply 8. Patent Owner contends that Petitioner "fails to provide any circuit diagrams illustrating how Oliver and Mandal circuits can be combined, or specific connection points in any combined circuits." *Id.*

Patent Owner's argument is unavailing. As discussed above, Petitioner explains specifically how a person of ordinary skill in the art would have incorporated Oliver's controllable DC bias voltages into the Mandal '947 patent's rectifier. Pet. Opp. 13–14; Ex. 1009 ¶¶ 81–87. Petitioner shows that it would have been obvious to combine the Mandal '947 patent and Oliver so that 1) a controllable DC bias voltage is coupled between the gate of the Mandal '947 patent's first transistor and the averaging node; and 2) a controllable DC bias voltage is coupled between

the gate of the Mandal '947 patent's second transistor and the averaging node. Pet. Opp. 13–14; Ex. 1009 ¶¶ 81–82. Petitioner also shows that it would have been obvious to combine the Mandal '947 patent and Oliver so that Oliver's controllable DC bias voltages are functions of and controlled based on an amplitude of the RF signal on the Mandal '947 patent's first and second antenna inputs. Pet. Opp. 14; Ex. 1009 ¶¶ 84–87.

m. Summary

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that proposed substitute claims 16–30 would have been obvious over the Mandal '947 Patent and Oliver.

2. Obviousness of Proposed Substitute Claims 16–30 over the Mandal '947 Patent and Kotani

Petitioner argues that proposed substitute claims 16–30 would have been obvious over the Mandal '947 patent and Kotani. Pet. 64–120; Pet. Opp. 14–20. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that proposed substitute claims 16–30 would have been obvious over the Mandal '947 patent and Kotani.

a. Overview of Kotani

Kotani describes a multi-stage rectifier “for converting an alternating current signal into direct current power.” Ex. 1011 ¶ 1. Kotani's Figure 1 is reproduced below. *Id.* at Fig. 1.

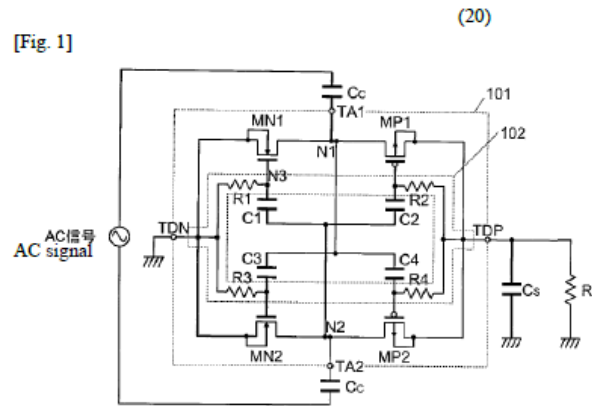


Figure 1 depicts rectifier cell 101 that includes transistors MN1, MN2, MP1, MP2. *Id.* ¶ 40. Rectifier cell 101 also includes bias circuit 102 for setting the DC potential of the gates of transistors MN1, MN2, MP1, MP2. *Id.* ¶ 42. Kotani's Figure 9 is reproduced below. *Id.* at Fig. 9.

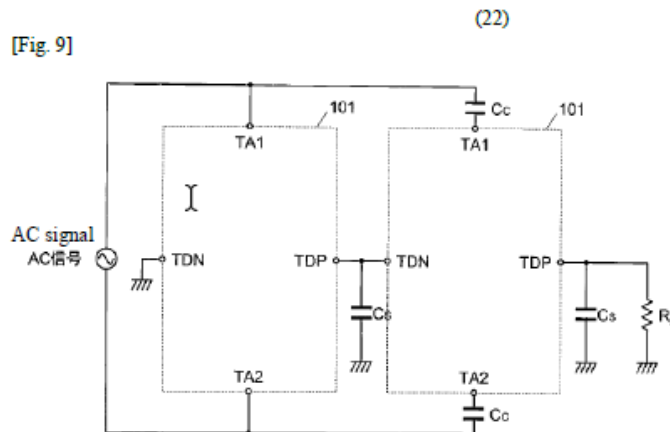


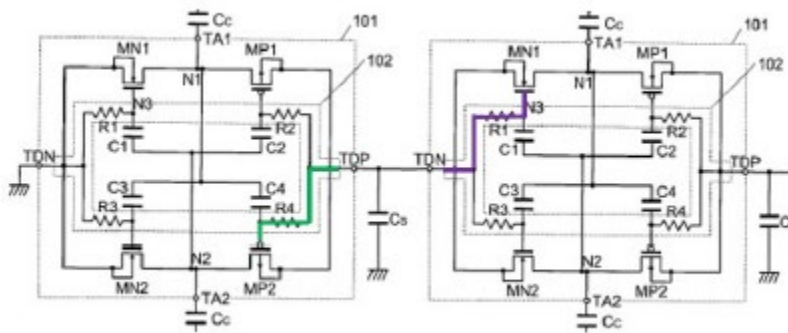
Figure 9 depicts a two-stage rectifier circuit formed using two of the rectifier cells shown in Figure 1. *Id.* ¶ 127.

b. Proposed Substitute Claims 16, 21, and 26

Petitioner relies on the same arguments and evidence discussed above for the Mandal '947 patent for most of the limitations of proposed substitute claims 16, 21, and 26. Pet. 64–101; Pet. Opp. 15; *see* Sections II.E.1.b, II.E.1.g. As discussed above, Petitioner's arguments and evidence show that

the Mandal '947 patent teaches those limitations of proposed substitute claims 16, 21, and 26. *See* Sections II.E.1.b, II.E.1.g. Patent Owner's arguments regarding those limitations are unavailing for the same reasons discussed above. *See id.* Petitioner relies on Kotani for the underlined limitations that Patent Owner seeks to add in proposed substitute claims 16, 21, and 26 in the Motion to Amend (Pet. Opp. 15–20), and, thus, we discuss those limitations below.

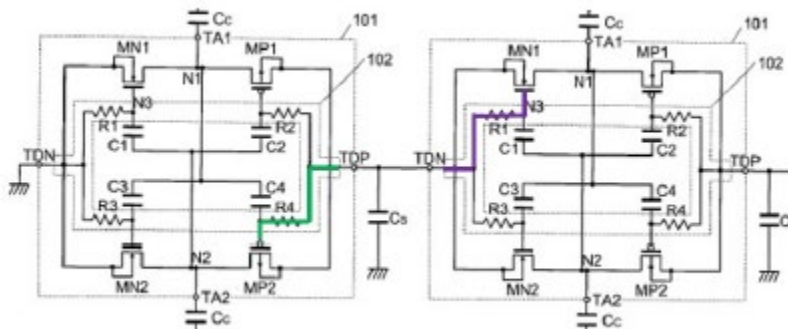
Proposed substitute claim 16 recites “a first, controllable DC bias voltage is coupled between the gate of the first transistor and the averaging node,” and “a second, controllable DC bias voltage is coupled between the gate of the second transistor and the averaging node.” Mot. Amend, Appx. A at 2. Proposed substitute claims 21 and 26 recite similar limitations. *Id.* at 4, 8. Kotani's Figure 1 teaches a rectifier cell, and Kotani's Figure 9 teaches a two-stage rectifier formed by using two of the rectifier cells in Figure 1. Pet. Opp. 15–16; Ex. 1011 ¶¶ 40, 127, Figs. 1, 9. The evidence of record shows that the transistor cell in Kotani's Figure 1 can be inserted into each stage of the rectifier in Kotani's Figure 9. Pet. Opp. 18–19; Ex. 1009 ¶ 105. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 1 and 9 of Kotani. Pet. Opp. 18–19.



The above figure shows first transistor MP2, second transistor MN1, and an averaging node between TDP and TDN. Pet. Opp. 18–19; Ex. 1009 ¶ 105.

The above figure also shows a first, controllable DC bias voltage coupled between the gate of first transistor MP2 and the averaging node via resistor R4, and a second, controllable DC bias voltage coupled between the gate of second transistor MN1 and the averaging node via resistor R1. Pet. Opp. 16, 18–19; Ex. 1009 ¶¶ 104–105; Ex. 1011 ¶ 42. As discussed in more detail below, it would have been obvious to a person of ordinary skill in the art to combine the cited teachings of the Mandal '947 patent and Kotani so that 1) a controllable DC bias voltage is coupled between the gate of the Mandal '947 patent's first transistor and the averaging node; and 2) a controllable DC bias voltage is coupled between the gate of the Mandal '947 patent's second transistor and the averaging node. Pet. Opp. 17–18; Ex. 1009 ¶ 99.

Proposed substitute claim 16 recites “the first and second DC bias voltages are functions of and controlled based on an amplitude of an RF signal on the first and second antenna inputs.” Mot. Amend, Appx. A at 2. Proposed substitute claims 21 and 26 recite a similar limitation. *Id.* at 5, 8. Petitioner presents the following annotated figure showing the rectifier formed by combining Figures 1 and 9 of Kotani. Pet. Opp. 18–19.



The above figure shows that the DC bias voltage at the gate of first transistor MP2 is based on the DC voltage at TDP and the value of resistor R4, and that the DC bias voltage at the gate of second transistor MN1 is based on the DC voltage at TDP and the value of resistor R1. Pet. Opp. 19–20; Ex. 1009 ¶ 107. Further, Kotani teaches that the DC voltages at TDN and TDP are “obtained by rectifying an alternating current signal” from AC terminals TA1 and TA2. Pet. Opp. 19–20; Ex. 1009 ¶ 107; Ex. 1011 ¶¶ 40, 130. As a result, the DC voltages at TDN and TDP (and, thus, the DC bias voltages at the gates of the first and second transistors) are functions of and controlled based on an amplitude of an RF signal at the antenna inputs. Pet. Opp. 19–20; Ex. 1009 ¶ 107.

Patent Owner responds that Kotani’s DC bias voltages are not functions of or controlled based on an amplitude of an RF signal. PO Reply 4–6. Specifically, Patent Owner argues that Kotani’s resistor R1 “is selected such that the gate and the TDN remain at the same voltage potential, and thus any purported DC bias that is established by [resistor] R1 in Kotani would remain static.” *Id.* at 4–5 (citing Ex. 1011 ¶ 46; Ex. 2007 ¶¶ 32–35, 41–43, 48–55). According to Patent Owner, because the DC bias voltage at the gate of a transistor is static, the DC bias voltage is “not a function of the RF signal.” *Id.* at 5.

Patent Owner’s argument is unavailing. The portion of Kotani cited by Patent Owner states that “[t]he resistance R1 is for connecting the gate electrode of the N-channel MOS transistor MN1 to the direct current terminal TDN, . . . and making the direct current potential the same as that of the direct current terminal TDN.” Ex. 1011 ¶ 46. In other words, Kotani teaches that the DC potential at the gate of transistor MN1 is the same as the

DC potential at TDN. *Id.* Although the DC potential at those points in the rectifier may be the same, the cited portion of Kotani does not state that the DC potential is static. *See id.* Rather, as discussed above, Kotani teaches that the DC voltages at TDN and TDP are “obtained by rectifying an alternating current signal” from AC terminals TA1 and TA2. Ex. 1009 ¶ 107; Ex. 1011 ¶¶ 40, 130. Thus, the DC voltage at TDN (and, thus, the gate of transistor MN1) changes based on the RF signal from which the DC voltage is obtained. Ex. 1009 ¶ 107.

For the foregoing reasons, Petitioner shows sufficiently that the Mandal ’947 patent and Kotani combination teaches the limitations of proposed substitute claim 16.

c. Proposed Substitute Claims 17–20, 22–25, and 27–30

Petitioner relies on the same arguments and evidence discussed above for the Mandal ’947 patent for the limitations of proposed substitute claims 17–20, 22–25, and 27–30. Pet. 101–120; *see* Sections II.E.1.c–II.E.1.f, II.E.1.h–II.E.1.k. As discussed above, Petitioner’s arguments and evidence show that the Mandal ’947 patent teaches the limitations of proposed substitute claims 17–20, 22–25, and 27–30. *See* Sections II.E.1.c–II.E.1.f, II.E.1.h–II.E.1.k. Patent Owner’s arguments regarding those claims are unavailing for the same reasons discussed above. *See id.*

d. Reasons for Combining the Mandal ’947 Patent and Kotani

Petitioner presents evidence that a person of ordinary skill in the art would have had reason to combine the cited teachings of the Mandal ’947 patent and Kotani. Pet. Opp. 15–20 (citing Ex. 1009 ¶¶ 91–109). We agree with Petitioner’s rationale. Specifically, the Mandal ’947 patent and Kotani

relate to the same field of endeavor as the '875 patent, namely, using a multi-stage rectifier for an RFID tag. Pet. 1–2, 12–13; Pet. Opp. 15–16; Ex. 1001, 1:14–16, 7:16–18, Fig. 8A; Ex. 1004, 1:22–26, 11:44–46, Fig. 18; Ex. 1009 ¶¶ 91; Ex. 1011 ¶¶ 1, 38, 127. Further, it would have been obvious to a person of ordinary skill in the art to incorporate Kotani's controllable DC bias voltage into the Mandal '947 patent's rectifier because doing so would have improved the Mandal '947 patent's rectifier by improving its efficiency and optimizing its power conversion. Pet. Opp. 16–18; Ex. 1009 ¶¶ 96–97, 99; Ex. 1011 ¶¶ 38, 85. Patent Owner does not dispute that it would have been obvious to combine the cited teachings of the Mandal '947 patent and Kotani.

Petitioner also presents evidence showing how a person of ordinary skill in the art would have combined the cited teachings of the Mandal '947 patent and Kotani. Pet. Opp. 17–20; Ex. 1009 ¶¶ 99, 104–105, 107. Specifically, it would have been obvious to a person of ordinary skill in the art to combine the cited teachings of the Mandal '947 patent and Kotani so that 1) a controllable DC bias voltage is coupled between the gate of the Mandal '947 patent's first transistor and the averaging node; 2) a controllable DC bias voltage is coupled between the gate of the Mandal '947 patent's second transistor and the averaging node; and 3) the controllable DC bias voltages are functions of and controlled based on an amplitude of the RF signal on the Mandal '947 patent's first and second antenna inputs. Pet. Opp. 17–20; Ex. 1009 ¶¶ 99, 104–105, 107. Doing so would have been obvious because Kotani teaches this specific arrangement. Pet. Opp. 17–20; Ex. 1009 ¶¶ 99, 104–105, 107.

e. Summary

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that proposed substitute claims 16–30 would have been obvious over the Mandal ’947 patent and Kotani.

3. Other Asserted Grounds

Petitioner also argues that proposed substitute claims 16–30 would have been obvious over 1) the Mandal Thesis; 2) the Mandal Thesis and Oliver; 3) the Mandal Thesis and Kotani; and 4) Kotani, and that proposed substitute claims 16–30 are unpatentable for lack of enablement. Pet. Opp. 2–14, 20–25. Because Petitioner has shown that proposed substitute claims 16–30 are unpatentable based on the asserted grounds discussed above, we do not reach these additional asserted grounds. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (“The Commission . . . is at perfect liberty to reach a ‘no violation’ determination on a single dispositive issue.”); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (recognizing that “[t]he Board has the discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”).

4. Summary

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that proposed substitute claims 16–30 are unpatentable, and, thus, we deny Patent Owner’s request to add proposed substitute claims 16–30.

III. CONCLUSION⁹

We grant Patent Owner's non-contingent request to cancel original claims 1–15, and we deny Patent Owner's request to add proposed substitute claims 16–30.

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–15	103	Mandal Thesis ¹⁰		
1–15	102(a), (e)	Mandal '947 patent ¹¹		
Overall Outcome				

Motion to Amend Outcome	Claims
Original Claims Cancelled by Amendment	1–15
Substitute Claims Proposed in the Amendment	16–30
Substitute Claims: Motion to Amend Granted	
Substitute Claims: Motion to Amend Denied	16–30
Substitute Claims: Not Reached	

⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

¹⁰ We do not reach this asserted ground. See Section II.D.

¹¹ We do not reach this asserted ground. See Section II.D.

IV. ORDER

It is hereby

ORDERED that Patent Owner's Motion to Amend is *granted* as to the non-contingent request to cancel original claims 1–15;

FURTHER ORDERED that Patent Owner's Motion to Amend is *denied* as to the request to add proposed substitute claims 16–30; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-00544
Patent 8,344,857 B1

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