

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

INVENSAS CORPORATION,
Patent Owner.

IPR2020-00603¹
Patent 6,232,231 B1

Before MICHAEL R. ZECHER, BRYAN F. MOORE, AND LYNNE E.
PETTIGREW, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Semiconductor Components Industries, LLC d/b/a ON Semiconductor, the petitioner in IPR2020-01729, is joined as a party to this proceeding.

I. INTRODUCTION

NVIDIA Corporation (“Petitioner”) requested an *inter partes* review (“IPR”) of claims 1–8 (the “challenged claims”) of U.S. Patent No. 6,232,231 B1 (Ex. 1001, “the ’231 patent”). Paper 1 (“Petition” or “Pet.”). Invensas Corporation (“Patent Owner”) filed a Corrected Preliminary Response. Paper 8 (“Prelim. Resp.”). Additionally, pursuant to our authorization, Petitioner filed a Reply addressing the factors laid out in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). Paper 9. Patent Owner filed a Sur-Reply also addressing the *Fintiv* factors. Paper 10.

On September 3, 2020, we instituted trial. Paper 11 (“Inst. Dec.” or “Decision to Institute”). Patent Owner filed a Response. Paper 30 (“PO Resp.”). Petitioner filed a Reply. Paper 36 (“Reply”). Patent Owner filed a Sur-Reply. Paper 45 (“Sur-Reply”). An oral argument was held on June 9, 2021, and a transcript was entered into the record. Paper 51 (“Tr.”).

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–8 of the ’231 patent are unpatentable.

II. BACKGROUND

A. *The Challenged Patent (Ex. 1001)*

The ’231 patent relates to manufacturing interconnects in integrated circuits. Ex. 1001, 1:8–10. A process known as chemical-mechanical polishing (“CMP”) is used to form a planarized layer during manufacturing of integrated circuit interconnects. *Id.* at 1:49–54. The ’231 patent describes undesirable elevational disparities that may result during this process,

making it difficult to print high resolution features. *Id.* at 1:28–48. In particular, the '231 patent describes two such disparities: (i) metal “dishing” and (ii) oxide erosion. *Id.* at 2:67–3:1, 3:24–27. Figure 4 of the '231 patent is reproduced below.

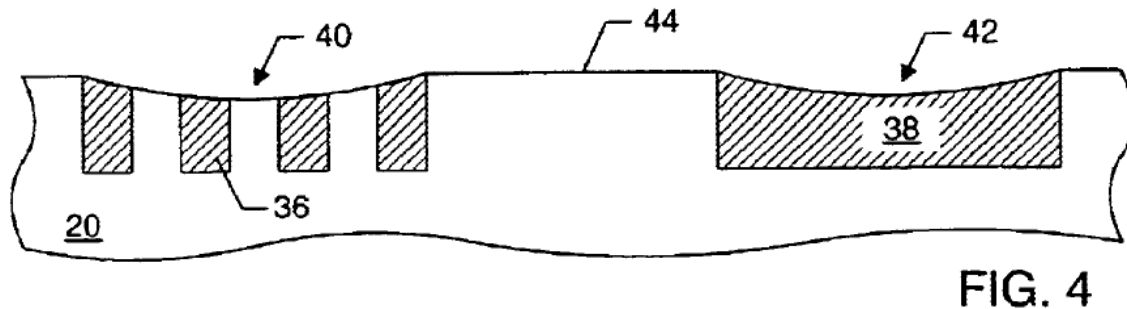


Figure 4 depicts a series of relatively narrow interconnects 36 formed in narrow trenches and relatively wide interconnect 38 formed in a wide trench. *Id.* at 2:53–59. Narrow interconnects 36 electrically connect underlying active devices with conductive elements of the semiconductor. *Id.* at 2:59–61. Wide interconnect 38 serves as, *inter alia*, a bond pad. *Id.* at 2:61–62.

Recessed area 42 depicts a localized thinning or “dishing” problem experienced by conventional metal CMP processes. *Id.* at 2:34–36, 2:67–3:1. The metal dishing causing recessed area 42 results from the polishing pad used in the CMP process flexing or conforming to initial deformities in the metal used to create interconnect 38. *Id.* at 3:1–22.

Recessed area 40 depicts a disparity known as oxide erosion. *Id.* at 3:24–27. Dielectric 20 is composed of silicon oxide. *Id.* at 3:26–27. During the CMP process, an abrasive chemical is used to polish the metal of narrow interconnects 36. *Id.* at 3:27–30. A component of this chemical reacts with the metal at a faster rate than with the silicon oxide, creating metal “steps” below the level of the oxide. *Id.* at 3:30–35. The polishing pad used in the

CMP process removes oxide surrounding the “steps,” resulting in recessed area 40. *Id.* at 3:35–42.

The '231 patent seeks to avoid metal dishing and oxide erosion through “a polishing process which can achieve global planarization across the entire topological surface of an interconnect level.” *Id.* at 3:43–45. The '231 patent discloses “placing a plurality of dummy conductors in a dielectric layer between a region defined by a relatively wide interconnect and another region defined by a series of relatively narrow interconnect.” *Id.* at 3:64–4:3. Figure 7 of the '231 patent is reproduced below.

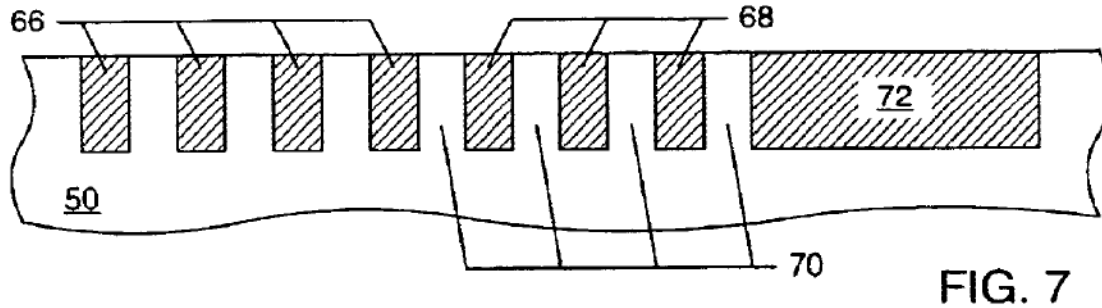


Figure 7 depicts a series of relatively narrow interconnects 66, a series of dummy conductors 68, and relatively wide interconnect 72. *Id.* at 7:49–51. Dummy conductors 68 and interposing dielectric protrusions 70 “replace a relatively wide dielectric region absent of any conductive material,” such as area 44 of Figure 4. *Id.* at 5:31–33.

According to one embodiment, dummy conductors 68 are formed by etching dummy trenches into the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. *Id.* at 4:12–16. “The lateral widths of the wide trench, the dummy trenches, and the narrow trenches are preferably greater than 50 microns, 1 to 5 microns, and less than 1 micron, respectively.” *Id.* at 4:18–21. Conductive material is then

deposited in the dummy trenches forming dummy conductors, which “serve no purpose except to improve the planarization of the interconnect level in which they reside.” *Id.* at 4:22–40.

The ’231 patent describes dummy conductors 68 as preventing metal dishing because the metal of the dummy conductors is softer than the surrounding dielectric and, therefore, does not cause flexing or contracting of the polishing pad during the CMP process. *Id.* at 5:33–44. The ’231 patent further describes dummy conductors 68 as preventing oxide erosion because the metal dummy conductors “may continue to be polished more rapidly than” the surrounding dielectric. *Id.* at 5:46–50. This allows dummy conductors 68 and narrow interconnects 66 to be polished down to a consistent level below the surrounding dielectric, which is itself “again made substantially coplanar with the dummy conductors and the interconnect.” *Id.* at 5:50–59.

B. The Challenged Claims

Petitioner challenges claims 1–8 of the ’231 patent, of which claim 1 is independent. Claim 1 is illustrative of the claimed subject matter and is reproduced below:

1. A method for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a first trench and a series of second trenches, wherein a lateral dimension of said first trench is greater than a lateral dimension of said second trenches;

filling said dummy trenches and said first and second trenches with a conductive material; and

polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said first and second trenches, wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect.

Ex. 1001, 9:9–26.

C. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Claims Challenged	35 U.S.C. § ²	Basis
1–4, 8	§ 103(a)	Jaso, ³ Stine1998 ⁴
1–4, 8	§ 103(a)	Jaso, Stine1998, Pramanik1997 ⁵
5–7	§ 103(a)	Jaso, Stine1998, Robinson ⁶
5–7	§ 103(a)	Jaso, Stine1998, Pramanik1997, Robinson

Pet. 15. Petitioner submits the Declaration and Reply Declaration of Duane S. Boning, Ph.D. (Ex. 1002, Ex. 1052) in support of its arguments. Patent Owner submits the Declaration of John H. Givens, Ph.D. (Ex. 2011) in support of its arguments.

² The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended several provisions of 35 U.S.C., including § 103. Because the ’231 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA version of 35 U.S.C. § 103.

³ U.S. Patent No. 6,093,631 (issued July 25, 2000). Ex. 1004.

⁴ Brian E. Stine, et al., *The Physical and Electrical Effects of Metal-Fill Patterning Practices for Oxide Chemical-Mechanical Polishing Processes*, IEEE Transactions on Electron Devices, vol. 45, no. 3, 665 (March 1998). Ex. 1005.

⁵ Dipankar Pramanik & Milind Weling, *Integration of CMP into Deep Sub-Micron Multilevel Metallization Circuits*, Proceedings of the First International Symposium on Chemical Mechanical Planarization, vol. 96–22, 1 (1997). Ex. 1006.

⁶ U.S. Pat. No. 5,879,222 (issued Mar. 9, 1999). Ex. 1008.

D. Related Matters

Both Petitioner and Patent Owner state that the '231 patent is related to the following district court litigation: *Invensas Corporation and Tessera Advanced Technologies, Inc. v. NVIDIA Corporation*, No. 1:19-cv-00861 (D. Del.). Pet. 5; Paper 5, 1.

E. Real Parties-in-Interest

Petitioner identifies NVIDIA Corp. as the real party-in-interest. Pet. 5. Patent Owner identifies Invensas Corporation, Tessera Intellectual Property Corporation, Tessera Technologies, Inc., and Xperi Corporation as the real parties-in-interest. Paper 5, 1.

III. ANALYSIS

A. Principles of Law

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner, except in limited circumstances not present here. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective evidence of non-obviousness, i.e., so-called secondary considerations such

as commercial success, long felt but unsolved needs, and failure of others.⁷ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). The obviousness inquiry further requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)).

B. Claim Construction

Because the Petition was filed after November 13, 2018, we construe the challenged claims using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2020).⁸ This rule adopts the same claim construction standard used by Article III federal courts, which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. Under this standard, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent, including the specification. *See Phillips*, 415 F.3d at 1312–13.

We address two contested limitations below.

⁷ Neither party has argued that secondary considerations or objective evidence of nonobviousness exists. Thus, we do not address secondary considerations or objective evidence of nonobviousness.

⁸ *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (final rule).

“etching . . . trenches in a dielectric layer”

Patent Owner requests that we construe “etching . . . trenches in a dielectric layer” of claim 1 to mean “removing some amount of dielectric material from areas in a dielectric layer to create openings in the dielectric layer.” PO Resp. 15 (citing Ex. 2011 ¶¶ 40–48). Specifically, Patent Owner asserts a “POSA [person of ordinary skill in the art] would know that damascene processes remove dielectric material from a dielectric layer to form openings into which metal is subsequently deposited, and would understand that the term ‘trench’ refers to such openings.” *Id.* at 15–16 (citing Ex. 1001, 2:9–19 (describing such a process), Figs. 2, 5; Ex. 2011 ¶¶ 44, 45; Ex. 2023, 1).

Patent Owner asserts the Decision to Institute incorrectly describes a subtractive process as creating a “trench” because, unlike the trenches described in the ’231 patent “a subtractive process *first* forms the metal line and *then* surrounds it with dielectric, so the ‘space’ ultimately occupied by the line never exists as a defined region that could be called a ‘trench.’” PO Resp. 16. Finally, Patent Owner asserts Petitioner’s declarant, Dr. Boning, “could not identify *a single instance*—other than the [Decision to Institute]” where a subtractive process was referred to as a “trench.” *Id.* (citing Ex. 2013, 93:13–25).

Petitioner responds that, because Jaso discloses a damascene process with trenches, Patent Owner’s proposed claim construction is “unnecessary.” Reply 32. We agree that the damascene process of Jaso is the same damascene process to which Patent Owner seeks to limit this claim term. Patent Owner does not argue otherwise in its Sur-reply. *See* Sur-reply. Thus, we decline to construe the term “etching . . . trenches into a dielectric layer.”

“a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches”

Patent Owner also requests that we construe “a plurality of laterally spaced dummy trenches in a dielectric layer, between a first trench and a series of second trenches” to be limited to “not allowing intervening trenches or other structures between the structures formed by the steps of the claim.”

PO Resp. 16–17. Patent Owner further specifies that this means

(1) the claimed plurality of laterally spaced dummy trenches/conductors must be formed in a dielectric region that otherwise has no conductive metal; (2) a relatively wide trench/conductive line (i.e., the “first trench”) must be formed immediately next to one side of that dielectric region; and (3) a series of relatively narrow trenches/conductive lines (i.e., the “series of second trenches”) must be formed immediately next to the opposite side of that dielectric region.

Id.

In support of its proposed construction, Patent Owner relies on the following statement from the Specification:

the presence of the plurality of dummy conductors between the series of relatively narrow interconnect and the relatively wide interconnect provides for global planarization of the topography employing the trenches. **In particular, the dummy conductors and the interposing dielectric protrusions replace a relatively wide dielectric region absent of any conductive material.**

PO Resp. 17–18 (quoting Ex. 1001, 5:27–33 with emphasis added). Patent Owner suggests this passage justifies importing a limitation that the region to which the dummy trenches are added “*has no conductive structures.*” *Id.* at 18. Additionally, Patent Owner asserts the problem the ’231 patent is trying to solve arises “*specifically because there is a large dielectric region immediately adjacent to the conductive line(s) of interest.*” *Id.* (citing Ex. 1001, 2:64–3:22, 3:23–42).

Patent Owner also asserts that Petitioner’s reading of the claim, in which the word “comprising” allows additional structures between the wide trench and the narrow trenches, would allow a configuration with a wide trench on one side of the chip, narrow trenches on the other side of the chip, and “thousands of other trenches and structures in the center of the chip—as long as there is a plurality of laterally spaced, intermediately sized dummy trenches *also* located somewhere in the center of the chip.” PO Resp. 18–19. According to Patent Owner, this reading would fall outside the scope of the claim because it would fail to solve the problem addressed by the ’231 patent. *Id.* at 19. Specifically, Patent Owner asserts

a POSA would know that: (1) the hypothetical chip described above would not *necessarily* suffer from dishing of the wide conductive line on the one edge of the chip, or oxide erosion on the relatively narrow conductive lines on the opposite edge of the chip; and (2) even if one or both of these problems *did* arise, placing dummy conductors in the center of the chip—far removed and separated by many other structures from the relevant conductive lines — would *not* be expected to do anything to alleviate the problems. The latter is true because, as a POSA would understand, the presence of the intervening structures frustrates the very mechanism by which dummy conductors simultaneously solve the [problems allegedly solved by the ’231 patent.] *Id.* (citing Ex. 2011 ¶ 55; Ex. 1001, 3:47-51, 3:54-59, 4:12-15, 5:27-31, 6:18-23, 7:4-6, 8:59-65).

Id. at 19–20.

Patent Owner is correct that “[a] patent’s statement of the described invention’s purpose informs the proper construction of claim terms.”

Kaken Pharm. Co. v. Iancu, 952 F.3d 1346, 1352 (Fed. Cir. 2020).

Nevertheless, a claim is not required to encompass all of the advantages or purposes of the invention. *See Howmedica Osteonics Corp. v. Wright Med. Tech., Inc.*, 540 F.3d 1337, 1345 (Fed.Cir.2008) (“An invention may

possess a number of advantages or purposes, and there is no requirement that every claim directed to that invention be limited to encompass all of them.”) (citations omitted). Additionally, notwithstanding the importance of a specification, limitations in the specification must not be read into the claims absent lexicography or disclaimer/disavowal. *Hill-Rom Services, Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014).

Petitioner contends that the use of the transitional phrase “comprising” in the claim means that the claim allows additional intervening structures. Reply 32 (citing *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997)). Additionally, Petitioner contends that specifying that the region to which the dummy trenches are added has no conductive structures would add a negative limitation to the claim and require “express disclaimer or independent lexicography in the written description that would justify adding [it].” *See id.* at 33 (citing *Omega Engineering, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1322–23 (Fed. Cir. 2003)) (quotation added here).

Patent Owner asserts that intervening structures would frustrate the purpose of the invention by suggesting a hypothetical where there is a large distance between the wide trench and the narrow trenches with “thousands” of intervening structures (PO Resp. 18–19), and by suggesting that “[i]f enough intervening structures” exist, “a POSA would expect the dummy trenches to have no impact whatsoever on metal dishing in the area of the first trench and oxide erosion in the area of the series of second trenches” (Ex. 2011 ¶ 55). We credit Dr. Boning’s testimony that “[t]he hypothetical is not technically meaningful to a POSITA . . . Consideration of conductors at opposite ends of the chip is not something a POSITA would do.” Ex. 1052 ¶ 10. We determine that, even if we accept that the

sole purpose of the invention is to prevent metal dishing and oxide erosion, Patent Owner does not sufficiently tie its proposed hypothetical to examples from the specification or real world examples.

Additionally, the statement in the specification that “the dummy conductors and the interposing dielectric protrusions replace a relatively wide dielectric region absent of any conductive material” is not explicit enough to be a disavowal of scope or lexicography by the Patentee. *Hill-Rom Services, Inc.*, 755 F.3d at 1371. For example, the statement does not say “absent conductive material” is the invention or that “absent conductive material” is a necessary condition to achieve the objective of the ’231 patent. Moreover, it is not clear to us how Patent Owner makes the leap from “absent of any conductive material,” which is the specific language cited in the specification, to its proposed construction that requires that there be no intervening trenches or other structures. *See* Tr. 30:3–20 (upon inquiry, Patent Owner acknowledging that there appears to be a disconnect between the specific language cited in the specification and Patent Owner’s proposed construction).

Additionally, Patent Owner does not argue that the asserted prior art is necessarily in a configuration that would frustrate the purpose of the invention, but rather that it might be in such a configuration. For example, Patent Owner asserts that Figure 8 of Stine1998 “might contain metal features that are not visible due to rendering limitations.” PO Resp. 56. Patent Owner’s expert admits that “[o]ne cannot even tell from the image [in Figure 8 of Stine1998] if the white regions are filled with dense metal lines.” Ex. 2011 ¶ 206. This uncertainty, even if we accept it as true, does not justify asserting that Figure 8 of Stine1998 cannot solve the problems of metal dishing and oxide erosion allegedly required by the specification.

Given that Patent Owner's construction would read into the claims a negative limitation that is not recited explicitly in the claims for the purpose of avoiding a hypothetical situation not shown sufficiently to be relevant in this IPR, we decline to adopt Patent Owner's proposed construction.

No other claim terms are contested. Thus, we decline to construe any other claim terms for purposes of this Final Written Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’”).

C. Level of Ordinary Skill in the Art

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)).

Petitioner argues that one of ordinary skill in the art at the time of the invention of the '231 patent “would have had a Bachelor of Science degree in physics, chemistry, materials science, electrical engineering, mechanical engineering, or related discipline, in addition to 3–5 years of experience in the fabrication of integrated circuit devices. Additional years of experience could substitute for formal education, and vice versa.” Pet. 22 (citing Ex. 1002 ¶ 35). Patent Owner “does not dispute Petitioner's description of the qualifications of a POSA for the purposes of this IPR.” PO Resp. 9.

We regard Petitioner's formulation of the level of skill as consistent with the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355

(Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Therefore, for purposes of this Final Written Decision, we adopt Petitioner's assessment of the level of skill in the art because it is consistent with the '231 patent and the asserted prior art, and we apply it in our analysis below.

D. Dr. Boning's Declaration

Patent Owner asserts that Dr. Boning's credibility is "seriously compromised" because "he failed to inform the Board or [Patent Owner] about certain materials of which he is aware that cast doubt on key aspects of his testimony" and "he has taken positions and offered opinions that strain credibility or suffer from other problems." PO Resp. 29.

Patent Owner argues that Dr. Boning should have disclosed the so called "StineThesis" (Ex. 2016) which is a Ph.D dissertation by Brian Stine, the lead author of the Stine1998 reference, and because it purportedly describes the work that is the subject matter of Stine1998. PO Resp. 29. During cross-examination, Dr. Boning admitted to reviewing this document a year ago. *Id.* Dr. Boning, however, testified he did not disclose this document in his declaration because he believed it to be consistent with Stine1998. *Id.* (citing Ex. 2013, 198:1–25.) Patent Owner asserts that differences between Figure 8 of Stine1998 and Figure 7.7 of the StineThesis are relevant to the determination of whether Stine1998 meets the claim limitations. *Id.* at 29–30. We do not find that any discrepancies between the StineThesis and Stine1998 rise to a level such that they would undermine Dr. Boning's credibility.

Patent Owner also asserts Dr. Boning failed to produce his own publications that contradict positions he has taken in this case. *Id.* at 30. We find that it is not incumbent upon Dr. Boning to anticipate what issue Patent Owner will focus on in this IPR or to scour his publications for positions that

could be characterized as contrary to positions he is now taking. To the extent Patent Owner has specified such alleged inconsistencies, we will evaluate them individually but we do not find that Dr. Boning's credibility overall is undermined by not finding and reporting these alleged inconsistencies.

Patent Owner also asserts that Dr. Boning's arrangement of Figures from Jaso to resemble the '231 patent was misleading, involved hindsight, and undermines his credibility. *Id.* at 31. Petitioner cites Dr. Boning's testimony in this proceeding to support Petitioner's contention that a person of ordinary skill in the art faced with the prior art at issue would find the claims of the '231 patent obvious. It is the trier of fact's job to assess whether his opinions are tainted with hindsight. Again, we do not find that Dr. Boning's credibility overall is undermined by this alleged hindsight reconstruction.

Patent Owner also asserts that Dr. Boning used an incorrect construction of the claim allowing intervening structures which allegedly further undermines his credibility. *Id.* Nevertheless, we did not adopt that construction. Again, it is the trier of fact's role to determine the correct claim construction. Finally, Patent Owner asserts Dr. Boning's role as "author" of Stine1998--Dr. Boning supervised the student thesis that is lead to the Stine1998 reference)--means that he cannot form an objective opinion regarding the reference and he can be expected to have bias typical of inventors. *Id.* Leaving aside whether his role as a supervisor over a student's thesis would make him an "inventor" of a patent based on that paper, experts in patent cases routinely engage in the legal fiction of putting themselves in the mind of a person of ordinary skill in the art who is often a person of less skill than the expert. Additionally, the typical bias that an

inventor would have is driven by his personal motivation to find his own invention valid. Here, Dr. Boning is paid to be an expert and has the same inherent bias of any other paid expert. His prior knowledge of the specific prior art would tend to make him *more* qualified to testify about the art but his bias, if any, does not go to upholding anything specifically about Stine1998, the validity of which is not at issue in the IPR.

Overall, we have considered all of Patent Owner's arguments but do not find that they undermine the overall credibility of Dr. Boning. However, we will consider any question regarding his credibility on any specific issue raised by Patent Owner in the obviousness analysis below, where appropriate.

E. Overview of the Asserted Prior Art

1. Jaso (Ex. 1004)

Jaso is a U.S. Patent titled "Dummy Patterns for Aluminum Chemical Polishing (CMP)." Ex. 1004, code (54). Jaso is directed to "planarizing damascene metallic circuit patterns of a plurality of discrete integrated circuit chips." *Id.* at code (57). By way of background, Jaso describes that, in "the damascene process, metallization of [circuit] interconnects is performed by etching the desired circuitry in the dielectric layer" of the chip. *Id.* at 1:66–2:2. Then, a "thin layer of conductive metal is deposited . . . over the entire wafer." *Id.* at 2:2–4. After that deposit, the "unwanted portions of this metal layer are removed by CMP leaving the thin lines of metals as interconnects." *Id.* at 2:4–6. However, Jaso states that, problematically, the "CMP process [used] to polish the [chip's] wafer" results in "dishing," creating "a non-planar surface." *Id.* at 2:9–12. Figure 10C of Jaso is reproduced below.

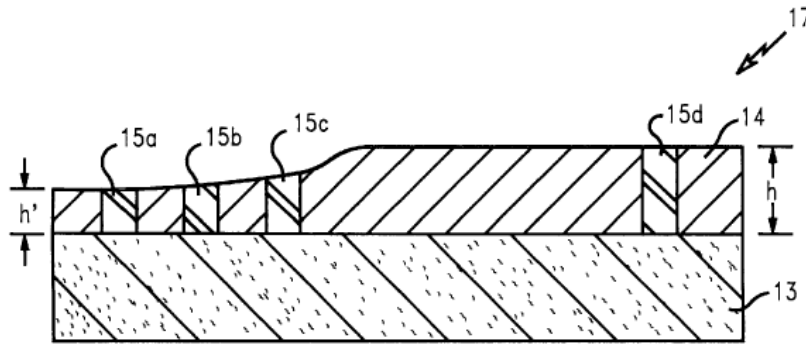


FIG. 10C

Figure 10C shows such undesirable dishing on a chip after the CMP process. *Id.* at 4:66–67, 6:40–47. Jaso states that, to “overcome the dishing effect and other non-planarization,” Jaso’s “invention decreases the differences in pattern factors for regions on the chip” to provide “a uniform metal density (pattern factor) across the surface of the chip and, concomitantly, of the wafer.” *Id.* at 3:29–37; *see id.* at 3:3–5. In particular, Jaso uses “dummy circuitry to provide a uniform metallized dielectric surface.” *Id.* at 6:21–23. Figures 11A and 11B of Jaso are reproduced below.

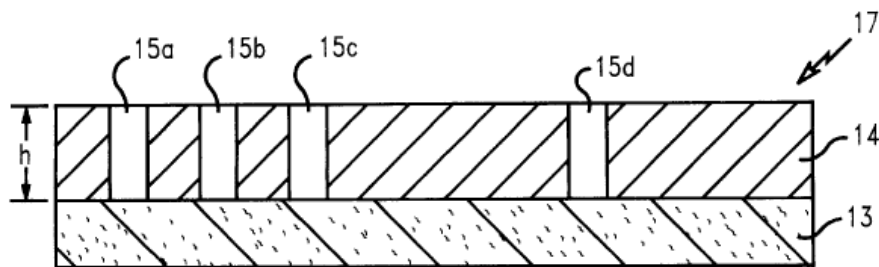


FIG. 11A

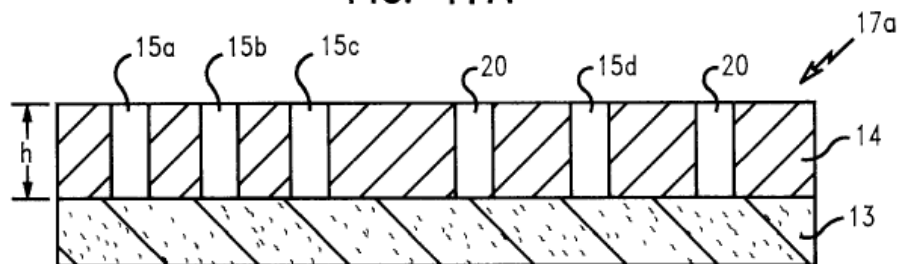


FIG. 11B

Figures 11A and 11B show, respectively, an etched chip without and with added dummy circuitry. *Id.* at 6:1–9. As shown in Figure 11A, region 17 on the wafer includes “openings 15a, 15b, 15c and 15d [which] are formed for interconnect openings.” *Id.* at 6:3–4. Figure 11B shows “the addition of dummy lines 20,” which increase the circuitry density in region 17, resulting in uniform circuit density. *Id.* at 6:7–9; *see id.* 5:37–42. As such, region 17 does not suffer from the aforementioned dishing after the CMP process. *See id.* at 6:44–47; *compare with id.* Figs. 10B–10C with Figs. 11C–11D.

2. *Stine1998 (Ex. 1005)*

Stine1998 is an article titled “The Physical and Electrical Effects of Metal-Fill Patterning Practices for Oxide Chemical-Mechanical Polishing Processes.” Ex. 1005, 665. Stine1998 states that “CMP processes are hampered by layout pattern sensitivities which cause certain regions on a chip to have thicker dielectric layers than other regions due to differences in the underlying topography.” *Id.* That is, Stine1998 recognizes a problem that is similar to, if not the same as, dishing and erosion caused during the CMP process for chip making. Stine1998 states that “reducing layout pattern dependent dielectric thickness variation,” can be provided by changing the chip’s “layout pattern itself via the introduction of metal-fill patterning.” *Id.* “Metal-fill patterning is the process of filling the large open areas on each metal layer with a metal pattern, which is either grounded or left floating.” *Id.*

Figure 4 of Stine1998 illustrates a “metal-fill patterning scheme” and is reproduced, in relevant part, below. *Id.* at 669.

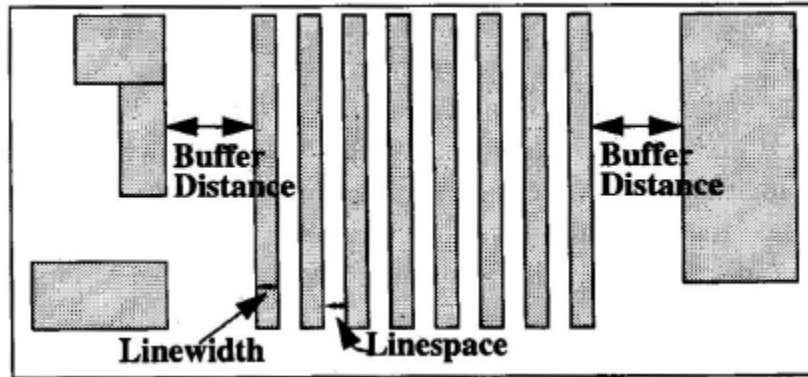


Figure 4 shows “a metal-fill patterning scheme of vertically oriented lines” having a “a buffer distance . . . between the nearest active circuit region and a metal-fill line.” *Id.* That is, Figure 4 shows a number of metal-fill lines spaced between first and second circuit elements.

Using its metal-fill patterning scheme, Stine1998 presents a case study in which metal-fill patterning is “exercised on the layout . . . of a 256 bit x 32 bit 24-port memory register containing over 65 000 transistors.” *Id.* at 671. Figure 8 of Stine1998 is reproduced below.

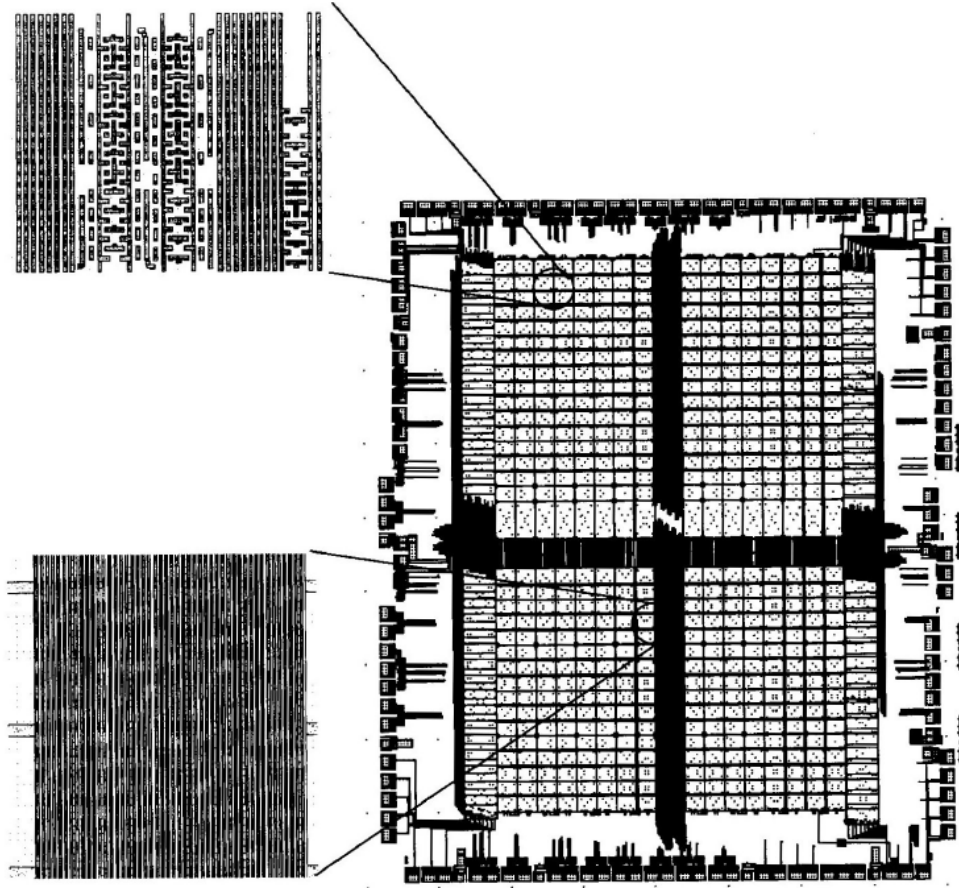


Figure 8 shows the layout of the chip to which metal-fill patterning is applied. *Id.* at 671, 673, 678 n.17. Stine1998 states that the layout shown in Figure 8 “is about 7.9 mm x 9.2 mm and the minimum linewidth and space at metal-1 is 3 μ m.” *Id.* at 673.

Stine1998 also describes a “case study,” in which the authors applied their dummy metal optimization method to the layout of a chip described in a 1991 paper titled “Memory Chip for 24-Port Global Register File” (“Maly1991”). Ex. 2004. Stine1998 uses the chip layout described in Maly1991, cited in footnote 17. Ex. 1005, 673, 678 n.17. Stine1998 presents data from simulations of interlevel dielectric (ILD) thickness variation and parasitic capacitance, and analyzes the tradeoffs between the two based on several parameters. *See generally id.* at 671–75. Figure 8 of

Stine1998 is a rendering of the Maly1991 chip’s “metal-1” layer (the lowest of three metal layers), along with two magnified insets. *See id.* at 673.

A reference hereinafter called the StineThesis (Ex. 2016) is a Ph.D dissertation by Brian Stine, the lead author of the Stine1998 reference. Ex. 2013, 196:14–20; Ex. 2014, 253:5–20. The StineThesis describes the same work—including the Maly1991 “case study”—that is the subject matter of Stine1998. Ex. 2013, 198:6–13. The StineThesis includes a Figure 7.7 showing the “metal-1” layer of the Maly1991 chip, which is the same chip/layer purportedly depicted in Figure 8 of Stine1998. Ex. 2016, 165.

3. *Pramanik1997 (Ex. 1006)*

Pramanik1997 is an article titled “Integration of CMP into Deep Sub-Micron Multilevel Metallization Circuits.” Ex. 1006. Pramanik1997 states that “[m]etal CMP is used for planarizing the metal . . . in the DAMASCENE process for planarizing the interconnect” for the circuit. *Id.* at 50. Pramanik1997 describes that “grooves are etched into a deposited oxide in the shape of the interconnect pattern” and the metal interconnect “filling process will have to handle a wide variety of sizes of grooves from the minimum linewidth to wide bus areas.” *Id.* at 52. Parmanik1997 also describes that the CMP process has “to deal with dishing of the wide metal buses” and does so by “the use of dummy metal fill so as [to] equalize the effective area density of the interconnect.” *Id.*

4. *Robinson (Ex. 1008)*

Robinson is a U.S. Patent titled “Abrasive Polishing Pad with Covalently Bonded Abrasive Particles.” Ex. 1008, code (54). Robinson is directed to a “polishing pad []used for planarizing semi-conductor wafers or other substrates with a mechanical or CMP process.” *Id.* at code (57).

Robinson’s “polishing pad preferably has a body made from a matrix material, bonding molecules bonded to the matrix material, and abrasive particles bonded to the bonding molecules in a manner that affixes the abrasive particles to the matrix material” in order “to substantially prevent the abrasive particles from detaching from the pad during planarization.” *Id.*

F. Asserted Obviousness of Claims 1–4 and 8 over Jaso and Stine1998

Petitioner relies on Jaso and Stine1998 as teaching all the limitations of claims 1–4 and 8, and provides reasoning as to why one of ordinary skill in the art would have been prompted to combine the teachings of these references. Pet. 32–74. For the reasons that follow, we determine that Petitioner has shown persuasively the combination of Jaso and Stine1998 would have rendered claims 1–4 and 8 of the ’231 patent obvious.

Petitioner’s analysis, as supported by the Boning Declaration, demonstrates where Petitioner contends each element of claims 1–4 and 8 is disclosed in the combined teachings of Jaso and Stine1998, and that there is a sufficient rationale to combine their respective teachings. Pet. 32–74.

1. Independent Claim 1

a) Preamble

The preamble of claim 1 recites a “method for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit.” Ex. 1001, 9:9–12. To the extent this preamble should be treated as limiting, Petitioner argues Jaso describes a “method and apparatus is provided for planarizing damascene metallic circuit patterns of a plurality of discrete integrated circuit chips on a metal coated silicon wafer,” resulting in a “substantially horizontal (planar) surface.” Pet. 42–44 (citing Ex. 1004, code (57), 6:11–20) (emphasis omitted). Further, Petitioner asserts Jaso

discloses “interconnects are formed in a layer above the active region of transistor devices, where ‘metallization of the interconnects is performed by etching the desired circuitry in the dielectric layer down to the active region of the device.’” *Id.* at 43 (citing Ex. 1004, 1:18–36, 1:63–2:2) (emphasis omitted).

Based on the foregoing, Petitioner has shown sufficiently that Jaso teaches this subject matter. Patent Owner does not present substantive arguments as to this limitation. *See generally* PO Resp.

b) etching a plurality of laterally spaced dummy trenches into a dielectric layer

Limitation 1.a⁹ recites “etching a plurality of laterally spaced dummy trenches into a dielectric layer.” Ex. 1001, 9:13–14. Petitioner argues Jaso discloses a “damascene process, which etches trenches for [both] the dummy pattern (dummy trenches) and the interconnect patterns . . . (the ‘first trench’ and ‘series of second trenches’[]).” Pet. 44–45 (citing Ex. 1004, 1:28–31, 8:5–8) (emphasis omitted). Highlighting Figure 11B, Petitioner argues that the trenches for interconnects 15a–15c teach a “series of second trenches;” the trench for interconnect 15d teaches a “first trench;” and dummy trenches 20 are spaced between and amongst the first and second trenches. *Id.* at 45 (citing Ex. 1004, 6:1–11). Petitioner further argues that Jaso determines “how many dummy trenches to etch and where to put them” based on the circuit pattern density in a chip region. *Id.* at 44–45 (citing Ex. 1004, 3:57–64, 5:19–26). Petitioner asserts that applying certain exemplary parameters described by Jaso results in “at least four . . . laterally spaced dummy

⁹ Petitioner identifies limitations by a format where the claim number is followed by lettered limitations. *See, e.g.*, Pet. 44 (limitation 1.a). We adopt Petitioner’s format for discussion purposes in this Final Written Decision.

trenches” added to low pattern density chip regions. *Id.* at 46–47 (citing Ex. 1004, 3:10–13, 3:31–34, 3:51–56, 4:2–5; Ex. 1002 ¶ 147) (emphasis omitted).

Analysis of Patent Owner’s Arguments

As an initial matter, Patent Owner argues that “[t]he ’231 patent describes a ***specific configuration of structures*** that may exist in a semiconductor chip fabricated using a damascene process, namely: a relatively wide conductive line, separated only by a dielectric region that contains no conductive material, from a series of relatively narrow conductive lines.” PO Resp. 1. Patent Owner defines this as the “Relevant Configuration.” *Id.* Throughout Patent Owner’s analysis it refers to this Relevant Configuration in lieu of discussing specific claim limitations. We decline to limit the claims to a Relevant Configuration that includes, for example, a damascene process not recited in the claims, and a limitation to “a dielectric region that contains no conductive material” which also is not recited in the claims.

Second, Patent Owner asserts “[t]he inventors of the ’231 patent recognized that the two particular problems they identify and define—dishing and oxide erosion—will occur simultaneously in each location on a chip where the [so called] Relevant Configuration exists.” *Id.* at 7. Patent Owner refers to these problems as the “Relevant Problems.” *Id.* Finally, Patent Owner asserts “[t]he Relevant Solution that the ’231 patent discloses involves forming a plurality of laterally spaced ‘dummy’ trenches (subsequently filled with conductive material to form ‘dummy conductors’) in the dielectric region located in the middle of the Relevant Configuration.” *Id.* at 7–8.

Obviousness is not analyzed by comparing the prior art to a relevant configuration or relevant problems or solutions but by comparing the prior art to properly construed claims. For example, it is well-settled that simply because a reference has a different objective does not preclude a person of ordinary skill in the art from using its teachings in an obviousness evaluation. *In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) (“The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned.”); *In re Applied Materials, Inc.*, 692 F.3d 1289, 1298 (Fed. Cir. 2012) (“A reference must be considered for everything that it teaches, not simply the described invention or a preferred embodiment.”). With that in mind, we discuss Patent Owner’s arguments to the extent they can be understood to relate to a claim construction—not a “Relevant Configuration,” “Relevant Problems,” or “Relevant Solution.”

Patent Owner also frequently makes conclusory statements that a reference does not meet a claim limitation or the Relevant Configuration, Problem, or Solution untethered to substantive arguments. *See, e.g.*, PO Resp. 37 (“Stine1998 does not disclose at least a relatively wide conductive line, a dielectric region that contains no conductive lines, a series of relatively narrow conductive lines immediately adjacent to such a dielectric region, or a plurality of laterally spaced dummy conductors inserted into such a dielectric region—all of which are required for the Relevant Configuration and the Relevant Solution.”). We do not respond to those statements individually because, unless they are accompanied with detailed arguments, they are not substantive arguments that address the merits of Petitioner’s contentions.

As to the limitation of “dummy trenches,” Patent Owner asserts that because Jaso simply finds a region where the metal within that region does not meet a certain threshold and teaches adding dummy metal to that region, Jaso is not “concerned” about a particular structure. *Id.* at 34. Patent Owner also asserts “Jaso simply states that one would use an undisclosed ‘computer...algorithm...to generate dummy circuitry’ to increase pattern density as needed in certain regions.” *Id.* at 59 (citing Ex. 1004, 3:65–4:2). Additionally, Patent Owner asserts that “Jaso [] does not tell the POSA to look for a specific configuration, and then insert dummy metal into a particular location within that configuration (as the Relevant Solution does).” *Id.* at 34. Nevertheless, claim 1 is not limited to how you arrive at a specific configuration. It is not relevant to our obviousness analysis how Jaso arrives at a configuration but rather whether the configuration it arrives at meets the claim language. Here, as explained above Jaso discloses placing dummy conductors in low pattern density regions, thus disclosing a plurality of laterally spaced dummy trenches in a dielectric layer between a first trench and a series of second trenches. Pet. at 44–47.¹⁰ Patent Owner’s argument above does not undermine that showing.

Based on the foregoing, Petitioner has shown sufficiently that Jaso teaches this subject matter.

c) *between a first trench and a series of second trenches, wherein a lateral dimension of said first trench is greater than a lateral dimension of said second trenches*

Limitation 1.b recites that the dummy trenches are “between a first trench and a series of second trenches, wherein a lateral dimension of said

¹⁰ For brevity and to avoid redundancy, we discuss the first and second trenches in detail in the section below.

first trench is greater than a lateral dimension of said second trenches.”
Ex. 1001, 9:14–17. Petitioner argues that the combination of Jaso and Stine1998 teaches this limitation. Pet. 47–66. Petitioner asserts that Stine1998 improves CMP planarity on a chip by using “a plurality of laterally-spaced dummy conductors” in “large open areas or sparse regions.” Pet. 47–48 (citing Ex. 1005, 670), 55 (citing Ex. 1005, 671, Fig. 5(b)), 58–59 (citing Ex. 1005, Fig. 4) (emphasis omitted). Petitioner further asserts that Stine1998 suggests placing dummy conductors within open areas between wide metal “bond pads” and “narrow metal interconnects.” *Id.* at 50–52 (citing Ex. 1005, 670).

Petitioner argues it would have been obvious to a person of ordinary skill in the art to combine Jaso and Stine1998 “to etch a plurality of dummy trenches in a dielectric layer between a first (wider) trench and a series of second (narrower) trenches.” *Id.* at 66 (citation omitted). Petitioner argues that a person of ordinary skill in the art “would be motivated to combine the teachings in Jaso and Stine1998, as both references are directed to the addition of dummy conductors to equalize pattern density to improve CMP planarity.” *Id.* at 38–39 (citing Ex. 1004, code (57), 3:29–64; Ex. 1005, 668). In particular, Petitioner states that “Stine1998 enhances and improves upon the disclosure in Jaso by providing general teachings and specific methods that are widely applicable to dummy metal-fill techniques for addressing added capacitance.” *Id.* at 39 (citing Ex. 1005, 670–672). Petitioner points out that “Stine1998 expressly motivates a [person of ordinary skill in the art] to apply its teachings to a damascene process requiring dummy-fill to enhance planarity” because Stine1998 states its methodology can be extended to “inlaid metal techniques such as copper

damascene.” *Id.* at 41–42 (citing Ex. 1005, 676; Ex. 1002 ¶ 131) (emphasis omitted).

Analysis of Patent Owner’s Arguments

1) Prior Art Does not “Look for” a Specific Configuration

Patent Owner argues “Stine1998 does not tell the POSA to look for a *specific configuration of structures*, and then insert dummy metal into a particular location within that configuration (as the Relevant Solution does.)” PO Resp. 36–37. Patent Owner also argues that Jaso and Stine1998 “together accordingly tell the POSA to *focus on pattern density*, and to take steps to ensure that *variations* in pattern density across the chip are minimized” as opposed to looking for the particular configuration called out by the claims. *Id.* at 58. There is no requirement in the claims for the prior art to “look for” specific structures, but rather it must disclose those structure required by the claims. For the reasons articulated in the Petition, we agree that the combined teachings of Jaso and Stine1998 teach the structure required by claim 1. Pet. 38–39 (citing Ex. 1004, code (57), 3:29–64; Ex. 1005, 668), 50–52 (citing Ex. 1005, 670). We also credit Dr. Boning’s testimony that these references’ teachings “to locate dummies in sparse regions proximate to wide and narrow lines...*would obviously include placing dummies in regions between such lines.*” Ex. 1002 ¶ 183 (emphasis added). The fact that Jaso and Stine1998 may not purposefully seek out the configuration relied on by Patent Owner does not undermine Petitioner’s showing that the proper configuration would result from an obvious combination of the references. Thus, we are not persuaded by these arguments.

2) *Stine1998 Does Not Teach Trenches or the Location of Dummy Trenches*

We also disagree with Patent Owner’s argument that “Stine1998 does not teach or suggest any ‘trenches in a dielectric layer.’” PO Resp. 47, 55–56. Patent Owner argues that Stine1998’s “subtractive process used for the manufacture of the disclosed chip does not involve the formation of such trenches.” *Id.* at 47 (citing Ex. 2011 ¶ 171). That is, Patent Owner asserts Stine1998 deposits a dielectric layer around already-formed metal lines. This argument, however, is not commensurate with the scope of the claims as properly construed. As noted above, to the extent that a damascene process is required, Jaso teaches such a process. Pet. 44. Additionally, assuming *arguendo* Patent Owner’s argument is correct, it stands to reason that the spaces where dielectric is not deposited are free of dielectric (due to the presence of metal lines) and, therefore, the “trenches” are free of dielectric.

Patent Owner also asserts Stine1998 does not disclose dummy trenches because it “states in passing that certain areas of its test chip would be ‘prime candidates’ for ‘metal-fill,’ but does not actually disclose the *particular* location of any alleged ‘dummy’ conductor.” PO Resp. 56 (citation omitted) (citing Ex. 2011 ¶ 205). Patent Owner’s argument improperly attacks Stine1998 alone when Petitioner argues that the combination of Jaso and Stine1998 teaches “trenches.” *See In re Keller*, 642 F.2d 413, 426 (CCPA 1981). Petitioner points out that Jaso describes “a damascene method wherein, in general, a via or trench pattern is etched into a planar dielectric layer.” Pet. 44 (emphasis omitted) (citing Ex. 1004, 1:28–31; 8:5–8; Ex. 1002 ¶¶ 142–144). Petitioner states that Figure 11B of Jaso includes “trenches (15a-d) [which] correspond to trenches for interconnects

(the “first trench” and “series of second trenches” in limitation 1.b).” *Id.* at 45. Patent Owner does not address the trenches taught by Jaso, much less teachings of Jaso in combination with the teachings of Stine1998. *See* PO Resp. 33–36, 55–61. Accordingly, we are not persuaded that the combination of Jaso and Stine1998 fails to teach “trenches.”

3) Stine1998 Solves a Different Problem

In addition, we are not persuaded by Patent Owner’s argument that Stine1998 is not “salient to the Relevant Problems disclosed in the ’231 patent” because Stine1998 “relates to *oxide CMP* in a *subtractive process*,” which, according to Patent Owner, is directed to different problems, and different CMP than the metal CMP in a damascene process. PO Resp. 36. As Petitioner points out, Jaso, Stine1998, and the ’231 patent each address the “erosion of dielectric and dishing of metal” during CMP, which gives rise to “a non-planar surface.” Pet. 7 (citing Ex. 1001, 2:63–3:22), 32 (citing Ex. 1004, 2:7–19), 38–39 (citing Ex. 1004, 3:29–64; Ex. 1005, 668). Patent Owner’s assertion that different issues cause dishing and erosion too narrowly confines the problem that the references address. *See Unwired Planet v. Google*, 841 F.3d 995, 1001 (Fed. Cir. 2016) (“The field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field.”). Patent Owner also asserts “Jaso’s reference to ‘dishing’ is categorically different from the problems with which the ’231 patent is concerned: dishing of wide interconnect and erosion of oxide between dense narrow interconnect.” PO Resp. 62. We are not persuaded by this

conclusory statement.¹¹ Furthermore, to the extent Patent Owner argues the references are non-analogous art, all the references are directed to the creation of metal lines in chip manufacturing, as discussed above, and fall within the same field of endeavor.

4) Figure 8 is not at Sufficient Resolution and is Unreliable

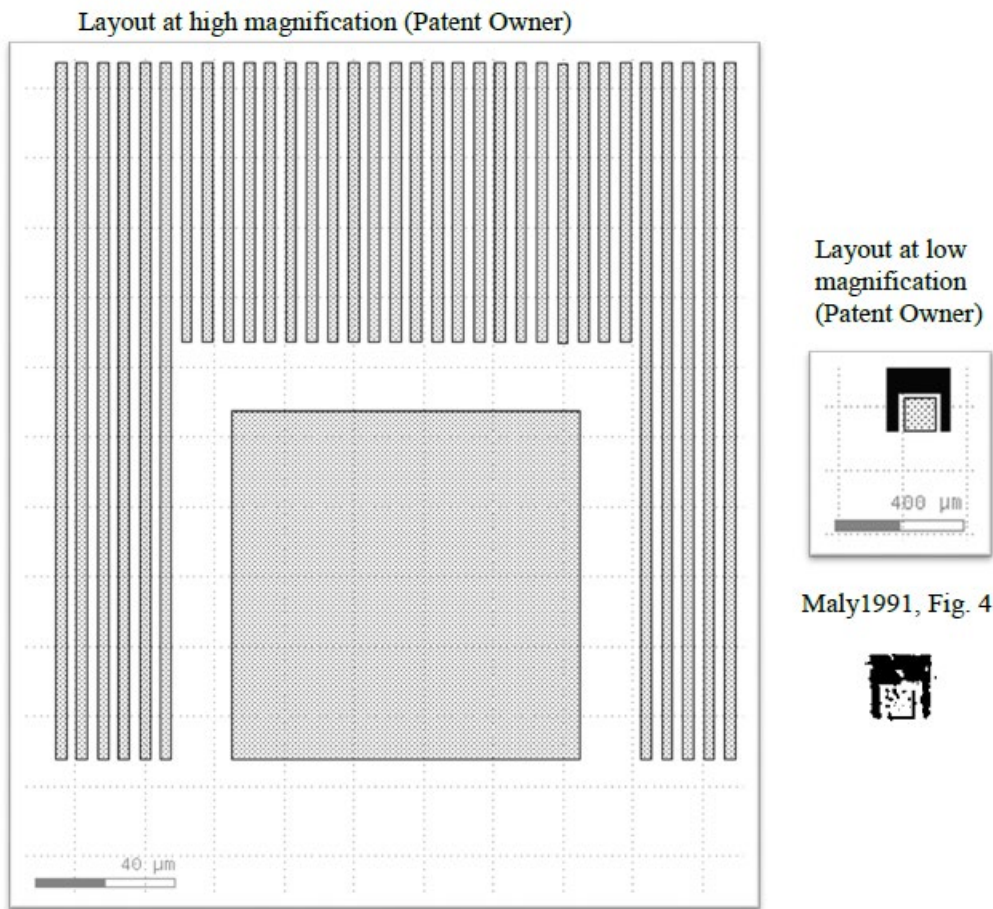
Patent Owner argues that Figure 8 of Stine1998 lacks the resolution or reliability for a POSA to see whether Stine1998 teaches inserting metal-fill between “bond pads” and “relatively narrow” interconnects. PO Resp. 38–46.¹² To exemplify this point, Patent Owner’s declarant, Dr. Givens, used a

¹¹ Patent Owner cites paragraphs 219–224 of Dr. Given’s declaration for this conclusory statement. To the extent Patent Owner means to incorporate arguments from the declaration, our rules do not allow incorporation by reference (*see* 37 C.F.R. § 42.6(a)(3)), so we decline to address any such arguments.

¹² Patent Owner also refers to its argument in its Preliminary Response that Figure 8 of Stine 1998 was not drawn to scale. PO Resp. 46. Patent Owner appears to have dropped that argument in favor of an argument that Figure 8 has insufficient resolution, but to the extent it maintains that argument we reiterate that

Stine1998 is a technical paper published by the IEEE (Ex. 1005, 1), but Patent Owner relies on cases from our reviewing court addressing figures in *patent drawings*. Prelim. Resp. 30 (*citing Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes”)), 37 (*citing Nystrom v. TREX Co.*, 424 F.3d 1126, 1148-49 (Fed. Cir. 2005)). Stine1998 presents a “case study” that applies its metal-fill methodology to a specific IC chip, i.e., “a 256 bit x 32 bit 24-port memory register containing over 65 000 transistors,” whose design was the subject of an earlier IEEE technical paper. Ex. 1005, 671, 678 n.17; *see* Ex. 2004, Abstract. Patent Owner has not directed us to any authority for the proposition that

tool called KLayout to render high magnification structures and then render those structures at decreased magnification. *Id.* at 39–42. For example, as reproduced below, Dr. Givens compares a layout containing multiple lines around a large square, which at low magnification, appears as a dark solid area around the square. *Id.* at 40.



Reproduced above from the Patent Owner Response, Patent Owner presents several screen prints including a screen labeled “Layout at high magnification (Patent Owner)” containing multiple lines around a large

figures in a reputable technical journal fail to disclose the relative proportions of elements.

Inst. Dec. 32.

square, a screen shot labeled “Layout at low magnification (Patent Owner)” that appears to show a dark solid area where the multiple lines were around the square, and below the low magnification, Figure 4 of the Maly1991 reference. *Id.* The Maly1991 reference also has a dark area surrounding a square similar to the low magnification screen shot. *Id.* at 41. The point of this exercise by Patent Owner is to suggest that Figure 8 of Stine1998 may not show what appears to be open spaces or bond pads etc. Patent Owner asserts, and its declarant testifies, “a POSA would not rely on Figure 8 of Stine1998 to determine what structures are present in the depicted layout, nor would such a person draw—or be able to draw—conclusions about what the visible geometric shapes look like when viewed at an appropriate magnification.” *Id.* at 42. Patent Owner also faults Dr. Boning for attempting to explain inconsistencies between Figure 8 of Stine1998, Maly1991, and the StineThesis and for admitting and explaining areas of Figure 8 that are difficult to see at the resolution of Figure 8. *Id.* at 42–43. For example, Patent Owner asserts Dr. Boning testified:

- The lines in the magnified insets “are too narrow to be resolved at the magnification of the overall layout as shown in Fig. 8 of Stine1998.” Ex. 1002, ¶ 153.

- The white rectangles in the “core” of the chip are “highly dense regions.” Ex. 2014, 265:6-20, 266:14-267:13.

- Yet, the same “highly dense region” in the core of the same chip shows up as almost entirely black in Figure 7.7 of the StineThesis. Dr. Boning explains this by saying that “different renderings of those may well depict them with different degrees of approximation or -- or artifacts.” Ex. 2014, 268:9-269:14, 294:15-295:12.

- While the white rectangles in the core are “highly dense regions,” *id.*, 265:14-20, the white areas around the “core” are open or sparse areas, Ex. 1002, ¶¶ 156-57. Also, the white areas around the core are “not always devoid of lines on that particular metal layer.” Ex. 2014, 272:3-273:2.

- The black rectangles around the perimeter of the chip “quite likely [include] regions that are large and -- likely solid metal regions” and “there may be also regions of Metal-1 circuitry associated with—with or part of the bond pad.” Ex. 2014, 283:11-288:1.

- The fact that the black rectangles are not aligned in Figure 8 of Stine1998, but are perfectly aligned both in StineThesis and in Maly1991 (all three of which show the same chip) “quite possibly could be a rendering issue.” Ex. 2014, 292:10-18, 295:14-296:12.

Id.

Finally, Patent Owner asserts, “there is simply no way for a POSA to look at Figure 8 and form any understanding of its structures *at all*” and thus, Dr. Boning’s opinions should be disregarded in their entirety. *Id.* at 44 (citing Ex. 2011 ¶¶ 191–199). We find that the explanations by Dr. Boning are a reasonable attempt to explain what one of ordinary skill in the art, with general background knowledge in the art, would glean from Figure 8 of Stine 1998 and are supported by additional cited references, such as Maly1991 and the StineThesis. *See, e.g.*, Ex. 1052 ¶¶ 72 (citing Maly Fig. 4), 92 (citing Ex. 2016 (StineThesis), 92 (Ex. 2016, 165), 93. “[A] skilled artisan’s background knowledge is relevant to the reading of the prior art on which the obviousness challenge is based and . . . it is permissible, and sometimes even necessary, to establish such background knowledge by pointing to other prior art.” *Rovalma, S.A. v. Bohler-Edelstahl GmbH & Co. KG*, 856 F.3d 1019, 1027 (Fed. Cir. 2017).

Despite Patent Owner’s criticism, Dr. Boning’s testimony cited by Patent Owner evidences Dr. Boning’s opinion that a person of ordinary skill in the art was aware of common artifacts and limitations in downscaled

layouts. Reply 22 (citing PO Resp. 38–39; Ex. 1052 ¶¶ 65, 98).¹³ Dr. Boning also relies on secondary references to support his testimony about the general background knowledge of one of ordinary skill in the art. Ex. 1002 ¶¶ 65 (citing Ex. 1009 (Mead Textbook)), 74 (citing Ex. 1010 (Rabaey Textbook)), 75, 76, 152–157. Thus, we credit Dr. Boning’s testimony and do not disregard his testimony wholesale based on those alleged inconsistencies. Below, we focus on the testimony that is at issue in this IPR.

There are three main reasons why Figure 8 of Stine1998 is at issue. First, Petitioner asserts that the white areas in Figure 8 are open areas between a wide trench and narrow trenches with no metal lines into which dummy conductors would be placed. *See* Pet. 37–38; Ex. 1002 ¶¶ 112, 152, 157. Patent Owner opposes that contention (PO Resp. 56) but, as explained in association with claim construction, we do not rely on a construction that requires no intervening trenches or other structures between the wide trench and narrow trenches. Additionally, Petitioner relies on the typical layout of chips and the figures of Jaso to support its interpretation of Figure 8. Pet. 45–46, 52–53.

¹³ Dr. Givens testifies that, because there is a discrepancy in Dr. Boning’s testimony regarding the inserts for various regions of Figure 8 of Stine1998 and the lack of any other inserts one of ordinary skill in the art would not assume the white areas contain no metal lines. Ex. 2011 ¶¶ 195–196. And, based on his magnification experiment, Dr. Givens testifies that Figure 4 of Maly1991 may contain metal lines. *Id.* We consider the fact that Dr. Givens’s testimony is largely based on what a person of ordinary skill in the art could discern from Figure 8 of Stine1998 and Figure 4 of Maly1991 alone rather than what one of ordinary skill in the art may glean based on their background knowledge in the art—for example whether Figure 8 of Stine1998 is consistent with conventional chip designs as Dr. Boning testified. Thus, we give slightly more weight to Dr. Boning’s testimony.

Second, Petitioner relies on “densely packed metal lines (signal interconnects) in the ‘core region’” of the chip to show the “series of second trenches.” Pet. 53 (citing Ex. 1002 ¶ 158).¹⁴ Patent Owner disputes these contentions based on its general assertion that Figure 8 of Stine1998 is unreliable, its argument that Stine1998’s “subtractive process” cannot form “trenches,” and a conclusory statement that Stine1998 does not teach the Relevant Configuration. PO Resp. 36, 47, 55. For reasons discussed above, we are not persuaded by the Patent Owner’s argument regarding Figure 8 of Stine1998. We are not persuaded by the “subtractive process” argument because, as explained above in the claim construction section, Jaso discloses trenches made with a “subtractive process.” Pet. 44. We are also not persuaded by Patent Owner’s conclusory reference to the Relevant Configuration.

Third, Petitioner asserts Figure 8 of Stine1998 discloses “bond pads” that are the “first trench.” Pet. 50–51 (citing Ex. 1005, 670). Patent Owner argues a “POSA would readily understand that Figure 8 of Stine1998 *does not show any bond pads.*” PO Resp. 47 (citing Ex. 2011 ¶¶ 172–180). This is because, according to Patent Owner, although bond pads are generally on the periphery of chips, they are also generally placed on the top metal layer of chips and Figure 8 depicts the alleged bond pads on the bottom metal layer. *Id.* Patent Owner also points out that unlike Maly1991 and the StineThesis, Stine1998 has the alleged “bond pads” offset from each other in places. *Id.* Dr. Givens testifies he has “never seen a chip with bond pads

¹⁴ Petitioner also relies on Figure 11B of Jaso, arguing that the trenches for interconnects 15a–15c teach a “series of second trenches.” Pet. 45 (citing Ex. 1004, 6:1–11).

offset from one another in the same way as the alleged features shown in Fig. 8” of Stine1998. *Id.* at 48 (citing Ex. 2011 ¶ 179).

Dr. Boning, however, testifies a person of ordinary skill in the art would have known that the chip in Figure 8 of Stine1998 included bond pads, that the pads are on the periphery, and that the pads include large metal conductors in the 100-200µm size range. Ex. 1002 ¶¶ 65–78. He testifies that “[b]ond pads and power lines were well-known standard features that were incorporated in virtually all ICs (Integrated Circuits).” *Id.* at 75. Thus, we credit Dr. Boning’s opinion that a person of ordinary skill in the art would have known there are bond pads in Figure 8. Pet. 48–53, 59–62; Ex. 1002 ¶¶ 65–78, 152–157; Ex. 1052 ¶¶ 65–69.

Patent Owner also argues that Dr. Boning, at his deposition, did not refer to the structures of Figure 8 of Stine1998 as “bond pads” but rather “bond pad structures” that may be partially on lower metal layers may not contain a large metal square and may contain different circuitry. PO Resp. 54. For that reason, Patent Owner asserts Petitioner has failed to show that Figure 8 contains “bond pads.” *Id.*

In response, Petitioner argues that obviousness does not require Petitioner to show that the structures of Figure 8 of Stine1998 “necessarily” are “bond pads.” Reply 23–24. Petitioner also argues that Maly1991 does, indeed, show “bond pads” and it is the same chip as Figure 8 of Stine1998. *Id.* at 23. Petitioner argues that it is “conventional” to have bond pads on the periphery of chips based on the Rabaey textbook. *Id.* at 23. Petitioner also argues that three level bond pads exist that could have a large metal pad on the bottom layer. *Id.* at 24–25. Petitioner asserts “rendering variations” explain why the alleged bond pads in Figure 8 are misaligned. *Id.* at 26.

Finally, Petitioner argues that a “bond pad” is interchangeable with a “bond pad structure” that includes all metal layers. *Id.* at 26–27.

We discern that there are, as Patent Owner suggests, discrepancies regarding the disclosure of bond pads in Figure 8 of Stine1998. For example, Maly1991 which is the same chip as Stine1998, shows bond pads on the upper layer not the lower layer, and in Maly1991 the bond pads are aligned but in Figure 8 the alleged “bond pads” are not aligned. PO Resp. 46–55. Additionally, Stine1998 does not discuss explicitly “bond pads” or “bond pad structures.” Ex. 2035, 123:7–13.

Patent Owner maintains the differences between Maly1991 and Stine1998 are too numerous to be caused by rendering variations. PO Resp. 23–24, 29–30; Ex. 2011 ¶¶140–41; Ex. 1042, 582:18–22. We disagree. We agree with Dr. Boning’s testimony above that Figure 8 must be read, as to the features relevant to this IPR, from the perspective of one of skill in the art aware of conventional chip designs. *See Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1361 n.3 (Fed. Cir. 2008) (“What a prior art reference discloses or teaches is determined from the perspective of one of ordinary skill in the art.”).

Although Patent Owner references alleged inconsistencies that indicate that Figure 8 of Stine1998 may be unreliable in some respects, as discussed above, the weight of the evidence before us favors Petitioner’s assertion that Figure 8 of Stine1998, indeed, shows wide bond pads and “relatively narrow” metal interconnections, as required by independent claim 1. Pet. 53. Figure 8 of Stine1998 shows expanded portions of the interconnections at the core of an exemplary chip, i.e., a “256 bit x 32 bit 24-port memory register containing over 65 000 transistors” (Ex. 1005, 671; *see* Ex. 2004, Fig. 4), having “minimum linewidth and space at metal-1 [of] 3

μm” (Ex. 1005, 673). Further, according to Dr. Boning, who is “a co-author of [Stine1998]” (Ex. 1002 ¶ 5), Figure 8 “shows large bond pads (black square-shaped features) around the perimeter of the chip” (*id.* ¶ 153) because the “metal layout arrangement in Fig. 8 of Stine1998 is typical of IC circuits at the time with respect to the relative placement of bond pads” (*id.* ¶ 158). Dr. Boning explains that “bond pads are examples of ‘commonly used layout items normally required in any project,’” “are generally placed at the periphery of a chip in the layout,” have “widths in the range of 100μm to 200μm,” are “significantly larger than signal interconnects,” and are “known to a [person of ordinary skill in the art] as distinctive and readily recognizable features in the overall metal layout.” *Id.* ¶ 65 (citations omitted). Based on Stine1998’s disclosures and Dr. Boning’s supporting testimony, we agree that Stine1998 shows interconnections at its core that are “relatively narrow compared to” bond pads located at the periphery of the chip. Accordingly, we are not persuaded, based on Patent Owner’s arguments regarding alleged flaws in Petitioner’s annotation of Stine1998’s figures fails to teach or suggest the claimed interconnections “relatively narrow compared to” bond pads.¹⁵

¹⁵ Based on its assertion that Figure 8 of Stine1998 is unreliable, Patent Owner also argues that combination of Figure 5 and Figure 8 showing where dummy conductors would be added to Figure 8 represented on page 52 of the Petition is “*doctored and augmented*,” thereby suggesting it is similarly unreliable. PO Resp. 56. Patent Owner asserts that “there is nothing in Stine1998 to teach the POSA where in Figure 8 to place dummy conductors, in what number or configuration, or whether in a manner that matches the Relevant Solution disclosed in the ’231 patent.” *Id.* We disagree. Petitioner relies on more than just Figure 8, by itself. As explained above, Petitioner relies on Dr. Boning’s testimony about the general background knowledge in the art regarding the conventional organization of chips together with disclosures in Stine1998 that discuss improving CMP planarity on a chip by

5) Motivation to Combine Jaso and Stine1998

Patent Owner argues that “as of 1998, copper damascene CMP was still in its infancy, Ex. 2011, ¶¶ 232-33, meaning that a POSA was more likely to be working on the fundamentals than exploring topics such as how to adapt a method to ‘optim[ize] dummy-fill geometry’ to ‘decreas[e] parasitic capacitance.’” PO Resp. 63. However, Petitioner points out that “Stine1998 enhances and improves upon the disclosure in Jaso by providing general teachings and specific methods that are widely applicable to dummy metal-fill techniques for addressing added capacitance.” Pet. 39 (citing Ex. 1005, 670–672). Even if Stine1998’s damascene CMP was in its infancy as Patent Owner argues, Patent Owner does not explain persuasively why an ordinarily skilled artisan would not attempt to apply such a known process to improve a technology in a similar field, i.e., chip manufacturing.

Patent Owner also suggests that the statement in Stine1998 that its “generic methods” for dielectric planarization “can potentially be adapted to . . . damascene . . . polishing processes” would not have enabled a POSA to “adapt” the method. PO Resp. 63–64. Patent Owner argues that one of ordinary skill in the art would not be able to “dive into issues like parasitic capacitance.” *Id.* at 64. We are not persuaded that a person of ordinary skill in the art would not have the skill to look into options for dealing with parasitic capacitance. As Petitioner explains, “Jaso recognizes the potential drawbacks of metal-fill (parasitic noise and delay), but does not offer any design tradeoff analysis” and “Stine1998 addresses this issue directly.”

using “a plurality of laterally-spaced dummy conductors” in “large open areas or sparse regions.” Pet. 47–48 (citing Ex. 1005, 670), 55 (citing Ex. 1005, 671, Fig. 5(b)), 58–59 (citing Ex. 1005, Fig. 4) (emphasis omitted).

Pet. 39 (citing Ex. 1004, 4:9–12; Ex. 1005, 670; Ex. 1002 ¶ 128). We agree with Petitioner that Stine1998 details a technique to address capacitances and parasitic noise. *Id.* We credit Dr. Boning’s testimony that this technique would have been of interest to one of ordinary skill in the art. Ex. 1002 ¶¶ 128–129. Additionally, the prior art itself may reflect an appropriate level of skill. *Okajima*, 261 F.3d at 1355. In this case Stine1998’s discussion of parasitic capacitance suggests it would not have been beyond the level of skill in the art.

Patent Owner also suggests that the motivation to combine asserted by Petitioner limits how the references can be combined. PO Resp. 64–65. Patent Owner cites to cases that state that motivation to combine and reasonable expectation of success are limited to how Petitioner has framed those issues. *Id.* at 64. This may be true but Patent Owner does not cite a case for the proposition that the motivation to combine effectively limits how the references must be combined to meet the claim limitations. In fact, the opposite is true, once one of ordinary skill is motivated to look to a reference, that reference is prior art for all it teaches. *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985). Therefore, we disagree that once Petitioner pointed to Stine1998’s “analytical framework” its entire obviousness combination was limited to only to combining the teachings of Jaso to that “analytical framework.”

Patent Owner also asserts that “the combination of Jaso and Stine1998 is directed to the problem of reducing variations in surface topography of an as-deposited material prior to its being subjected to CMP. The concern is about the *starting* surface. The ’231 patent, on the other hand, is directed to problems that arise at the *end* of metal CMP, and that introduce new sources of nonplanarities.” PO Resp. 61. Based on this difference, Patent Owner

asserts one of skill would not have looked to the prior art to solve the problem presented by the '231 patent except through improper hindsight. *Id.* As we noted above, the use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. *In re Heck*, 699 at 1333.

Patent Owner also argues that, because the prior art is not tailored to the exact “solution” as Patent Owner describes it, the problem would not be completely solved, i.e., the problem could still occur in some cases. PO Resp. 62. This argument is unfounded. The prior art to an apparatus claim is only required to meet the structural requirements of the claim, not to fully resolve the problem allegedly solved by the challenged patent. The fact that the prior art may not always solve the problem of the challenged patent would be irrelevant to the analysis *even if* the claims were limited to solving a particular problem. *See Unwired Planet*, 841 F.3d at 1002 (“[C]ombinations of prior art that sometimes meet the claim elements are sufficient to show obviousness.”); *see also Hewlett–Packard Co. v. Mustek Sys., Inc.*, 340 F.3d 1314, 1326 (Fed. Cir. 2003) (“Just as ‘an accused product that sometimes, but not always, embodies a claimed method nonetheless infringes,’ a prior art product that sometimes, but not always, embodies a claimed method nonetheless teaches that aspect of the invention.” (quoting *Bell Commc’ns Research, Inc. v. Vitalink Commc’ns Corp.*, 55 F.3d 615, 622–623 (Fed. Cir. 1995) (internal citations omitted))).

6) Summary

We determine that Petitioner has shown sufficiently that an ordinarily skilled artisan would have combined Jaso and Stine1998, and that the proposed combination teaches or suggests “a first trench and a series of

second trenches, wherein a lateral dimension of said first trench is greater than a lateral dimension of said second trenches.”

d) filling said dummy trenches and said first and second trenches with a conductive material

Limitation 1.c recites “filling said dummy trenches and said first and second trenches with a conductive material.” Ex. 1001, 9:18–19. Petitioner argues “Jaso discloses filling said dummy trenches and said first and second trenches with a conductive material.” Pet. 66 (citing Ex. 1004, 1:28–31, 6:9–11, Fig. 4).

Based on the foregoing, Petitioner has shown sufficiently that Jaso teaches this subject matter. Patent Owner does not present substantive arguments as to this limitation. *See generally* PO Resp.

e) polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said first and second trenches

Limitation 1.d recites “polishing said conductive material to form dummy conductors exclusively in said dummy trenches and interconnect exclusively in said first and second trenches.” Ex. 1001, 9:20–22. Petitioner asserts that Jaso discloses that “[t]he metallized wafer of FIG. 11C is now chemical mechanically polished using conventional means to remove metal layer 16 down to the surface of dielectric 14” and “the polishing needs to be carried out until the patterned metal is cleared on the entire wafer leaving metal exclusively in previously etched lines.” Pet. 66–67 (citing Ex. 1004, 3:20–23, 6:15–18, Figs. 11C–11D) (emphasis omitted). Petitioner argues Jaso’s “dummy conductors reside exclusively in the dummy trenches (but not in the first and second trenches), and the interconnects reside exclusively in the first and second trenches (but not in the dummy trenches).” *Id.* at 68.

Based on the foregoing, Petitioner has shown sufficiently that Jaso teaches this subject matter. Patent Owner does not present substantive arguments as to this limitation. *See generally* PO Resp.

f) wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect

Limitation 1.e recites “wherein said dummy conductors are electrically separate from said plurality of electrically conductive features and co-planar with said interconnect.” Ex. 1001, 9:23–25. Petitioner argues “Jaso discloses the dummy conductors are electrically separate from any active devices (such as the transistors identified as the “plurality of electrically conductive features”) that function as an integrated circuit.” Pet. 68–69 (citing Ex. 1004, 1:62–2:2, 4:7–9; Ex. 1002 ¶ 198).

Based on the foregoing, Petitioner has shown sufficiently that Jaso teaches this subject matter. Patent Owner does not present substantive arguments as to this limitation. *See generally* PO Resp.

For the reasons set forth above, we determine Petitioner has shown a by a preponderance of the evidence that independent claim 1 would have been obvious over the combined teachings of Jaso and Stine1998.

2. Dependent claims 2–4 and 8

Petitioner relies on its explanations and supporting evidence regarding the combination of Jaso and Stine1998 to challenge dependent claims 2–4 and 8. *See* Pet. 69–74. During trial, Patent Owner does not address separately Petitioner’s explanations and supporting evidence as to how the

combined teachings of Jaso and Stine1998 account for the limitations of claims 2–4 and 8. *See* PO Resp. 66.

a) Claim 2

Claim 2 depends from claim 1 and further recites “wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.” Ex. 1001, 9:26–29. Petitioner asserts that Jaso’s disclosure that “any metal may be used to metallize the damascene openings in the wafer surface with suitable metals including aluminum, copper, tungsten and the like” meets this limitation. Pet. 69 (citing Ex. 1004, 7:3–6; Ex. 1002 ¶¶ 203–204).

Patent Owner’s Response does not provide a rebuttal to Petitioner’s analysis of this dependent claim in light of the teachings of Jaso and Stine1998. Based on the information set forth in the Petition and the testimony of Dr. Boning, Petitioner has shown by a preponderance of the evidence that dependent claim 2 would have been obvious over Jaso and Stine1998.

b) Claim 3

Claim 3 depends from claim 1 and further recites “wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said first and second trenches.” Ex. 1001, 9:30–33. Petitioner asserts that Jaso’s disclosure of “a metal layer 16 is coated on top of dielectric layer 14 filling the openings 15a-15d and the dummy openings 20,” together with “[t]he metallized wafer of FIG. 11C is now chemical mechanically polished using conventional means to remove

metal layer 16 down to the surface of dielectric 14,” meets this limitation. Pet. 70–72 (citing Ex. 1004, 6:9–17, Figs. 3–9, 11C; Ex. 1002 ¶¶ 206–207).

Patent Owner’s Response does not provide a rebuttal to Petitioner’s analysis of this dependent claim in light of the teachings of Jaso and Stine1998. Based on the information set forth in the Petition and the testimony of Dr. Boning, Petitioner has shown by a preponderance of the evidence that dependent claim 3 would have been obvious over Jaso and Stine1998.

c) Claim 4

Claim 4 depends from claim 1 and further recites “wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.” Ex. 1001, 9:34–38. Petitioner asserts that Jaso’s portions of the dielectric layer adjacent to the newly formed trench openings are “dielectric protrusions” that meet this limitation. Pet. 72–74 (citing Ex. 1004, 6:14–20, Figs. 4B, 7A, 7B, 8B, 11C; Ex. 1002 ¶¶ 210–213).

Patent Owner’s Response does not provide a rebuttal to Petitioner’s analysis of this dependent claim in light of the teachings of Jaso and Stine1998. Based on the information set forth in the Petition and the testimony of Dr. Boning, Petitioner has shown by a preponderance of the evidence that dependent claim 4 would have been obvious over Jaso and Stine1998.

d) Claim 8

Claim 8 depends from claim 1 and further recites “wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said

conductive material while rotating said polishing pad surface relative to said upper surface” Ex. 1001, 9:53–57. To meet this limitation, Petitioner relies on Jaso’s disclosure of “[T]he chemical-mechanical planarization (CMP) process involves pressing a semiconductor wafer against a moving polishing surface that is wetted with a chemically reactive, abrasive slurry... In the CMP process, the wafer is typically secured to a carrier plate ... so as to press the wafer into frictional contact with the polishing pad mounted on a rotating turntable. The carrier and pressure plate also rotate.” Pet. 74 (citing Ex. 1004, 1:39–57; Ex. 1011, 30, 31; Ex. 1002 ¶ 215) (emphasis omitted).

Patent Owner’s Response does not provide a rebuttal to Petitioner’s analysis of this dependent claim in light of the teachings of Jaso and Stine1998. Based on the information set forth in the Petition and the testimony of Dr. Boning, Petitioner has shown by a preponderance of the evidence that claim 8 would have been obvious over Jaso and Stine1998. .

e) Summary

We have reviewed Petitioner’s explanations and supporting evidence regarding these dependent claims and find them persuasive. *See* Pet. 69–74. Petitioner, therefore, has shown by a preponderance of the evidence that the combined teachings of Jaso and Stine1998 would have rendered dependent claims 1–4 and 8 obvious.

G. Asserted Obviousness of Claims 1–4 and 8 over Jaso, Stine1998, and Pramanik1997

Petitioner alternatively asserts that Jaso, Stine1998, and Pramanik1997 teach or suggest all the limitations of claims 1–4 and 8, and provides reasoning as to why one of ordinary skill in the art would have been prompted to combine the teachings of these references. Pet. 75–79. For the reasons that follow, we determine that Petitioner has shown

persuasively that the combination of Jaso, Stine1998, and Pramanik1997 would have rendered claims 1–4 and 8 of the '231 patent obvious.

1. Independent Claim 1

Petitioner's analysis, as supported by the Boning Declaration, demonstrates where Petitioner contends each element in claims 1–4 and 8 is disclosed in Jaso, Stine1998, and Pramanik1997. Pet. 75–79; *see id.* at 31–79. In particular, Petitioner's relies on its treatment of Jaso and Stine1998, discussed above, and further incorporates Pramanik1997 to teach dummy trenches that are “between a first trench and a series of second trenches, wherein a lateral dimension of said first trench is greater than a lateral dimension of said second trenches,” as recited in limitation 1.b. *Id.* at 47. Our discussion above addresses Petitioner's combination of Jaso and Stine1998 and Patent Owner's corresponding arguments. *See supra* Section III.F. Accordingly, our discussion here focuses on whether the combination of Jaso, Stine1998, and Pramanik1997 accounts for limitation 1.b.

Petitioner states Pramanik1997 “discloses forming wide buses and narrow metal lines using metal CMP in a damascene process.” Pet. 76 (citing Ex. 1006, 47 50, 52; Ex. 1002 ¶ 221). Petitioner asserts that a person of ordinary skill in the art “would look to Pramanik1997 for further teaching that dummy fill is necessary to deal with dishing and erosion problems when CMP is used in the damascene process with wide buses and narrow lines.” *Id.* at 77. Petitioner states, “the modification would constitute no more than combining Jaso's known method to the type of layout specified in Pramanik1997 to yield a predictable result (improved pattern factor uniformity to achieve CMP planarity).” *Id.* at 78.

Petitioner further contends that an ordinarily skilled artisan would have a reasonable expectation of success in combining the cited teachings of Pramanik1997, Jaso, and Stine1998 because:

The complementary teachings [of these pieces of art] fit together like pieces of the same puzzle. Where Pramanik1997 is silent on the specific details of [its] general solution, this is expressly disclosed in Jaso and Stine1998. Ex[] 1002 ¶ 225. To the extent that Jaso does not specifically disclose wide and narrow trenches, this is expressly disclosed in Pramanik1997 (and obvious in view of Stine1998). *Id.* Accordingly, the modification would constitute no more than combining Jaso's known method to the type of layout specified in Pramanik1997 to yield a predictable result (improved pattern factor uniformity to achieve CMP planarity). *Id.*

Pet. 78.

Analysis of Patent Owner's Arguments

Patent Owner argues that, because Pramanik1997 uses a pattern density approach it “does not teach the POSA to look for a specific configuration, and then insert dummy conductors.” PO Resp. 68 (citing Ex. 2011 ¶¶ 249–251). We are not persuaded by this argument because, as explained above, claim 1 is not limited to “finding” a certain configuration.

Patent Owner also argues “Pramanik1997 does not disclose applying CMP to a layout comprising a wide interconnect adjacent to a series of closely spaced narrow interconnect [because] Pramanik1997's Figure 8 [] depicts interconnect in *three separate schematics* representing ‘different regions of a die’” and is focused on pattern density. PO Resp. 68 (citing Ex. 2015, 58; Ex. 1002 ¶ 252). Thus, according to Patent Owner, “[t]he combined teachings of Jaso, Stine1998, and Pramanik1997 would lead the POSA to understand that they are solving a fundamentally different problem, with a fundamentally different solution, and it would not lead the POSA to

the Relevant Solution as the answer to the Relevant Problems.” *Id.* at 69. As explained above, a pattern density solution still meets the claim limitations at issue. Nor does Pramanik1997 need to address the same problem and provide the same kind of solution as the ’231 patent to be applicable in an obviousness analysis. A reference “may be directed to an entirely different problem from the one addressed by the inventor, yet the reference will still anticipate if it explicitly or inherently discloses every limitation recited in the claims.” *In re Schreiber*, 128 F.3d 1473, 1478 (Fed. Cir. 1997).

Patent Owner argues “a POSA would know that consumables (e.g., slurries), process conditions, structure design, and process setup and integration for oxide CMP *do not* translate to metal CMP. PO Resp. 70 (citing Ex. 2011 ¶ 254). Patent Owner also asserts “[a] POSA would also understand that extensive experimentation would be necessary to determine whether a technique developed for oxide CMP could be successfully adapted to metal CMP.” *Id.* Patent Owner states the differences between oxide and metal CMP would “discourage” a POSA from looking to Stine1998 because of alleged differences between oxide and damascene and because Pramanik1997’s “sub-micron” process node is significantly different from Jaso and Stine1998. *Id.* at 70–72.

We are not persuaded by this argument. Petitioner explains why one of ordinary skill would readily be able combine oxide CMP with metal CMP. *See* Reply 17 (citing Ex. 1052 ¶ 140–152). As to Patent Owner’s argument that Pramanik1997’s “sub-micron” process node is different from Jaso and Stine1998, we credit Dr. Boning’s testimony that any differences are not beyond a person of ordinary skill’s abilities. Ex. 1052 ¶¶ 180–184. Additionally, Patent Owner does not address the fact that, regardless of the

differences between oxide and metal CMP, capacitance issues are similar in Jaso, Stine1998, and Pramanik1997 and provide a reason to combine them. *See* Pet. 41–42. For those reasons we are not persuaded by this argument.

2. Dependent claims 2–4 and 8

Petitioner relies on its explanations and supporting evidence regarding the combination of Jaso and Stine1998 to challenge dependent claims 2–4 and 8. *See* Pet. 75–79; *see also id.* at 69–74. Patent Owner does not address separately Petitioner’s explanations and supporting evidence as to how the combined teachings of Jaso, Stine1998, and Pramanik1997 fail to teach the limitations of claims 2–4 and 8. *See* PO Resp. 73. We have reviewed Petitioner’s explanations and supporting evidence regarding these claims, and we find them persuasive in accordance with our above findings. *See* Pet. 69–74. Petitioner, therefore, has shown persuasively that the combined teachings of Jaso, Stine1998, and Pramanik1997 would have rendered claims 2–4 and 8 obvious.

H. Asserted Obviousness of Claims 5–7 over Jaso, Stine1998, and Robinson

Petitioner asserts that Jaso, Stine1998, and Robinson teach or suggest all the limitations of claims 5–7, and provides reasoning as to why one of ordinary skill in the art would have been prompted to combine the teachings of these references. Pet. 79–83. For the reasons that follow, we determine that Petitioner has shown persuasively that the combination of Jaso, Stine1998, and Robinson would have rendered claims 5–7 of the ’231 patent obvious.

Petitioner asserts, “like Jaso and Stine1998, Robinson addresses a problem of non-uniformity in the CMP planarization process.” Pet. 79–80. According to Petitioner, Robinson discloses “an improvement on this art [i.e., conventional CMP processes using slurry solutions that include

abrasive particles] by providing ‘bonding molecules’ such that the abrasive particles are covalently bonded to the bonding molecules, which in turn are bonded to the matrix material of the polishing pad to ‘substantially inhibit[] abrasive particles from detaching from the pad.’” *Id.* at 80 (citing Ex. 1008, 2:59–3:8). Petitioner continues, “a [person of ordinary skill in the art] would be motivated to achieve the best planarization result by following the teachings of Jaso and Stine1998 in designing a metal layout including dummy patterns, and also use an abrasive pad in a slurry free of abrasive particles as taught in Robinson.” *Id.* at 81 (citing Ex. 1002 ¶¶ 231–232).

Claim 5 depends from claim 1 and further recites, “wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to the upper surface.” Ex. 1001, 9:39–42. Relying on its prior analysis of Jaso and Stine1998 regarding independent claim 1, Petitioner contends Robinson discloses the additional limitation of dependent claim 5 by teaching a method of polishing that comprises moving the upper surface of the wafer relative to an abrasive polishing pad 10. Pet. 81 (citing Ex. 1008, 2:24–26, 6:60–65).

Claim 6 depend from claim 5 and further recites, “wherein said polishing comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said conductive material.” Ex. 1001, 9:43–46. Relying on its prior analysis of claim 5, Petitioner contends Robinson discloses the additional limitation of dependent claim 6 by teaching “that ‘[i]n general, a particle-free planarizing liquid 148 is preferably used with the polishing pad 10’” Pet. 82 (citing Ex. 1008, 7:52–54).

Claim 7 depends from claim 5 and further recites, “wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.” Ex. 1001, 9:47–52. Relying on its prior analysis of claim 5, Petitioner contends Robinson discloses the additional limitation of dependent claim 7 by teaching:

The polishing pad 10 preferably has a body 11 made from a matrix material 12, abrasive particles 20 dispersed in the body 11, and bonding molecules 30 bonding the abrasive particles 20 to the matrix material 12. The matrix material 12 is generally polyurethane or nylon, [or] other polymeric matrix materials . . . The abrasive particles 20 are preferably made from silicon dioxide (SiO_2) or aluminum oxide (Al_2O_3).

Pet. 83 (citing Ex. 1008, 4:34–47) (emphases omitted).

We have reviewed Petitioner’s explanations and supporting evidence regarding dependent claims 5–7, and we find them persuasive in accordance with our above findings. *See* Pet. 79–83. Patent Owner does not address separately Petitioner’s explanations and supporting evidence regarding the combined teachings of Jaso, Stine1998, and Robinson. *See* PO Resp. 73. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the combined teachings of Jaso, Stine1998, and Robinson would have rendered claims 5–7 obvious.

I. Asserted Obviousness of Claims 5–7 over Jaso, Stine1998, Pramanik1997, and Robinson

Petitioner relies on its explanations and supporting evidence regarding the combination of Jaso, Stine1998, Pramanik1997, and Robinson to challenge dependent claims 5–7. Pet. 84; *see id.* 79–83. Patent Owner does

not address separately Petitioner's explanations and supporting evidence as to how the combined teachings of Jaso, Stine1998, Pramanik1997, and Robinson teach the limitations of dependent claims 5–7. *See* PO Resp. 73–74. As discussed above, we have reviewed Petitioner's explanations and supporting evidence regarding these claims, and we find them persuasive in accordance with our above findings. *See* Pet. 79–84. Petitioner, therefore, has demonstrated by a preponderance of the evidence that the combined teachings of Jaso, Stine1998, Pramanik1997, and Robinson would have rendered claims 5–7 obvious.

IV. MOTION TO EXCLUDE

Patent Owner seeks to exclude portions of the reply declaration of Petitioner's expert, Dr. Boning (Ex. 1052), and seven references cited in that declaration (Ex. 1044–1050) — all of which were previously sought to be stricken from the record by way of Patent Owner's request for leave to file a motion to strike. Paper 46 (“Mot. to Exclude”). We denied that request for leave to file a motion to strike because “any alleged new theories and evidence presented in the reply declaration were properly responsive to arguments in the Patent Owner Response.” Paper 43, 2. Nevertheless, we granted-in-part Patent Owner's alternative request that it be permitted to use 750 additional words in its Sur-reply. *Id.* at 2–3. In the Motion to Exclude, Patent Owner asserts that it “fully understands the Board's ruling and does not intend through this motion to revisit that ruling or to reargue the issues [rather Patent Owner] submits this motion to preserve its objections in the record.” Mot. to Exclude 1. Given that Motion to Exclude was filed merely “to preserve [] objections,” it is denied for the same reasons the request for leave to strike was denied. *See* Paper 43.

V. CONCLUSION

For the foregoing reasons, we determine Petitioner has established by a preponderance of the evidence the unpatentability of claims 1–8 of the '231 patent.¹⁶

In summary:

Claim(s)	35 U.S.C. §	References/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–4, 8	103(a)	Jaso, Stine1998	1–4, 8	
1–4, 8	103(a)	Jaso, Stine1998, Pramanik1997	1–4, 8	
5–7	103(a)	Jaso, Stine1998, Robinson	5–7	
5–7	103(a)	Jaso, Stine1998, Pramanik1997, Robinson	5–7	
Overall Outcome			1–8	

VI. ORDER

Accordingly, it is

ORDERED that claims 1–8 of U.S. Patent No. 6,232,231 B1 are unpatentable;

¹⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

FURTHER ORDERED that Patent Owner's Motion to Exclude Evidence is *denied*; and

FURTHER ORDERED that parties to the proceeding seeking judicial review of this Final Written Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2020-00603
Patent 6,232,231 B1

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